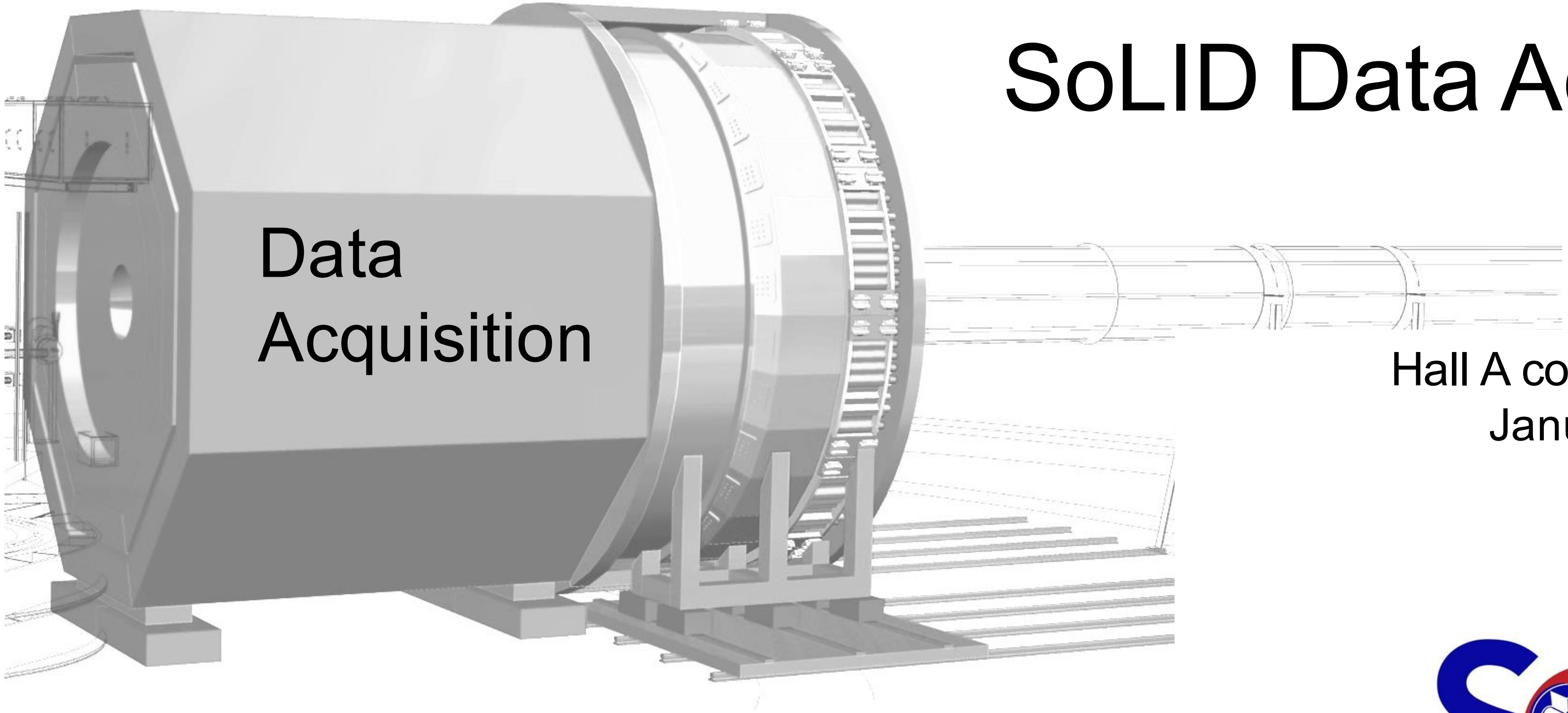
SoLID Data Acquisition



Hall A collaboration meeting
January 22nd 2026

Alexandre Camsonne

- Outline

- SoLID DAQ introduction
- GEM readout
- SBS experience
- Beam Test preparation
- HKS
- Streaming option

- Conclusion

Capital equipment DAQ

Requested

Item	cost/item	number	total
FADC 250	6000	104	624000
Gigabit serial connectors			40000
Cables	100	1664	166400
VETROC	4000	30	120000
TD	3000	16	48000
VTP	10000	31	310000
SSP	5000	4	20000
VTP	8000	1	13000
TS	4000	1	4000
TID	3000	31	93000
SD	2500	32	80000
VXS crate	15000	32	480000
VME CPU	7000	32	224000
		Total	2217400

Updated

Item	cost/item	number	total
FADC 250	6127	104	637208
Gigabit serial connectors	40000	1	40000
Cables	100	1664	166400
VETROC	4000	30	120000
TD	3000	16	48000
VTP	12500	31	387500
SSP	5000	4	20000
VTP	12500	1	12500
TS	4000	1	4000
TID	3000	31	93000
SD	2500	32	80000
VXS crate	19000	32	608000
VME CPU	9500	32	304000
		Total	2520608

Received

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VME CPU	9500	32	304000
		Total	2520608

- Test small scale during other experiments
  - Trigger logic and readout
  - Measure asymmetries
- Test full scale DAQ
  - 30 crates for PVDIS and SIDIS

Remaining tests for SoLID DAQ

- Achieve 100 KHz trigger rate for SIDIS
- Measure asymmetries at ppm level with full system for PVDIS

- Achieve 150 ps with TOF scintillator
- Achieve 25 ps timing resolution with MRPC
- Show full tracking efficiency above 85% level in full background
- Gas Cerenkov efficiency

Future SoLID testing

- Highest priority : GEM chip
  - 1) develop VMM optimized for GEM and uRWell with higher gain (500 K$)
  - 2) Continue testing VMM board signal to noise
  - 3) Evaluate SALSA chip in high background environment
  - 3) Find funding to develop dedicated ASIC chip for GEM (~ 2.5 M$)
  - Test with uRWell
- Calorimeter and Cerenkov readout
  - FADC ASIC to be placed on detector : only LV and optical fibers going out instead of BNC cables
- High resolution timing
  - AARDVARC test in beam
  - High resolution FADC timing ASICS
  - Timing distribution with CODA
- Measure physics asymmetries with small scale setup

GEM SBS experience

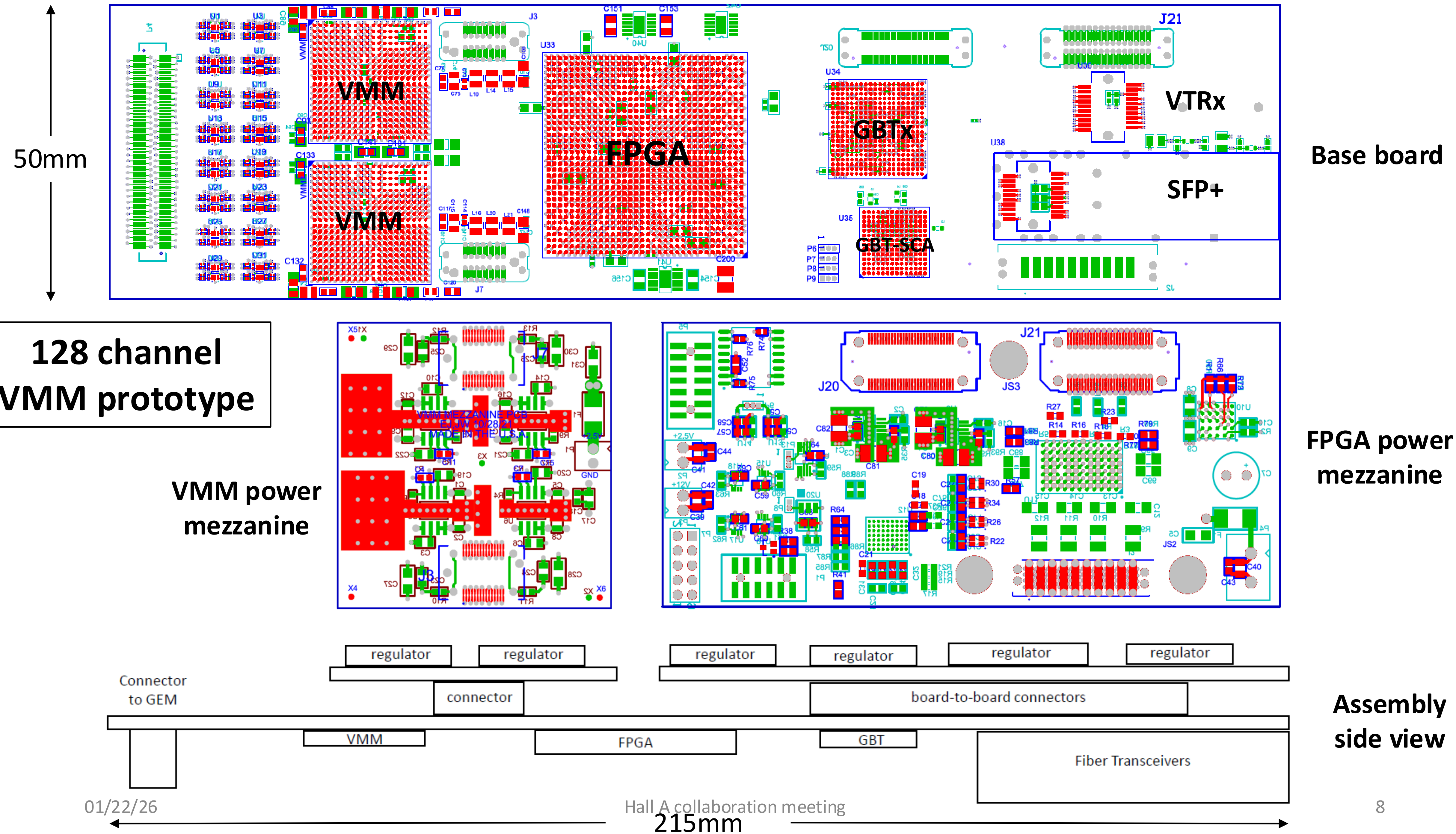
- Experiment supposed to run at 30 uA
- DAQ rate limited to 3 or 4 KHz for high live time (above 85%)
- Data rate limited to 3 GB/s

- Currently running at 20 uA limited by tracking efficiency
- Limited by data rates if going to 30 uA or more but firmware being developed to reduce data rate by 3
- Need to determine if occupancy higher than expected
- Possibly AIML based tracking might be more efficient
- VTP bugs ironed out : about 1 GEM crash every two hours – not clear if APV or MPD upsets
- High granularity and faster shaping time would have been helpful
- Unclear if experiments are possible with 1 time sample – currently reading 6 time samples

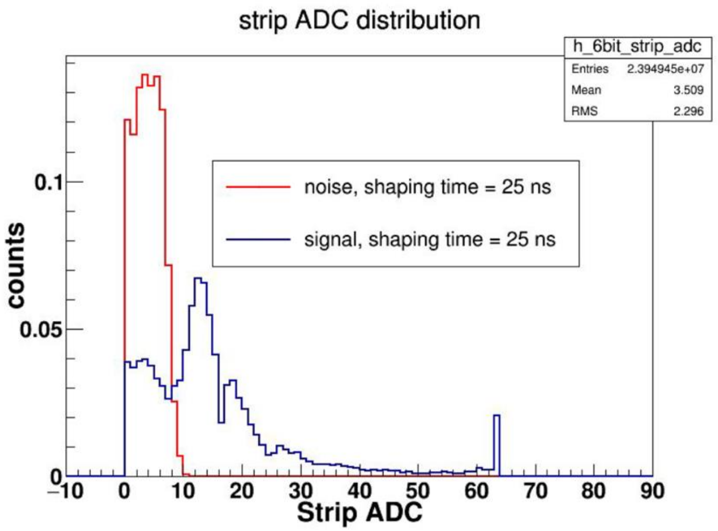
VMM test

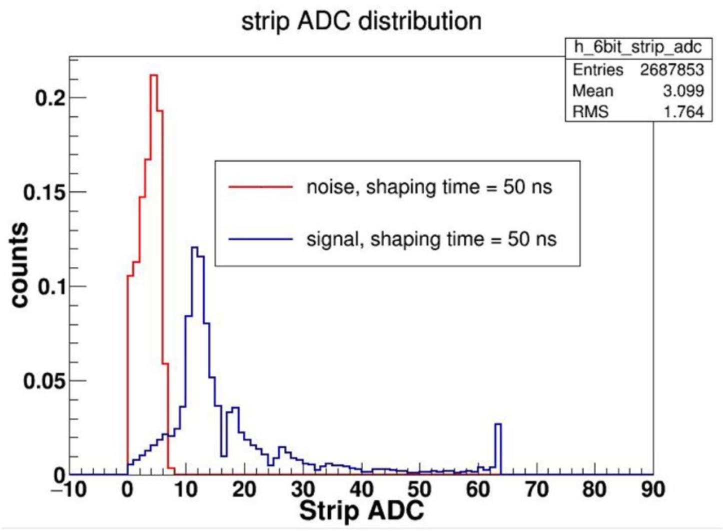
- Ordered two test board 1500 $ x 2
- Build 6 SoLID prototype boards
- Evaluation board : can look at data with detector small subset of channels
  - Issue with external trigger but waiting for new firmware
  - Can check pedestal width
  - Signal to noise with detector with source and cosmics
  - Look at direct readout signals for 12 channels of detector

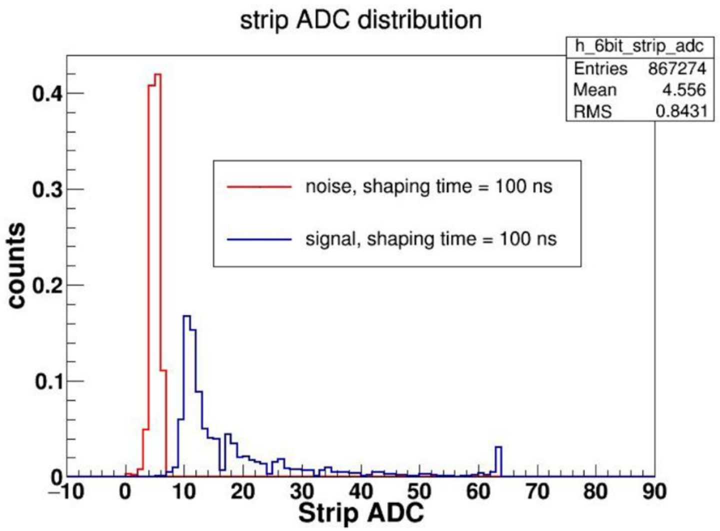
128 channel VMM prototype

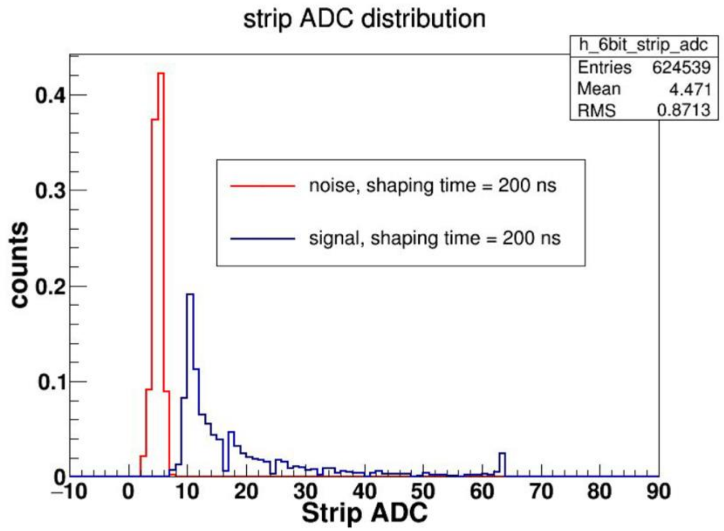


Noise 6 bit 16mV/fC Sr90







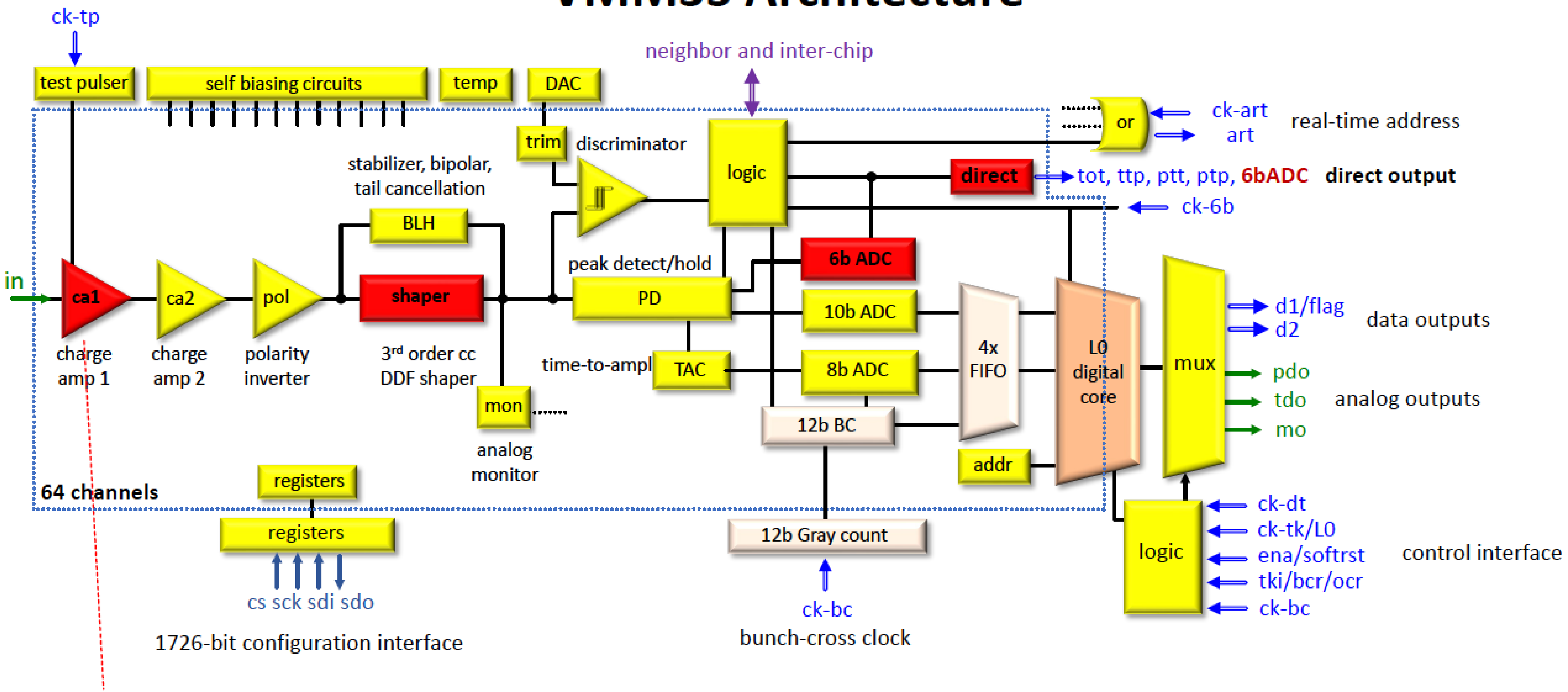


- Amplitude for MIP not change much
- Pedestal width dependent on peaking time

Conclusion VMM testing so far

- 90 ns dead time in 6 bit mode
- Some noise seen in prototype
- Noise larger with decreasing integration time
- MIP a bit low in dynamic range of 6 bit prototype
- Implementing 10 bit to cross compare with evaluation board
- 250 ns for 10 bit mode
- Investigating new VMM with high gains for GEM and uRWell (~500 K$) Hall B interested, need to reach out to SRS community
- Need implement Rad Hard DC DC converter and lpGBT radiation hard readout

VMM3S Architecture



SoLID MPGDs will initially operate with charges up to ~100,000e⁻:

- will integrate a higher gain setting 64mV/fC
- will deliver ENC ~1,500e⁻ @ 50pF, 25ns (ADC contribution ~450e⁻)

Salsa

- Collaboration of Irfu CEA Saclay and U. of Sao Paulo.
- SALSA

- 64-Ch, updated design from SAMPA V5, migrating to 65 nm CMOS.
- Peaking time: 50 – 500 ns
- Inputs: Cin optimized for 200 pF; Rates: 25 kHz/Ch; Dual polarity.
- ADC: 12 bits, 10 – 50 MSPS.
- Extensive data processing capabilities.
- Triggerless and triggered operation.
- Power: 15 mW/Ch
- Gbps links.
- I2C configuration.

- Evaluation board available this year - Might want a dedicated SoLID version to match tracker low gain operation and handle high rates at input
- Can bypass analog part but need to develop analog front end
- Data links somewhat limited

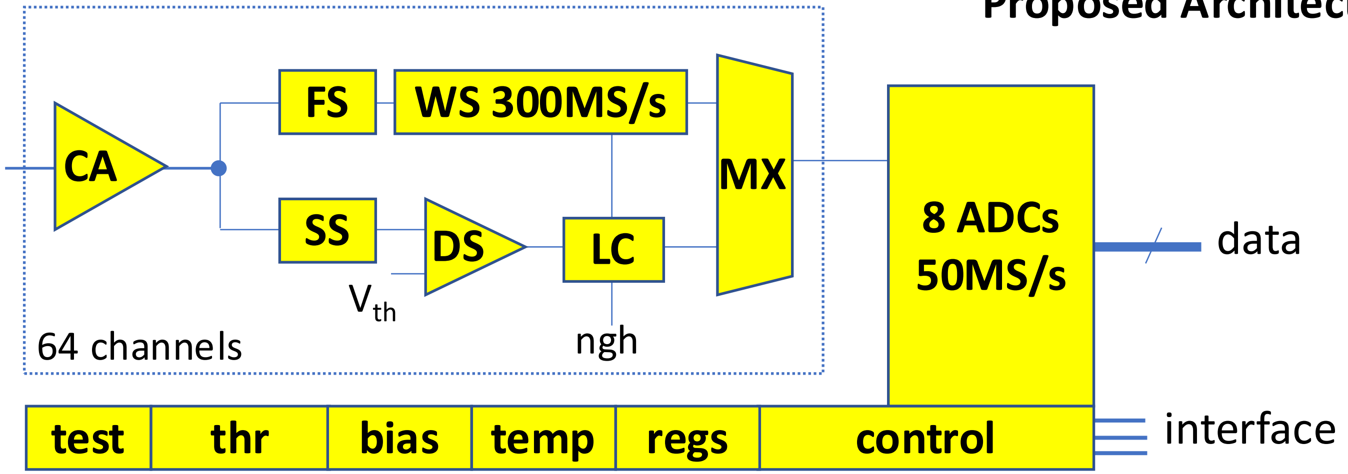
- Might want a dedicated version of SALSA

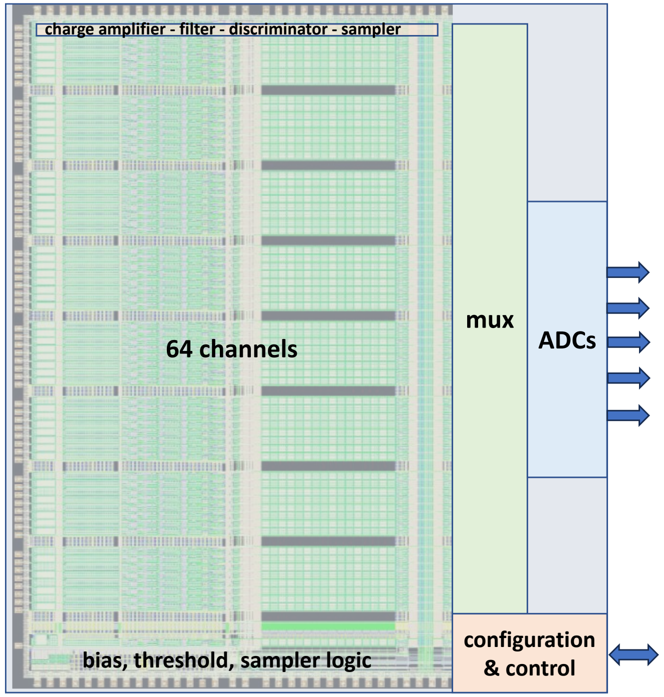
New potential dedicated ASIC

- High luminosity running need to run
- Pile-up and deadtime can be significant

- Dedicated chip
  - Optmized gain and dynamic range
  - Optimize shaping time for high rate operation : from 50 ns to 25 ns or better
  - Zero dead time
  - High speed links to allow streaming

Proposed Architecture





CA: charge amplifier
- optimized for 50-200pF
- programmable gain 25fC to 250fC

FS: fast shaper
- programmable 5-20ns

SS: slow shaper
- for discrimination (zero suppression)
- programmable 20-100ns

DS: discriminator
- trimmable per channel
- external trigger option

WS: waveform sampler
- 128 sampling cells (127 effective)
- continuous sampling until trigger
- 300MS/s → ~ 400ns waveform
- programmable pre-post trigger samples

LC: local control logic
- internal or external trigger
- neighbor (sub-threshold) logic

ADCs
- 8 operating at 10-bit 100MS/s
- waveform conversion time ~ 2.5µs

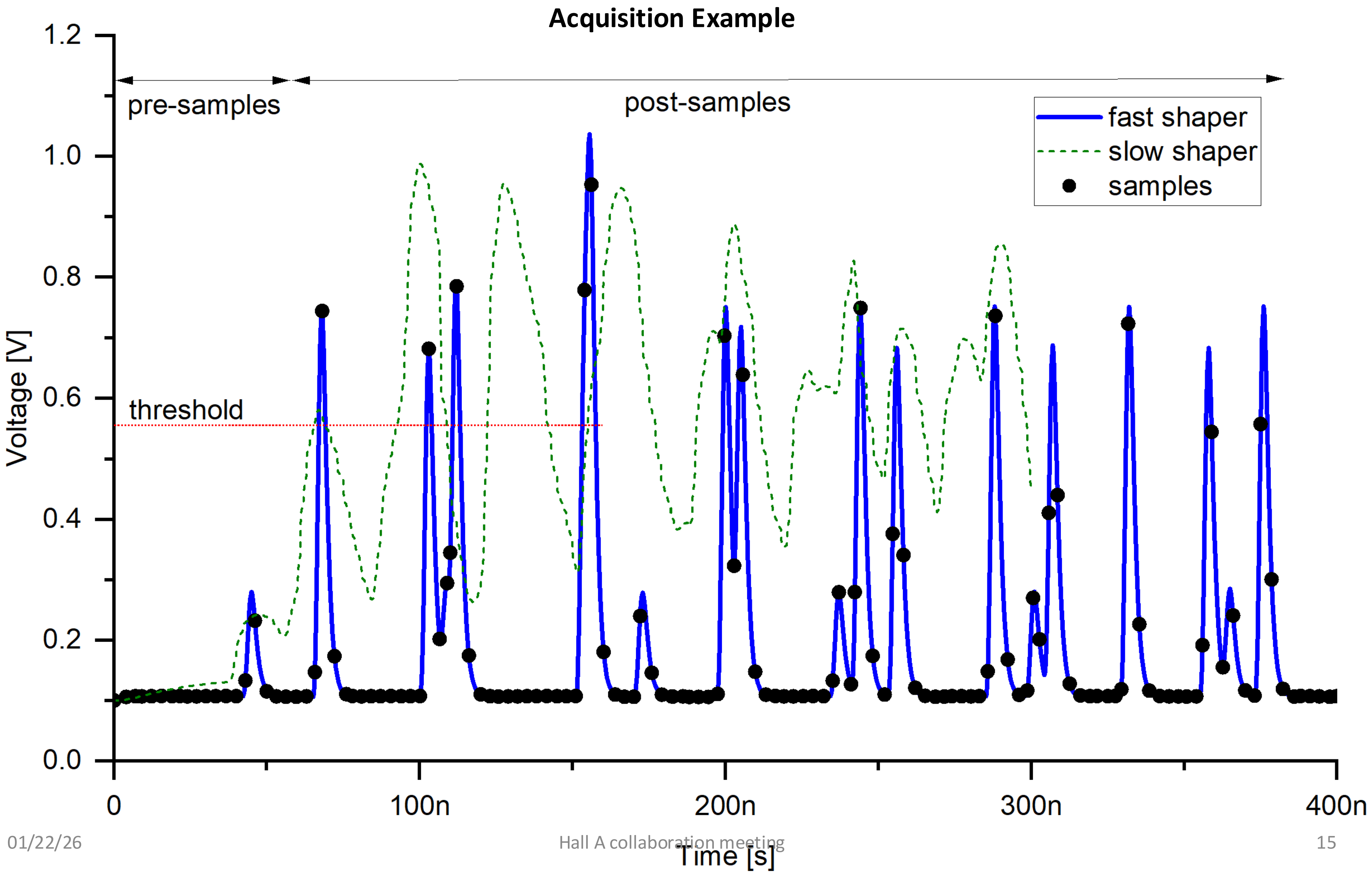
Data
- channel, trigger, 127 samples = 1,280 bits per waveform
- up to 8 waveforms with sub-threshold neighbors = 10,240 bits
- up to 8 SLVS outputs operating in DDR at ~ 500MS/s
- conversion/readout time (dead time) ~ 2.5µs per event
- maximum event rate ~ 330kHz
- maximum data rate ~ 4Gb/s

Architecture
- event-driven analog/digital with acquisition/readout
- SEU tolerant register and logic
- DSP-ready

Power, Size, Technology, Schedule
- power consumption below 3mW/channel
- anticipated die size ~ 6x8 mm^2
- technology TSMC 65nm 1.2V
- development time ~ 24 months (1^{st} proto in 12 months)

Design
- charge amplifier, shapers and samplers based on verified architectures
- ADCs from collaborative effort
- first prototype design time
  - ~ 12-13 months plus ADCs
  - ADC can be parallel effort
- second prototype design time
  - ~ 4-5 months

Key Features
- power-efficient analog zero-suppression
- efficient data generation and transfer
- highly flexible, highly programmable


Acquisition Example
pre-samples
post-samples
threshold
fast shaper
slow shaper
samples
Voltage [V]
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0
100n
200n
300n
400n
Time [s]

APV25 new MPD

- Upgrade MPD from 100 MBit to 10 GBit ethernet
- Should give max rate from APV25
- Need to improve DAQ stability
  - Not clear if
    - APV single upsets
    - MPD upsets
    - Others (VTP)

GEM new simulation work

- Estimate rates and occupancies with new shaping and sampling electronics
- Optimize segmentation of chambers to avoid
- Explore pads readout chamber to complement high rate tracking

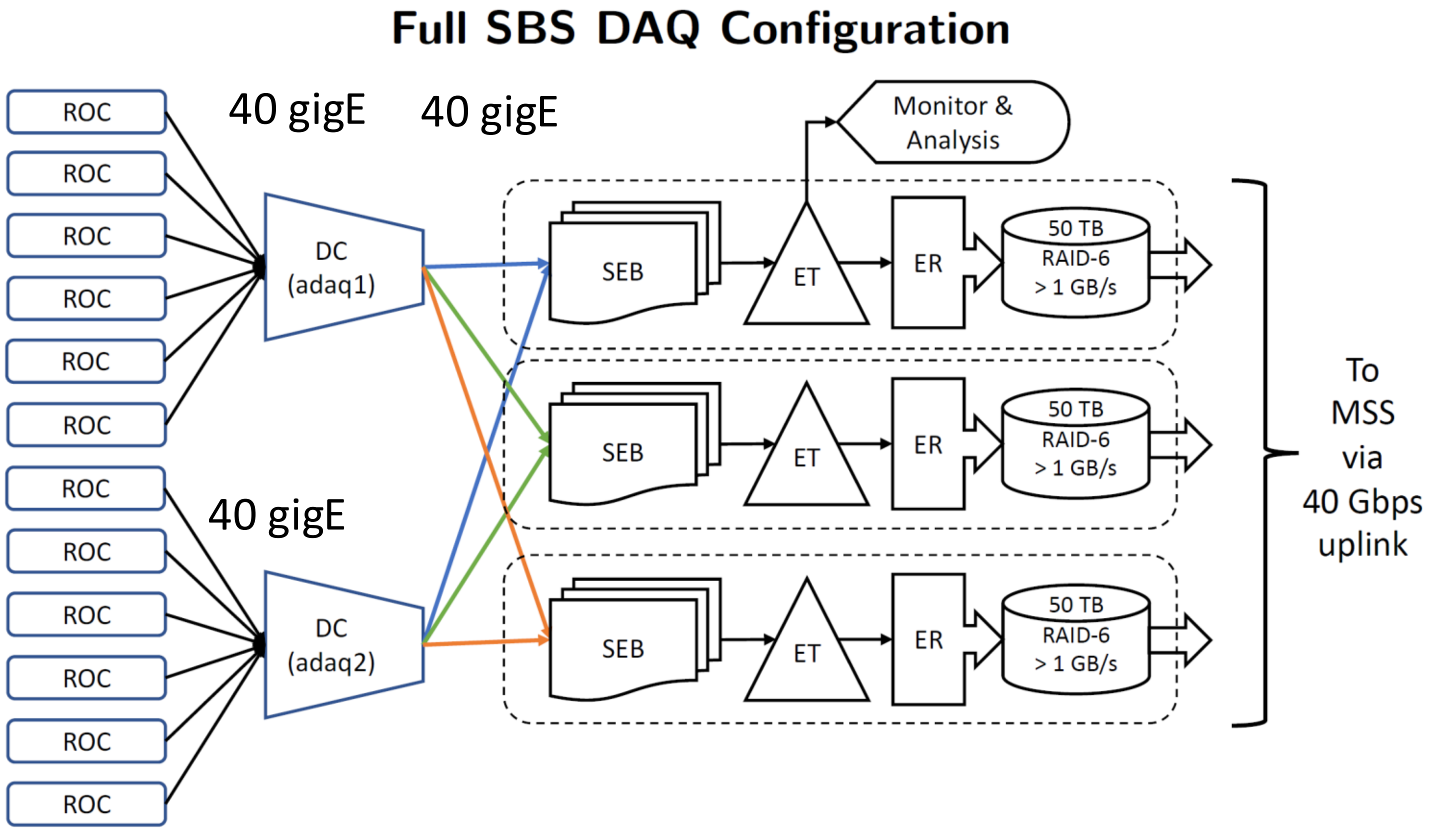
GEM data rates with latest occupancies

	Rate per cm2	Rate per plane	hits in 325 ns	occupancy	strip hits	XY	6 samples	bytes	Rate MB/s
1	170	1020	331.5	17%	1160.25	2320.5	13923	55696	278.48
2	230	1380	448.5	23%	1569.75	3139.5	18837	75348	376.74
3	260	1560	507	26%	1774.5	3549	21294	85176	425.88
4	275	1650	536.25	28%	1876.875	3753.75	22522.5	90090	450.45
5	280	1680	546	28%	1911	3822	22932	91728	458.64
6	285	1710	555.75	29%	1945.125	3890.25	23341.5	93370	466.85
7	225	1350	438.75	23%	1535.625	3071.25	18427.5	73710	368.55
8	240	1440	468	24%	1638	3276	19656	78624	393.12

	Rate per cm2	Rate per plane	hits in 325 ns	occupancy	strip hits	XY	6 samples	bytes	Rate MB/s
1	80	480	156	8%	546	1092	6552	26212	131.06
2	72	432	140.4	7%	491.4	982.8	5896.8	23587	117.94
3	66	396	128.7	7%	450.45	900.9	5405.4	21622	108.11
4	64	384	124.8	6%	436.8	873.6	5241.6	20966	104.83
5	62	372	120.9	6%	423.15	846.3	5077.8	20311	101.56
6	58	348	113.1	6%	395.85	791.7	4750.2	19005	95.03
7	55	330	107.25	6%	375.375	750.75	4504.5	18018	90.09
8	54	324	105.3	5%	368.55	737.1	4422.6	17690	88.45
								811155	
								Total	4055.78
				at 5 KHz	1		Total		4056MB/s
							Geometrical Factor		1352MB/s

CODA3

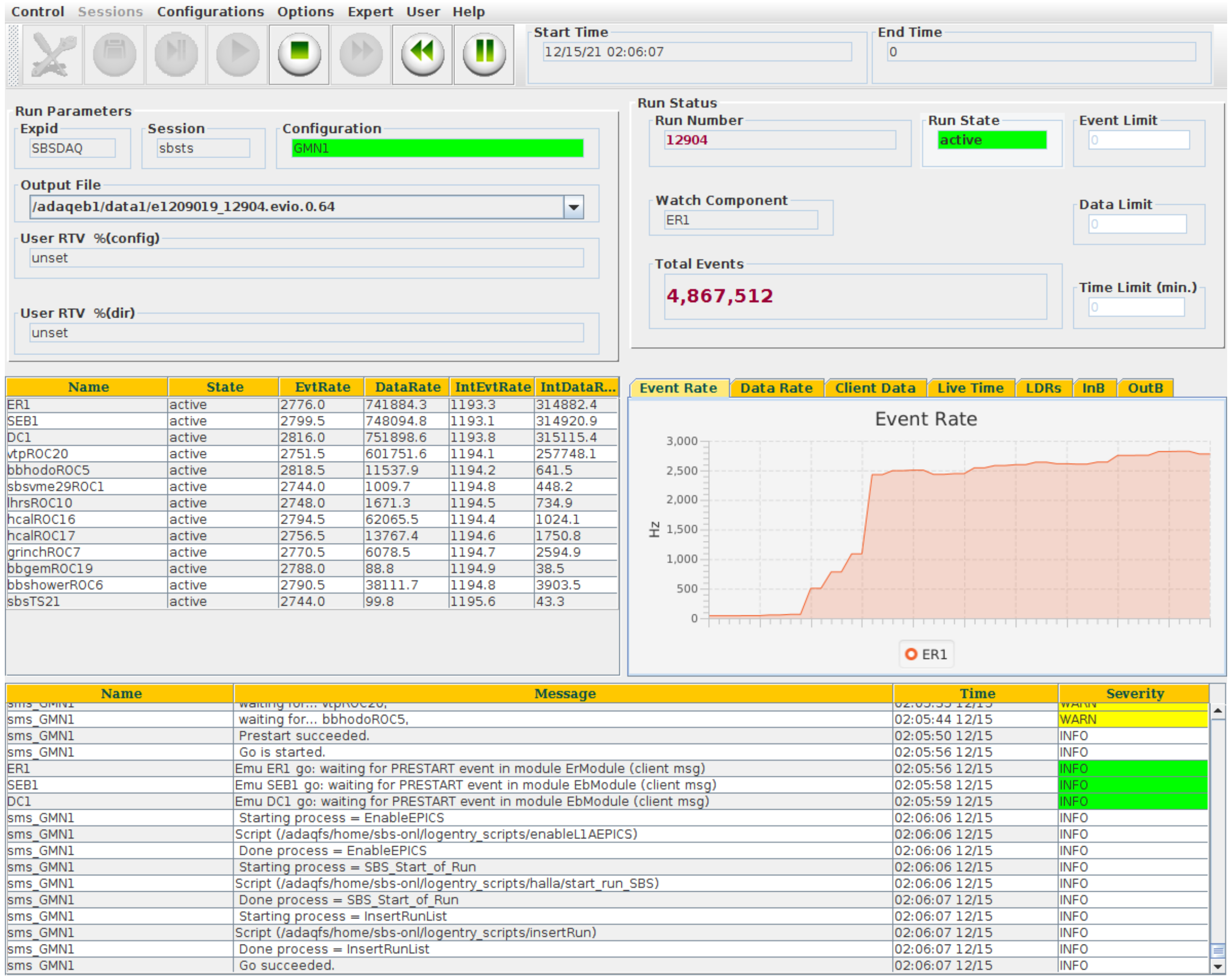
- TS/TI Fiber based
- Support for VTP
- Support for multiple stream



Production data during GMn

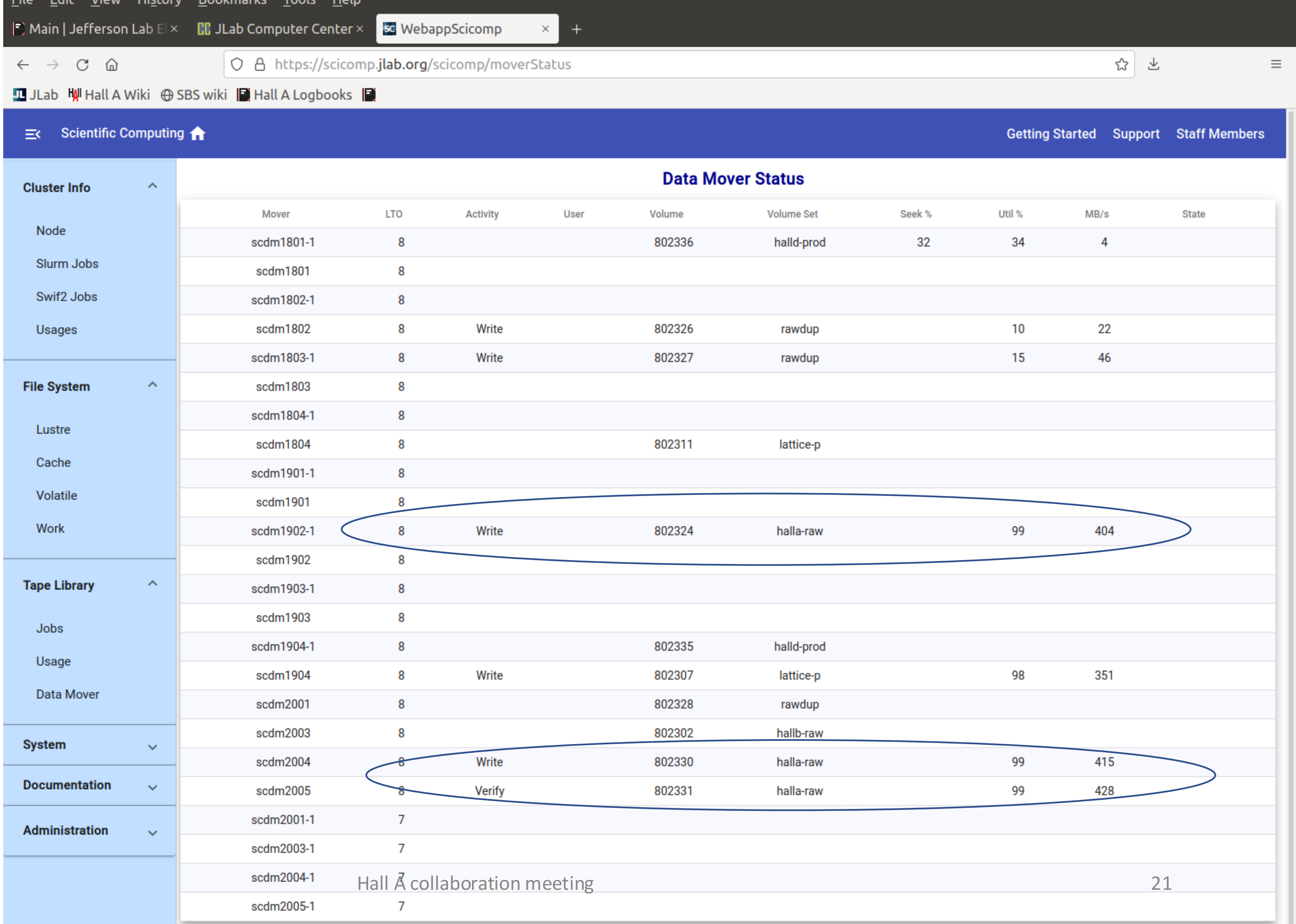
- Typical rate around 3 kHz
- 90% livetime with one event builder
- 600 MB/s from BigBite GEM
- 240 MB/s HCAL, shower FADCs
- 800 MB/s to disk

- Up to 2.4 GB/s using 3 event builder



Silo performance

- Achieved 800 MB/s continuous
- Catch up at 2 GB/s
  mainly need to allocate more arms



Data Mover Status

Mover	LTO	Activity	User	Volume	Volume Set	Seek %	Util %	MB/s	State
scdm1801-1	8			802336	halld-prod	32	34	4	
scdm1801	8								
scdm1802-1	8								
scdm1802	8	Write		802326	rawdup		10	22	
scdm1803-1	8	Write		802327	rawdup		15	46	
scdm1803	8								
scdm1804-1	8								
scdm1804	8			802311	lattice-p				
scdm1901-1	8								
scdm1901	8								
scdm1902-1	8	Write		802324	halla-raw		99	404	
scdm1902	8								
scdm1903-1	8								
scdm1903	8								
scdm1904-1	8			802335	halld-prod				
scdm1904	8	Write		802307	lattice-p		98	351	
scdm2001	8			802328	rawdup				
scdm2003	8			802302	hallb-raw				
scdm2004	8	Write		802330	halla-raw		99	415	
scdm2005	8	Verify		802331	halla-raw		99	428	
scdm2001-1	7								
scdm2003-1	7								
scdm2004-1	7								
scdm2005-1	7								

Completed and current testing

- SBS GMn GEn
  - VTP readout
  - APV25
  - High data rate : 2.1 GB/s
- NPS
  - Calorimeter trigger
- SBS GEp
  - Calorimeter trigger
  - Data rate : 2.5 to 3 GB/s
  - GEM readout experience

Calorimeter trigger and fast FADC readout

- Moller
  - Compton
  - Counting DAQ
- HKS
  - Trigger with Cerenkov
  - High resolution TOF with MRPC and vfTDC
- Hall C experiments in HMS and SHMS : measure physics asymmetries : VTP in HMS/SHMS
- Future parasitic beam tests
  - FADC + VTP + VETROC + VMM in on crate for testing : PVDIS one crate setup available with calorimeter and Cerenkov trigger
  - Acquired SAMPIC 64 channels sampler for MRPC
  - APV25 available after GEp5
- ESB
  - Test V3 FADC
  - VTP trigger
  - GEM readout APV25 and VMM3
  - Deadtime and max trigger rate

Beam test preparation (see Eric’s talk)

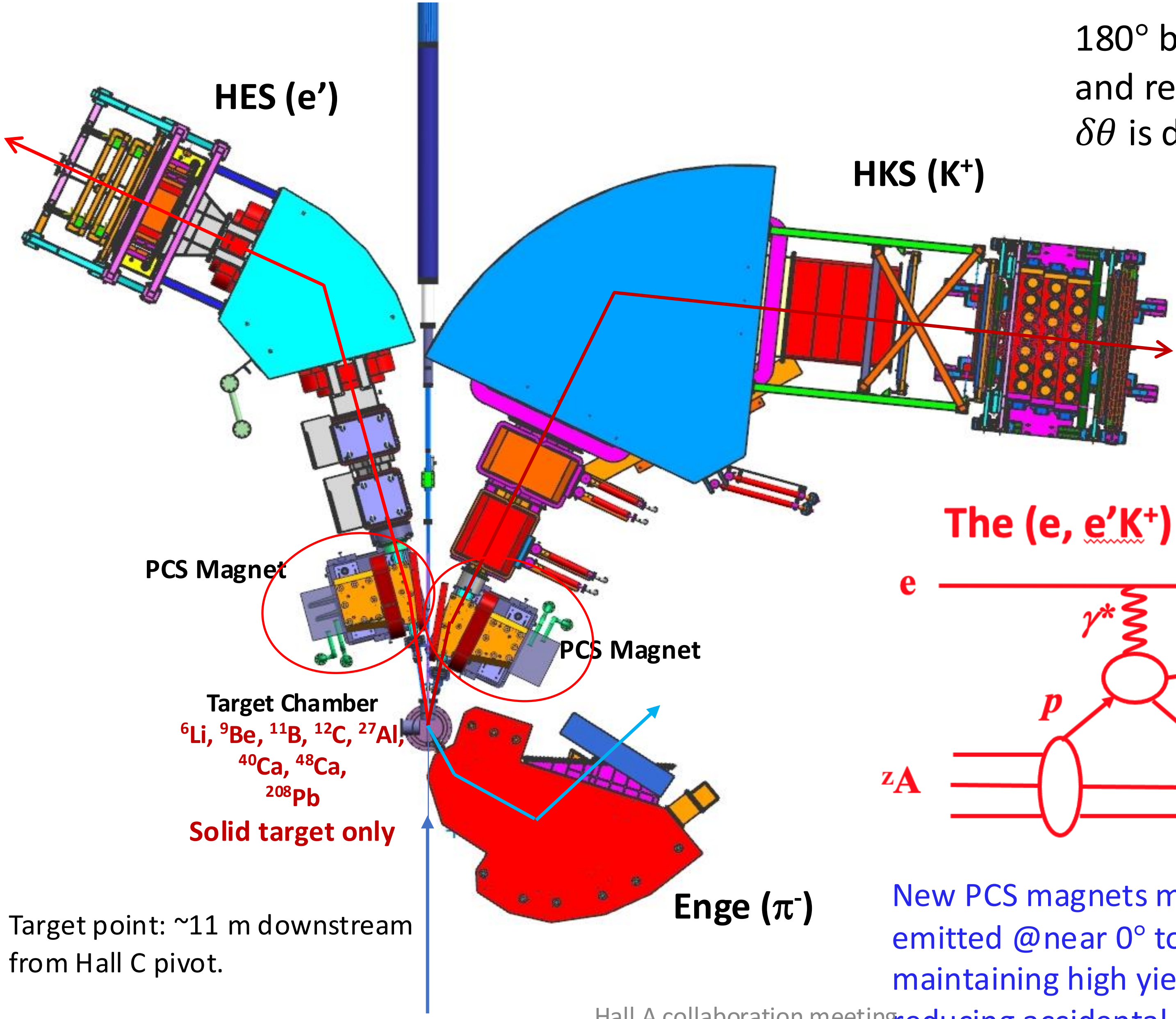
- 1 to 2 VXS crate
- 1 crate VTP + up to 16 FADCs or VETROCs
- 1 crate VTP + MPDs for GEMs
- Digital calorimeter cluster and Cerenkov trigger
- Max 5 KHz with GEM for testing GEM, VMM and uRWell
- 100 to 200 KHz should reachable with FADC and VETROC only
- 32 channels of SAMPIC for MRPC
- 8 channels of ASOC and 8 channels of AARDVARC for MRPC
- MRPC testing with vfTDC

HKS experiment

- Run same time as Moller
- 3 High resolution magnetic spectrometers
- Would benefit from high resolution timing for PID
- Opportunity to test detectors in HKS
- Test FADC trigger logic with Cerenkov

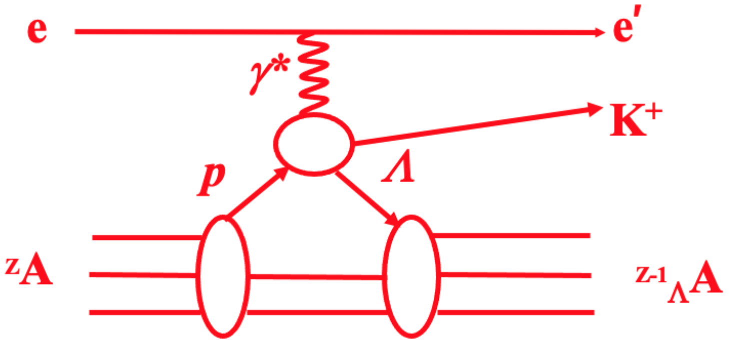
Schematic Layout of The Hypernuclear Spectrometer System

180° between scattering and reaction planes ($\Delta\phi_0$)
$\delta\theta$ is dominated by δx'



Target point: ~11 m downstream from Hall C pivot.

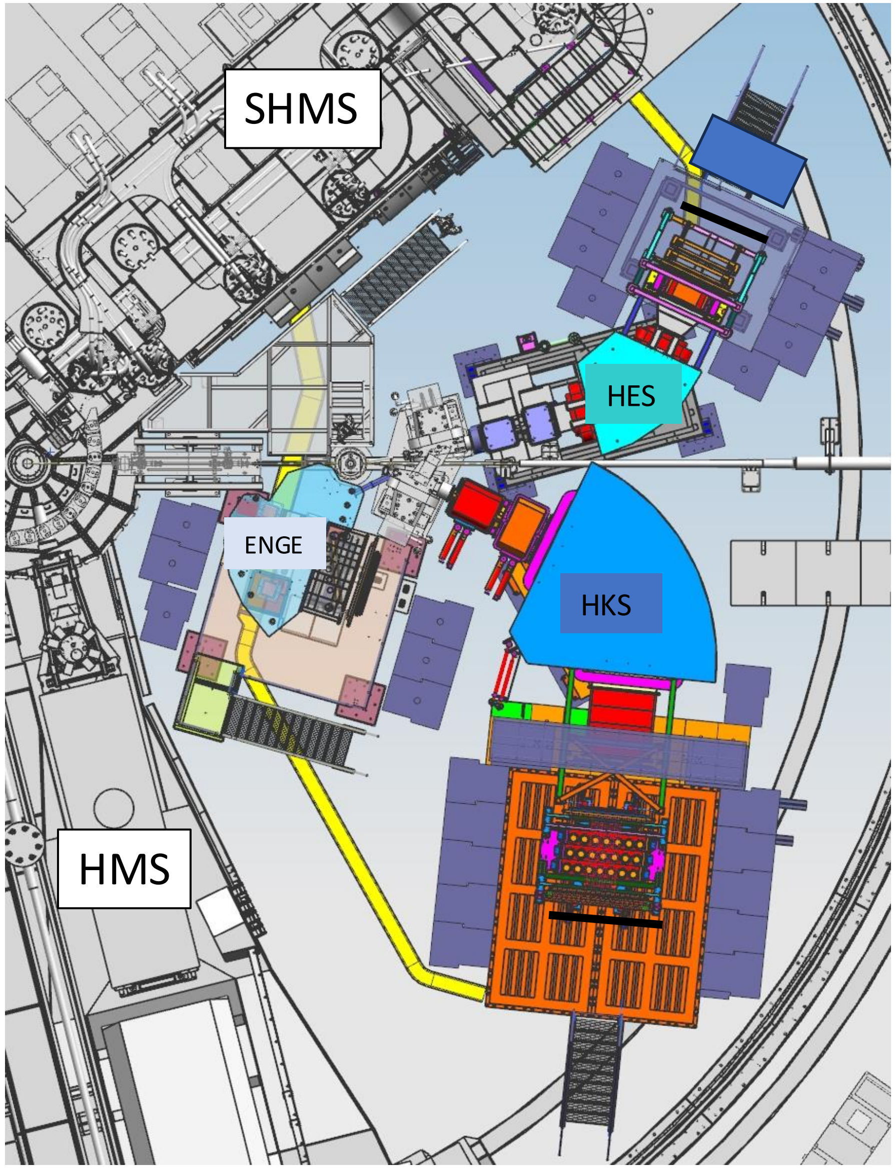
The (e, e'K+) Reaction



New PCS magnets minimize the particles emitted @near 0° to enter HES and HKS, maintaining high yield while significantly reducing accidental background

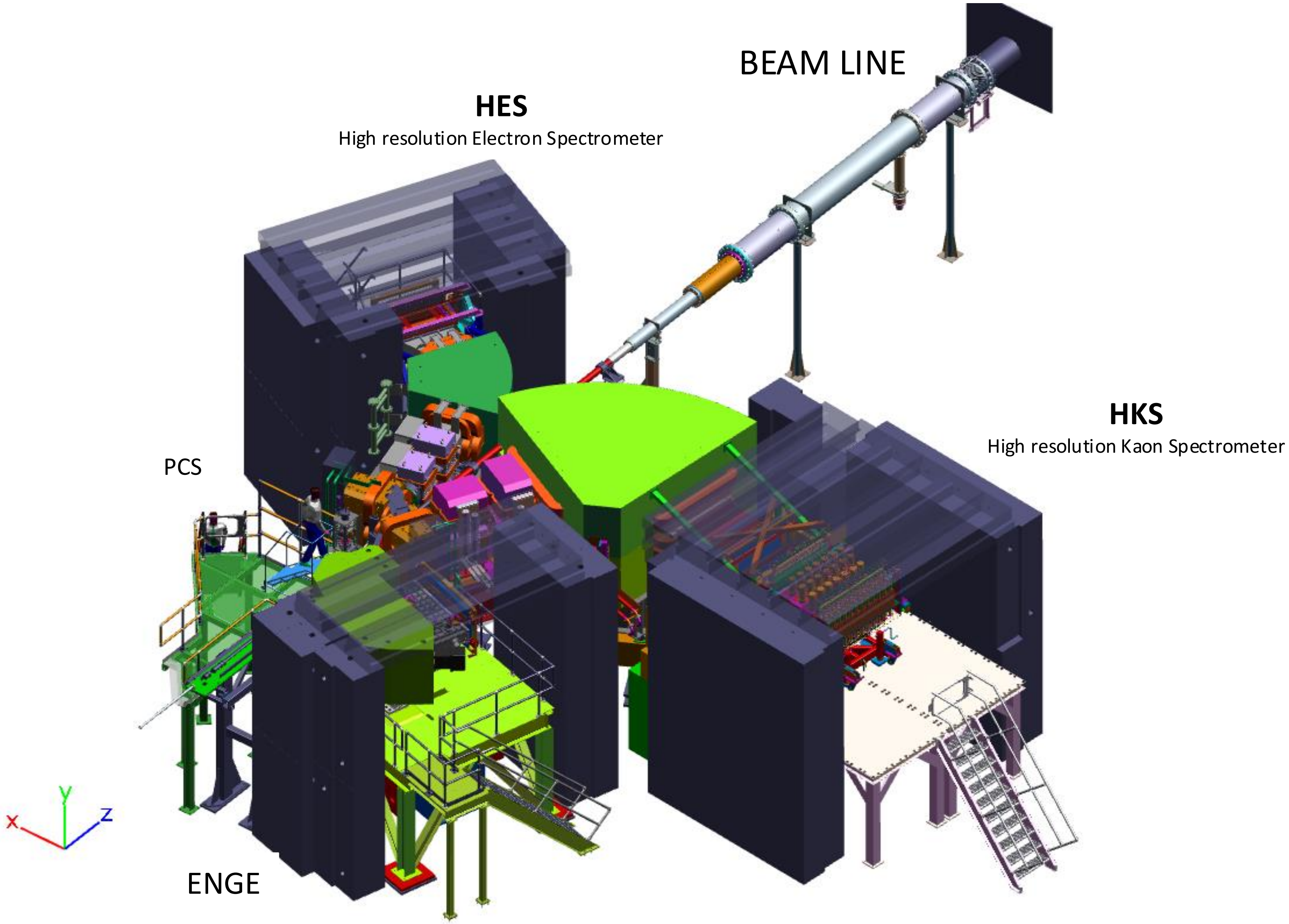
2

HYPER NUCLEAR – LAYOUT (TOP VIEW)



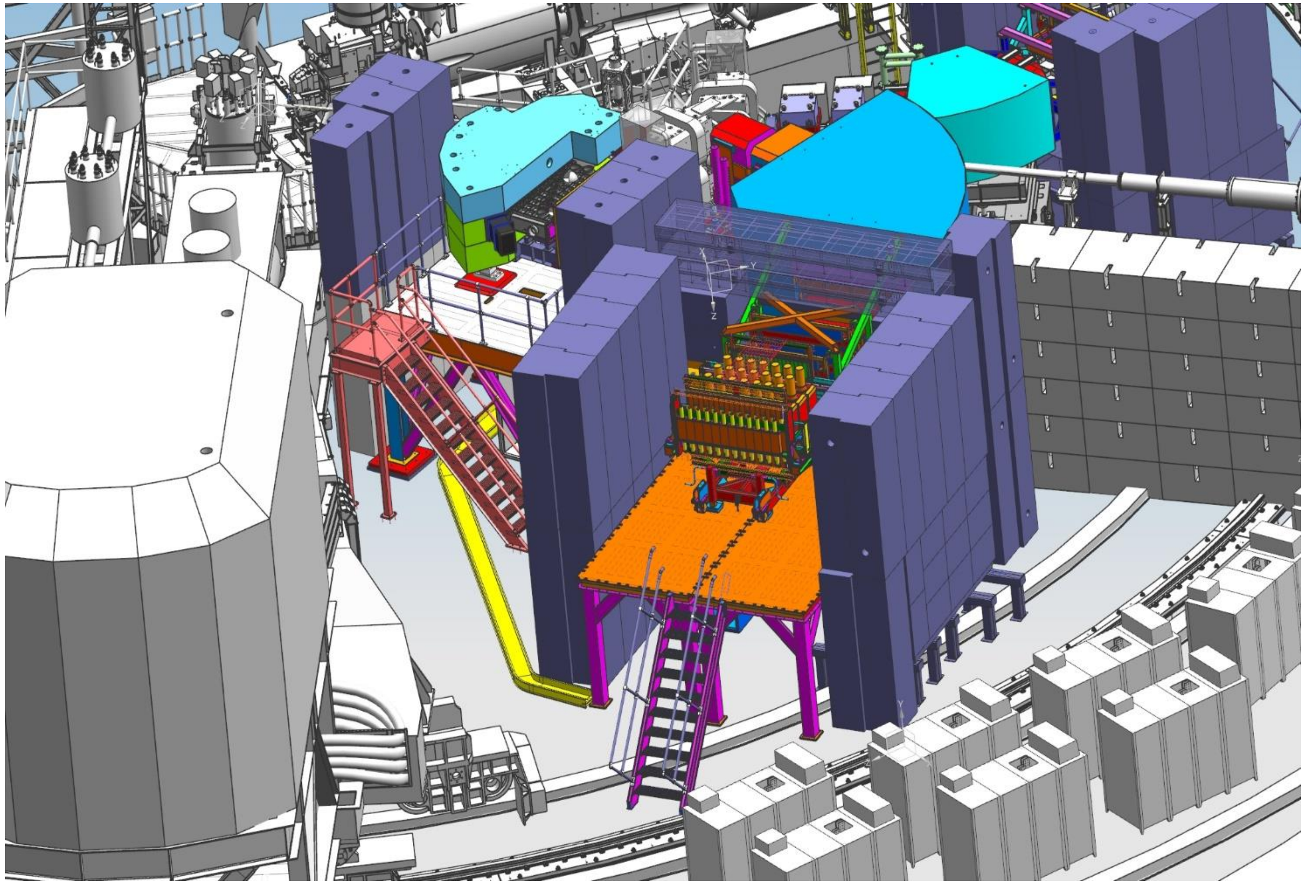
BEAM LINE

HYPER NUCLEAR – LAYOUT (ISO-VIEW)

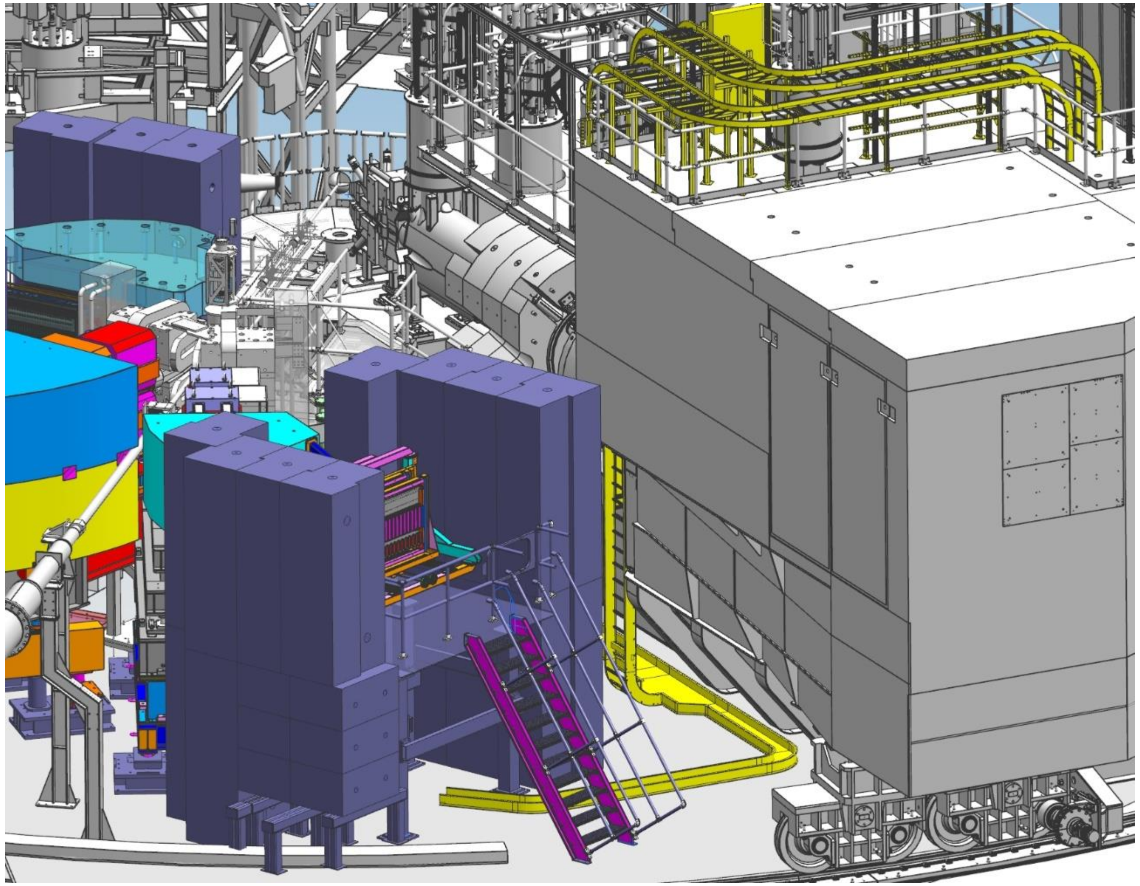


HYPER NUCLEAR – CABLE ROUTING

HKS

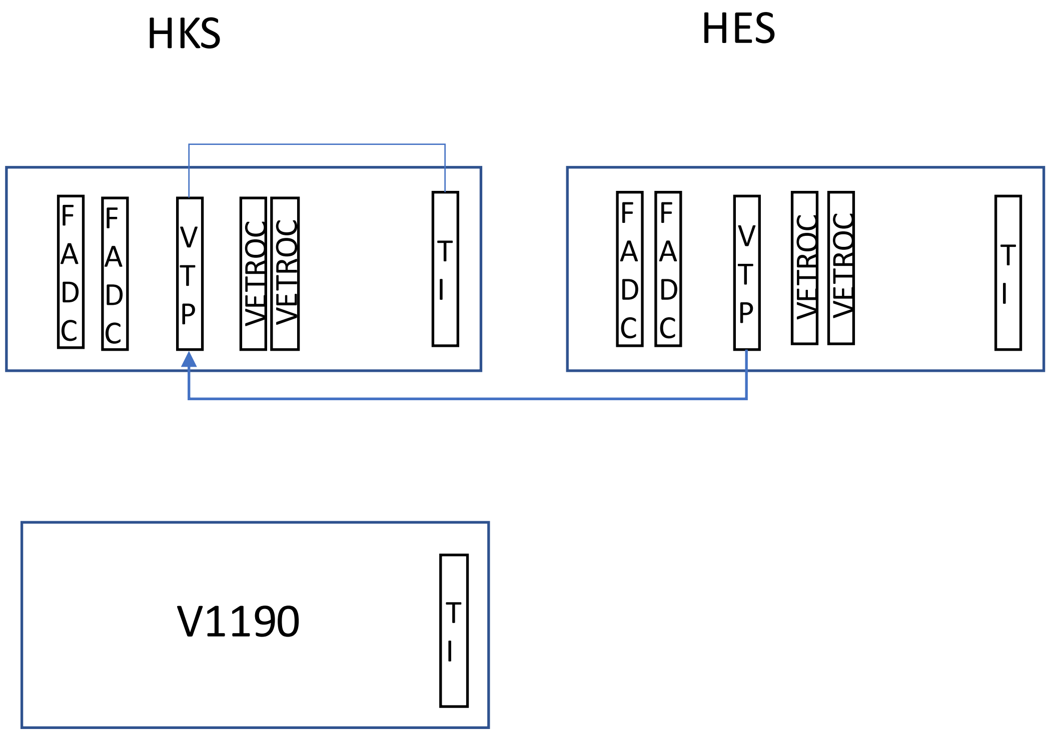


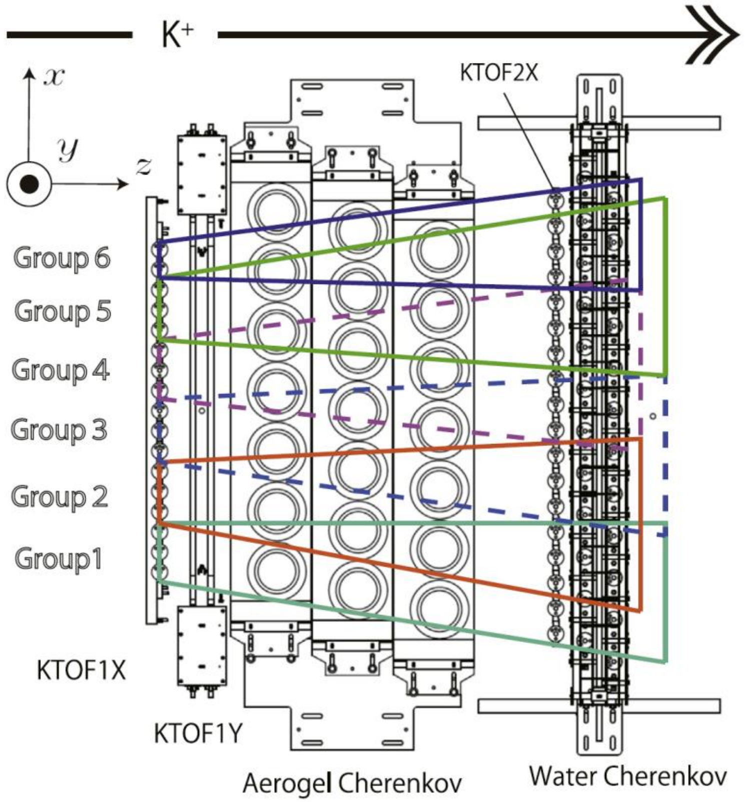
HES



CABLE TRAY LAYOUT FROM SUPER HMS(YELLOW)

Trigger





Can program VTP for coincidences between scintillators
If use VETROC instead of V1190 could add Drift Chamber to trigger

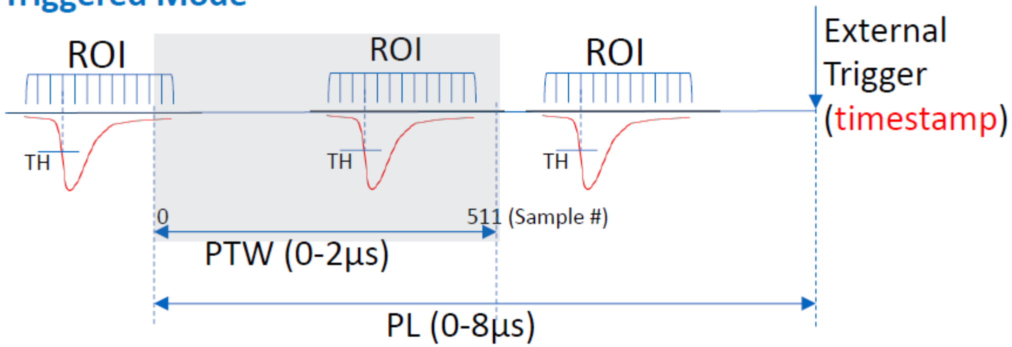
Streaming readout overview

Streaming readout

- Send all data from each detector continuously (or self triggered)
- Pro
  - No trigger
  - <u>If can be recorded : record all physics available</u>
  - If cannot be recorded : full reconstruction and record event of interest with advanced triggering or loose trigger
  - AIML algorithm very efficient with unbiased data samples
- Con
  - Need deadtime less electronics : ideally all FADCs (but high power comsuption)
  - Large amount of data to transfer to computer farm : cost in network
  - Large amount of data to be processed
  - Large amount of data to be recorded

FADCs - Triggered vs Streaming

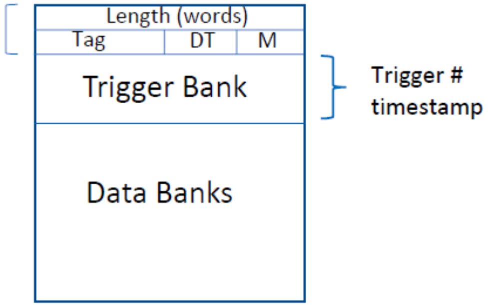
Triggered Mode



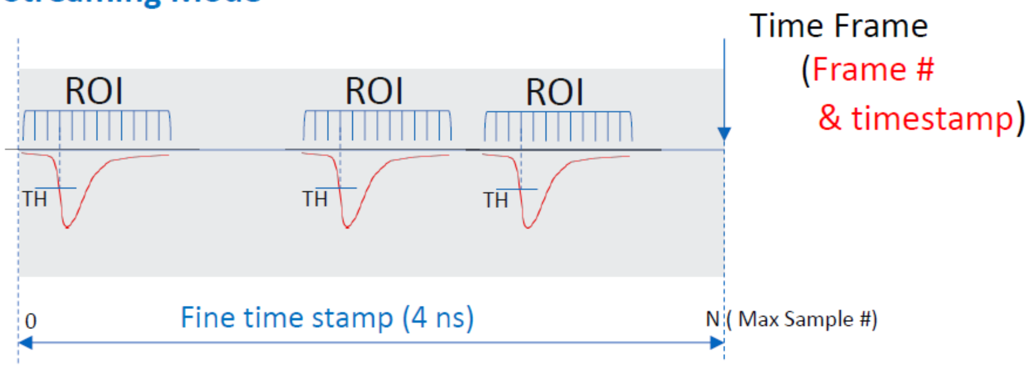
PL: Programmed Lookback
PTW: Time window

Data we get on a trigger:
- FADC waveform values for the ROI
- Threshold Sample # (hit time)
- Trigger absolute timestamp (48 bits)

ROC Data Format



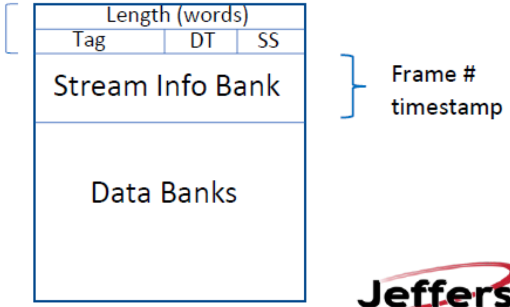
Streaming Mode



1 Frame = N Clocks (up to 16bits, currently 65536 ns)

Data we get for a Frame:
- Pedestal subtracted sums over an ROI for every hit over threshold
- Threshold sample # fine time stamp for each hit
- Frame # and absolute time stamp for the frame

ROC Data Format



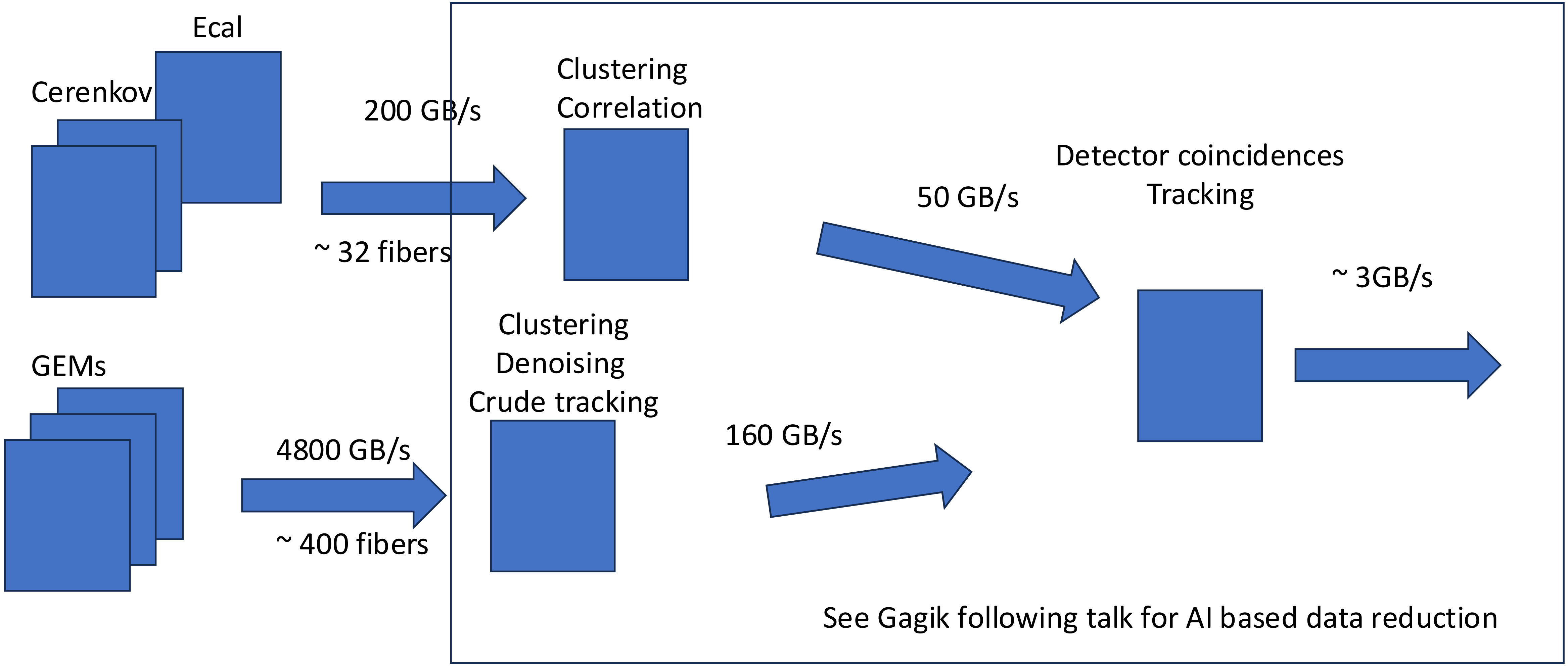
Streaming readout option numbers

Detector	Area m2	SIDIS Rate kHz per cm2	Singles rate MHz	Event size bytes	Data rate GB	PVDIS Rate kHz per cm2	Singles rate MHz	Event size bytes	Data rate GB	JPSi rate kHz per cm2	Singles rate MHz	Event size bytes	Data rate GB
LGC	0.7	16	112	16	1.792	80	560	88	49.28	40	280	16	4.48
HGC	1.2	160	1920	16	30.72		0	88	0		0	16	0
SPD_FA	15.2	0.02	3.04	16	0.04864		0	88	0	0.06	9.12	16	0.14592
SPD_LA	3.7	0.12	4.44	16	0.07104		0	88	0	0.25	9.25	16	0.148
EC_preshower_FA	19	33	6270	16	100.32	90	17100	88	1504.8	77	14630	16	234.08
EC_shower_FA	19	10	1900	16	30.4	9	1710	88	150.48	14	2660	16	42.56
EC_preshower_LA	4.1	45	1845	16	29.52		0	88	0	80	3280	16	52.48
EC_preshower_LA	4.1	5	205	16	3.28		0	88	0	19	779	16	12.464
GEM	37	800	296000	16	4736	500	185000	16	2960	1600	592000	16	9472
	Rate in GB/s				4932				4664				9818

Around 10 to 5 TB/s, about 1000 more data than triggered

Need around 400 fibers and 8 routers

SoLID streaming SIDIS



Updates from latest streaming workshops

- ASICs developments
- Streaming software
- AI data reduction

- https://indico.bnl.gov/event/24286/timetable/#20241202
- https://agenda.infn.it/event/47630/

Remaining items for SoLID

- GEM readout
  - Faster shaping
- TOF readout
  - Develop front-end with AARDVARC
    - Check radiation hardness
    - Check timing resolution
- Measure PV asymmetry with setup
- Streaming
  - Simulation to estimate ressources and additional costs
  - Development of streaming capable ASICs
  - AIML data reduction
  - Streaming software development (most likely will use ePIC developments)

Conclusion

- SoLID main FADCs available
- Development of GEM readout
  - VMM with higher gain
  - Funding for new GEM chip
  - Upgraded AVP25 option
- Different setup using SoLID developments
  - SBS
  - Moller
    - MAPS readout with VTP
    - Compton
    - Counting DAQ for Q2
  - ESB
    - Deadtime studies
    - GEM VMM readout
  - HKS
    - VTP trigger
    - MRPC
- Investigating streaming option for SoLID