MOLLER Integrating DAQ

Hanjie Liu

On behalf of the Integrating DAQ group

Hall A Winter Collaboration Meeting

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Integrating DAQ Abstract Idea

- Integrating DAQ is the primary data acquisition system used for production data taking.
- Data flow and data structure in the DAQ:
  - The electron beam polarization is flipped at the injector, defining distinct helicity states.
  - Meanwhile, detector signals stream continuously into the DAQ system.
  - The DAQ receives both helicity signals and detector signals. It organizes the detector data according to the helicity state.
  - Each helicity state is subdivided into several integration blocks. For each block, the DAQ records:
    - the sum of ADC samples
    - the number of samples contributing to the sum
- The integrated ADC sum is proportional to the detector response and encodes the physics information of interest

Integrating ADC ---- MOLLERADC

- The MOLLERADC is specifically designed for the integrating DAQ

16 Input channels

TI connection (clock, trigger)

Ethernet connection

Two types of input connectors

Twinax connector --- Differential MOLLERADC

For the integrating PMTs

BNC connector --- Single-ended MOLLERADC

For beamline monitors

Back panel

Power Input

Grounding

Power supply and distribution

Hall A DAQ bunker

- The original plan for Power over Ethernet (PoE) encountered grounding-related issues.
- DC power supplies are used to power the ADCs

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Integrating ADC ---- MOLLERADC

- MOLLER ADC Overview
  - 18-bit, high-impedance ADC with an input range of ±4.096 V
  - Sampling period: 68 ns
- Operating modes:
  - Streaming mode:

    Supports two channels at the full sampling rate for readout (can be prescaled)
  - Reduced streaming mode:

    Supports 16 channels at a reduced sampling rate for readout (can be prescaled)

  Diagnosis and Alignment
  - Integration mode:

    Upon receiving a trigger (either from TI or the onboard input), the ADC integrates over a configurable number of regions, with a configurable number of samples per region

  Production
- Readout architecture:
  - The MOLLERADC operates as an independent Readout Controller (ROC)
  - It can run standalone or as a slave to a VME ROC

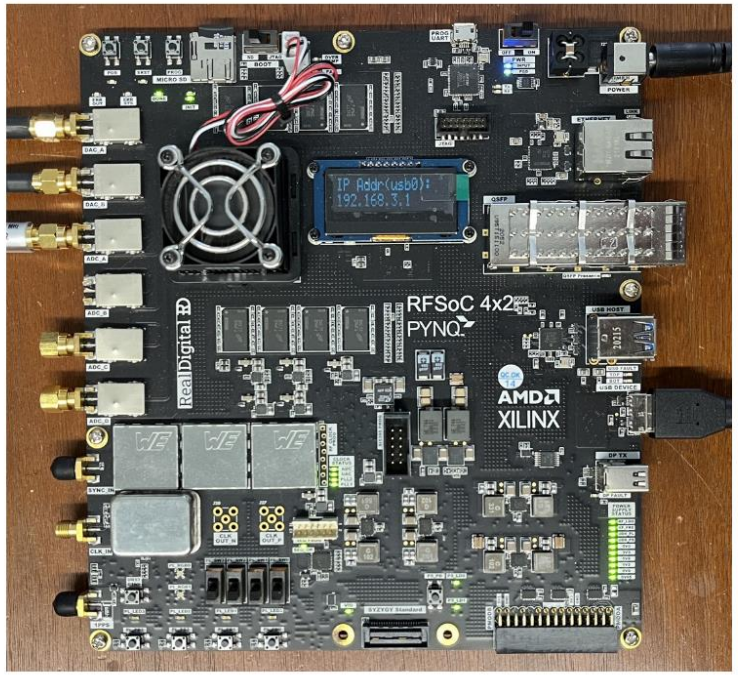
Integration mode channels

- Detector array (280 total)
  - 224 Main detectors, 28 shower-max detectors, 28 pion detectors
- SAMs, LAMs, and beamline (226 channels)
  - SAMs: 8
  - LAMs and diffuse background monitors: 42 (14 LAM + 28 DBM)
  - Injector beamline: 96 ISB building
  - Transport line and Hall beamline: 80
- Scanner (6+7 channels)
  - X/Y scanner: 2 PMTs + 2 position voltages (positions could go into a FADC or VQWK?)
  - Linear scanners: 4 PMTs + 4 position voltages
  - Reference voltage for positions
- Total: 512 channels → 32 16-channel modules
- Digital BCM expect to connect into CODA in same way as ADCs

Slide from Paul King MOLLER collaboration meeting June 2025c

Berkeley Digital BCM

- Based around RFSoC 4x2 (RF System-on-Chip)
  - Xilinx Zynq Ultrascale+ RFSoC FPGA
  - 64-bit Quad ARM Cortex-A53, dual-core ARM Cortex-R5F
  - 4x 14-bit 5 GSPS ADCs with I/Q support
  - 2x 4GB DDR4 (for PL, PS)
  - QSFP (100 Gb/s) interface
  - PYNQ (Python for Zynq) support
- Why use the RFSoC?
  - Improved phase noise → signal down conversion happens digitally in FPGA after sampling at high rates, compare to mixing with analog local oscillator
- RFSoC will sit in chassis repurposed from earlier non-SoC design of receiver
  - Gain control with 30dB amplifier and digital-step attenuators
  - Directional couplers for signal monitoring

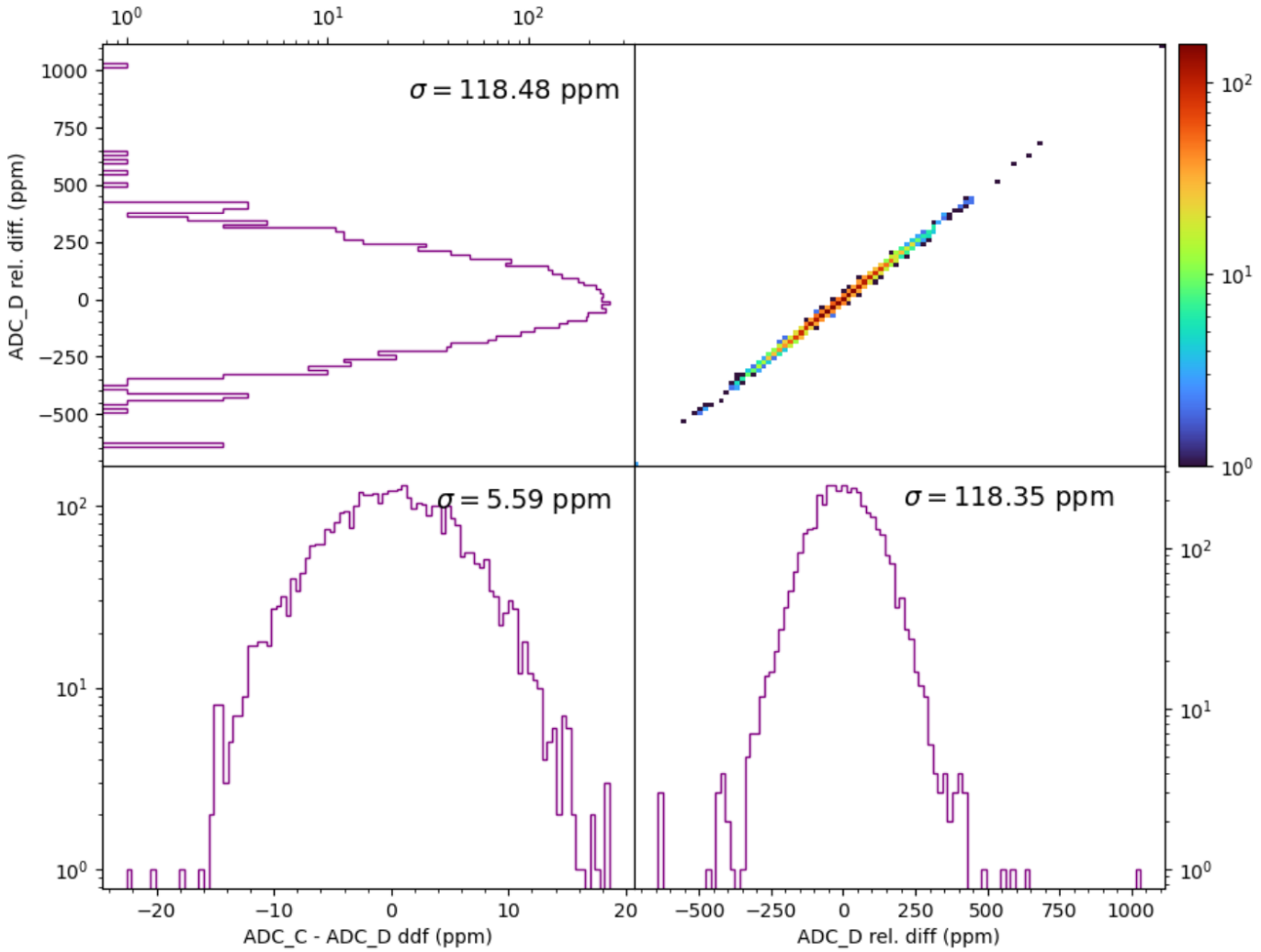


RFSoC 4x2 board

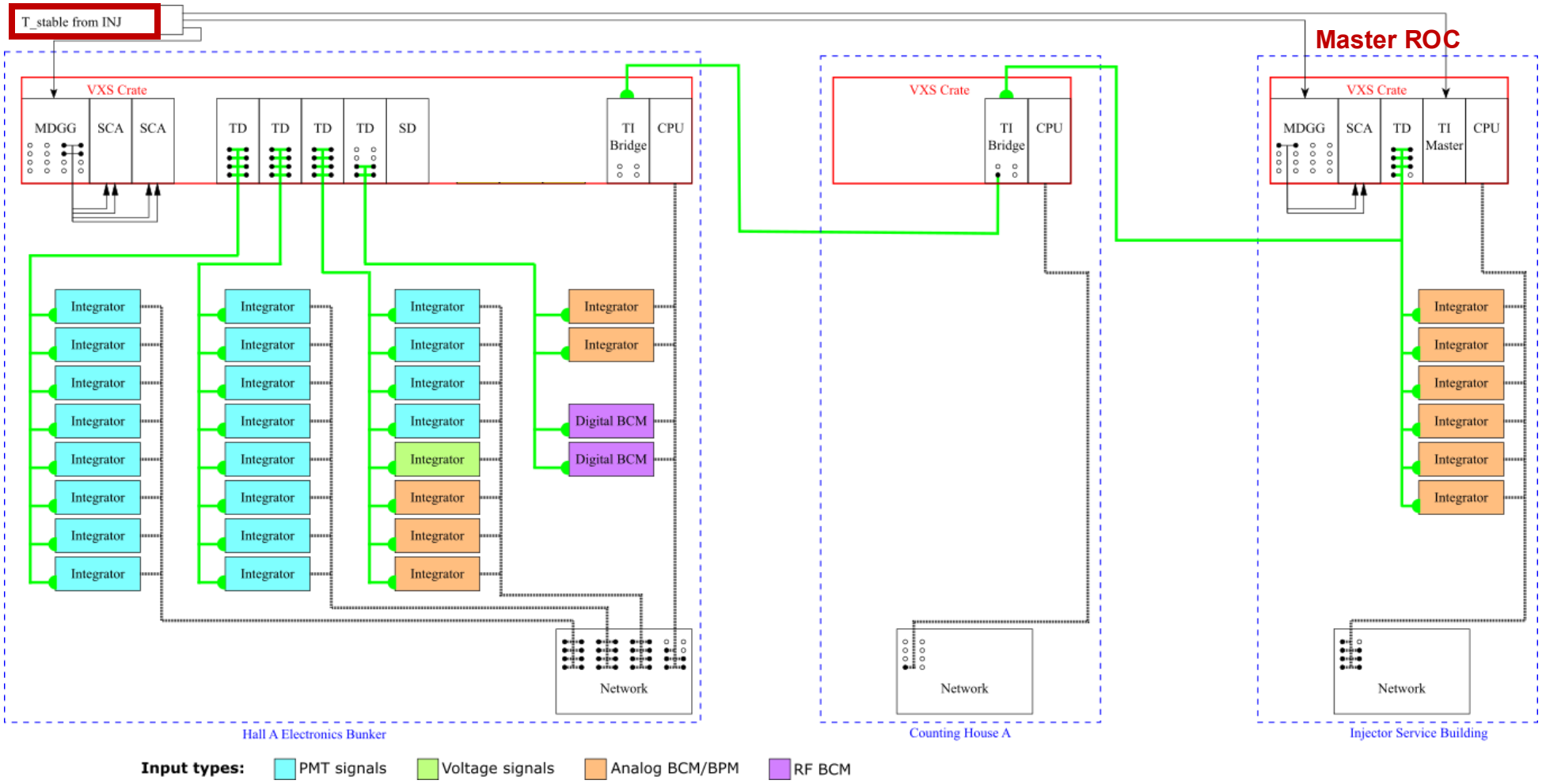
Receiver box

Berkeley Digital BCM (continued)

- Bench test for RMS noise of difference between 1.92 kHz window pairs: **5.6 ppm**
  - RF source was ERASynth+ signal generator split into two ADC channels
  - 320x decimation in firmware, effective sampling 15.625 MSPS
  - No front end amplifiers yet, prior bench tests w/ amplifiers added a few ppm of noise
  - Note: we care about width of noise between two ADCs (ddf) since width of noise in one ADC (rdf) can have fluctuations from signal.
- Next steps: integrate BCM into DAQ
  - Zynq Ultrascale+ FPGA is same class as integrating detector frontend, much firmware can be reused.
  - BCM firmware will integrate TI node directly in firmware with communication on QSFP interface.
  - (Hopefully) beam tests in the spring/summer in Hall C with synchronization to beam helicity signal



Integrating DAQ Layout



- Helicity trigger is formed in ISB
- TI Bridge feeds SD/TDs to distribute gates/triggers
- Helicity signal propagation to the hall is ~2.5 μs.
- At 5th pass, electrons travel to the hall time is ~21 μs
- Gate timing adjusted per module to account for ~20μs electron transit or other signal latencies; need ~0.1μs resolution

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DAQ Installation Status

- At Jlab, there are 20 differential and 12 single-ended MOLLERADCs (+ 2 at the FE group)
- Hall A DAQ bunker:
  - 17 MOLLERADCs (5 SE and 12 DF) are installed, out of 26 (5 SE+21 DF) MOLLERACs needed in the hall
  - One VXS crate is installed
  - A network switch and a fiber patch panel are installed
- PXE boot is set up at the Hall A machines; all installed MOLLERADCs are up and communicable.
- CODA configuration is set up and can take runs.
- The network and fiber installation at the ISB is on-going

MOLLERADC Testing Status

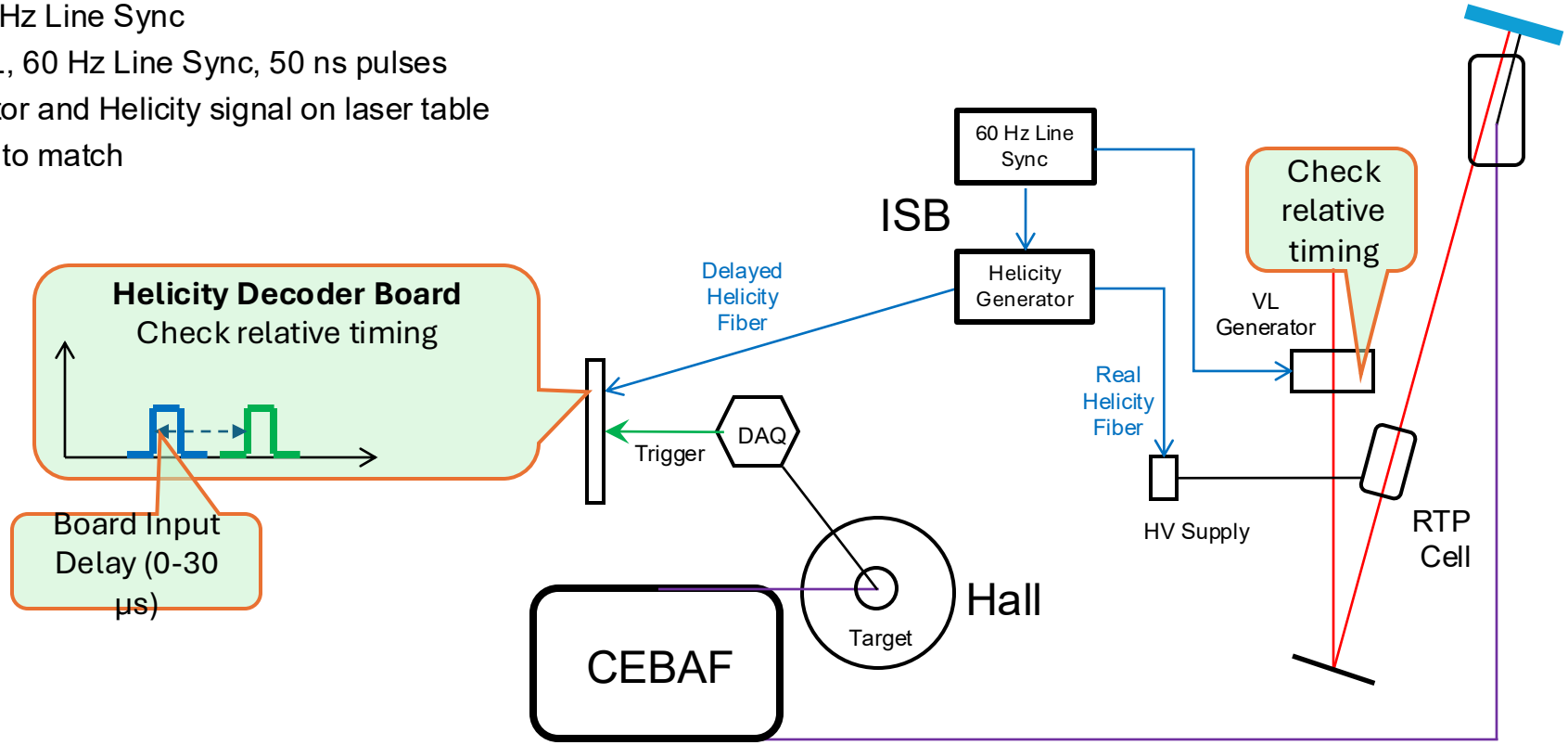
- All the MOLLERADCs are tested in Manitoba before arriving at Jlab
- Our goal is to integrate the MOLLERADCs into the CODA system and verify their performance
- A test stand is set up at the test lab including:
  - One VXS crate
  - Two SE MOLLERADCs, 3 DIFF MOLLERADCs
- An EVIO decoder is developed that is independent of Japan-MOLLER --- plan to use it as the streaming mode decoder
- The streaming firmware:
  - Became available in September
  - MOLLER ADCs run as standalone ROCs in CODA
  - Basic characterization tests—such as baseline, linearity, and bandwidth measurements—were performed → results look reasonable
- The integrating firmware:
  - Became available in November
  - MOLLER ADC runs as a slave ROC to the VXS ROC in CODA, with the MPS signal used as the trigger
  - Basic data sanity checks were performed.

Near future goal and plans

- KPP due in the near future:
  - Demonstrate the full DAQ system running
  - Demonstrate the data throughput at the 1.92 kHz helicity rate
- Perform ground loop testing at the W&M setup
- Characterize the integrating DAQ performance
  - Develop gate alignment procedure between the ISB and Hall A, and among different MOLLERADCs
  - Perform helicity correlated noise characterization
  - Set up the ET system interface with online monitoring

Adjusting for electron travel time

- With 10-20 μs T_Settle time, travel time from photocathode to Hall target becomes relevant. At 5th pass, travel time is ~21 μs. Helicity signal propagation to the hall is ~2.5 μs.
- How to set input time delays:
  - Helicity Board: 60 Hz Line Sync
  - Electron Beam: VL, 60 Hz Line Sync, 50 ns pulses
  - Check VL Generator and Helicity signal on laser table
  - Adjust gate timing to match



Slide courtesy of R. Suleiman

Helicity windows and patterns

- The start of the stable window in the INJ DAQ will be used as the master trigger
  - If the signal latency feeding the INJ ADCs is not long enough for us to use the start of Tstable as the start, we will use a delayed copy of the start of the settle period as the master trigger
- Each ADC will start its integration when it receives its copy of the master trigger
- Possible helicity timing for 1919.938 Hz
  - 500.85 μs stable, 20 μs settle
  - 7364 14.71-MHz samples (1841/block)
  - Patterns of 64 windows span ~1/30 s
- Raster frequency example: ~23040 Hz & ~24960 Hz
  - Per window: 12 X cycles, 13 Y cycles, one pattern