

Streaming Readout PET

LDRD Q2 Report – May 1, 2025

Cameron Clarke, BRIC Staff Scientist
Radiation Detector & Imaging (RD&I) Group



Biomedical Research
& Innovation Center



Q2 ACCOMPLISHED GOALS

A) Detector prototype development

- Design concept for v2.0 front end layout
- Iterated design for best thermal/light isolation
- Stagnated due to Ben Raydo's work in Hall A
- Work is proceeding in Q3 – PCB print soon

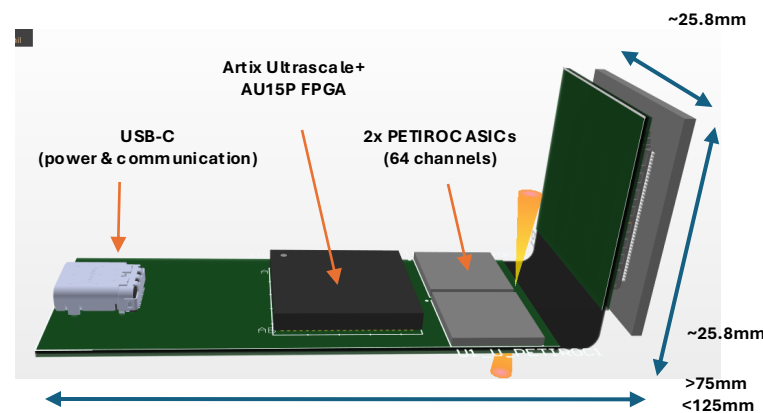
B) SRO data processing system development

- Successfully factorized analysis into ERSAP
- See improved multi-threading performance

C) Broader scope project work

- Provisional patent filed, IEEE MIC Abstracts
- Parts ordering – ASICs and Network Switch
- Parts ordering NEW – SiPMs
- Alternate LYSO supply secured

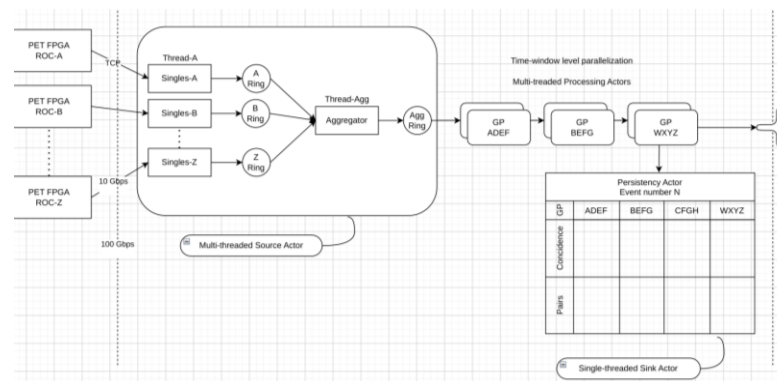
Q1 Starting Points



Potential Detector Front-end Electronics v2.0

Q2 Implementation Progress

- Fleshed out geometry constraints
- Purchased SiPMs (accelerate schedule – supply chain concerns)
- Located alternate LYSO Scintillator Crystal supply



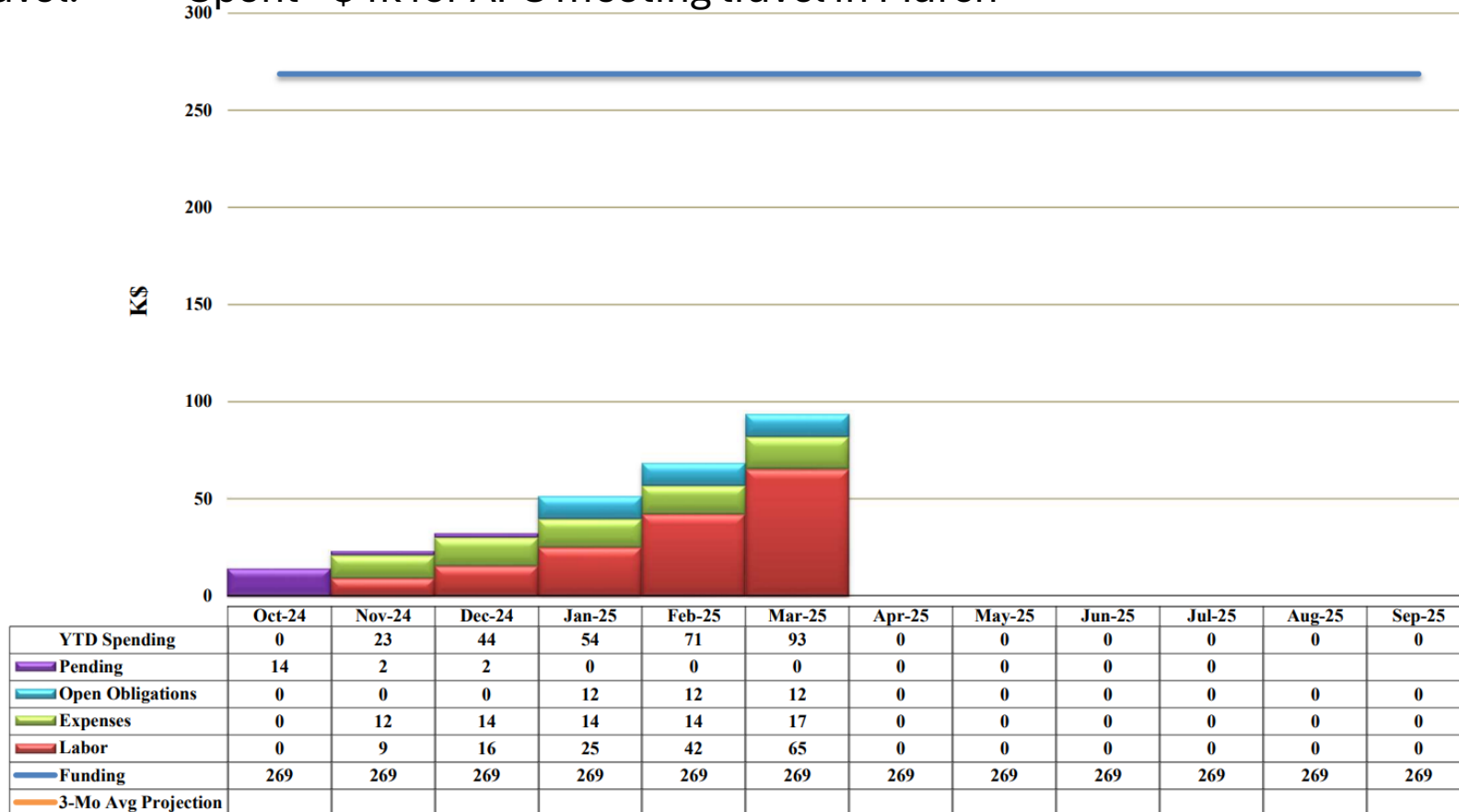
Potential Time-window interleaving ERSAP Architecture

- Factorized data processing into ERSAP
- Demonstrated improved multi-threaded performance
- Begin TCP-stream simulators work

SPENDING

- Spending is generally on target – slower progress due to beam-operations holding up Front-End work

- 1) Labor: Spent ~\$40k on labor direct, \$63k loaded
- 2) Equipment: Spent ~\$12k on ASICs for detector front end, pending:~\$11k for network switch, ~\$11k SiPMs
- 3) Travel: Spent ~\$4k for APS meeting travel in March



BACKUPS

DELIVERABLES

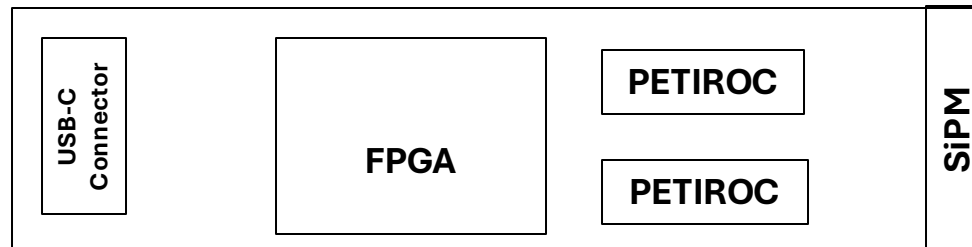
Deliverables – milestones and timeline:

- Three primary aims
 - 1) Implement ERSAP to existing SRO PET detectors, DAQ, and analysis system in FY 25
 - 2) Design and build improved version of modular PETIROC ASIC PET detectors in FY 25
 - 3) Deploy detector array, perform imaging and parallelized scaling tests with distributed computing in FY 26

Year 1			Year 2		
1)	Implement ERSAP in FY 25: ☐ (✓) Implement FPGA based PETIROC signal digitization ☐ (✓) Factorize analysis components into ERSAP microservices ☐ (✓) Reproduce old system performance with ERSAP system ☐ Develop vertical multi-threaded, horizontal multi-node scaling	FY 2025: • Month 3 • Month 6 • Month 9 • Month 12	3)	Deploy detector array, imaging and parallelized scaling tests in FY 26: ☐ Procure and test new detector front-ends ☐ Integrate modular 8-detector array with new SRO system ☐ Verify detector and imaging performance for new system ☐ Deploy the system and perform phantom imaging tests at UMAB ☐ Finalize reports on local and farm streaming scalability tests	FY 2026: • Month 3 • Month 3 • Month 6 • Month 6 • Month 12
2)	Design and build modular PETIROC ASIC PET detectors in FY 25: ☐ (✓) Optimize FPGA multi-detector readout firmware ☐ (✓) Optimize detector power supply and readout cabling ☐ (X) Design and order new PETIROC modular detector PCBs ☐ Get electronics parts, build, and test 8 new detector front-ends	FY 2025: • Month 3 • Month 3 • Month 6 • Month 12			

DETECTOR PROTOTYPE DEVELOPMENT

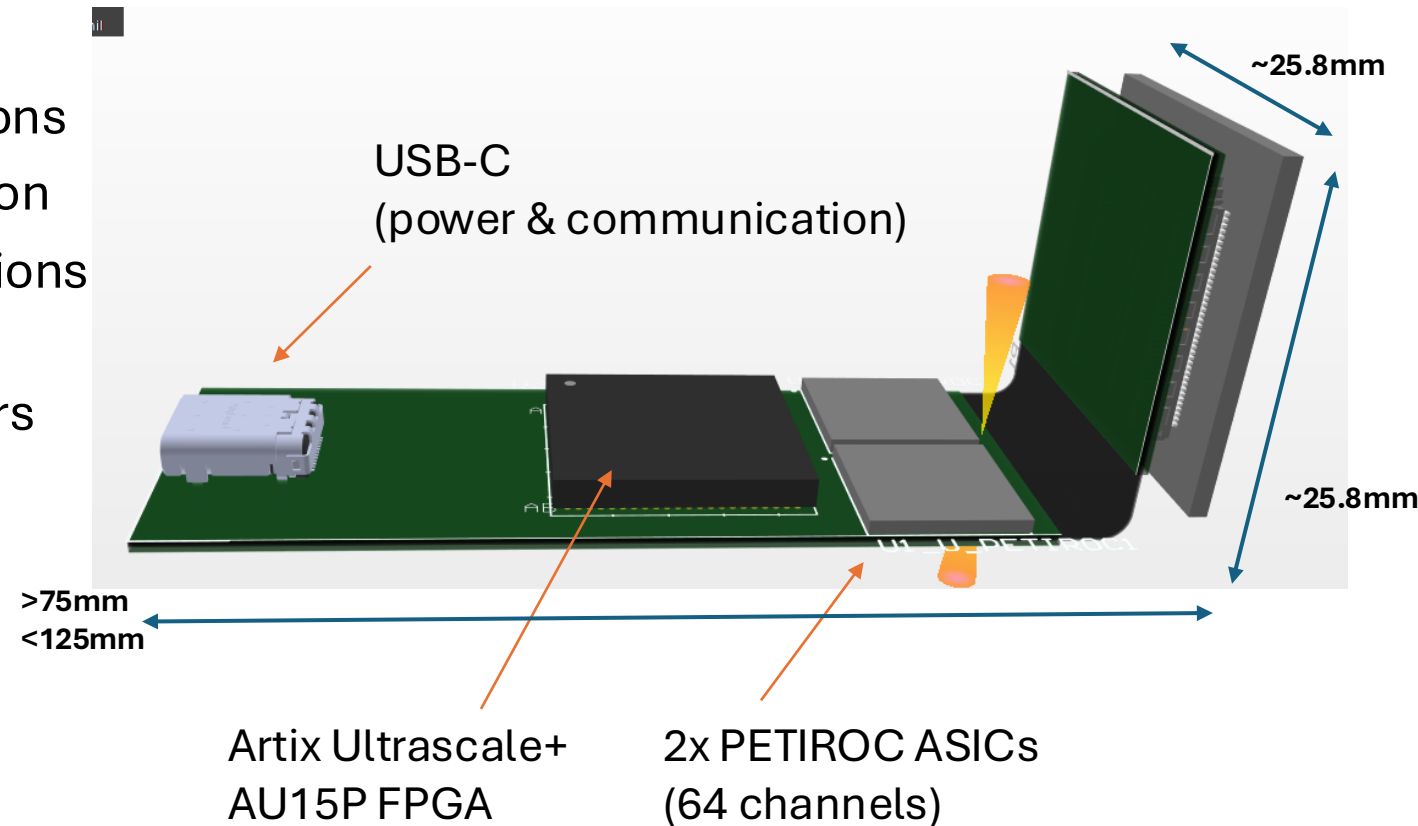
- Debugged existing prototype FPGA firmware
 - Issue with missing TCP packets/bad ethernet cable – removed bad cable
 - Implemented 10-Gig firmware wrapping around existing 1-Gig hardware
- Implemented off-ASIC ADC firmware
 - Implemented FPGA firmware to bypass PETIROC digitization, using faster on-board ADC now
- Designed concept for v2.0 front end layout
 - Modular detector design – locks in design choices for v2.0



DETECTOR PROTOTYPE DEVELOPMENT

- Designed concept for v2.0 front end layout

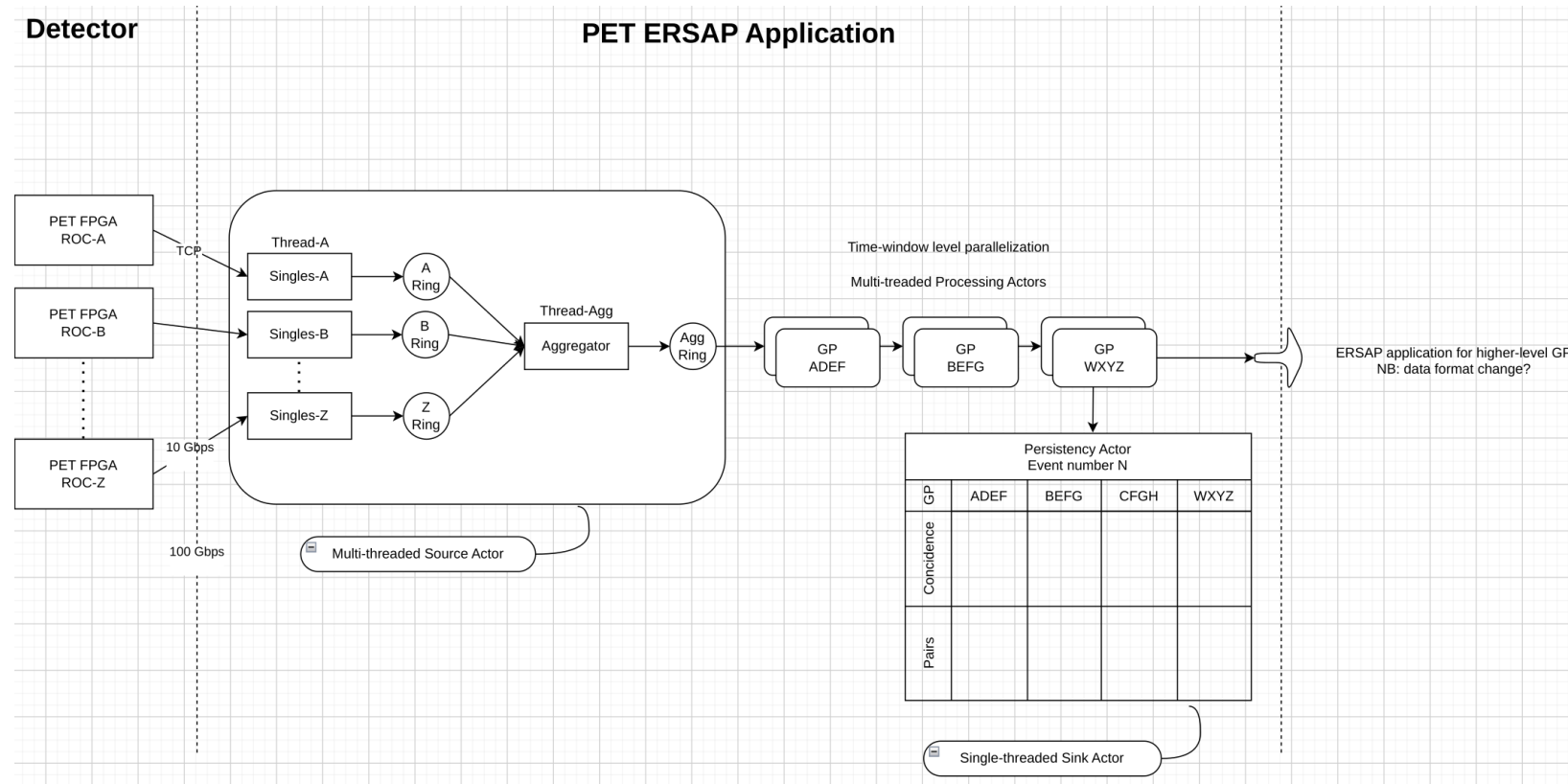
- Modular detector design
- Aiming for 4-side buttable
- SiPM and scintillator separated
- Flex cable permits multiple orientations
- & permits thermal and optical isolation
- USB-C connector simplifies connections
- Communication board (not shown) synchronizes and powers all detectors



SRO PLATFORM DEVELOPMENT

- Explored SRO analysis architecture options

- Event-based processing from FPGA
- Time-windowing at singles or geometry processor
- Potential for time-windowing in the FPGA
- Updated diagram for one potential architecture
 - All time-interleaving in a single actor option



- Finalized ERSAP-based software development

- Completed GitLab CD/CI implementation
- Finished converting KMax singles and geometry processors into ERSAP actors

BROADER PROJECT GOALS

- Invention Disclosure, APS Abstract, next IEEE Abstracts
 - Received provisional patent from USPTO
 - Presented summary talk and poster at 2025 APS Global Summit
 - IEEE 2025 Yokohama Japan Abstracts – SRO PET System and ERSAP-microservices abstracts
- Parts ordered
 - Purchased ASICs for 8+1 detectors
 - Purchased SiPMs for 8+2 detectors
 - Located alternate supply of LYSO crystals (supply chain concerns)
 - Purchased network switch (supply chain concerns delays into July)

SUMMARY

- We are on track to meeting deliverable goals
 - SRO platform development is proven, under iterative refinement
 - Detector front-end design work is underway, finishing up the details now
 - Sub-contracted imaging studies are on track for FY26
 - Talks at conferences are being planed