FY25Q2 Project Status

ID	Task	status	Comments
M15	Establish general framework for RTDP simulation	■	Significant work started on this, but not fully completed
M16	Create configurable CPU proxy component	✓	Fully configurable via command line
M17	Create configurable GPU proxy component (hardware and software)	✓	Working component in repository and tested using sciml nodes.
M18	Create configurable FPGA proxy component (hardware and software)	■	Initial R&D into Vitas. Plan for gaining access to U280 FPGA from EJFAT for hardware.
M19	Create functioning hardware GPU component (e.g., CLAS12 L3)		
M20	Create functioning hardware FPGA component (e.g., ML4FPGA)		
M21	Configure simulation of full SRO system using existing JLab hardware resources	■	Simple system using cylc exercised. Scaling to more complex configuration before milestone can be satisfied.
M22	Establish working test of system that transfers >=100Gbps from CH to compute center		
M23	Establish working test of system that includes GPU component for portion of the stream		
M24	Establish working test of system that includes FPGA component for portion of the stream		
M25	Test system with remote compute facility (e.g., BNL or NERSC) at limits of available resources		
M26	Configure system that results in stream(s) being received by JLab from external source		
M27	Collaborate with HPDF group to evaluate processing SRO data at JLab for external experiments		
M28	Complete documentation for platform to be used by non-experts		

Major Highlights

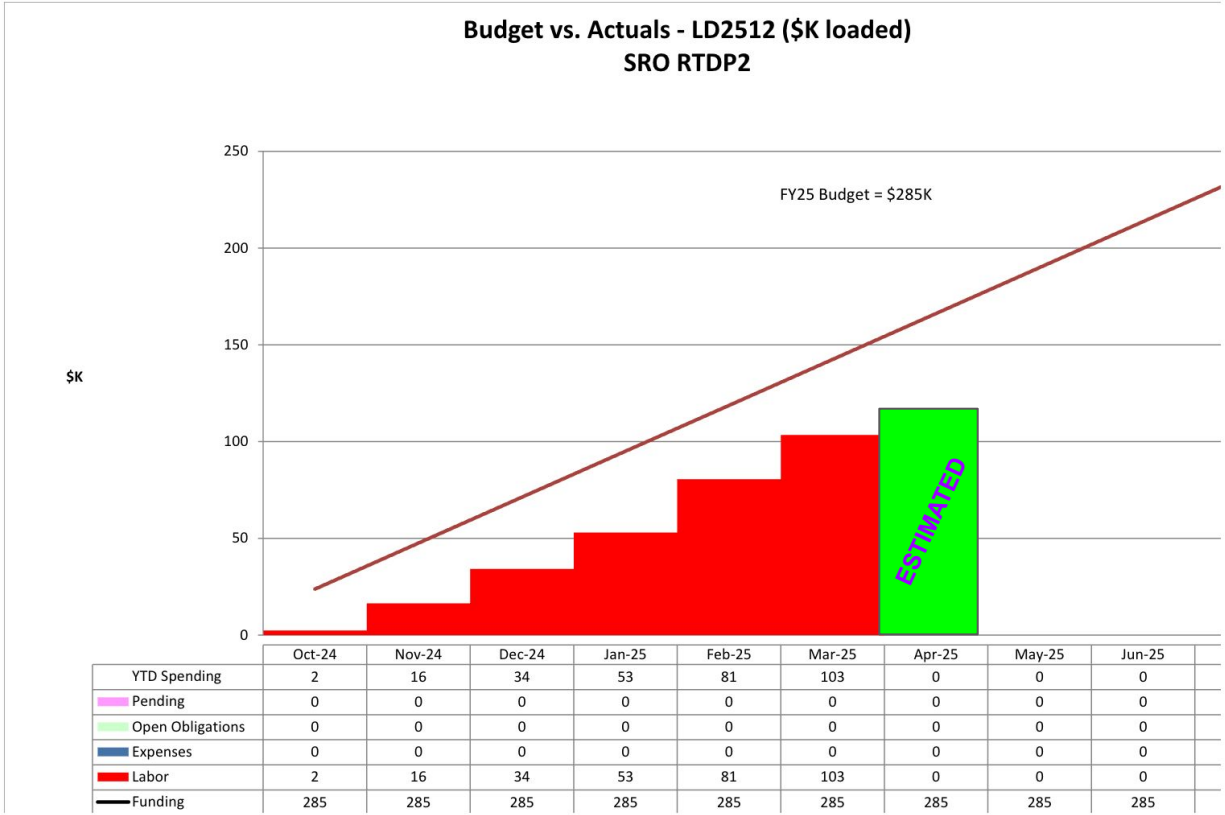
Work during FY25Q2 focused on development of proxy components for the system. These are software components that can simulate or actually use specific compute hardware for the simulation of a streaming system. The components have the ability to transfer data between them using zeromq.

Some work was also done to feed the data acquired during the CLAS12 packet capture exercise into CLAS12 reconstruction. This has turned out to be considerably more complex than anticipated so reconstructed calorimeter showers have still not been achieved.

The major highlights are:

- Configurable CPU proxy component completed
- Configurable GPU proxy component completed
- R&D started on configurable FPGA component

Budget



	Oct-24	Nov-24	Dec-24	Jan-25	Feb-25	Mar-25	Apr-25	May-25	Jun-25
YTD Spending	2	16	34	53	81	103	0	0	0
Pending	0	0	0	0	0	0	0	0	0
Open Obligations	0	0	0	0	0	0	0	0	0
Expenses	0	0	0	0	0	0	0	0	0
Labor	2	16	34	53	81	103	0	0	0
Funding	285	285	285	285	285	285	285	285	285

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Personnel adjustments have been made with new time assignments that should spend out remaining funds by end of FY25.

assigned FTEs for Q3-Q4		*RTDP
Goodrich	**Michael**	67%
Gyurjyan	**Vardan**	20%
Lawrence	**David**	25%
Tsai	**Jeng**	40%