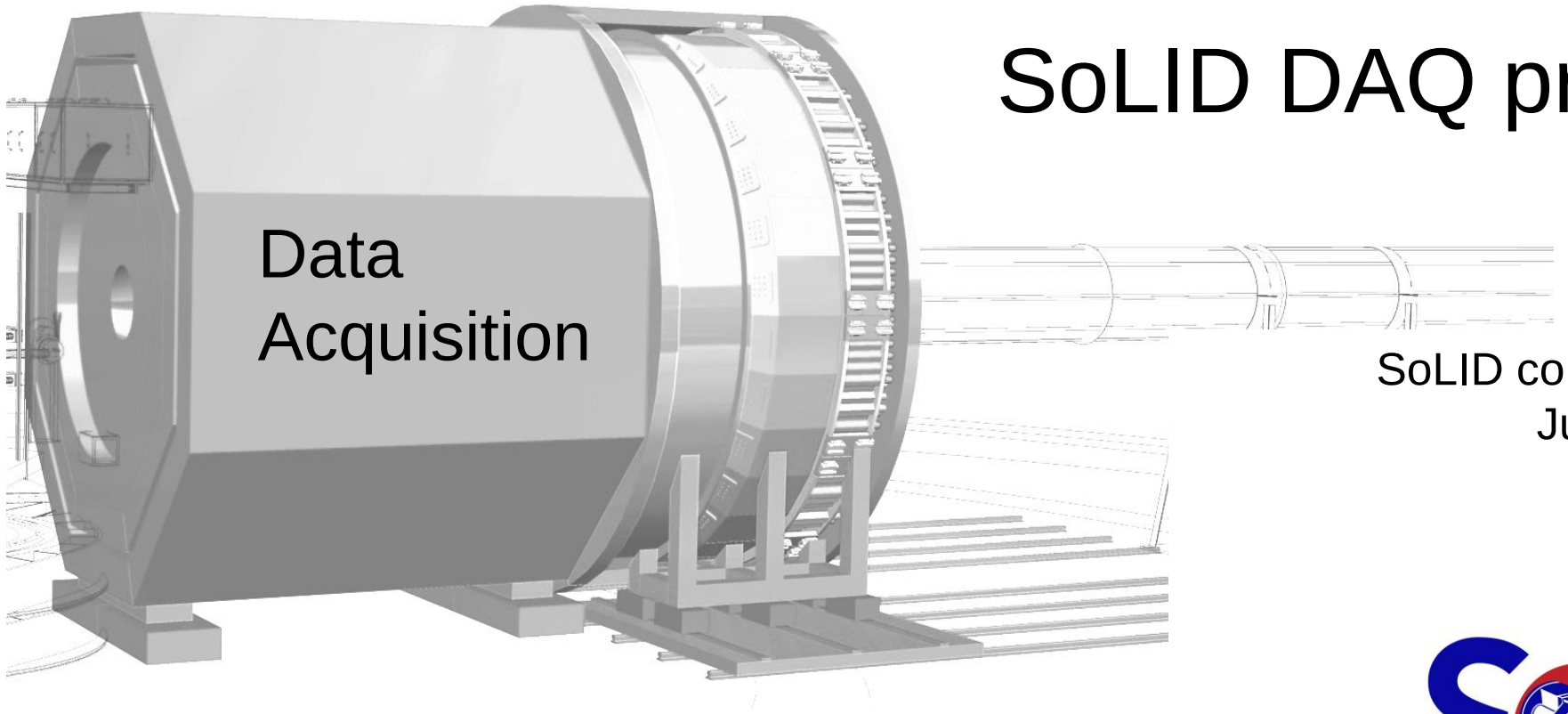



# SoLID DAQ preRD and plans

SoLID collaboration meeting
July 7th 2025

Alexandre Camsonne

- Outline

  - Capital
  - Testing
  - GEM readout
  - Beam Test preparation
  - HKS

  - Conclusion

# Capital equipement DAQ

## Requested

| Item | cost/item | number | total |
|---|---|---|---|
| FADC 250 | 6000 | 104 | 624000 |
| Gigabit serial connectors | | | 40000 |
| Cables | 100 | 1664 | 166400 |
| VETROC | 4000 | 30 | 120000 |
| TD | 3000 | 16 | 48000 |
| VTP | 10000 | 31 | 310000 |
| SSP | 5000 | 4 | 20000 |
| VTP | 8000 | 1 | 13000 |
| TS | 4000 | 1 | 4000 |
| TID | 3000 | 31 | 93000 |
| SD | 2500 | 32 | 80000 |
| VXS crate | 15000 | 32 | 480000 |
| VME CPU | 7000 | 32 | 224000 |
| | | Total | 2217400 |

## Updated

| Item | cost/item | number | total |
|---|---|---|---|
| FADC 250 | 6127 | 104 | 637208 |
| Gigabit serial connectors | 40000 | 1 | 40000 |
| Cables | 100 | 1664 | 166400 |
| VETROC | 4000 | 30 | 120000 |
| TD | 3000 | 16 | 48000 |
| VTP | 12500 | 31 | 387500 |
| SSP | 5000 | 4 | 20000 |
| VTP | 12500 | 1 | 12500 |
| TS | 4000 | 1 | 4000 |
| TID | 3000 | 31 | 93000 |
| SD | 2500 | 32 | 80000 |
| VXS crate | 19000 | 32 | 608000 |
| VME CPU | 9500 | 32 | 304000 |
| | | Total | 2520608 |

## Received

| Item | cost/item | number | total |
|---|---|---|---|
| FADC 250 | 6127 | 104 | 637208 |
| Gigabit serial connectors | 40000 | 1 | 40000 |
| Cables | 100 | 1664 | 120000 |
| VETROC | 4000 | 30 | 120000 |
| TD | 3000 | 16 | 48000 |
| VTP | 12500 | 31 | 387500 |
| SSP | 5000 | 4 | 20000 |
| VTP | 12500 | 1 | 12500 |
| TS | 4000 | 1 | 4000 |
| TID | 3000 | 31 | 93000 |
| SD | 2500 | 32 | 80000 |
| VXS crate | 19000 | 32 | 608000 |
| VME CPU | 9500 | 32 | 304000 |
| | | Total | 2520608 |

Plan to postpone cables to order computer and network switch to complete
ESB testing of deadtime and streaming
Buy new XVB603 CPU for VME320 readout

# Remaining tests for SoLID DAQ

- Achieve 100 KHz trigger rate for SIDIS
- Measure asymmetries at ppm level with full system for PVDIS

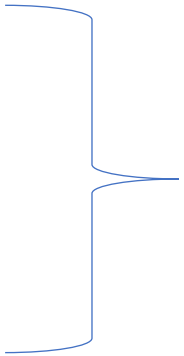
- Achieve 150 ps with TOF scintillator
- Achieve 25 ps timing resolution with MRPC
- Show full tracking efficiency above 85% level in full background
- Gas Cerenkov efficiency

# Future SoLID preRD

- Highest priority : GEM chip
  - 1) develop VMM optimized for  GEM and uRWell with higher gain ( 500 K$ )
  - 2) Continue testing VMM board signal to noise
  - 3) Evaluate SALSA chip in high background environment
  - 3) Find funding to develop dedicated ASIC chip for GEM ( ~ 2.5 M$ )
  - Test with uRWell
- Calorimeter and Cerenkov readout
  - FADC ASIC to be placed on detector : only LV and optical fibers going out instead of BNC cables
- High resolution timing
  - AARDVARC test in beam
  - High resolution FADC timing ASICS
  - Timing distribution with CODA
- Measure physics asymmetries ( Hall C? )

# Testing

- SBS GEn
  - VTP readout
  - APV25
  - High data rate : 2.1 GB/s
- NPS
  - Calorimeter trigger
- SBS GEp
  - Calorimeter trigger
  - Data rate : 2.5 to 3 GB/s
  - GEM readout experience
- Moller
  - Compton
  - Counting DAQ
- HKS
  - Trigger with Cerenkov
  - High resolution TOF with MRPC
- Hall C experiments in HMS and SHMS : measure physics asymmetries : VTP in HMS/SHMS
- Future parasitic beam tests
  - FADC + VTP + VETROC + VMM in on crate for testing : PVDIS one crate setup available with calorimeter and Cerenkov trigger
  - Acquired SAMPIC 64 channels sampler for MRPC
  - APV25 available after GEp5
- ESB
  - Test V3 FADC
  - VTP trigger
  - GEM readout
  - Deadtime and max trigger rate



Calorimeter trigger

# GEM SBS experience

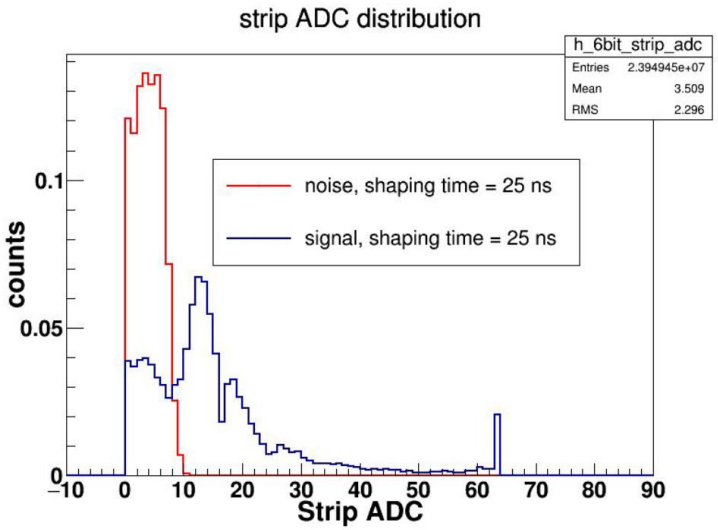
- Experiment supposed to run at 30 uA
- DAQ rate limited to 3 or 4 KHz for high live time ( above 85% )
- Data rate limited to 3 GB/s

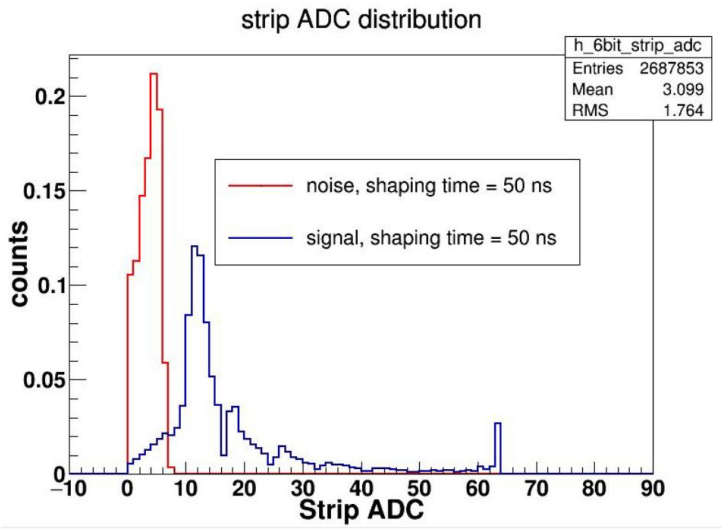
- Currently running at 20 uA limited by tracking efficiency
- Limited by data rates if going to 30 uA or more but firmware being developed to reduce data rate by 3
- Need to determine if occupancy higher than expected
- Possibly AIML based tracking might be more efficient
- VTP bugs ironed out : about 1 GEM crash every two hours – not clear if APV or MPD upsets
- High granularity and faster shaping time would have been helpful
- Unclear if experiments are possible with 1 time sample – currently reading 6 time samples

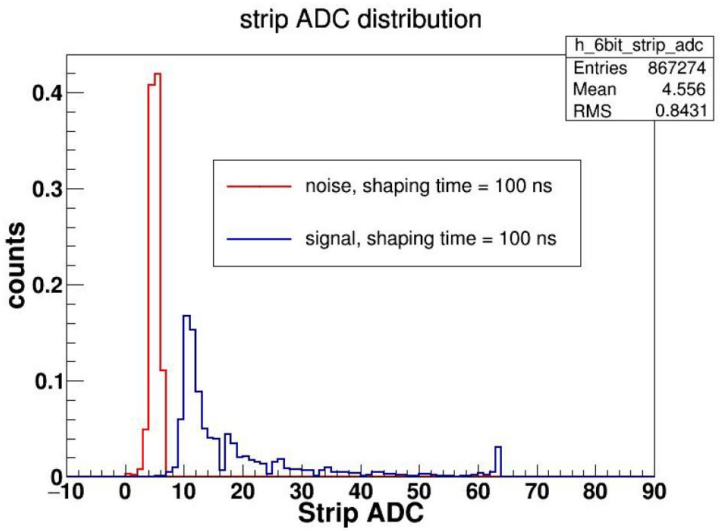
# VMM test

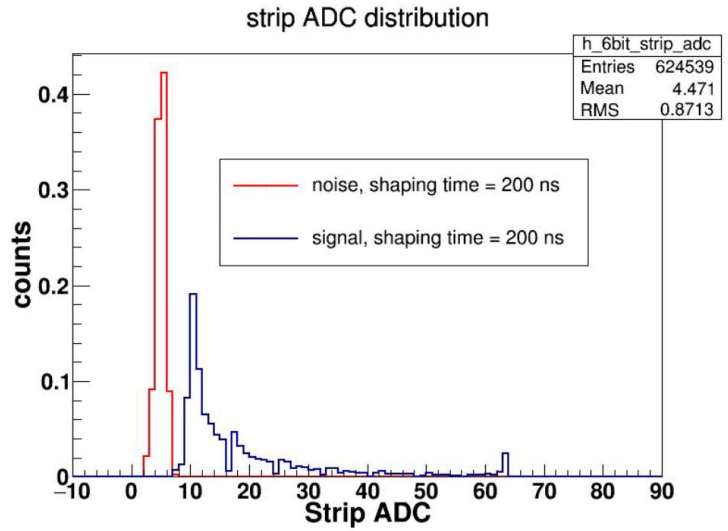
- Ordered two test board 1500 $ x 2
- Build 6 SoLID prototype boards
- Evaluation board : can look at data with detector small subset of channels
  - Issue with external trigger but waiting for new firmware
  - Can check pedestal width
  - Signal to noise with detector with source and cosmics
  - Look at direct readout signals for 12 channels of detector

# Noise 6 bit 16mV/fC Sr90




- Amplitude for MIP not change much
- Pedestal width dependent on peaking time

# Conclusion VMM testing so far

- 90 ns dead time in 6 bit mode
- Some noise seen in prototype
- Noise larger with decreasing integration time
- MIP a bit low in dynamic range of 6 bit prototype
- Implementing 10 bit to cross compare with evaluation board
- 250 ns for 10 bit mode
- Investigating new VMM with high gains for GEM and uRWell ( ~500 K$) Hall B interested, need to reach out to SRS community
- Need implement Rad Hard DC DC converter and lpGBT radiation hard readout

# Salsa

- Collaboration of Irfu CEA Saclay and U. of Sao Paulo.
- SALSA

- 64-Ch, updated design from SAMPA V5, migrating to 65 nm CMOS.
- Peaking time: 50 – 500 ns
- Inputs: Cin optimized for 200 pF; Rates: 25 kHz/Ch; Dual polarity.
- ADC: 12 bits, 10 – 50 MSPS.
- Extensive data processing capabilities.
- Triggerless and triggered operation.
- Power: 15 mW/Ch
- Gbps links.
- I2C configuration.

- Evaluation board available this year - Might want a dedicated SoLID version to match tracker low gain operation and handle high rates at input
- Can bypass analog part but need to develop analog front end
- Data links somewhat limited

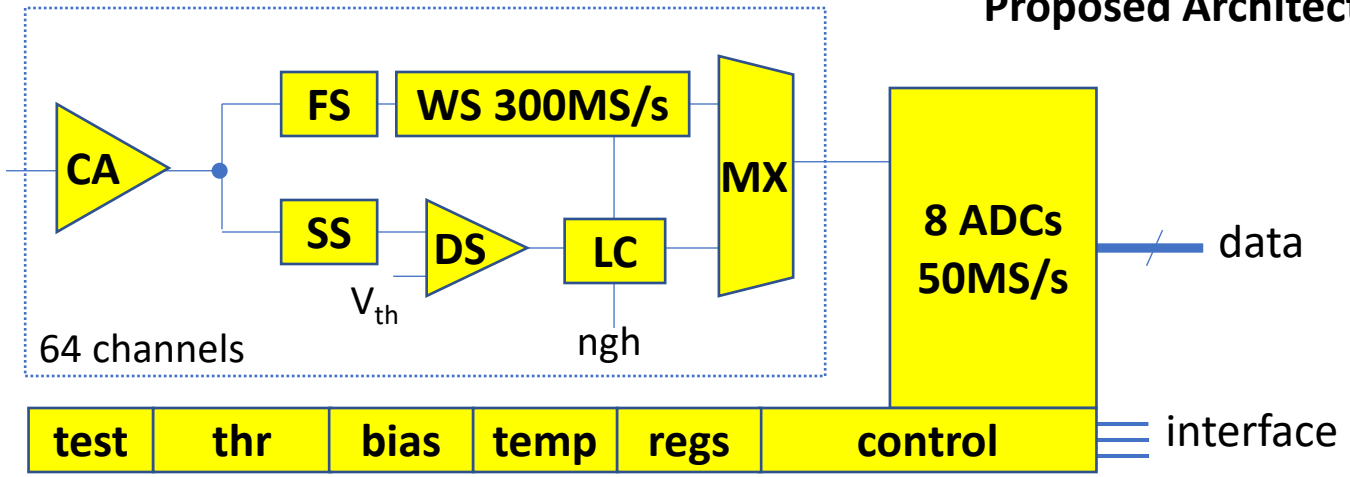
- Might want a dedicated version of SALSA

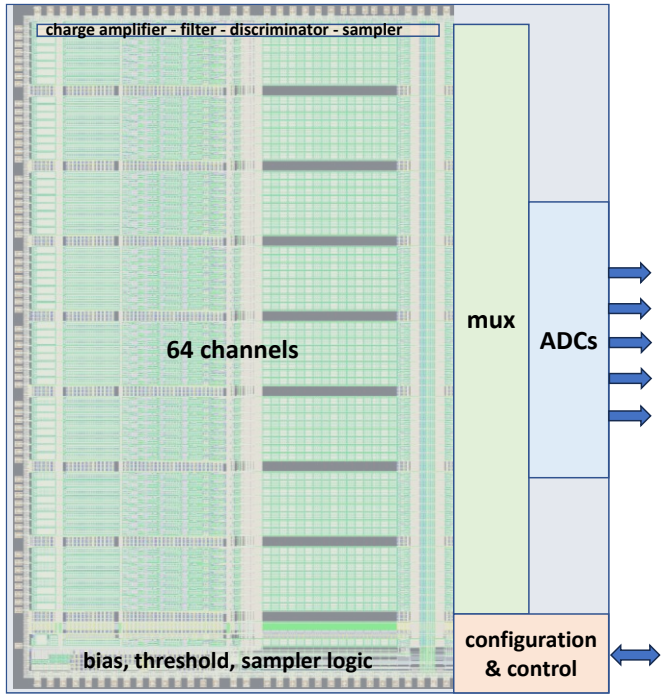
# New potential dedicated ASIC

- High luminosity running need to run
- Pile-up and deadtime can be significant

- Dedicated chip
  - Optmized gain and dynamic range
  - Optimize shaping time for high rate operation : from 50 ns to 25 ns or better
  - Zero dead time
  - High speed links to allow streaming

# Proposed Architecture




**CA: charge amplifier**
- optimized for 50-200pF
- programmable gain 25fC to 250fC

**FS: fast shaper**
- programmable 5-20ns

**SS: slow shaper**
- for discrimination (zero suppression)
- programmable 20-100ns

**DS: discriminator**
- trimmable per channel
- external trigger option

**WS: waveform sampler**
- 128 sampling cells (127 effective)
- continuous sampling until trigger
- 300MS/s → ~ 400ns waveform
- programmable pre-post trigger samples

**LC: local control logic**
- internal or external trigger
- neighbor (sub-threshold) logic

**ADCs**
- 8 operating at 10-bit 100MS/s
- waveform conversion time ~ 2.5µs

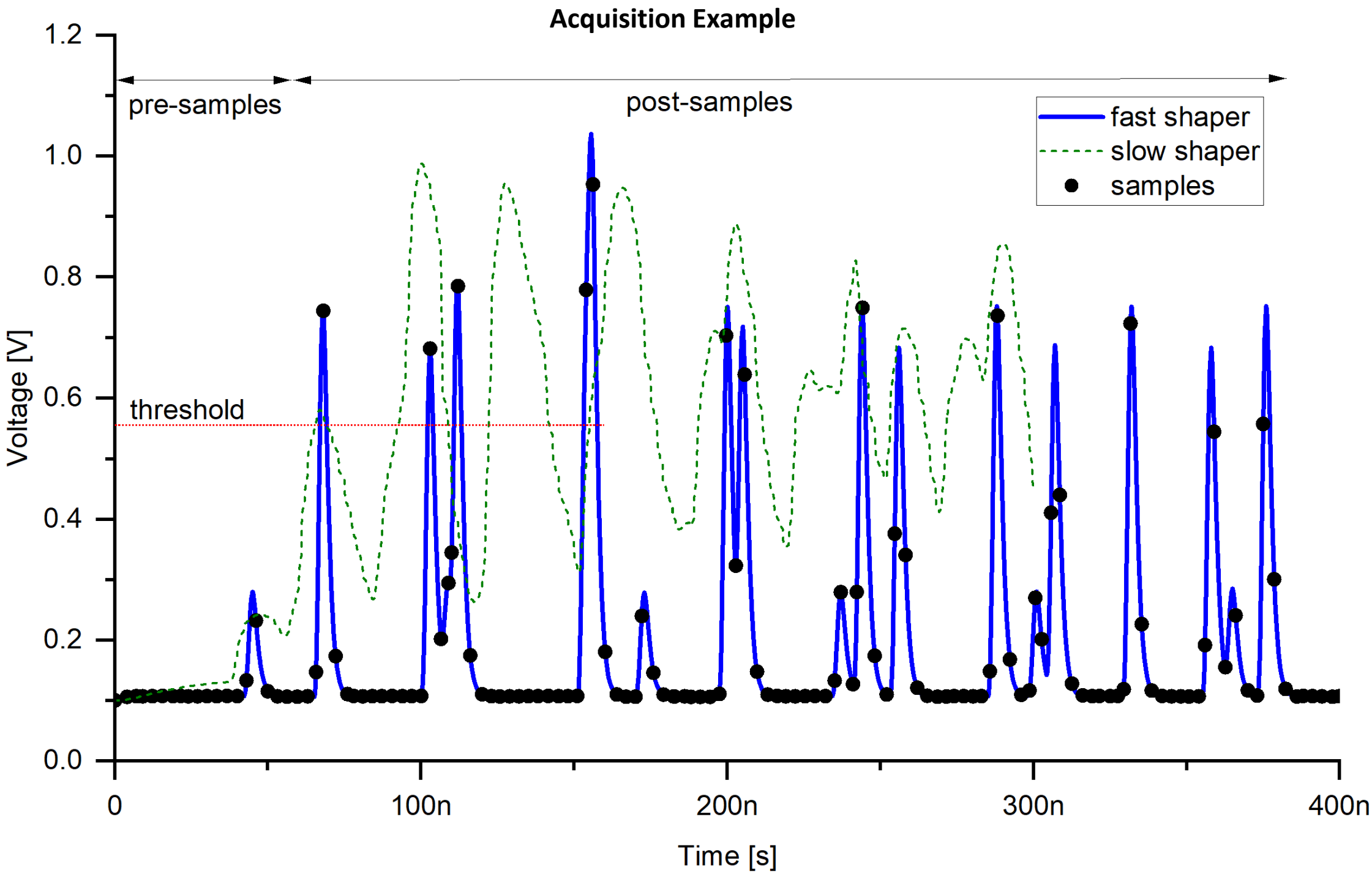
**Data**
- channel, trigger, 127 samples = 1,280 bits per waveform
- up to 8 waveforms with sub-threshold neighbors = 10,240 bits
- up to 8 SLVS outputs operating in DDR at ~ 500MS/s
- conversion/readout time (dead time) ~ 2.5µs per event
- maximum event rate ~ 330kHz
- maximum data rate ~ 4Gb/s

**Architecture**
- event-driven analog/digital with acquisition/readout
- SEU tolerant register and logic
- DSP-ready

**Power, Size, Technology, Schedule**
- power consumption below 3mW/channel
- anticipated die size ~ 6x8 mm²
- technology TSMC 65nm 1.2V
- development time ~ 24 months (1st proto in 12 months)

**Design**
- charge amplifier, shapers and samplers based on verified architectures
- ADCs from collaborative effort
- first prototype design time
  - ~ 12-13 months plus ADCs
  - ADC can be parallel effort
- second prototype design time
  - ~ 4-5 months

**Key Features**
- power-efficient analog zero-suppression
- efficient data generation and transfer
- highly flexible, highly programmable


Acquisition Example
pre-samples
post-samples
fast shaper
slow shaper
samples
threshold
Voltage [V]
Time [s]
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0
100n
200n
300n
400n

# APV25 new MPD

- Upgrade MPD from 100 MBit to 10 GBit ethernet
- Should give max rate from APV25
- Need to improve DAQ stability
  - Not clear if
    - APV single upsets
    - MPD upsets
    - Others ( VTP )

# GEM new simulation work

- Estimate rates and occupancies with new shaping and sampling electronics
- Optimize segmentation of chambers to avoid
- Explore pads readout chamber to complement high rate tracking

# Beam test preparation

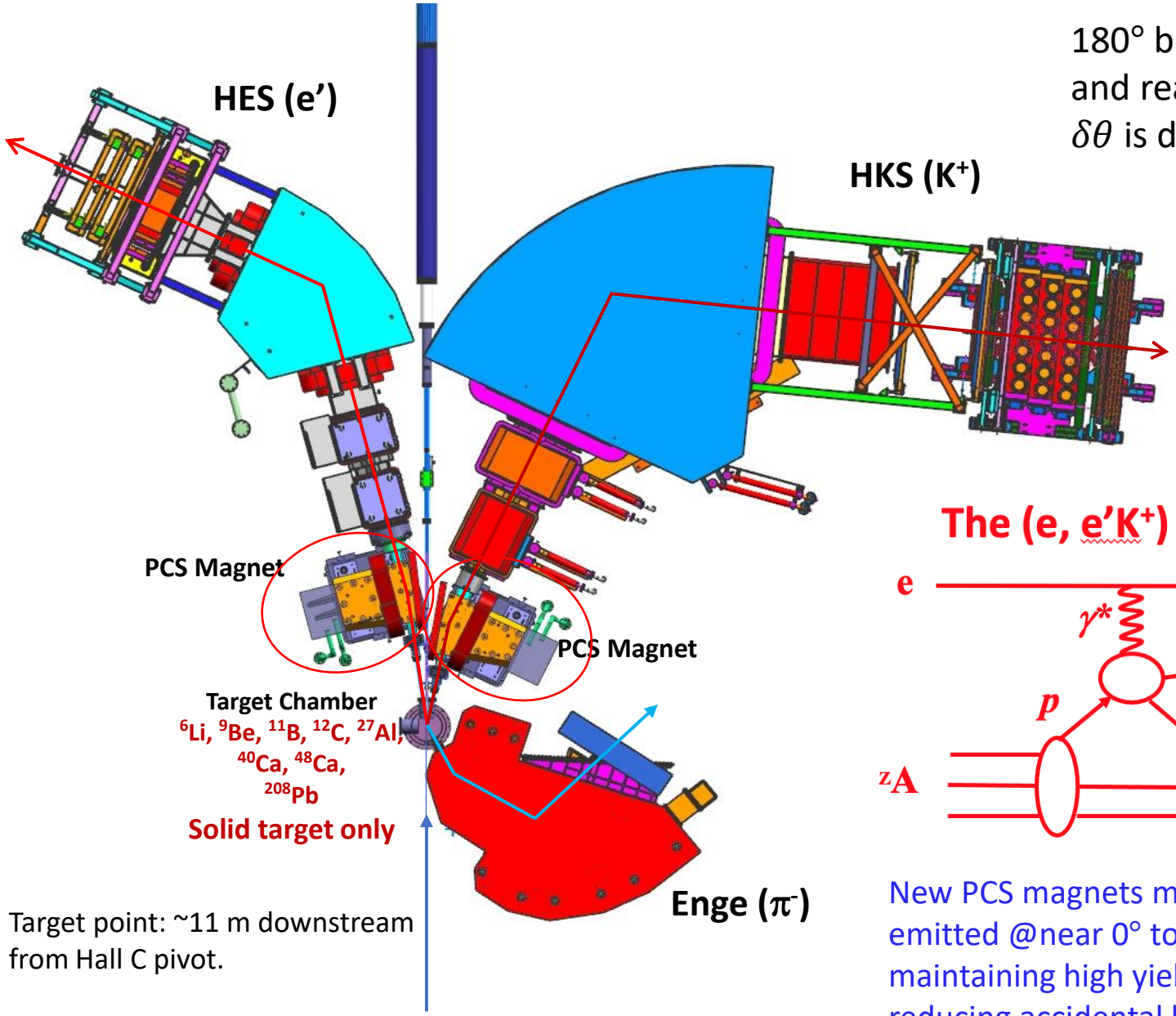
- 1 to 2 VXS crate
- 1 crate VTP + up to 16 FADCs or VETROCs
- 1 crate VTP + MPDs for GEMs
- Digital calorimeter cluster and Cerenkov trigger
- Max 5 KHz with GEM
- 100 to 200 KHz should reachable with FADC and VETROC only
- 32 channels of SAMPIC
- 8 channels of ASOC and 8 channels of AARDVARC

# HKS experiment

- Run same time as Moller
- 3 High resolution magnetic spectrometers
- Would benefit from high resolution timing for PID
- Trying to put MRPC planes in both arms
- Test FADC trigger logic

- Might require EIC timing system to reach the 5 ps electronics required resolution

# Schematic Layout of The Hypernuclear Spectrometer System




180° between scattering and reaction planes ($\Delta\phi_0$)
$\delta\theta$ is dominated by $\delta$x'

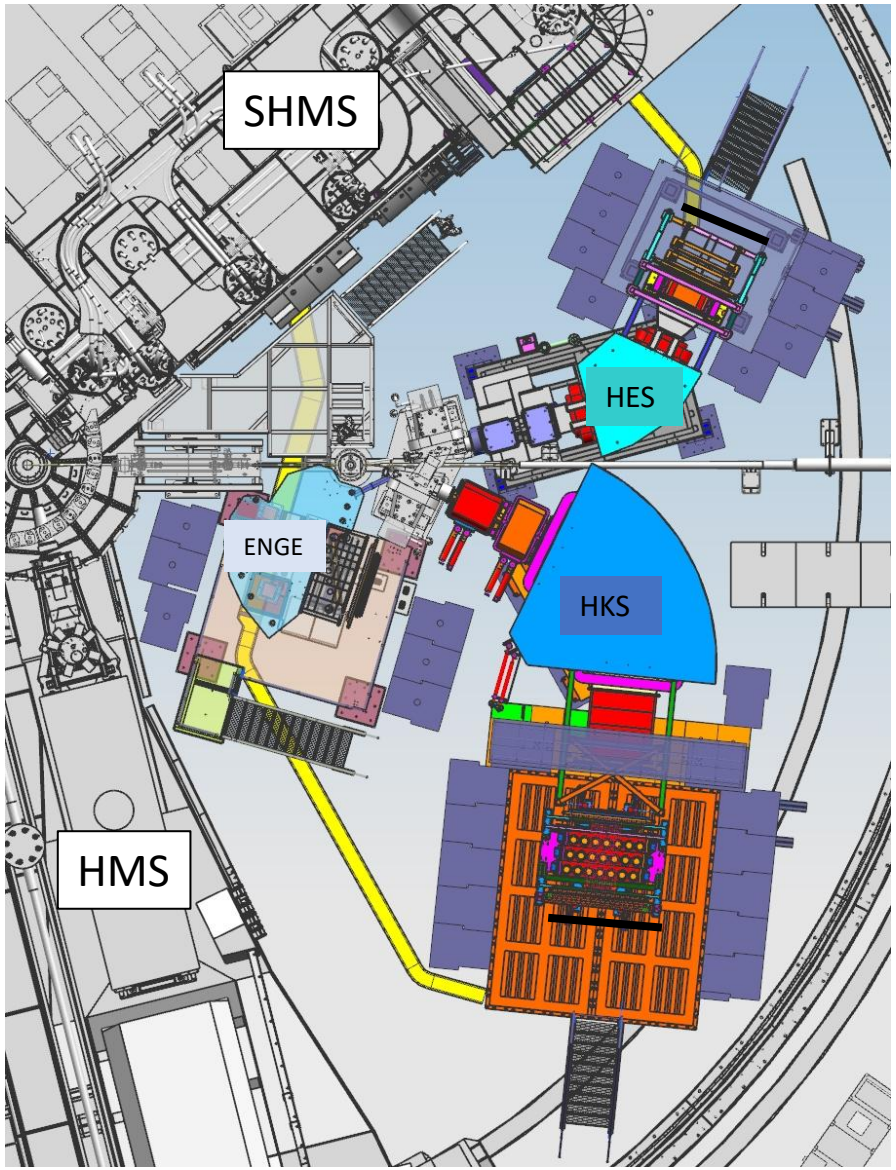
Target point: ~11 m downstream from Hall C pivot.

## The (e, e'K+) Reaction



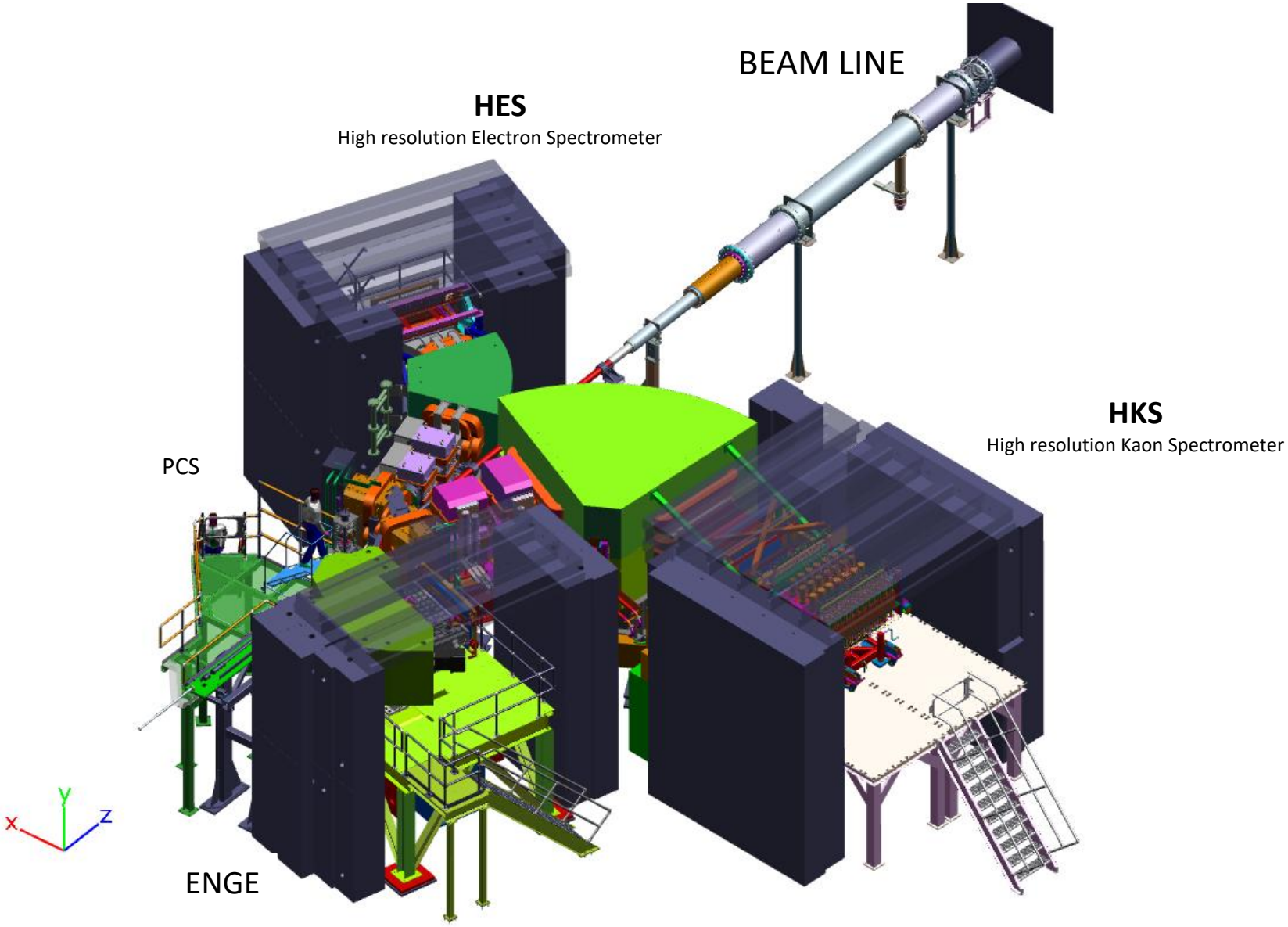

New PCS magnets minimize the particles emitted @near 0° to enter HES and HKS, maintaining high yield while significantly reducing accidental background

# HYPER NUCLEAR – LAYOUT (TOP VIEW)



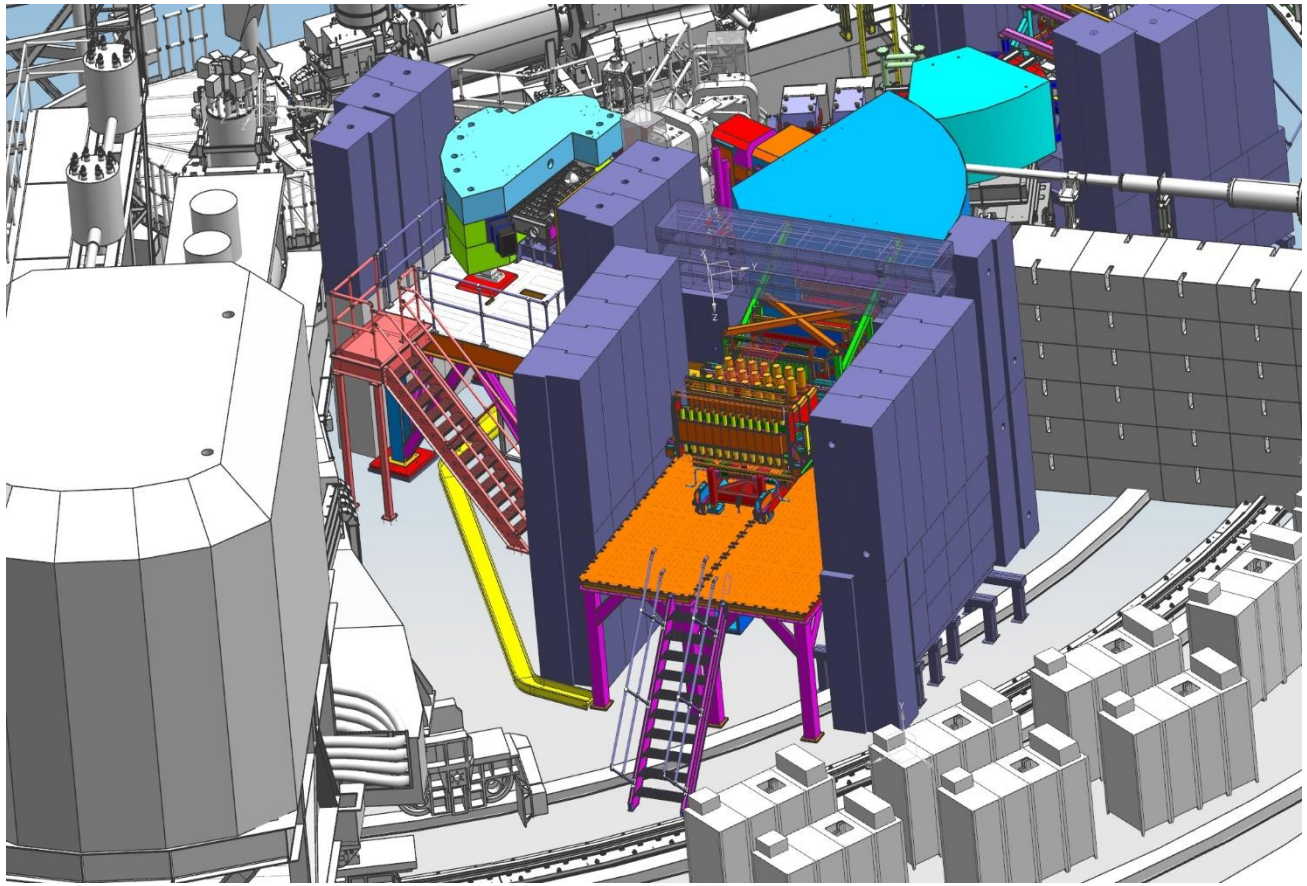

BEAM LINE

# HYPER NUCLEAR – LAYOUT (ISO-VIEW)

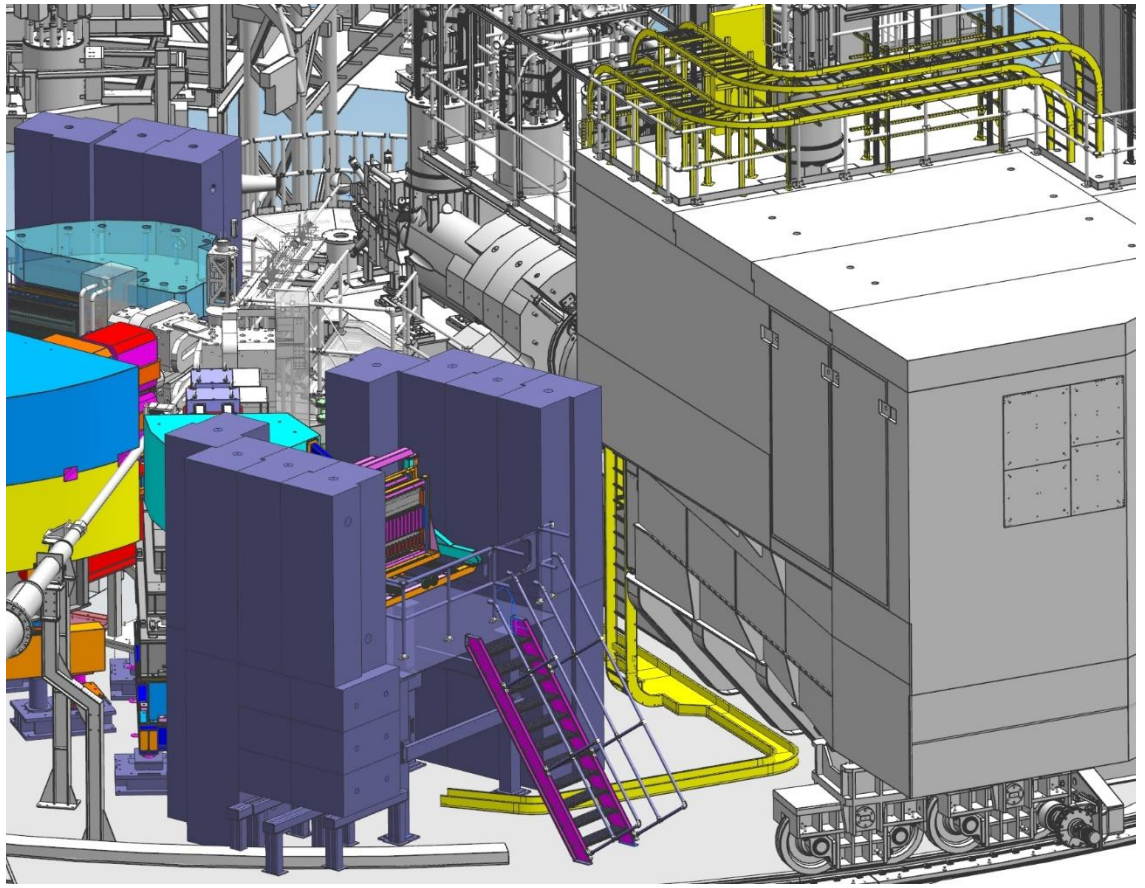


# HYPER NUCLEAR – CABLE ROUTING

HKS

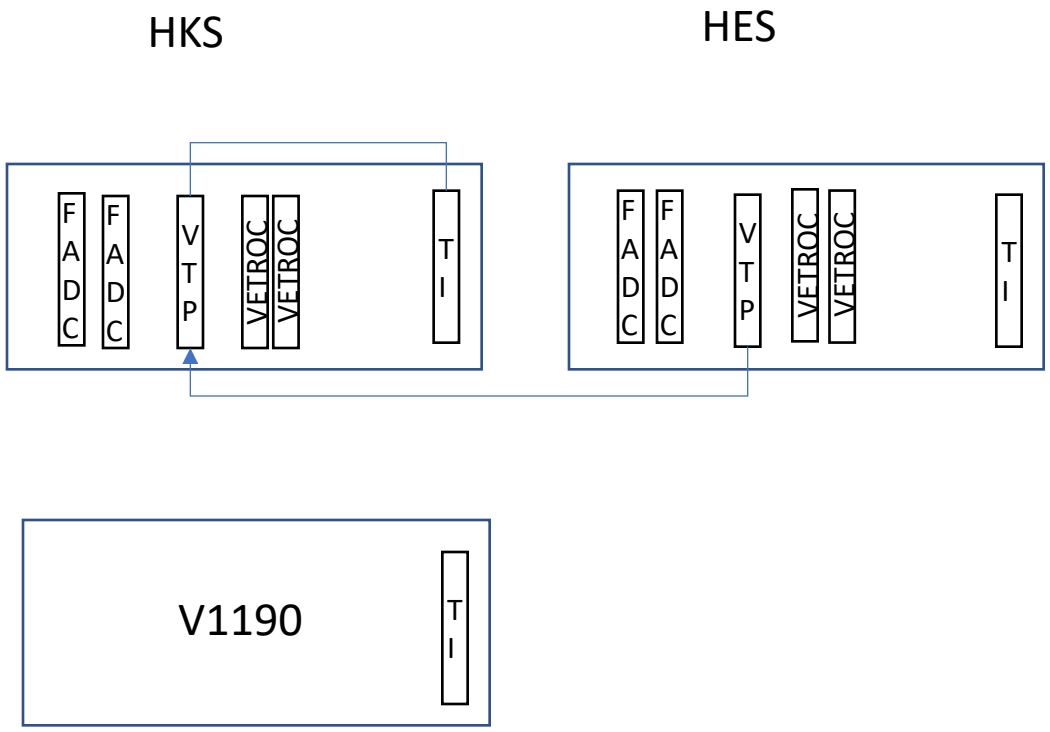


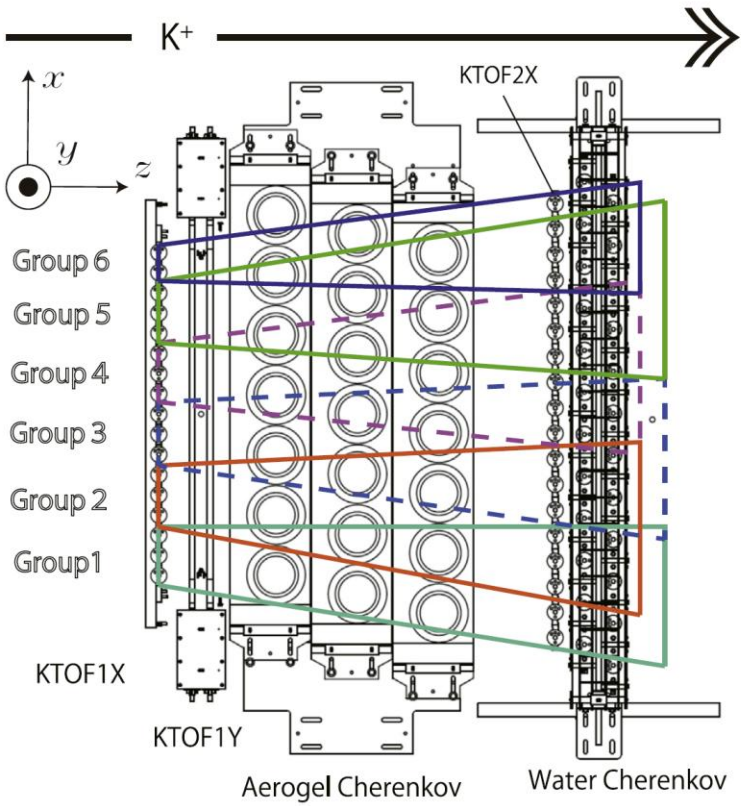
HES



CABLE TRAY LAYOUT FROM SUPER HMS(YELLOW)

# Trigger




Can program VTP for coincidences between scintillators
If use VETROC instead of V1190 could add Drift Chamber to trigger

# Conclusion

- Most Capital equipment on hand
- GEM readout
  - VMM with higher gain
  - Funding for new GEM chip
  - Upgraded AVP25 option
- Different setup using capital equipment
  - Moller
    - MAPS readout with VTP
    - Compton
    - Counting DAQ for Q2
  - ESB
    - Deadtime studies
    - GEM VMM readout
  - HKS
    - VTP trigger
    - MRPC