
# RFSoC-Based LLRF Development for CSNS-II LINAC

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*On Behalf of Linac RF Group*

*2025 LLRF Workshop*

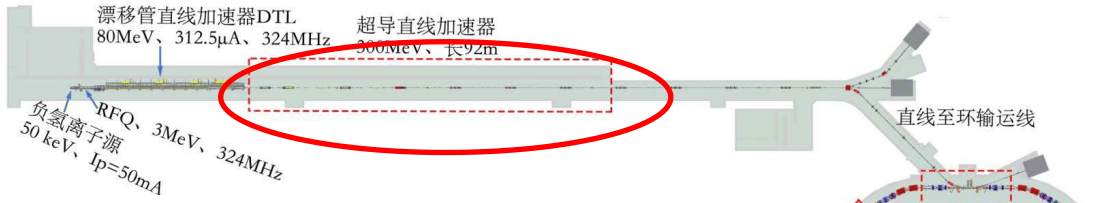
# OUTLINE

- Overview of CSNS-II
- Research on RFSoC
- RFSoC development and experimentation at CSNS II LINAC
- Conclusion

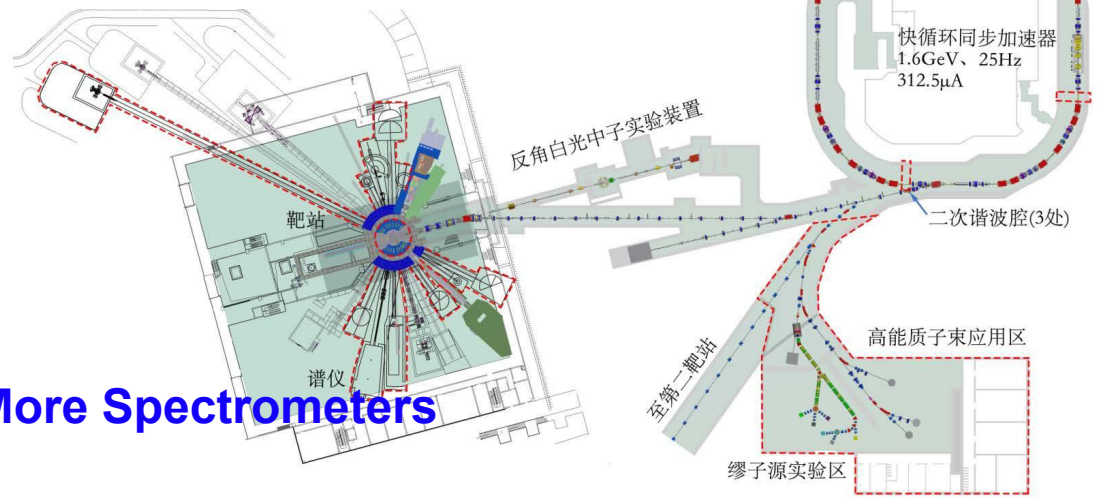
# CSNS-II Overview

- Construction Time:2023.12 ~ 2029.3
- A SRF section is to be added to increase energy from 80 to 300MeV.

**Linac Energy:**80MeV→300MeV




**Target Power:**100→500kW




**More Spectrometers**

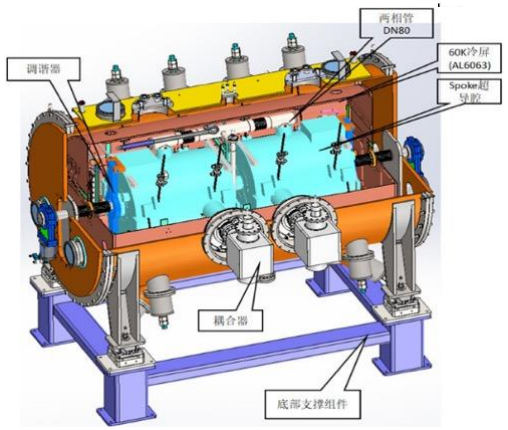
**Layout of CSNS**

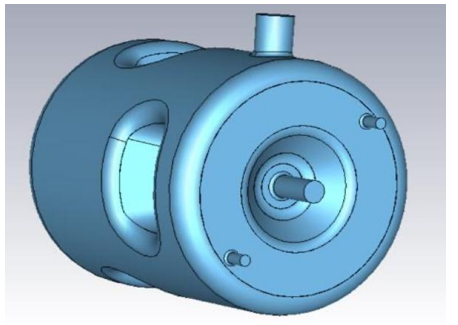
| CSNS | Phase I | Phase II |
|---|---|---|
| Beam power on target(kW) | 100 | 500 |
| Linac energy (MeV) | 80 | 300 |
| Extraction beam energy (GeV) | 1.6 | 1.6 |
| Average beam current (μA) | 62.5 | 312.5 |
| Linac Peak beam Current(mA) | 15 | 40 |
| Repetition(Hz) | 25 | 50 |
| Linac Beam Len(μs) | 500 | ~500 |

# SRF Section Accelerator

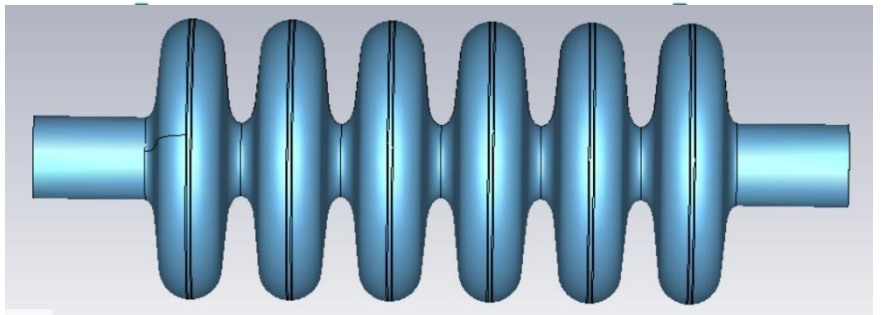

## ➢ SRF Specifications

| Items | SPOKE | SPOKE (Improved) | ELLIPTICAL |
|---|---|---|---|
| Freq(MHz) | 324 | 324 | 648 |
| Gradient(Mv/m) | 7.3 | 9 | 14 |
| Length(m) | 0.694 | 0.694 | 0.86 |
| R/Q（Ω） | 410 | 401 | 309 |
| QL | 3.8e5 | 3.8e5 | 9.6e5 |
| LFD Hz/(MV/m)² | -10.7 | -4.56 | -1.5 |
| LFD@ Max Gradient | 530 | 369 | 250 |
| $f_{3db}$ | 850 | 850 | 674 |
| df/dp(Hz/mbar) | 0.773 | 38 | 6.3 |



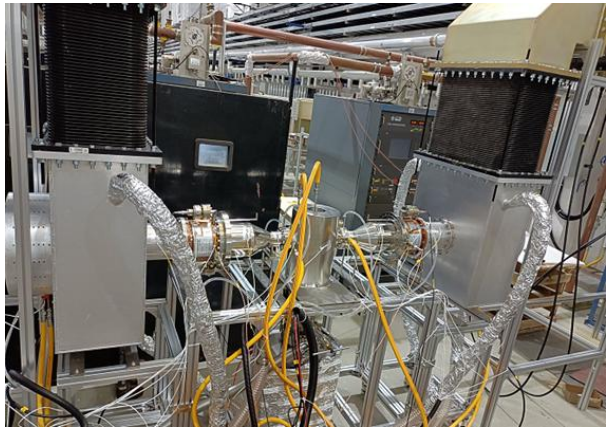


324MHz Double-Spoke Cavity X 20

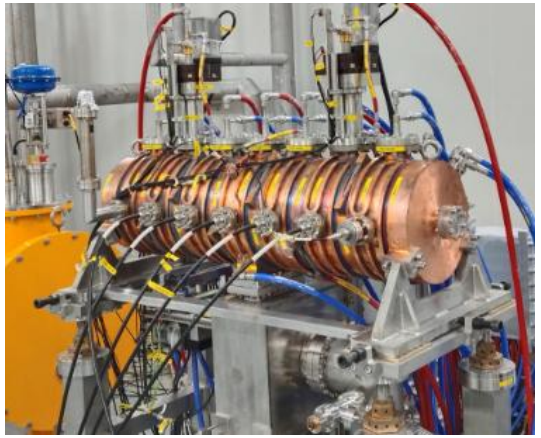


648MHz Elliptical Cavity X 24

# Some projects prepared for CSNS-II LINAC



324MHz coupler aging



648MHz debuncher LLRF

648MHz Klytron LLRF

C-Band Klytron

Spoke Horizontal Test

# OUTLINE

- Overview of CSNS-II
- Study on RFSoC
- RFSoC development and experimentation in CSNS II LINAC
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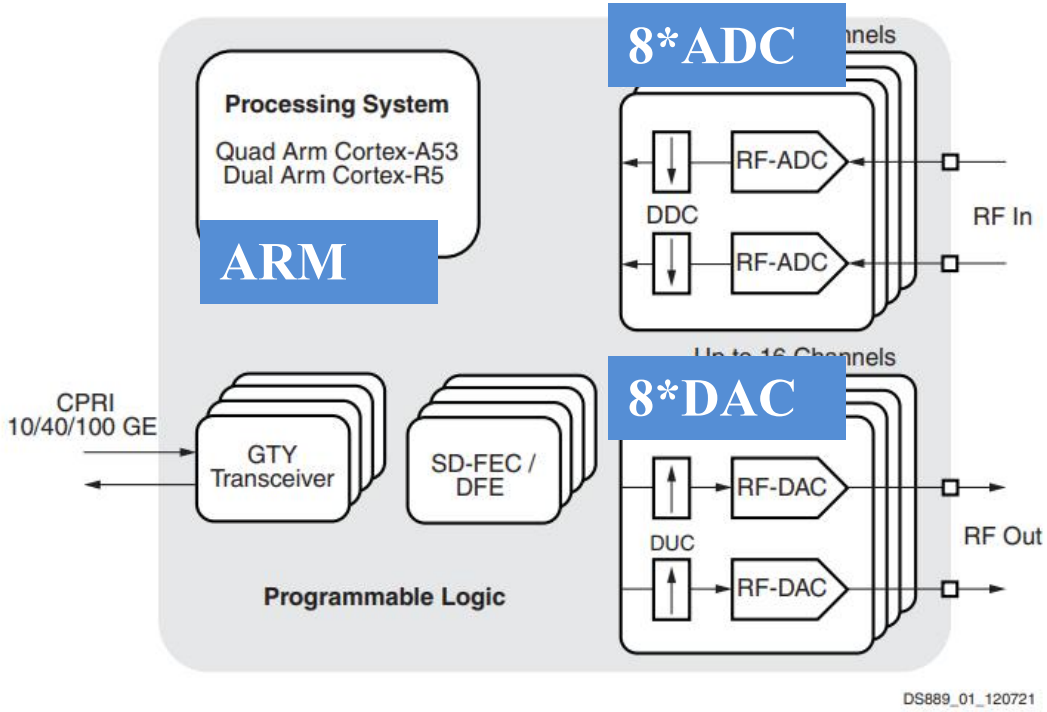
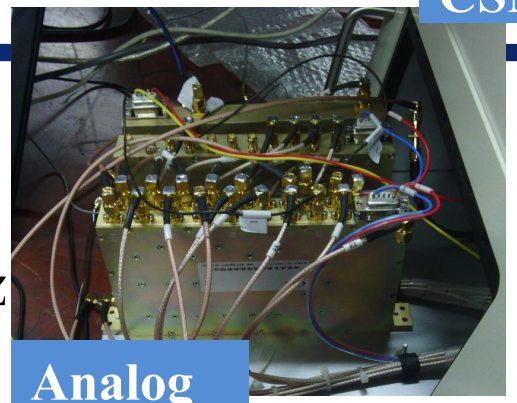
# RFSoC(RF System on Chip) introduce

- Low latency, High speed
- High integration, few components, easy to maintain
- The main clock frequency can reaches over 300MHz

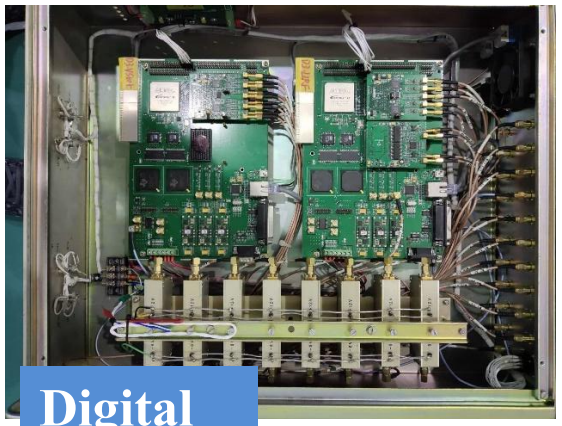



**8*RFADC，8*RFDAC，~6GHz sample rate，4-core ARM, abundant FPGA resources**

CSNS-I LLRF



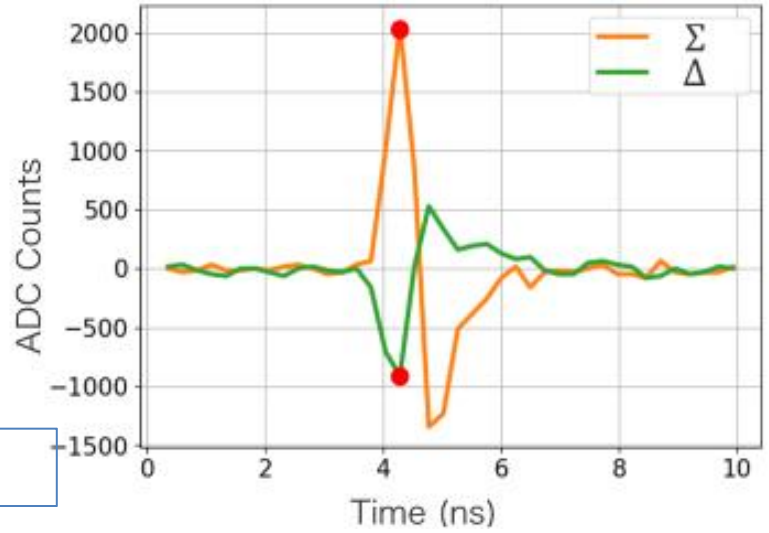
Analog



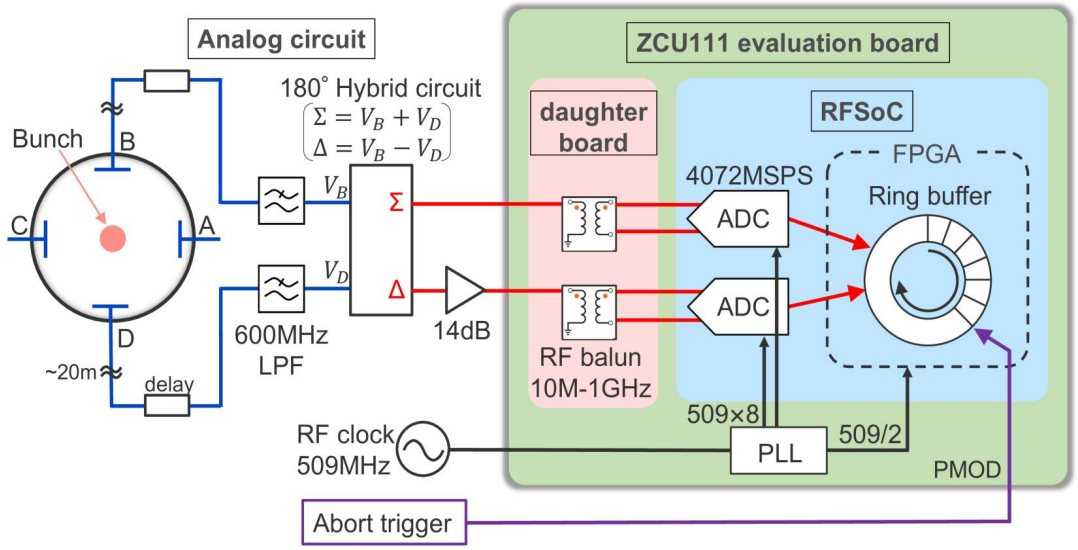
Digital


3.5cmx3.5cm

# RFSoC development in other accelerators




**SuperKEKB**




CERN

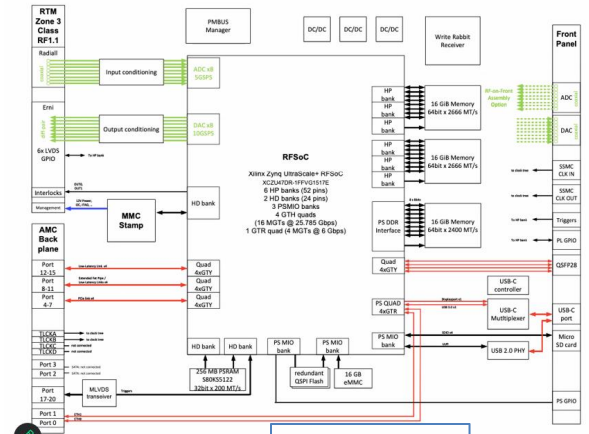
**CERN**

## RF System-on-Chip use in the CERN Beam Instrumentation group

Andrea Boccardi, slides from Irene Degl'Innocenti's presentation to the CERN 3rd SoC workshop – CERN SY-BI-BP

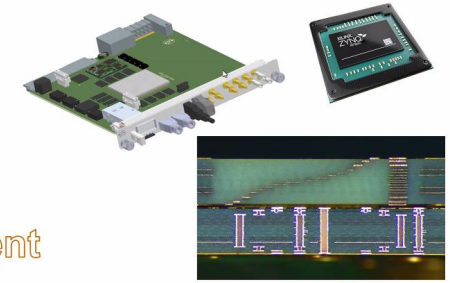
TWEPP 2023 - FPGA user group

### DAMC-DS5014DR: New Board based on AMD RFSoC




**Key facts:**

- 8x 14 bits **ADC, 5 GSPS, 6GHz** analog BW
- 8 x 14 bits **DAC, 10 GSPS, 4GHz** analog BW
- DC- and AC-operation (assembly option)
- White Rabbit timing support
- precise on-board clock generator
- Megtron-6, 16 Layer, 3mil technology
- Full HDI-Layer stackup, 0201 Components



HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

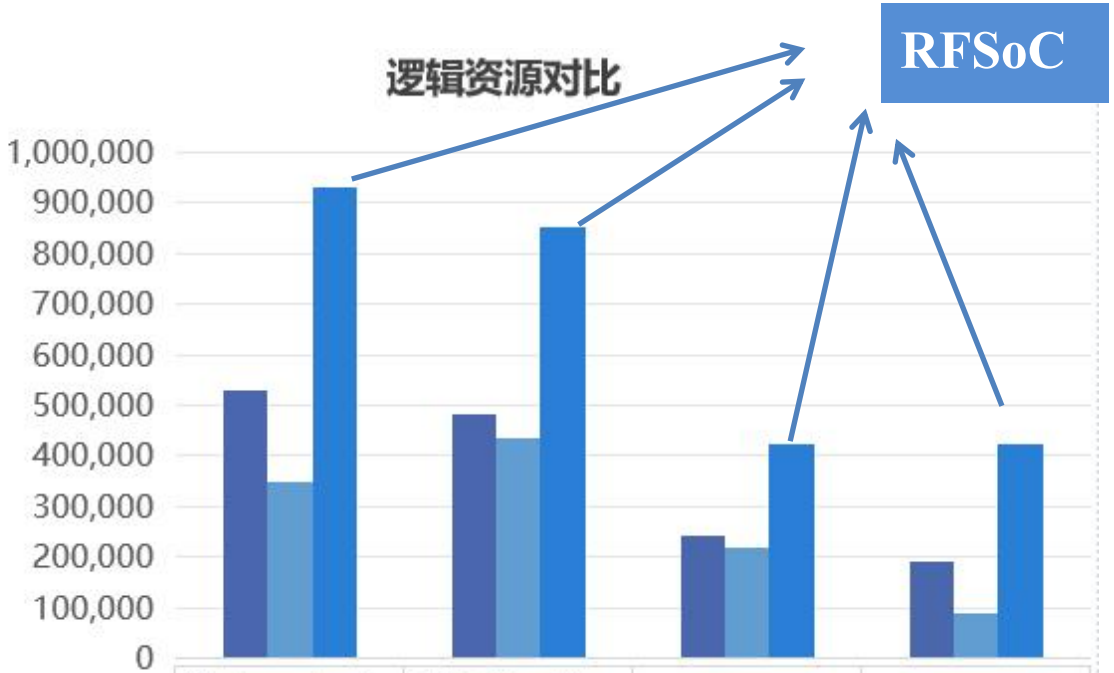
Under development

**DESY**

# Logical Resource Comparison

- FPGA resources are about twice that of conventional FPGA chips

- Kintex Ultrascale
- ZYNQ 7000
- RFSOC-47DR



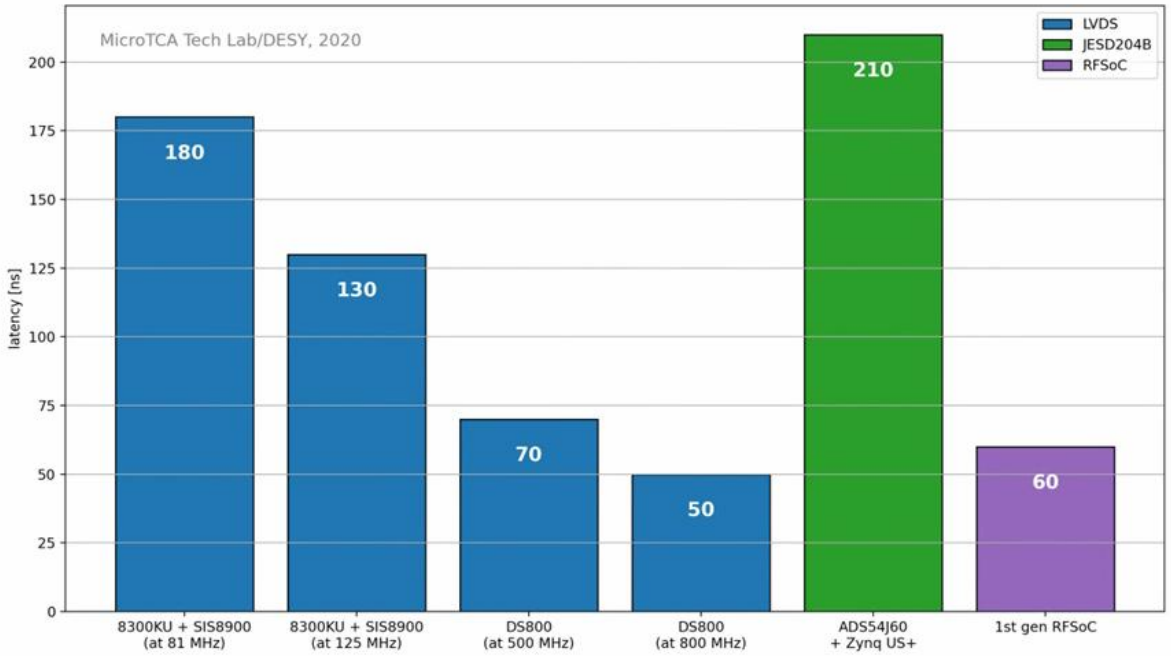

| | System Logic Cells | CLB Flip-Flops | CLB LUT | DSP(*100) |
|---|---|---|---|---|
| 8300KU | 530,000 | 484000 | 242000 | 192000 |
| ZYNQ-7000 | 350,000 | 437000 | 218000 | 90000 |
| RFSOC-47DR | 930,000 | 850000 | 425000 | 422700 |

NOTE：The real value of DSP resource must divide 100

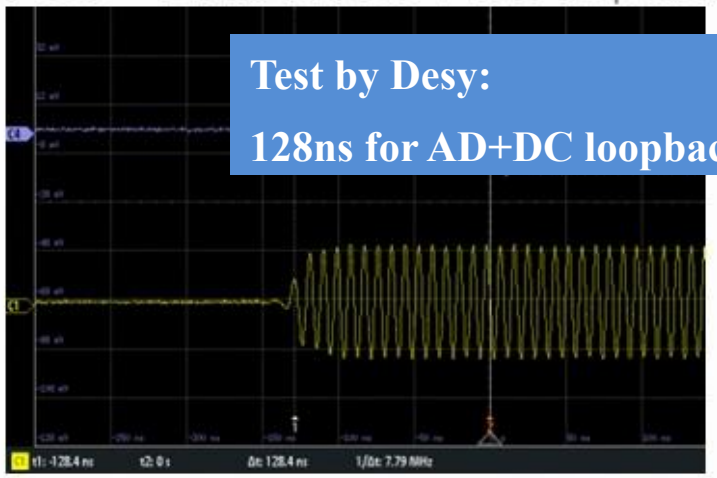
# RFSoC ADC+DAC LOOPBACK latence

| ADC | Board | Interface | Resolutions [bits] | Sampling rate [MSPS] |
|---|---|---|---|---|
| AD9268 | SIS8300-KU | LVDS | 16 | 125 |
| ADC12D800RF | DAMC-FMC2ZUP + DFMC-DS800 | LVDS | 12 | 800 |
| ADS54J60 | DAMC-FMC2ZUP + ADS54J60EVM | JESD204B | 16 | 1000 |
| XCZU28DR | ZCU111 | RFSoC | 12 | 4096 |



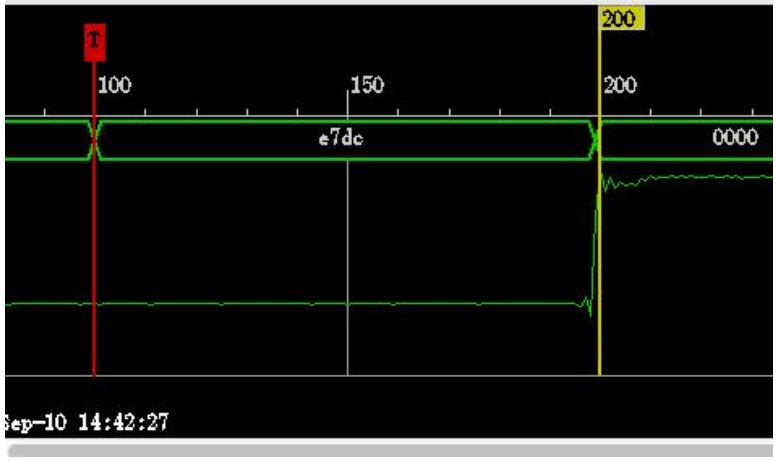



RFSoC - 128 ns for ADC + DAC loopback:



**Test by Desy:**

**128ns for AD+DC loopback**




✓ About 200ns for loopback in our test

# Comparison of Performance with Conventional ADC/ DAC

- Due to the wide sampling range of RF ADC and the need to cover the entire Nyquist sampling noise in SNR, it is not suitable for comparison. Generally, NSD (Noise Spectral Density) is used for comparison.

| Board and signal | | SNR(dBc) | SFDR(dBc) | NSD(dBFS/Hz) |
|---|---|---|---|---|
| SIS8300 | ADC-20MHz | 76 | 86 | -154 |
| | DAC-20MHz | 74 | 64 | -152 |
| RF SOC | ADC-240MHz | 59 | 86 | -152 |
| | ADC-900MHz | 58 | 79 | -151 |
| | DAC-900MHz | - | 81 | - |

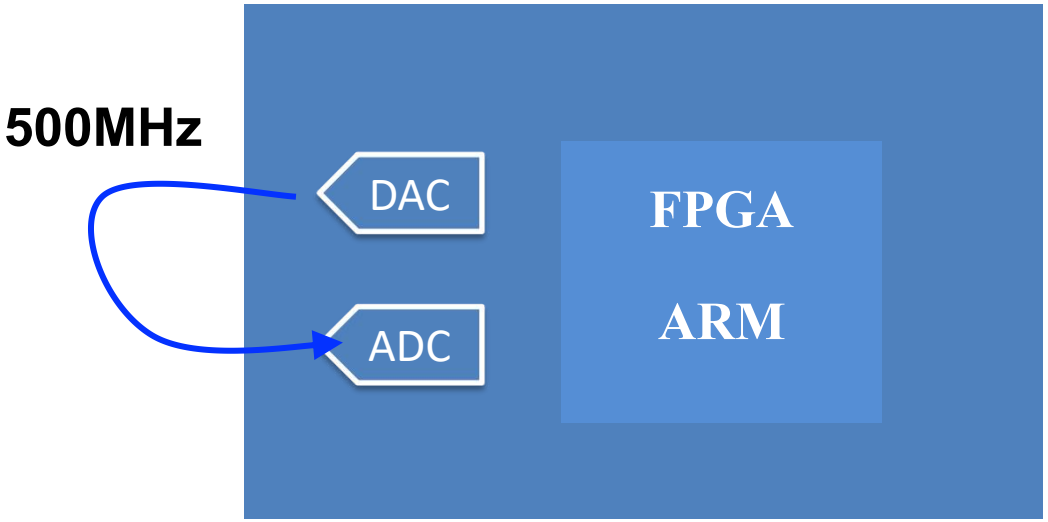
$$SNR_{(dB)} = 10\log_{10}\left(\frac{P_{fundamental\ signal}}{P_{noise\ (over\ Nyquist\ BW)}}\right)$$

$$NSD_{(dBFS/Hz)} = -SNR_{measured(dBFS)} - 10\log_{10}\left(\frac{fs}{2}\right)_{(Hz)}$$

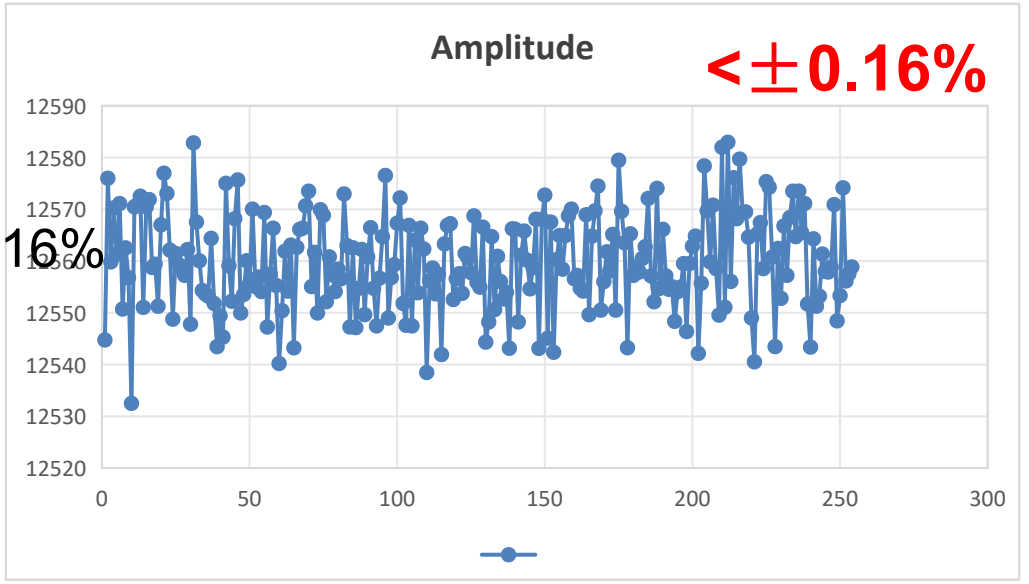
RFSoC and KU board NSD are close

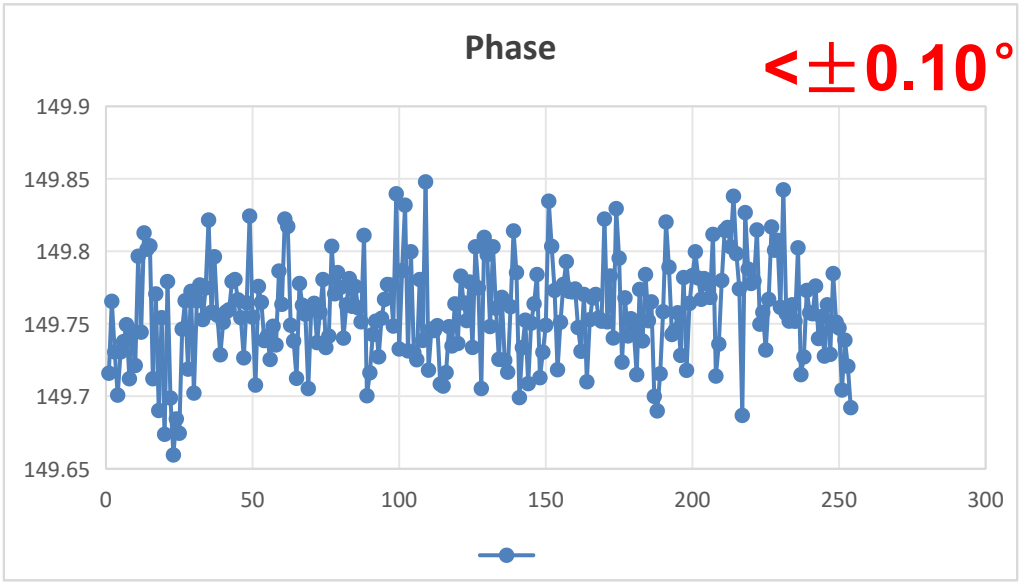
# ADC/DAC performance Loop Test

- Test conditions:
  - The center frequency is 500MHz.
  - The amplitude and phase are less than ± 0.16% and ± 0.1 ° , respectively.
  - Meet the requirements of CSNS II




RFSoC Loopback test



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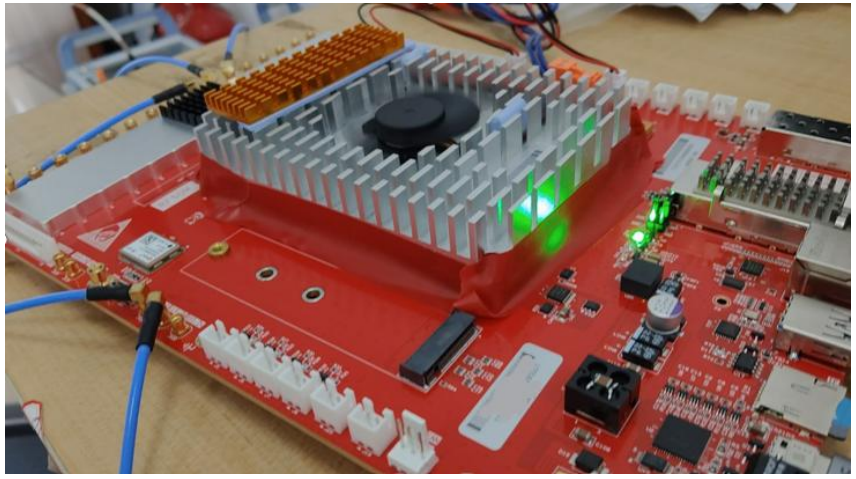
# Spoke Horizontal Test using RFSoC

- 47DR RFSoC board for spoke horizontal test
- 8 RX 14 bit (5Gsps) and 8 TX 14bit (9.8Gsps)
- Sampling rate of 2.592Gsps for 324MHz

**324MHz D-spoke cavity**



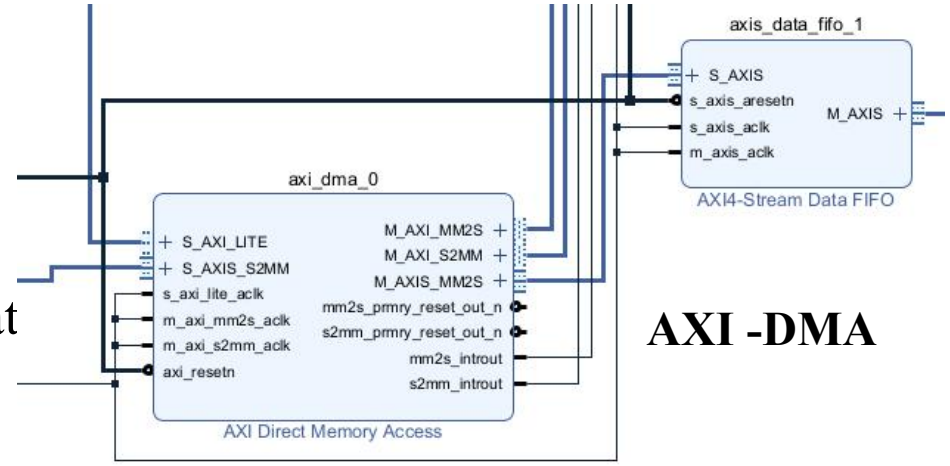
**RFSoC development board**

**RFSoC Casing**

**Spoke Cryomodule**

# Software and Firmware

- Building Linux system boot and kernel and rootfs file using Petalinux.
- Installed IOC/EPICS in Linux system
- Use a DMA driver to read and write pulse waveforms at a rate great than 1GB/s
- Data stream synchronized with RF pulse




**AXI -DMA**

```
➜ ZYNQ petalinux-config -c kernel
[INFO] generating Kconfig for project
[INFO] sourcing bitbake
[INFO] generating plnxtool conf
[INFO] generating meta-plnx-generated layer
[INFO] generating machine configuration
[INFO] configuring: kernel
[INFO] generating kernel configuration files
[INFO] bitbake virtual/kernel -c menuconfig
Parsing recipes:  78% |################################      | ETA:  0:00:08
```

**Petalinux**

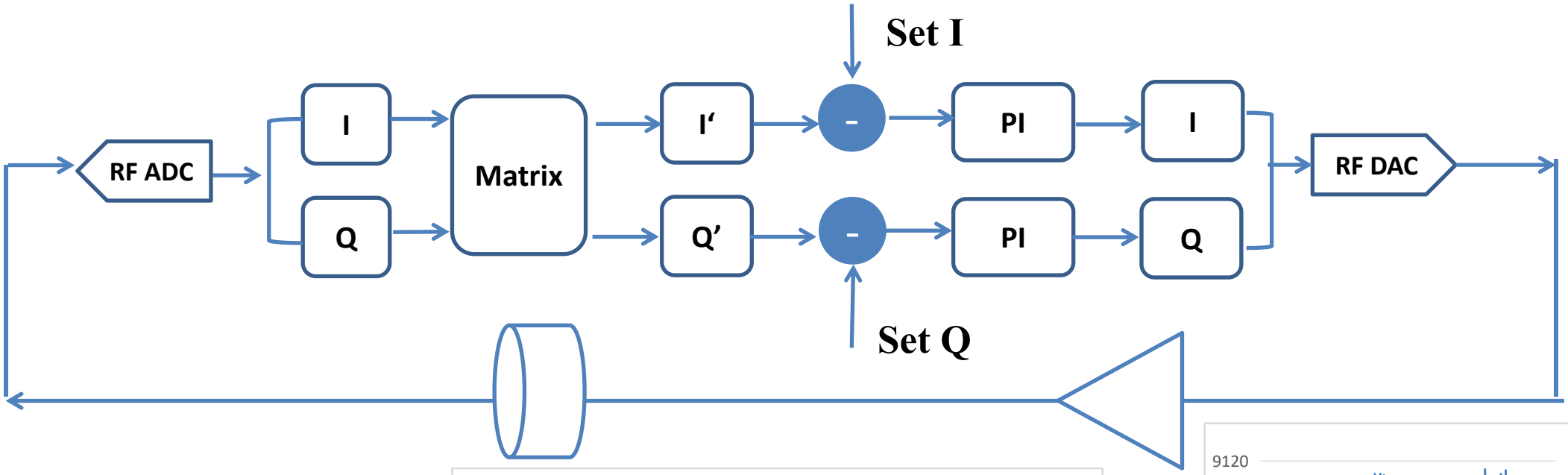
```
fpga@ubuntu-fpga: $ lsmod
Module                  Size  Used by
axidma                 36864  2
```

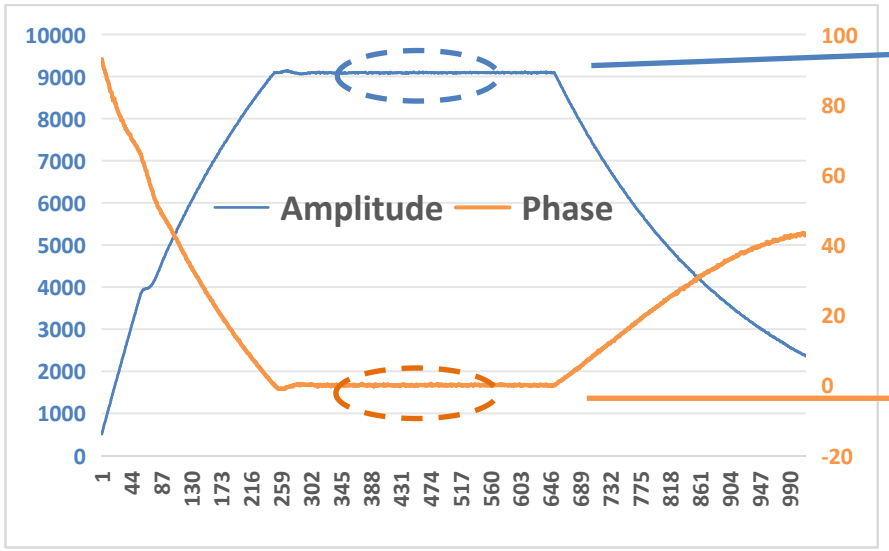
**DMA driver**

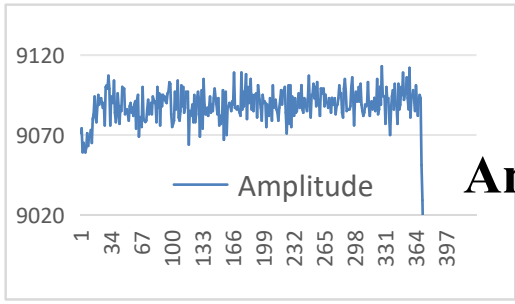
```
  PID USER      PR  NI    VIRT    RES    SHR S  %CPU  %MEM     TIME+ COMMAND
358883 root      20   0 2126956  97272   5896 S   2.0   2.4 157:24.26 st.cmd
374643 fpga      20   0    8832   3100   2668 R   0.3   0.1   0:00.06 top
    1 root      20   0  167252   7684   4344 S   0.0   0.2   0:20.11 systemd
```

**IOC:Cost 2% of cpu and mem**

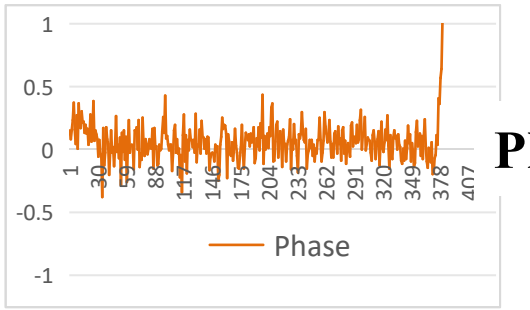
# Amp/Phase Feedback loop for Spoke cavtiy




Amp:±0.22%

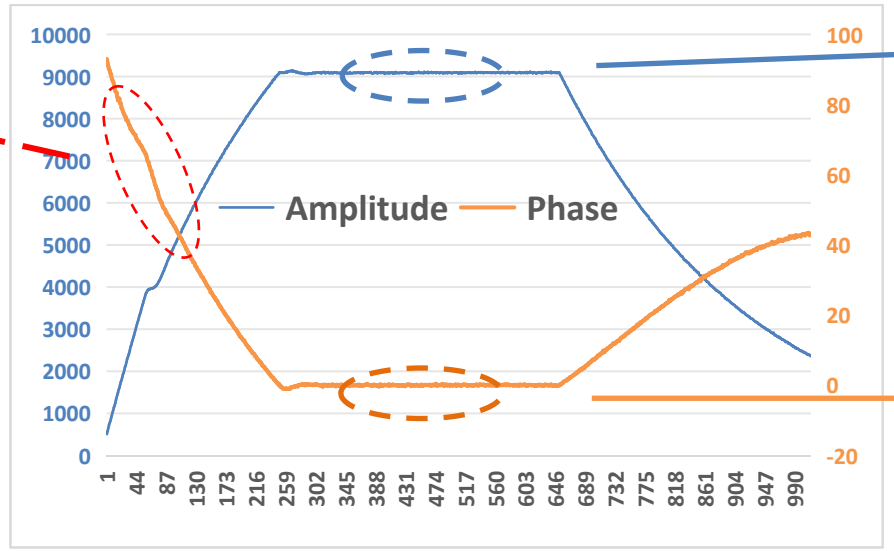


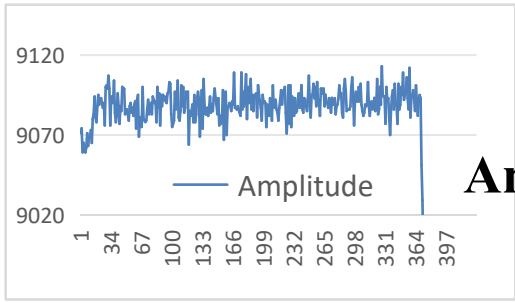

Phase:~±0.3°

# Frequency tracking to avoid using Piezo

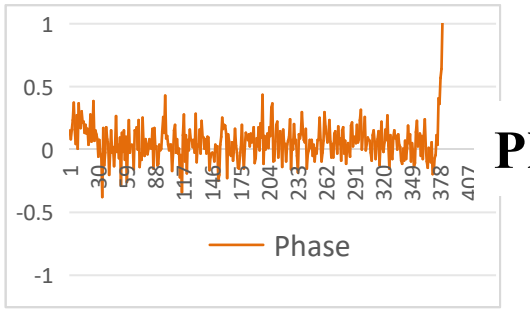
- Lorentz Force Detuning (LFD) poses a significant challenge for pulsed machines.
- The LFD coefficients are 10Hz/(Mv/m)^2, the detuning exceeds 1 kHz@10 MV/m, larger than the cavity's bandwidth.
- Typically, a piezo is used to control cavity detuning.
- Using a variable frequency to track LFD avoids the need for piezo or additional RF power.

Slope phase to track LFD



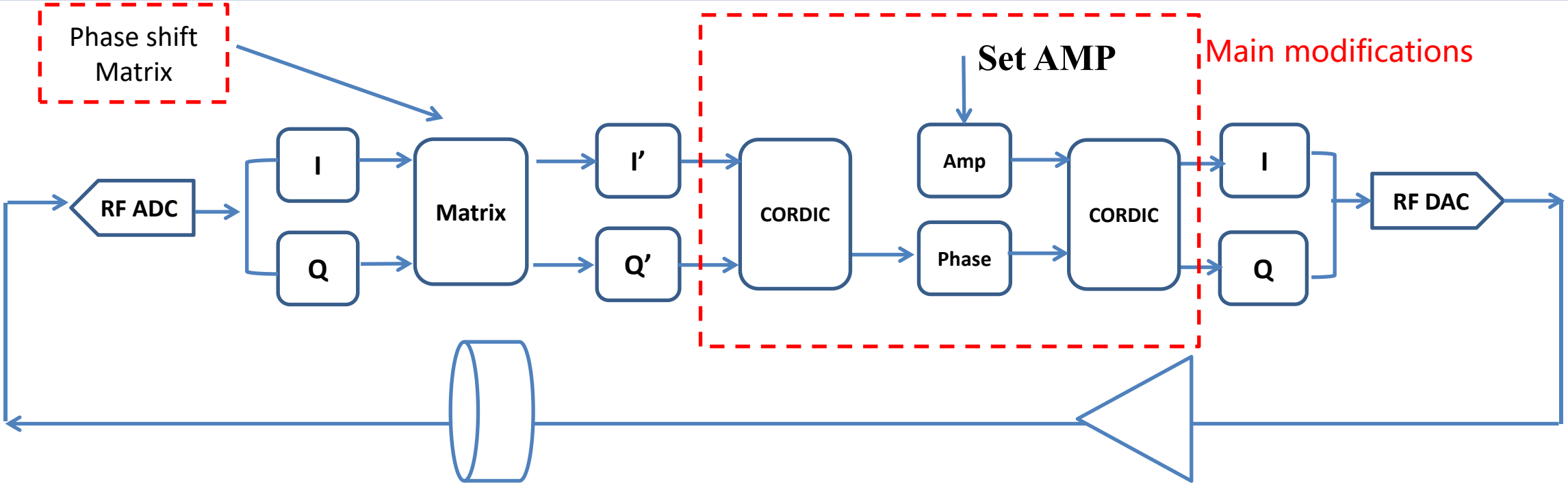



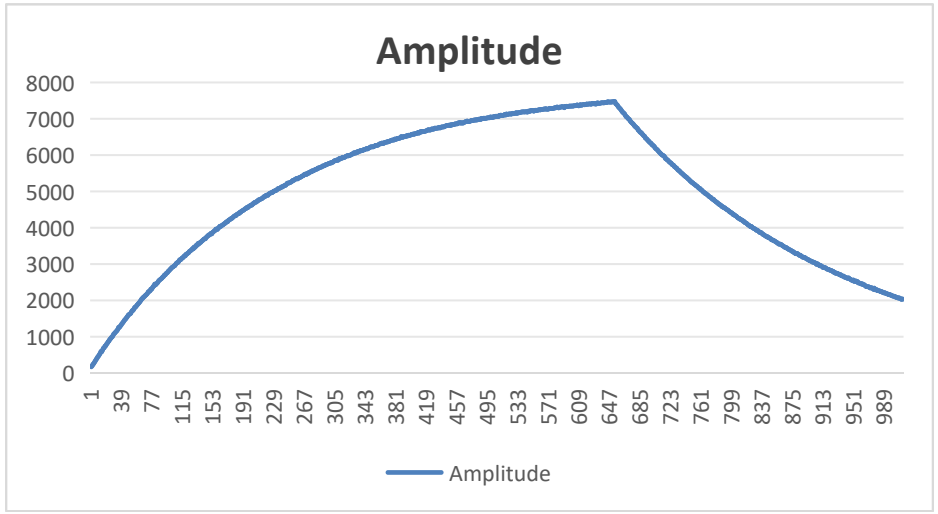

Amp:±0.22%

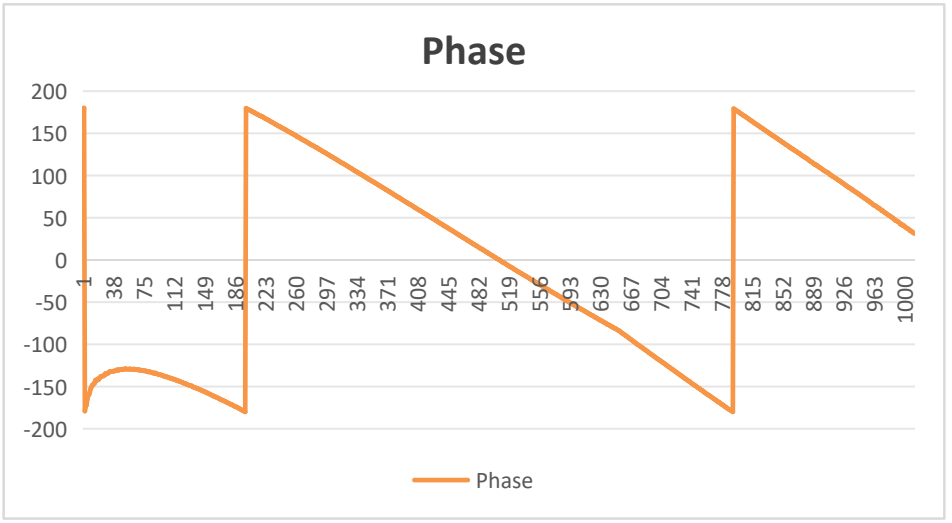



Phase:~±0.3°

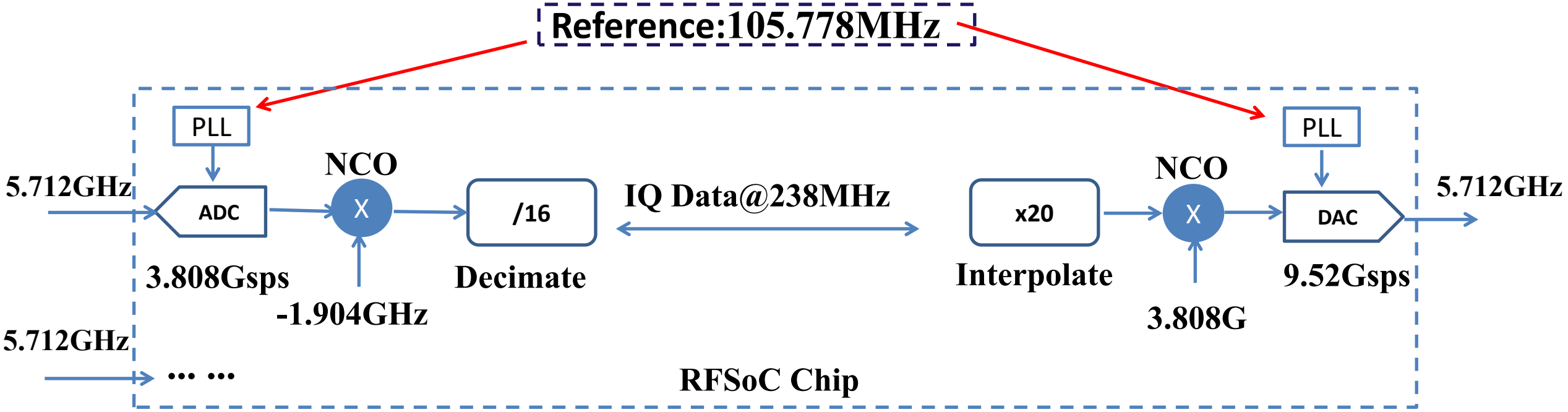
# Digital Self Excited Loop

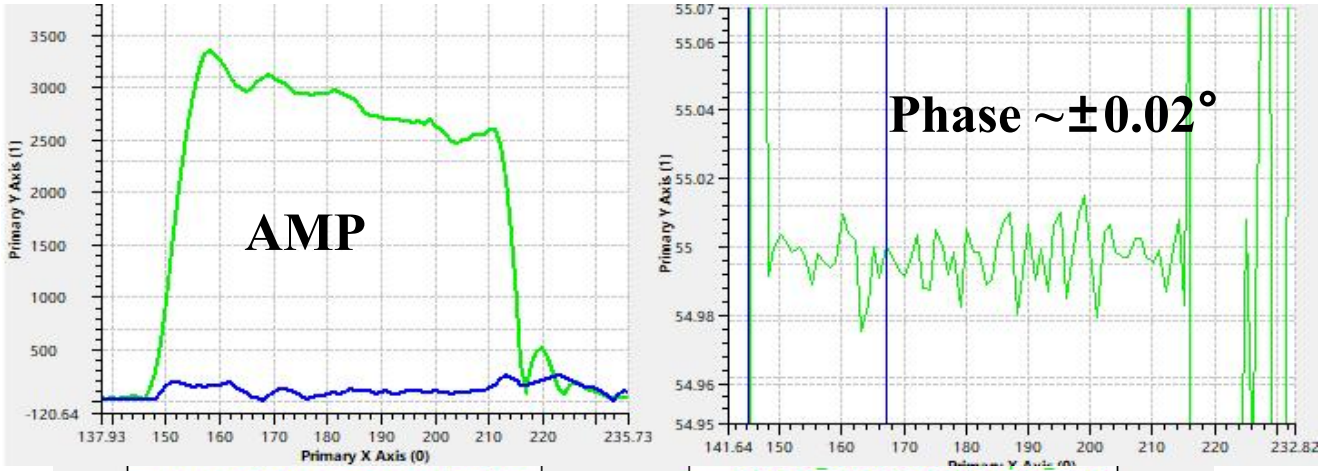


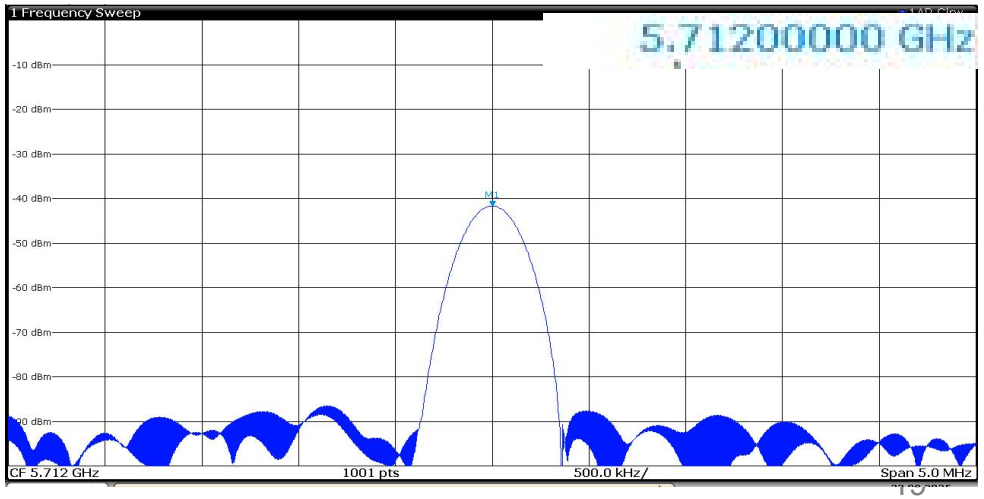
# RFSoC at C-BAND( 5.712GHz)









# Conclusion

- The RFSoC may be an ideal tool for building LLRF  systems, making them easier to implement and more high-performing.
- The horizontal testing of the superconducting cavity and C-BAND LLRF have been successfully completed.
- More research will be conducted in the future.

# Thank you!