A Universal Cavity Controller for testing SRF cavities at CERN

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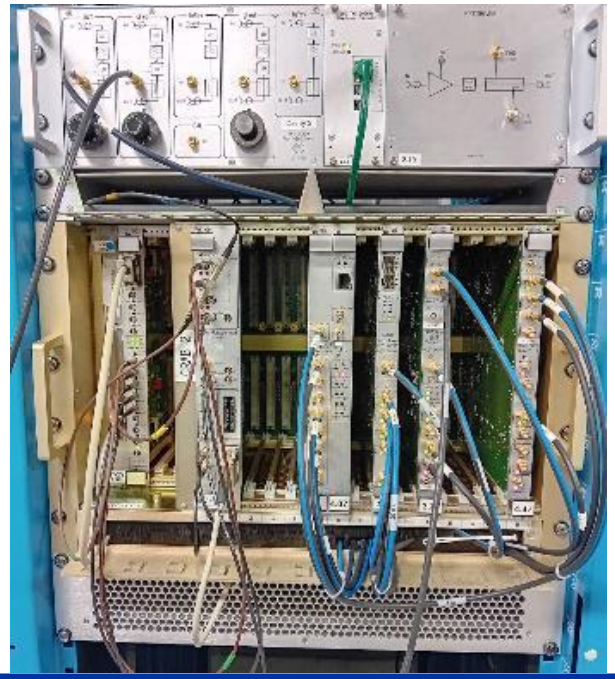
14/10/2025

Motivation

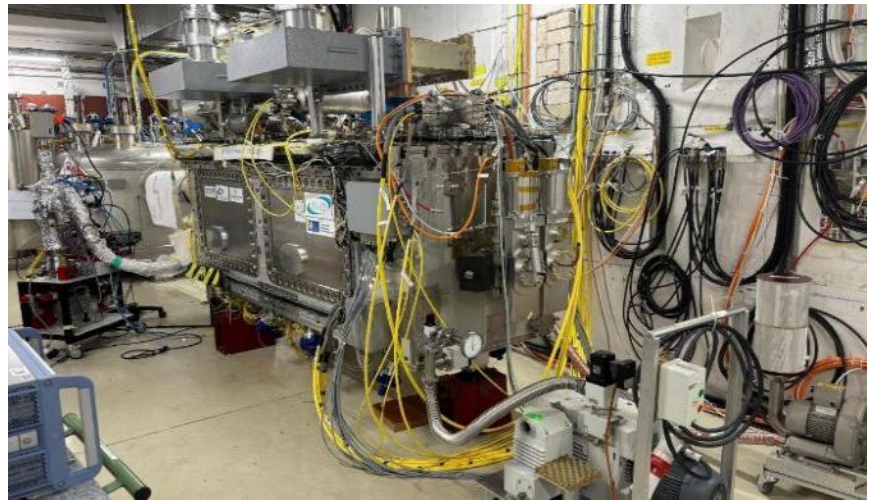
- **Development and validation of SRF Cavities**
  - **Purpose**: Measurement of high quality factor SRF cavities (Q_0 in 10^8 - 10^{11} range)
    - CERN has a variety of cavities with frequencies ranging from 101 -1300 MHz
    - LLRF framework must be adaptable to any given cavity type and specific R&D needs

Cavity validation

LLRF example system



Cryomodule validation



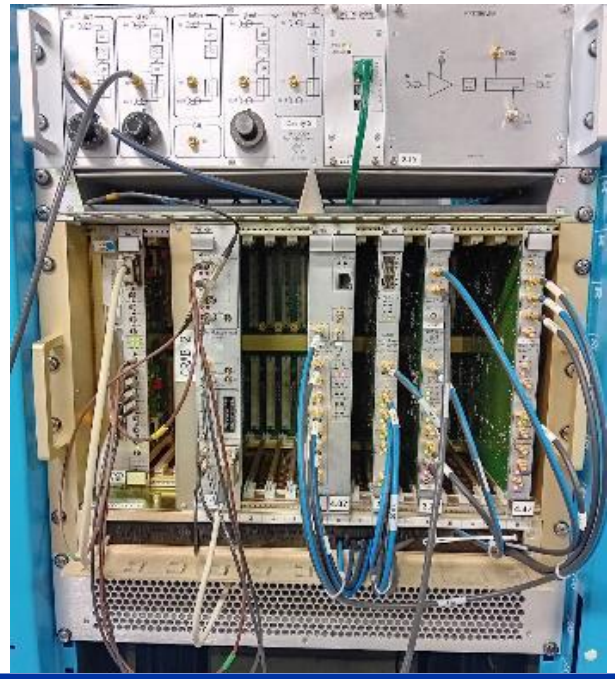
Images courtesy of HL-LHC WP4 – Crab Cavities

Motivation

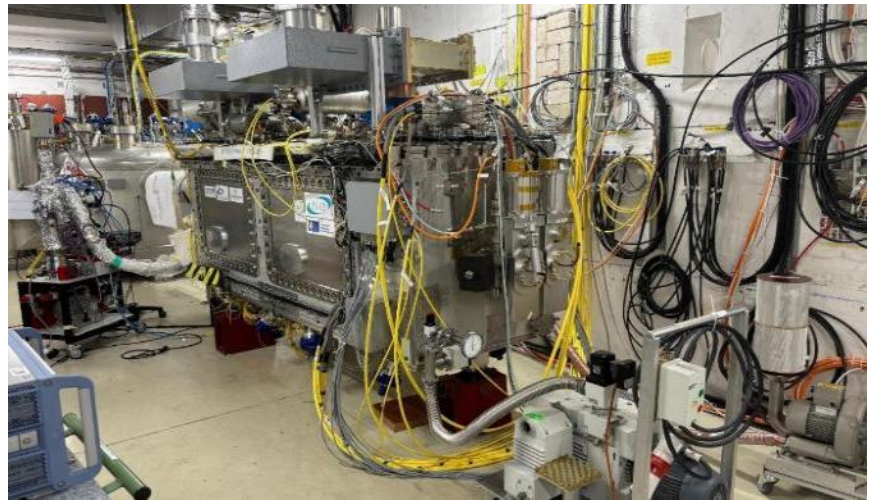
- **Development and validation of SRF Cavities**
  - **Context**: LLRF must follow cavity testing as they progress through their preparation cycle
    - RF measurement from bare cavities to beam-ready cryomodules

Cavity validation

LLRF example system



Cryomodule validation



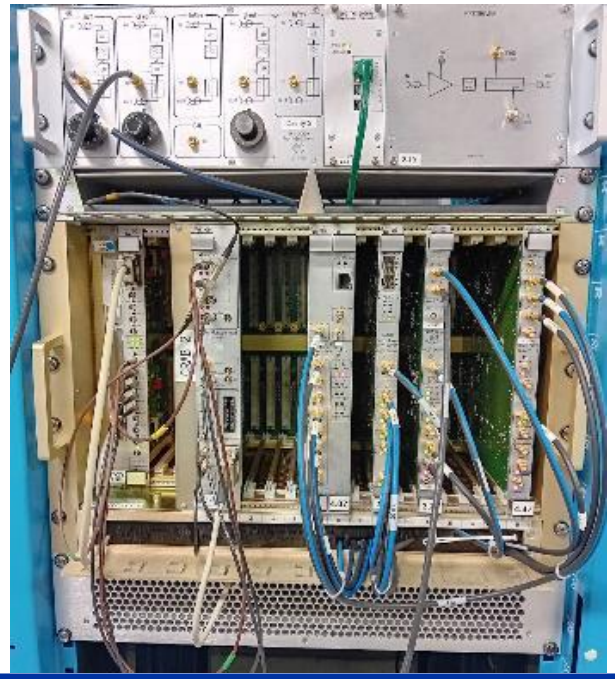
Images courtesy of HL-LHC WP4 – Crab Cavities

Motivation

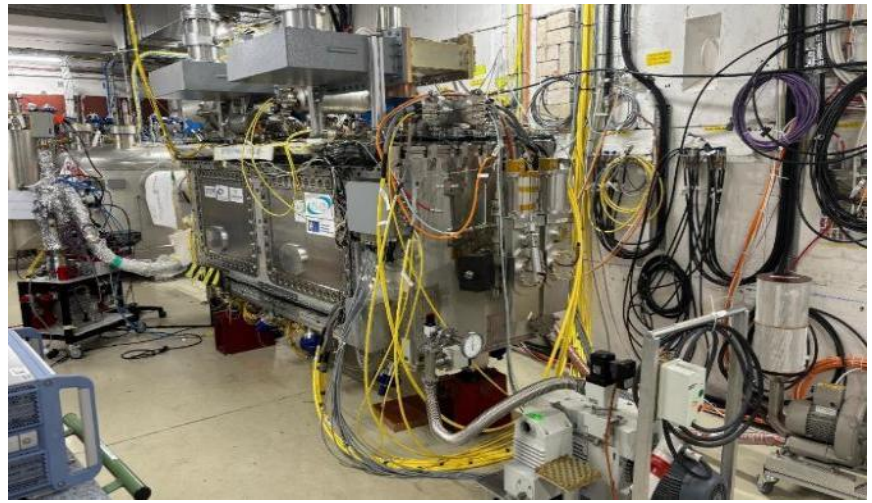
- **Development and validation of SRF Cavities**
  - **Requirement**: Common architecture to ensure coherence across measurement campaigns
    - Measurements include both pulsed and continuous powering operational modes
    - Self-Excited Loop and Generator Driven modes required

Cavity validation

LLRF example system

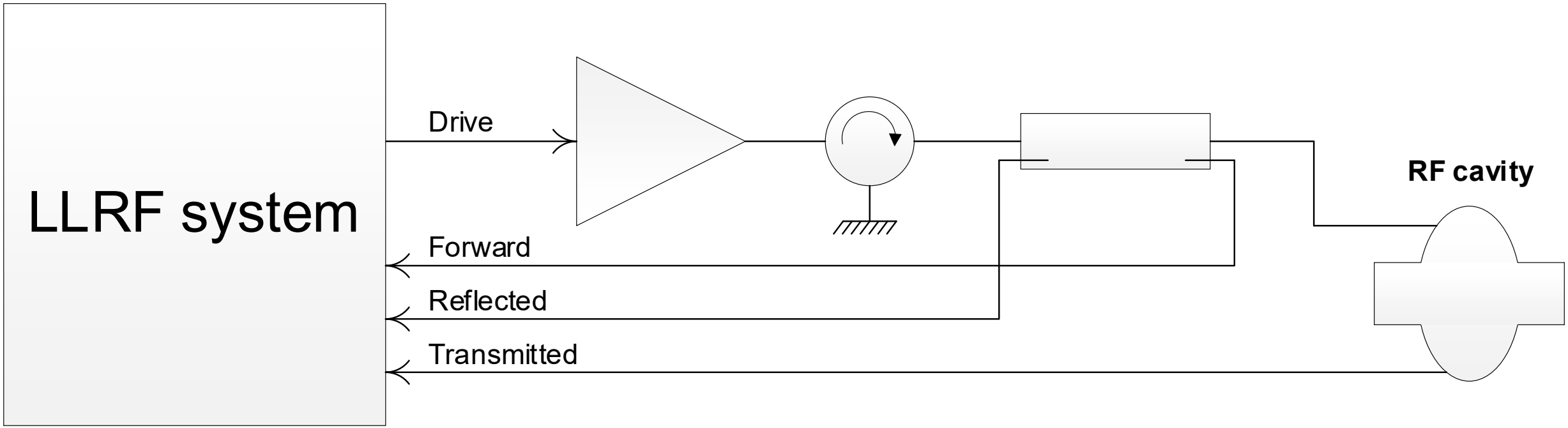


Cryomodule validation

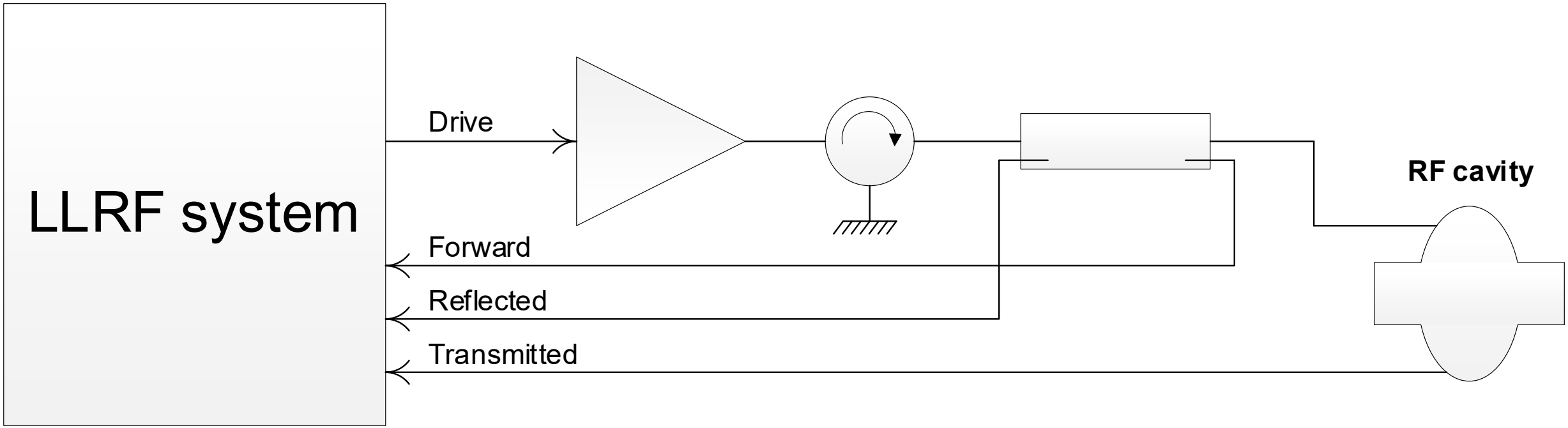


Images courtesy of HL-LHC WP4 – Crab Cavities

System architecture

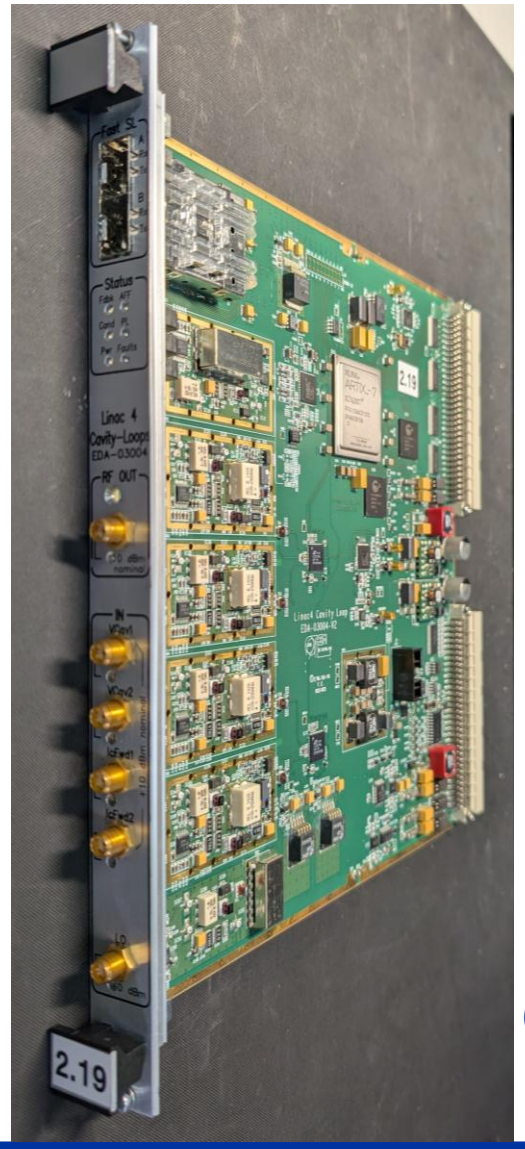


System architecture



LLRF cavity controller standardization

Hardware

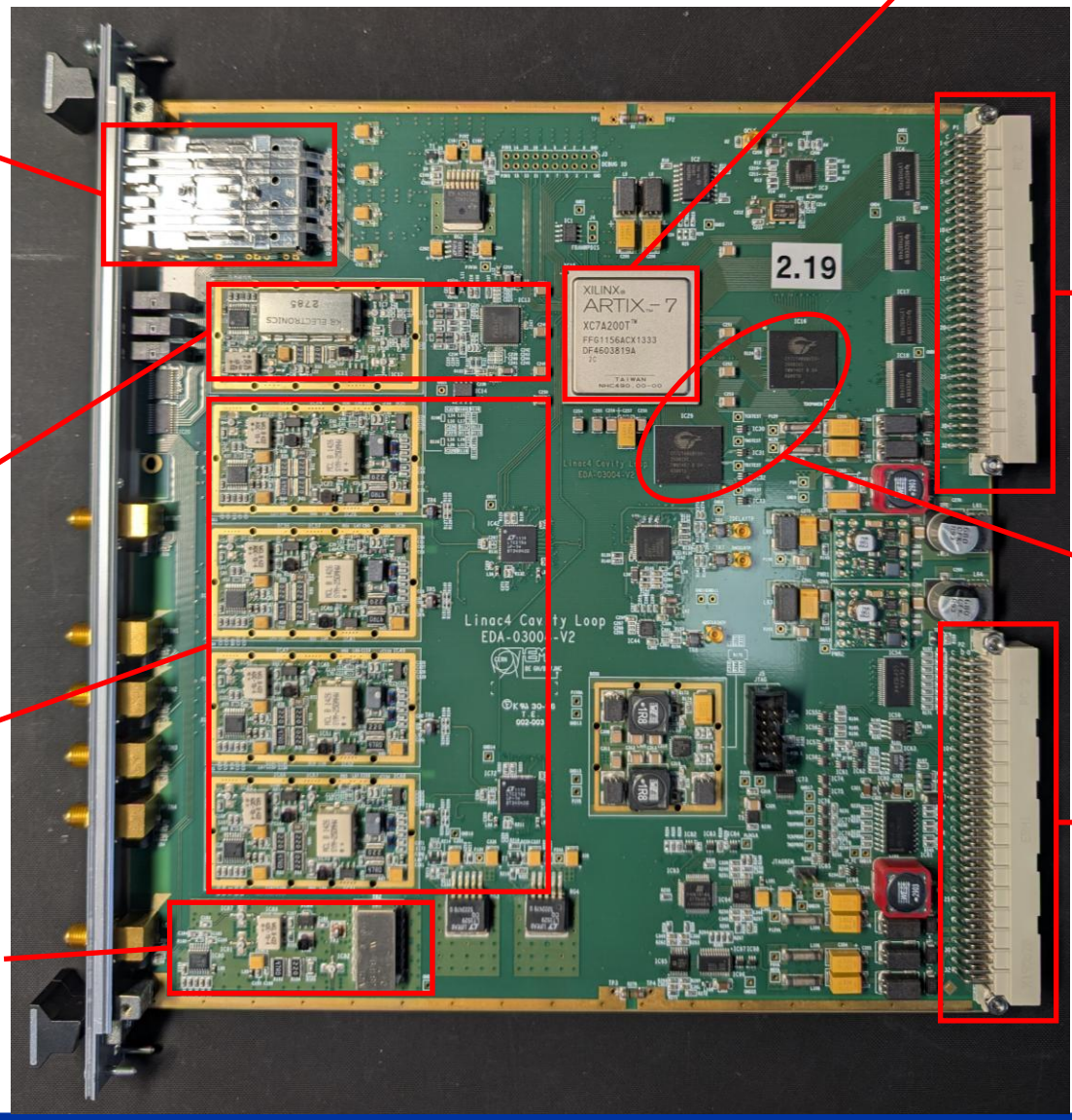


2x SFPs
(up to 2.5 Gbps)
PCI Express

16-bit IQ DAC +
Vector modulator
(BW = 25 MHz)

4 input channels
14-bit ADCs
(BW = 25 MHz)

LO distribution
(200 MHz – 1.5 GHz)



Artix-7 FPGA

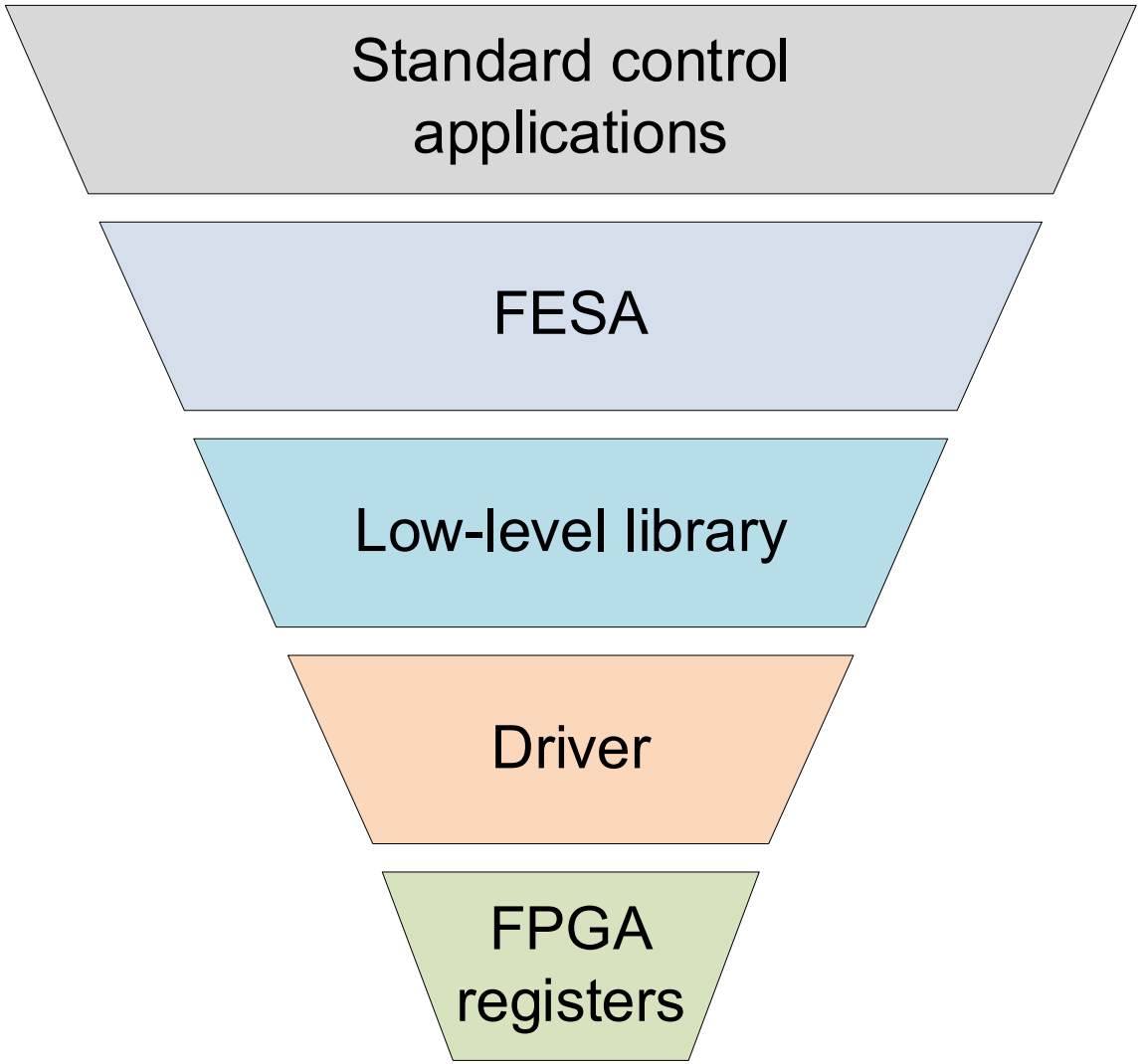
VME A24/D16

16 MB SSRAM

Clock,
triggers…

Software

- **CERN standard setup**
- **Reusing control applications layer**
- **Easy integration into CERN controls system**
- **Encapsulation of hardware related operations in low-level library**
- **Code generation for driver and FPGA registers layers**



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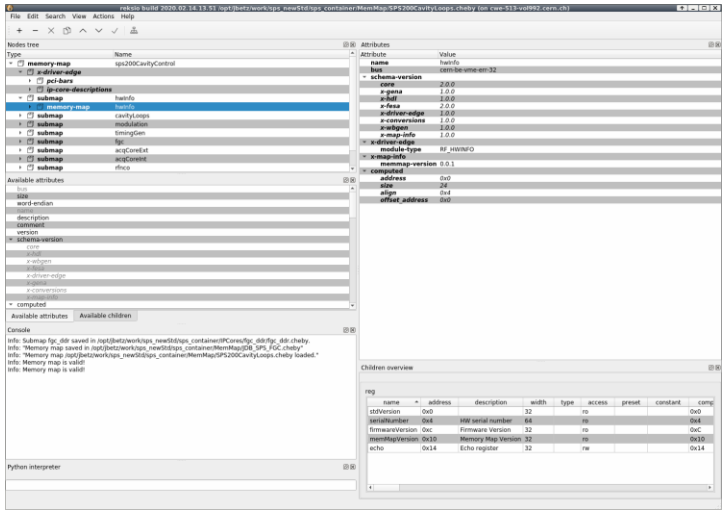
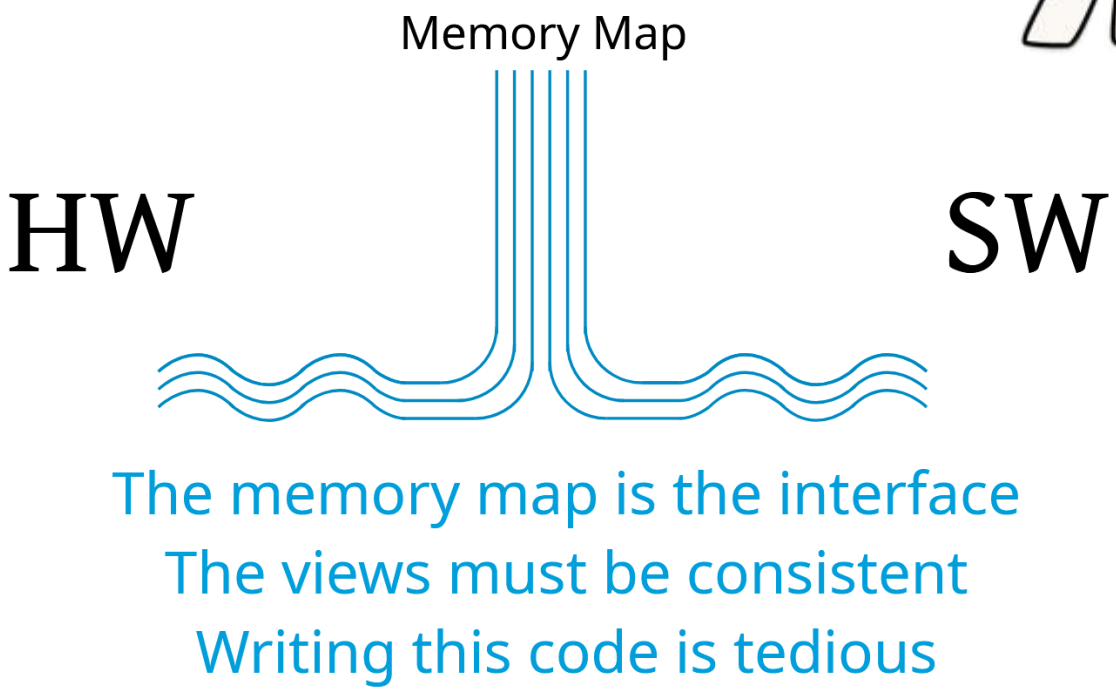




The memory map is the interface
The views must be consistent
Writing this code is tedious

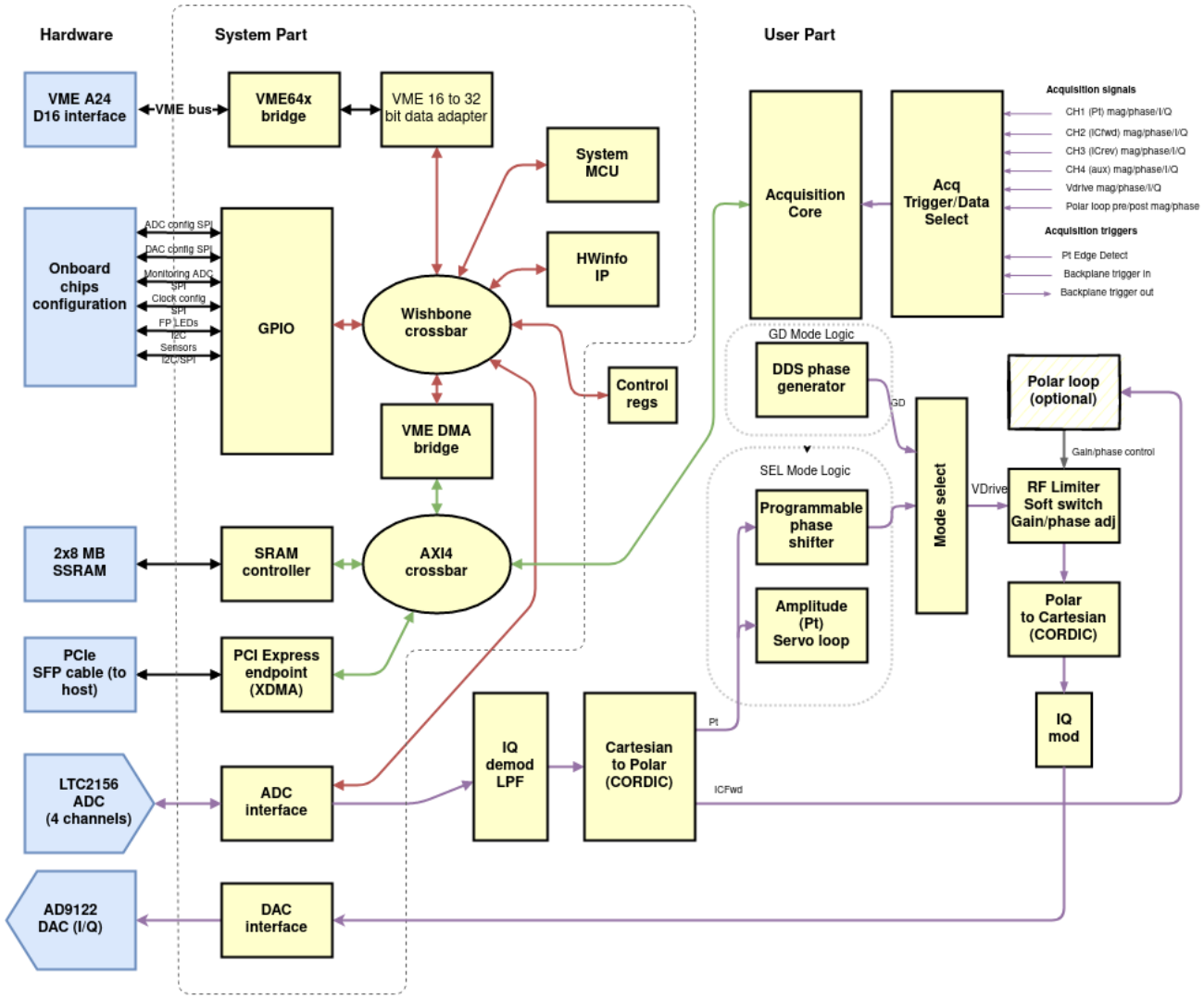
- **Create memory map with a graphical tool. Verify correctness**
- **Use code generators for HDL and C++ driver wrapper, FESA class skeleton**
- **Quick development/testing using Python**
- **Open-source tools**

T. Gingold, B. Bielawski - FPGA Developers' Forum 2025, CERN

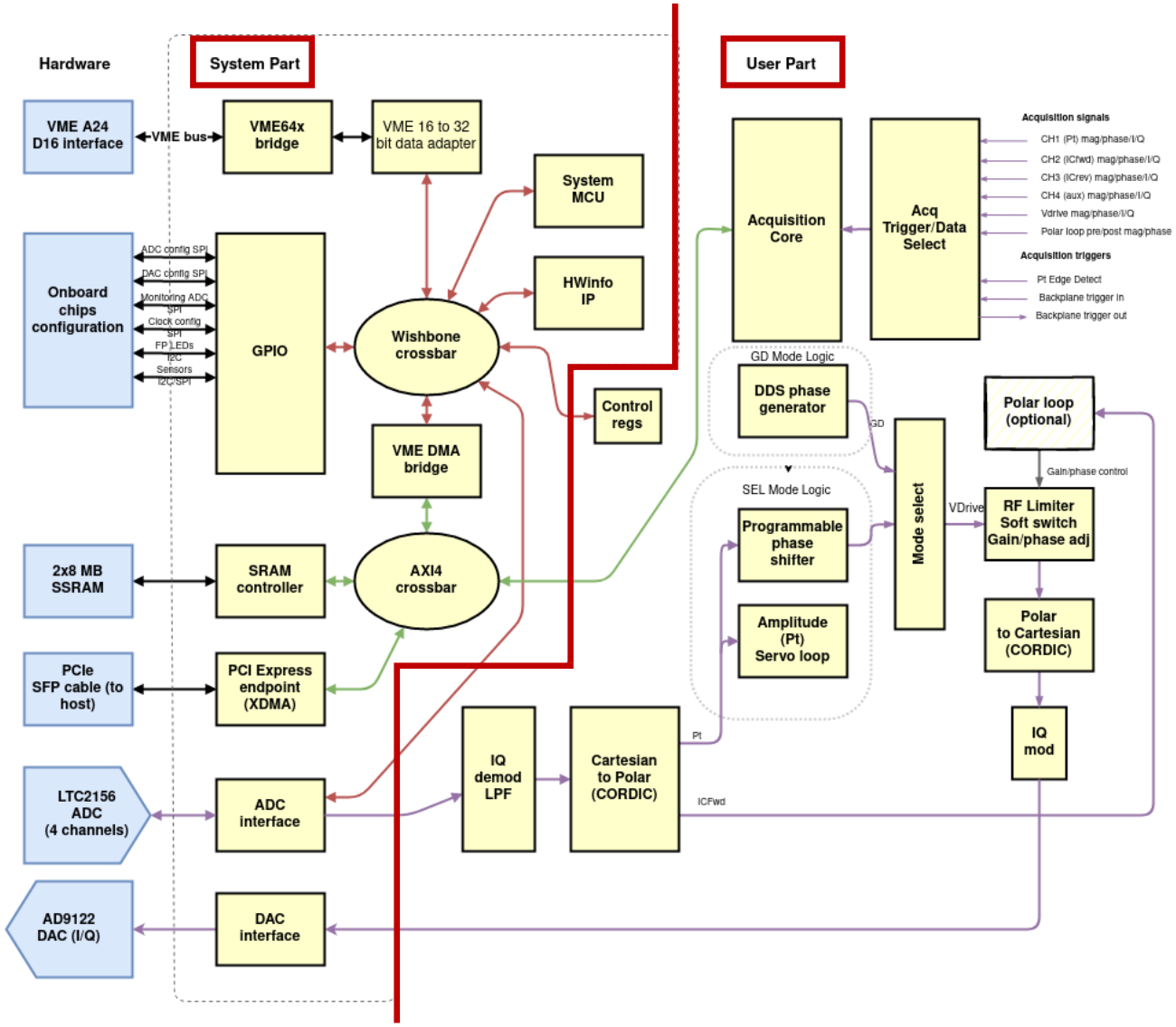
UCC architecture

- **Hardware independent architecture**
- **Reusability**
- **Standard blocks and processes**

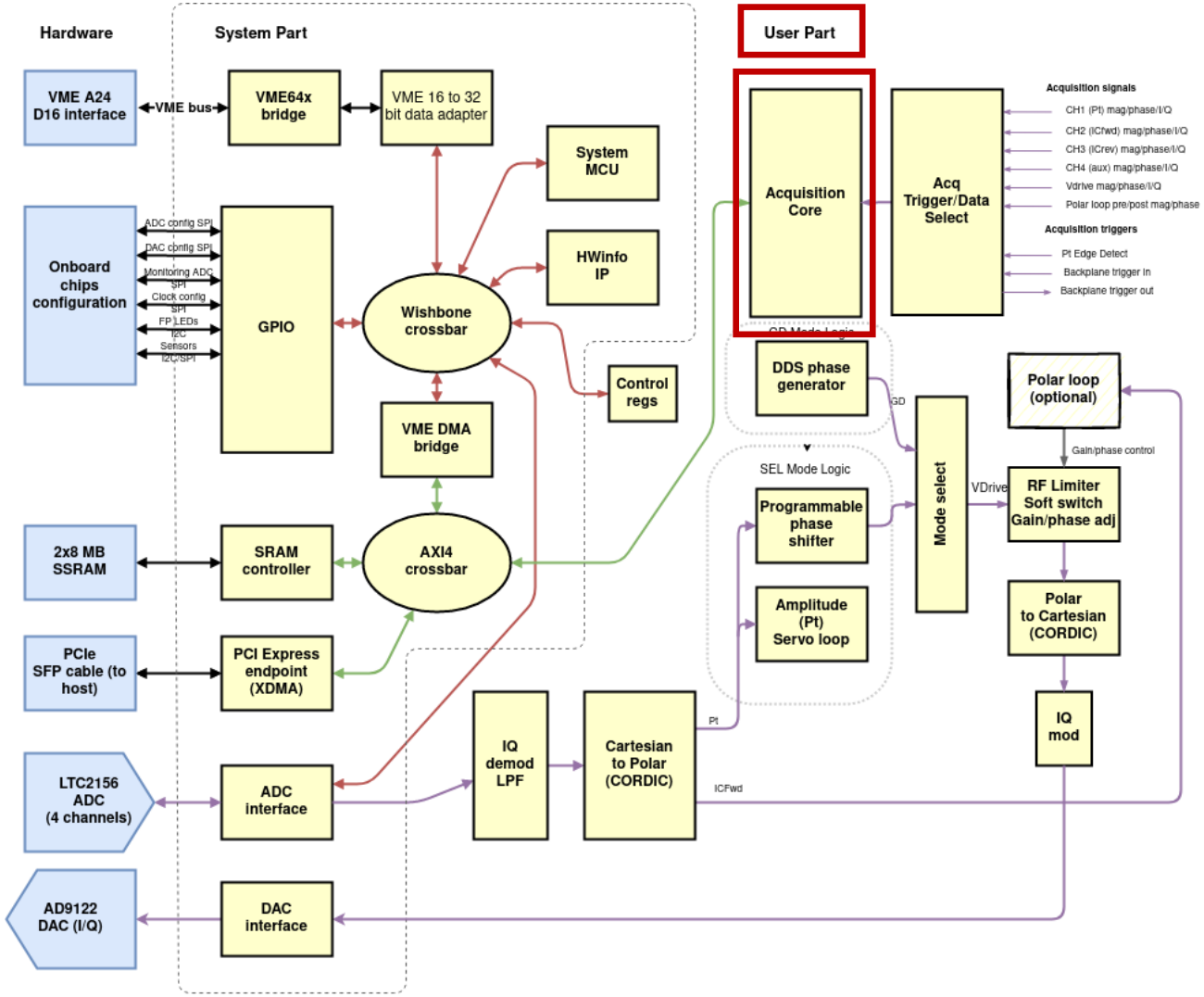
UCC architecture



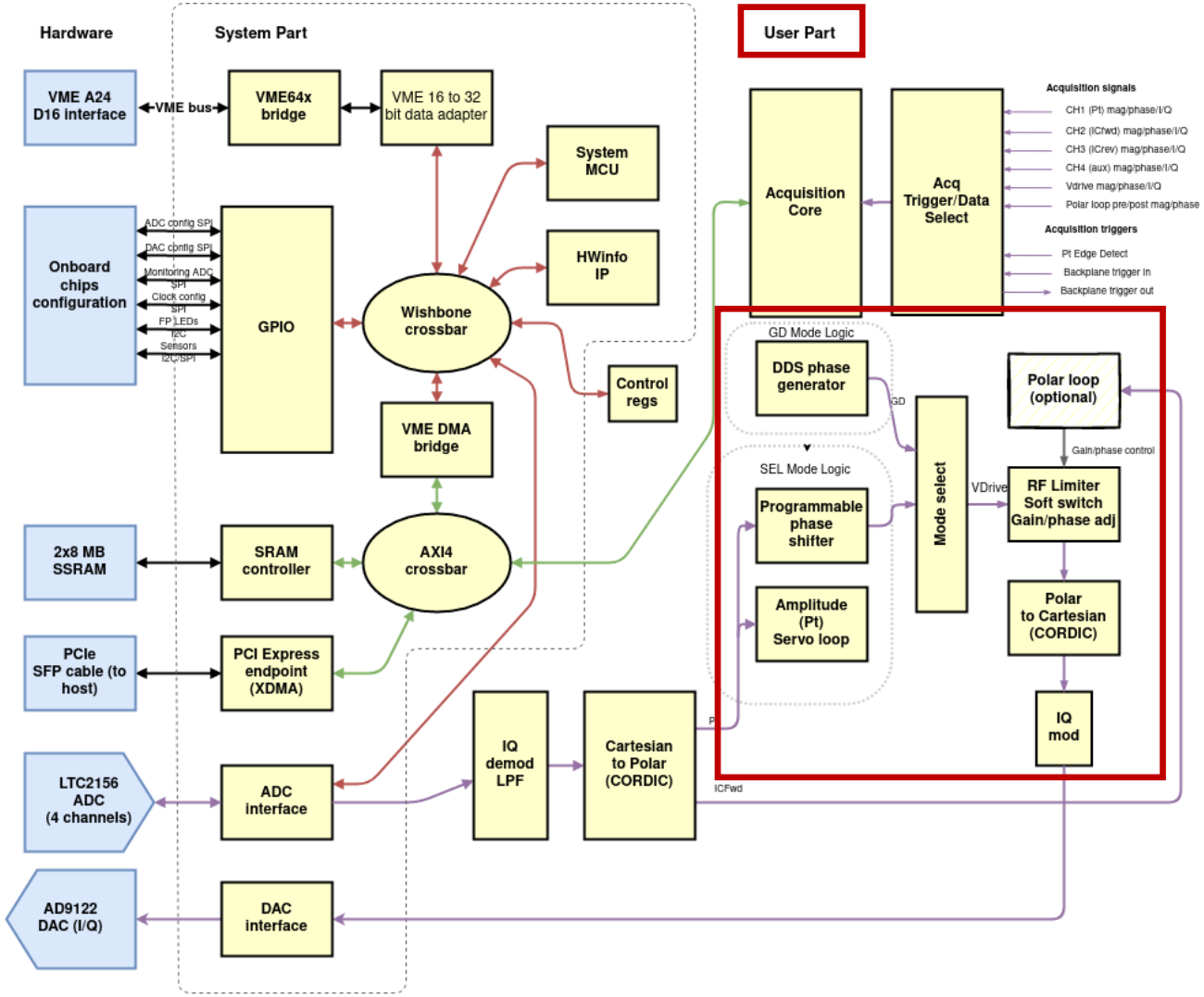
UCC architecture



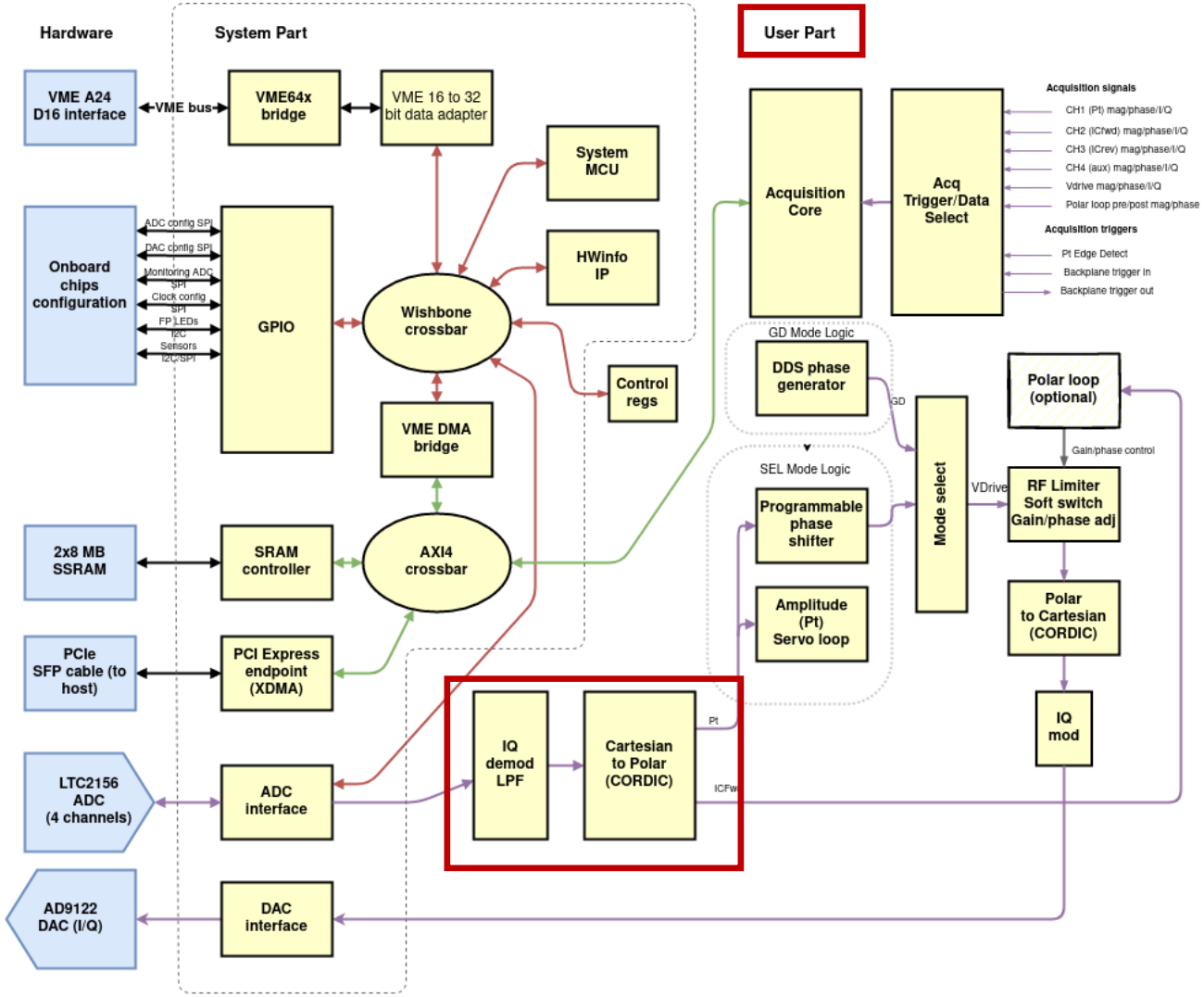
UCC architecture



UCC architecture

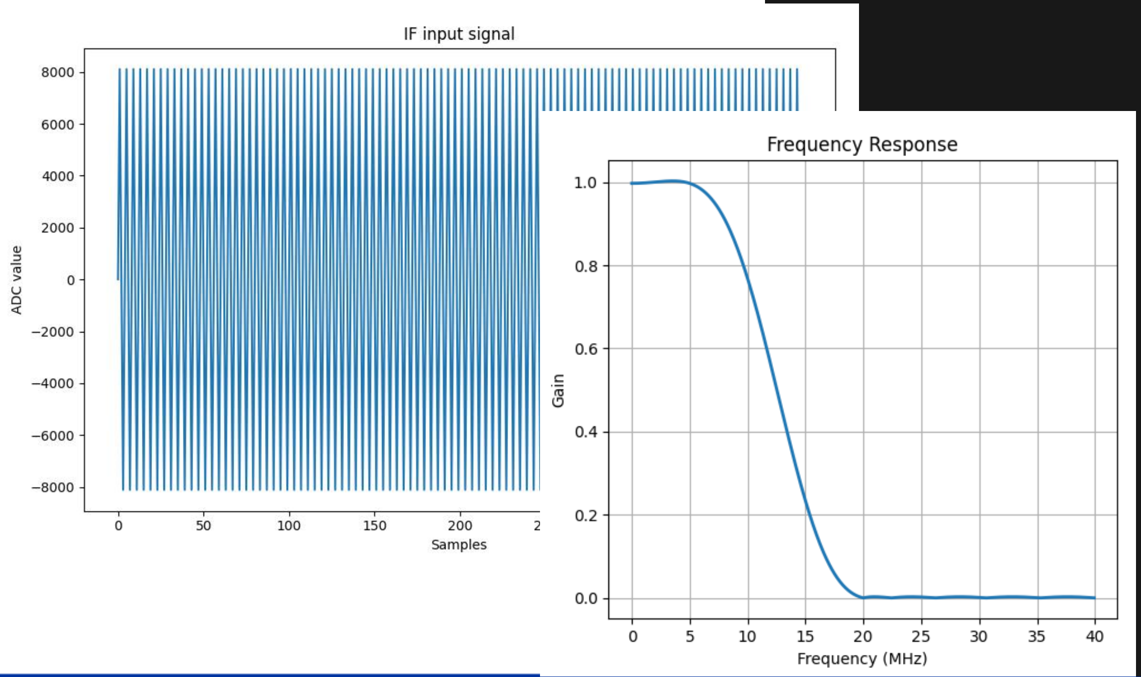


UCC architecture



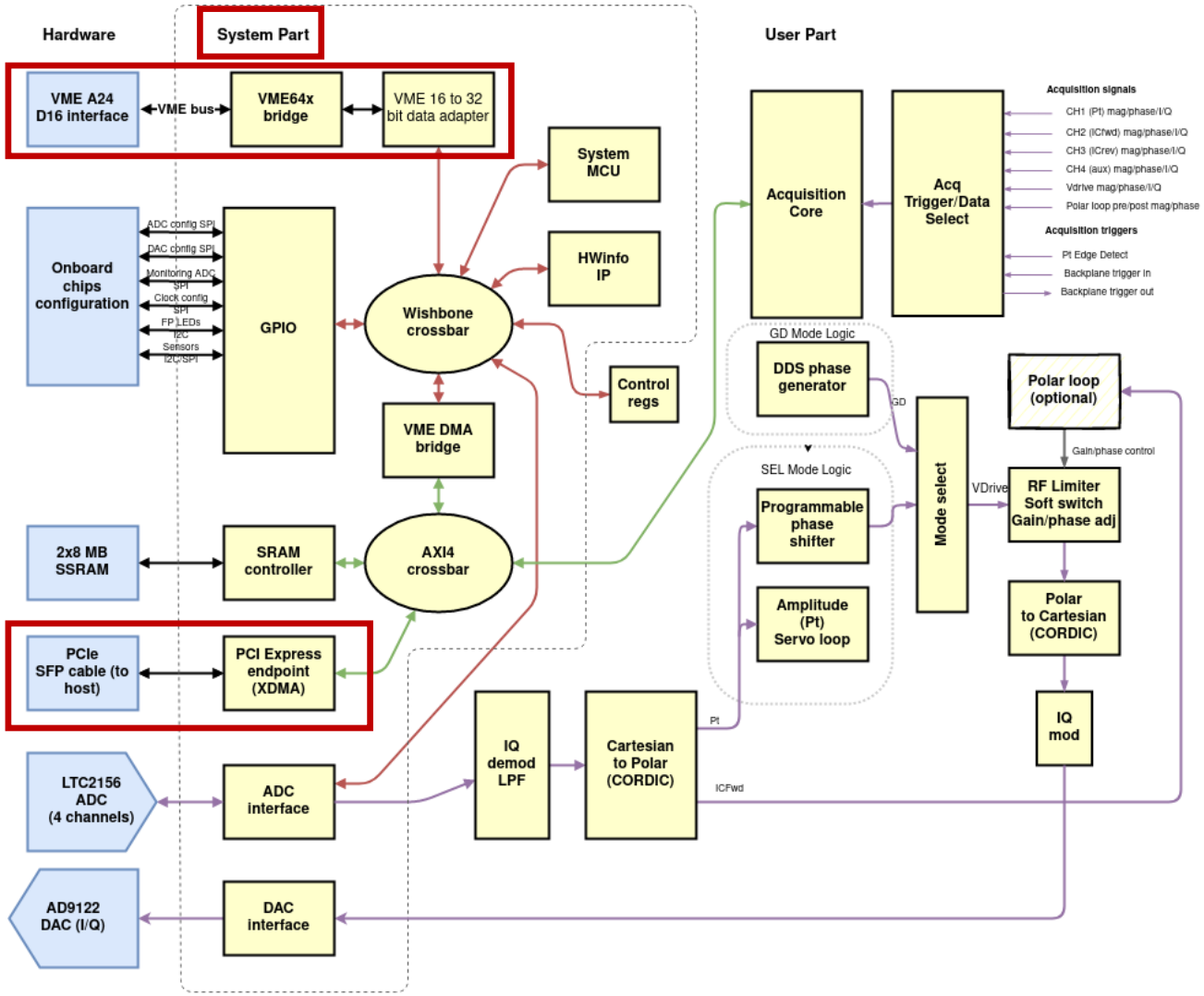
Ease development

- **Example:**
  1. Generate IF data with different attenuation, phase offset, frequency.
  2. Model demodulation, low-pass-filter, CORDIC
  3. Check magnitude, phase, frequency

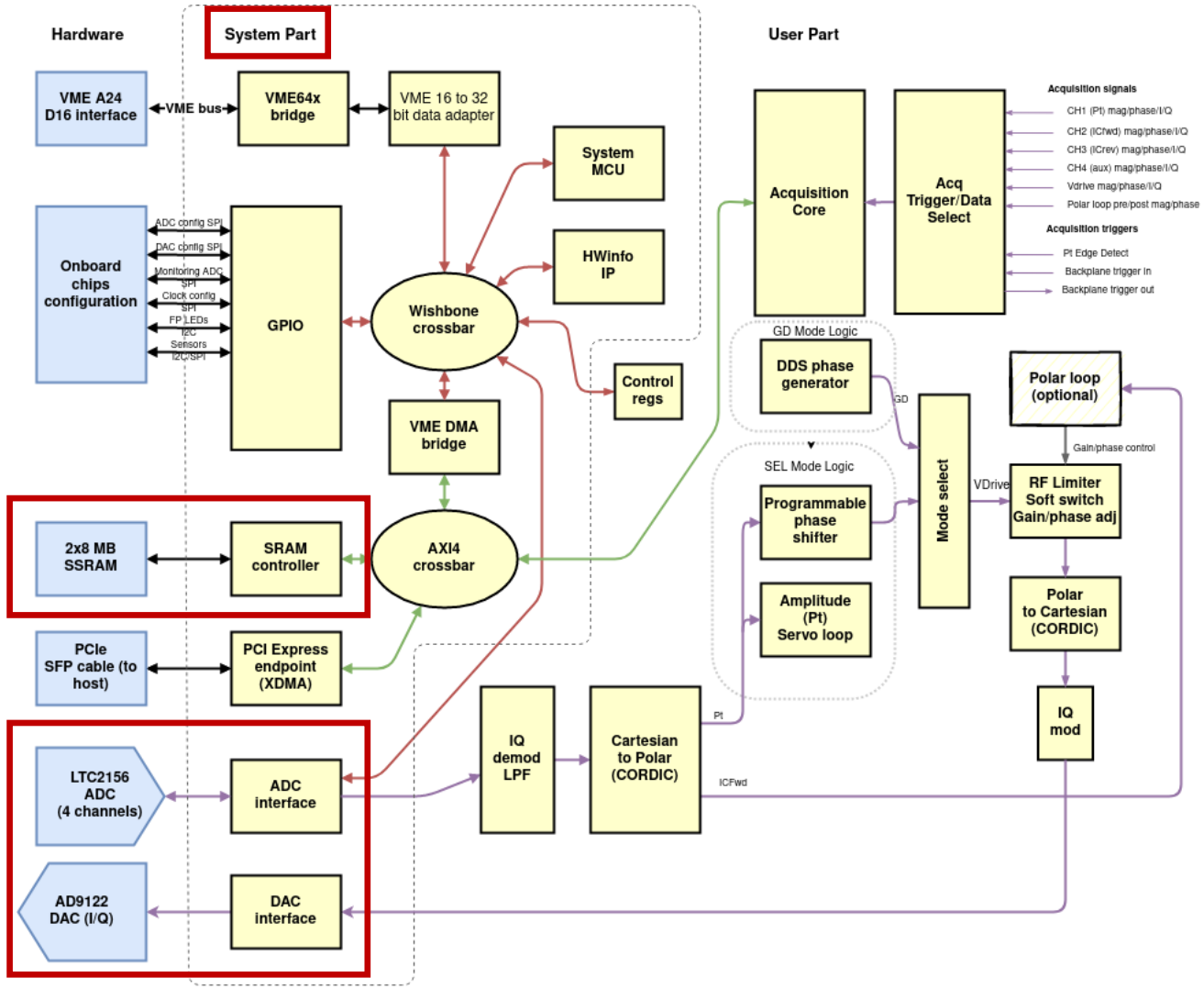



```
cocotb.regression
*******************************************************************************************************************
** TEST                                                        STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
*******************************************************************************************************************
** testbench_adc_iq_processing.testbench_adc_iq_processing_001   PASS        6543.75           0.88       7438.25  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_002   PASS        6543.75           0.86       7608.55  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_003   PASS        6543.75           0.82       8024.07  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_004   PASS        6543.75           0.81       8101.23  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_005   PASS        6543.75           0.63      10380.18  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_006   PASS        6543.75           0.60      10893.66  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_007   PASS        6543.75           0.58      11248.97  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_008   PASS        6543.75           0.68       9604.50  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_009   PASS        6543.75           0.74       8815.59  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_010   PASS        6543.75           0.86       7576.85  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_011   PASS        6543.75           0.96       6834.68  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_012   PASS        6543.75           0.89       7321.65  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_013   PASS        6543.75           0.74       8873.37  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_014   PASS        6543.75           0.70       9282.99  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_015   PASS        6543.75           0.69       9533.69  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_016   PASS        6543.75           0.68       9655.87  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_017   PASS        6543.75           0.68       9646.02  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_018   PASS        6543.75           0.70       9309.52  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_019   PASS        6543.75           0.75       8783.24  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_020   PASS        6543.75           0.83       7903.16  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_021   PASS        6543.75           0.85       7678.88  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_022   PASS        6543.75           0.77       8513.31  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_023   PASS        6543.75           0.71       9246.77  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_024   PASS        6543.75           0.68       9630.61  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_025   PASS        6543.75           0.68       9585.06  **
** testbench_adc_iq_processing.testbench_adc_iq_processing_026   PASS        6543.75           0.70       9409.97  **
```

UCC architecture



UCC architecture



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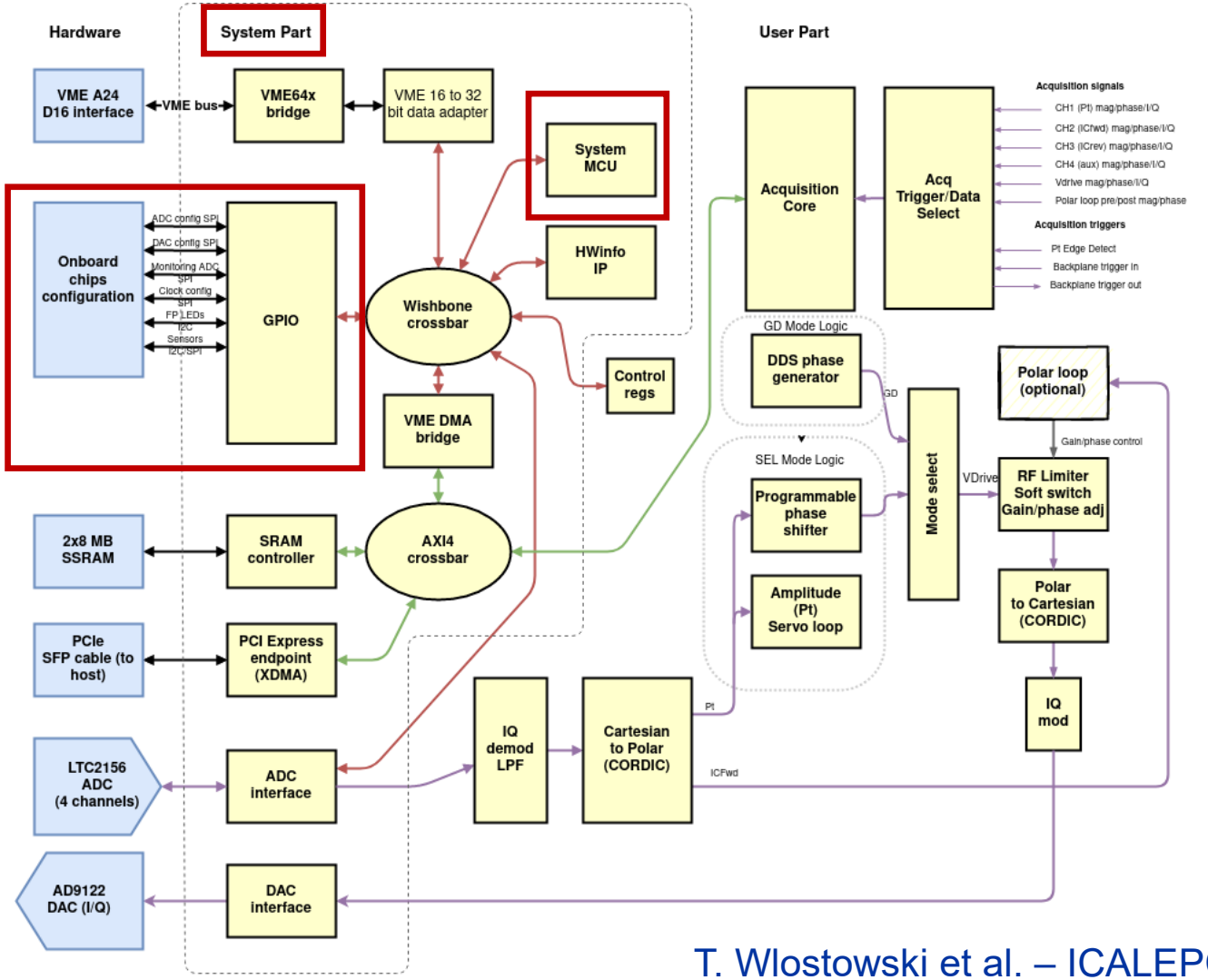
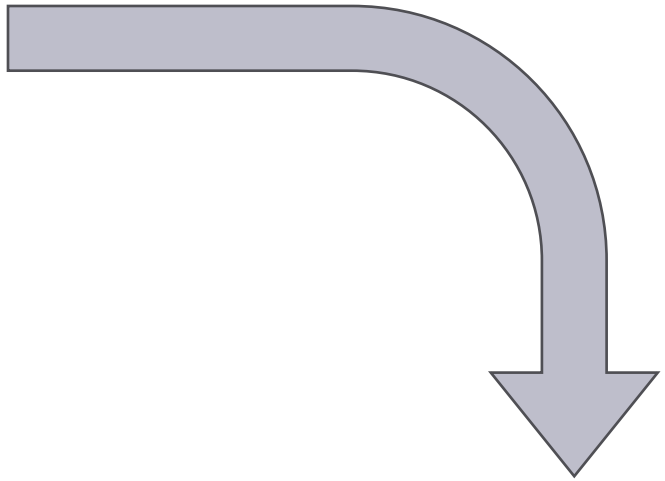


T. Wlostowski et al. – ICALEPCS 2015, Melbourne, Australia

UCC architecture

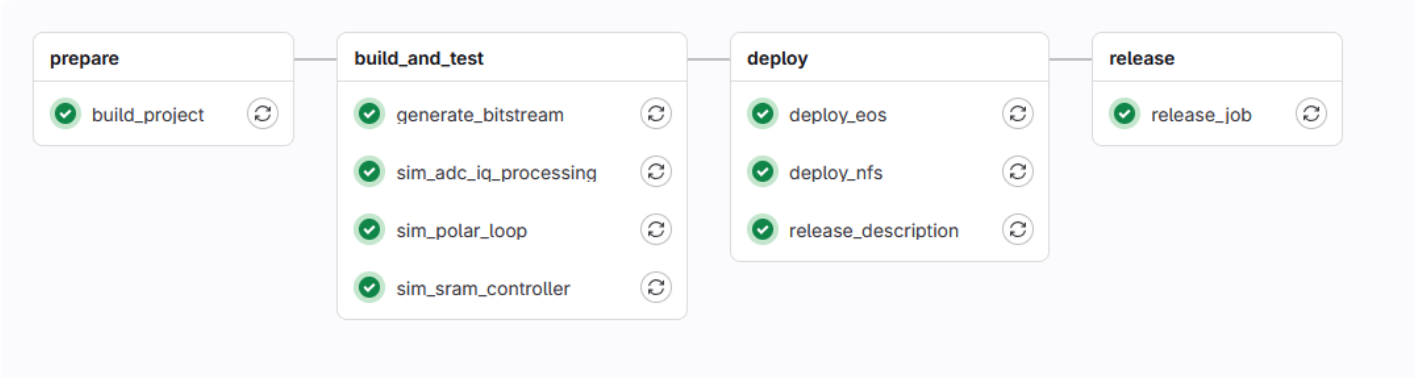
- **Hardware independent architecture**
- **Reusability**
- **Standard blocks and processes**



- **System/user parts**
- **MCU**
- **IP cores + shared libraries**
- **Continuous Integration**

Continuous Integration (CI)

- **Simulation, implementation, generation**



- **CI4FPGA service at CERN**
  - Scalable VM-based k8s clusters
  - Easy-to-use Docker images
  - Comprehensive documentation

C. Gentsos - FPGA Developers' Forum 2025, CERN

List of tools available as images

The following tools are available in the registry.cern.ch/ci4fpga project:

Toolchains

- Xilinx Vivado
- Xilinx ISE
- Microsemi Libero
- Intel Quartus
- Lattice Diamond

Simulators

- Riviera-PRO
- GHDL (GCC backend)
- GHDL (mcode backend)
- NVC
- QuestaSim
- ModelSim
- Icarus Verilog
- Altair DSim

Lint (and lin-related) tools

- VHDL Style Guide
- Aldec ALINT-PRO
- Verible

Documentation generation

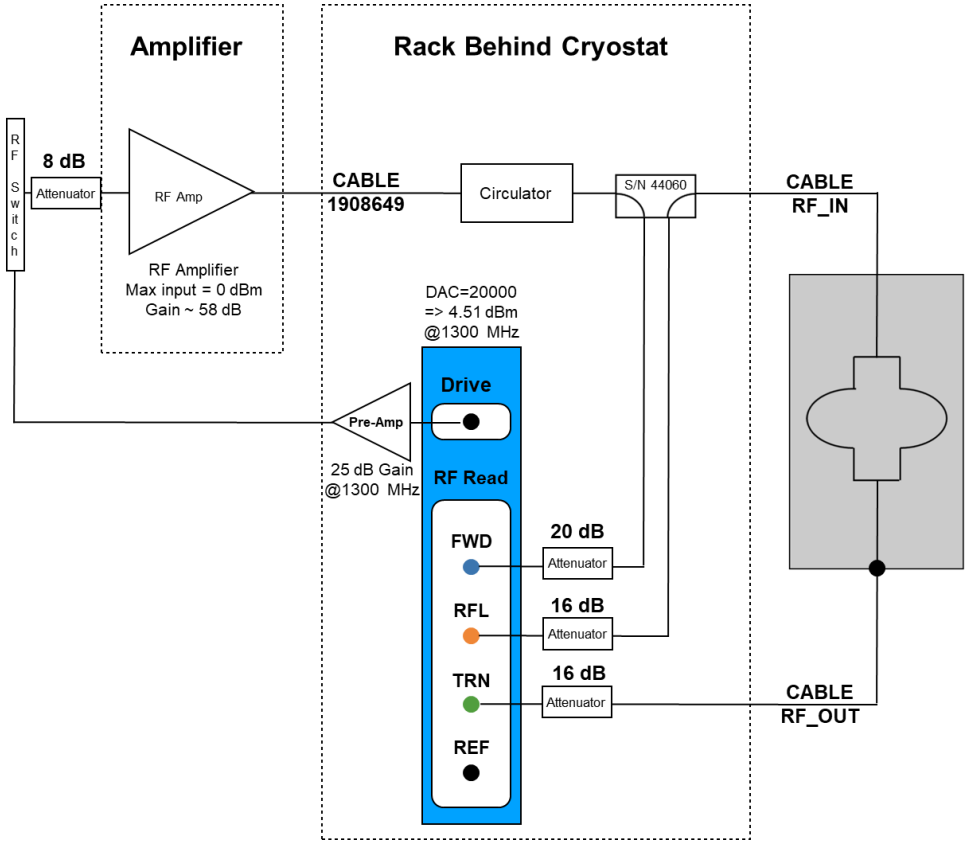
- AMIQ EDA DVT
- Doxygen

Assorted tools

- YosysHQ OSS CAD Suite
- PetaLinux
- VisualElite
- Synopsys Synplify

Cavity tests

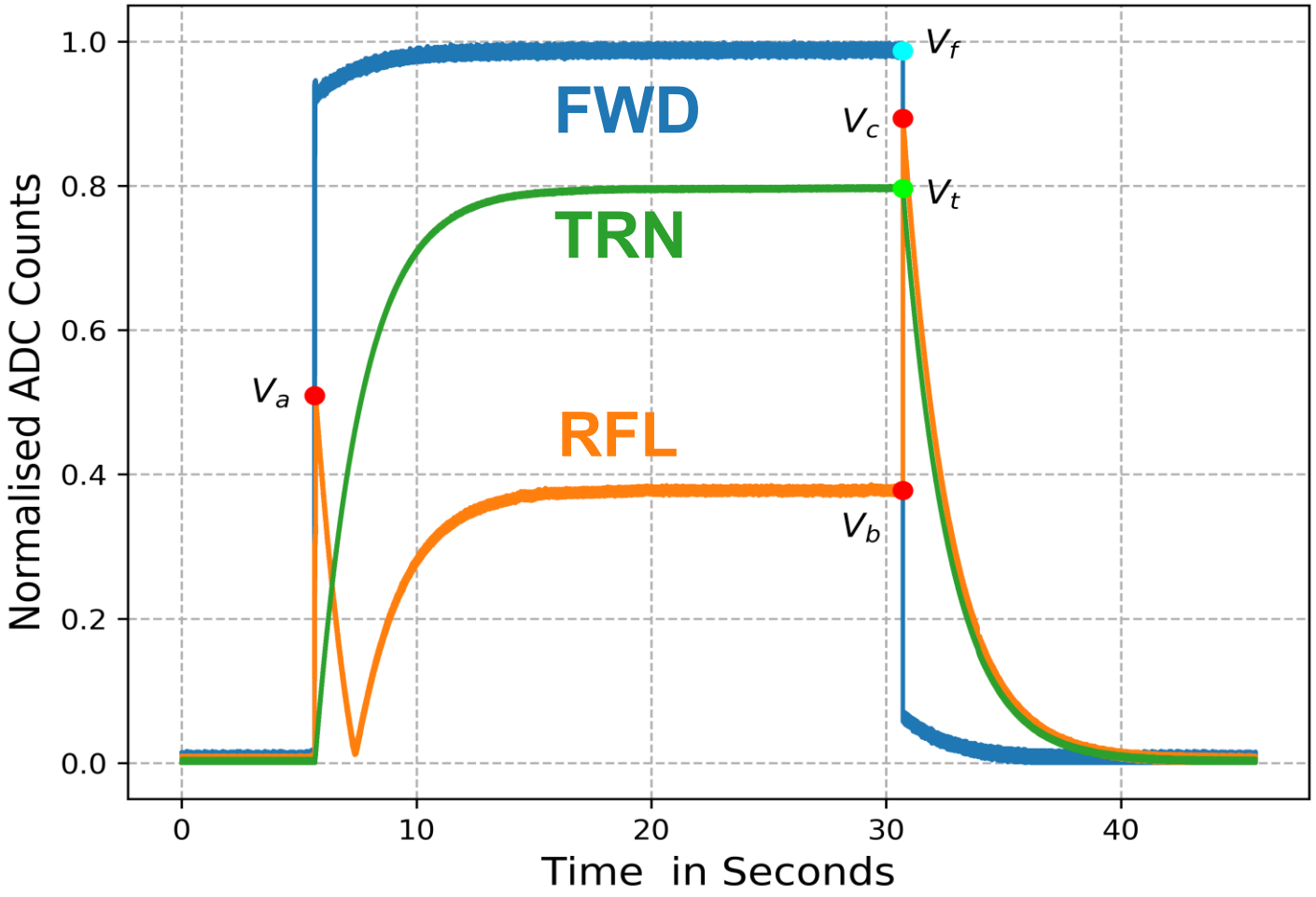
- **Tests setup installation**
- **Gradual deployment into all SRF test systems**



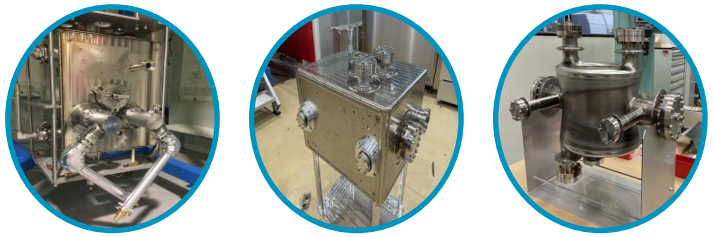
Mobile development setup

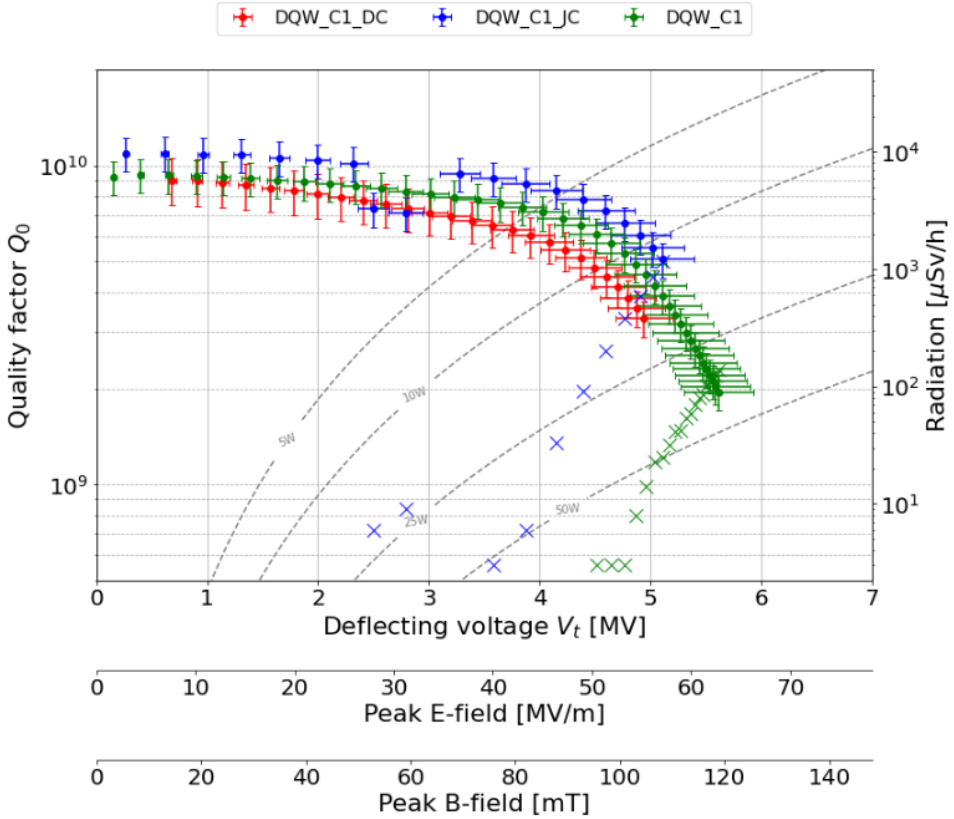
Cavity tests

Self-Excited Loop: Typical pulse measurement



Recent 400 MHz Crab cavity performance validation campaign



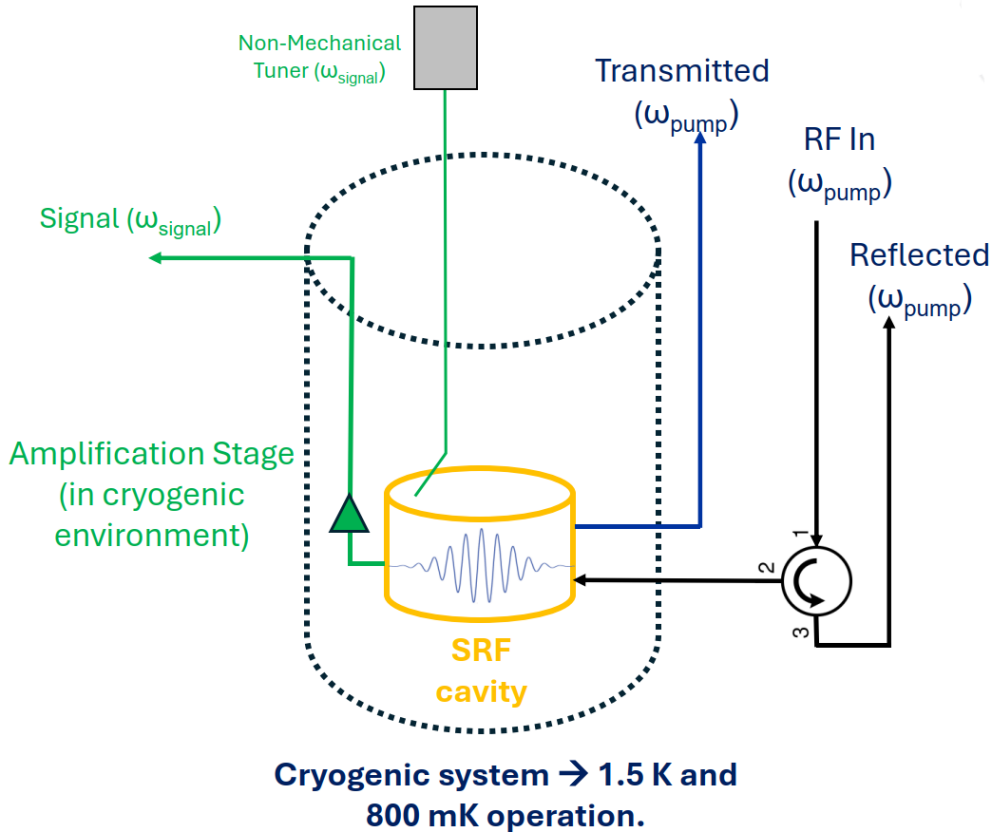


Courtesy of HL-LHC WP4 – Crab Cavities

Future challenges: Axion detection

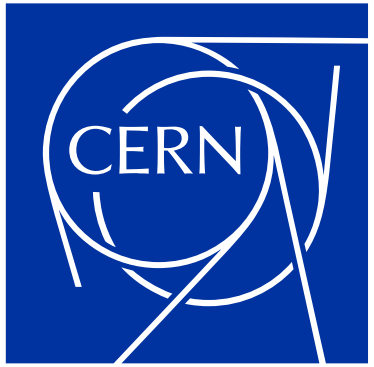
- **Heterodyne approach:**
  - Drive a high-Q cavity at a frequency, ω_{pump}.
  - Axion interacts with cavity field and transfers energy to a second mode at ω_{signal}.
  - Monitor ω_{sig}, the axion mass is given by the frequency difference ($\Delta\omega = \omega_{pump} - \omega_{signal}$).
  - Mass range can be scanned by varying $\Delta\omega$ → tuning system.
- **Initial tests in Q1 2026**

No external B-field required.



Cryogenic system → 1.5 K and 800 mK operation.

L. Millar et al. – 22nd International Conference on RF Superconductivity (SRF2025), Tokyo, Japan



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