U.S. DEPARTMENT OF ENERGY
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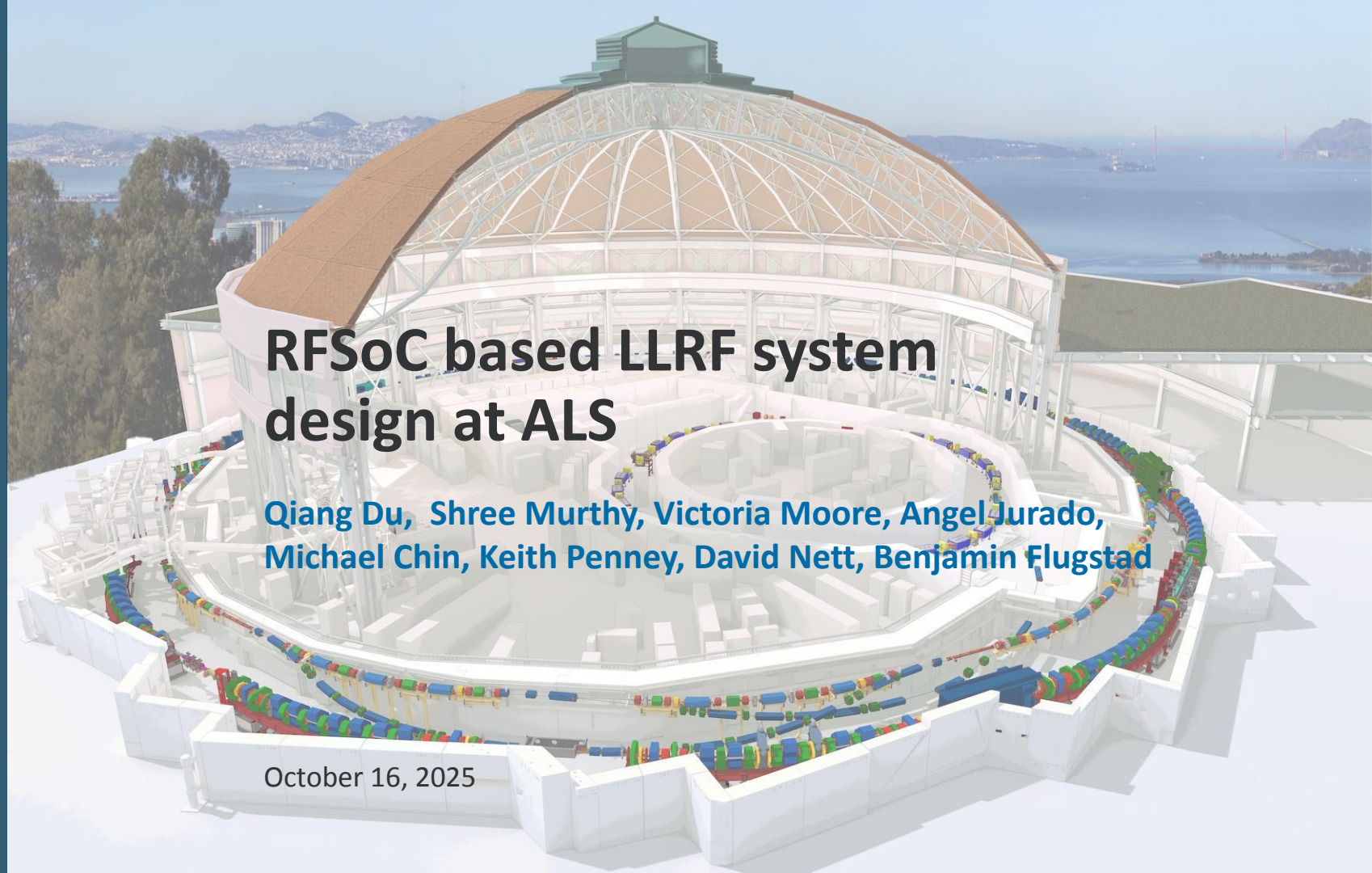
BERKELEY LAB

ALS-U
ADVANCED LIGHT SOURCE

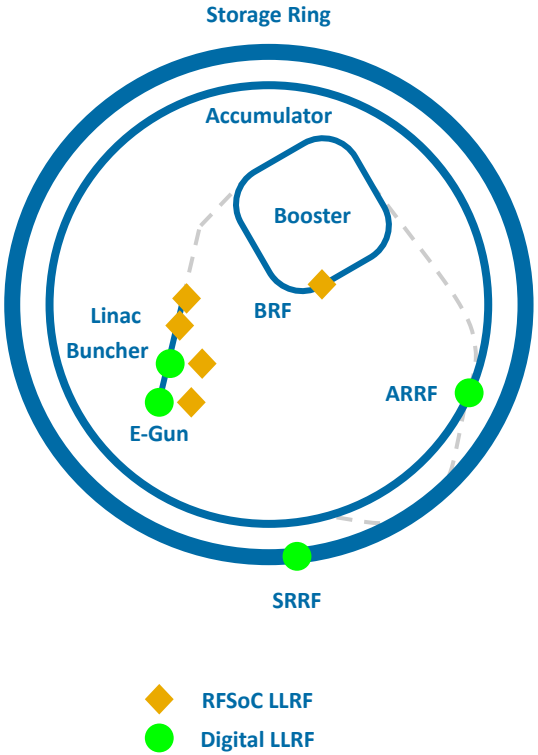


RFSoC based LLRF system design at ALS

Qiang Du, Shree Murthy, Victoria Moore, Angel Jurado, Michael Chin, Keith Penney, David Nett, Benjamin Flugstad

October 16, 2025

Roadmap of RFSoC based LLRF systems in ALS



2026? **Booster LLRF**
LBL208 RFSoC
500MHz, CW, **closed** loop

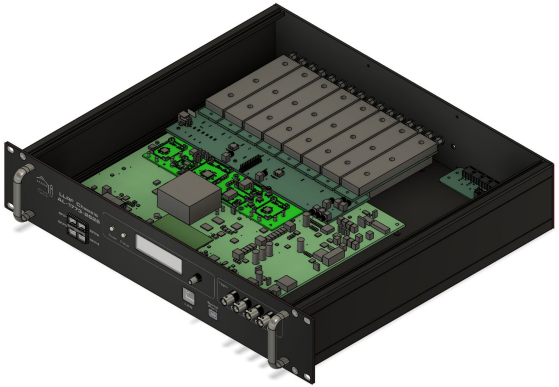
2025 **RFSoC Linac & Buncher LLRF**
LBL208 RFSoC
125MHz, 500MHz, 3GHz, pulsed, **closed** loop

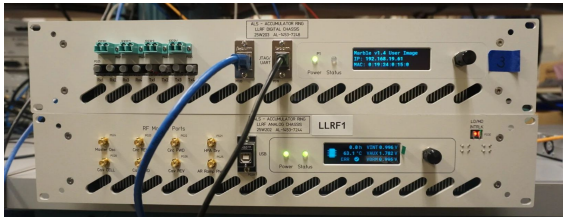
2023.5 **E-Gun LLRF**
Marble FPGA carrier
125MHz, pulsed

2022.8 **Buncher LLRF**
MarbleMini FPGA carrier
125MHz, 500MHz RF, pulsed

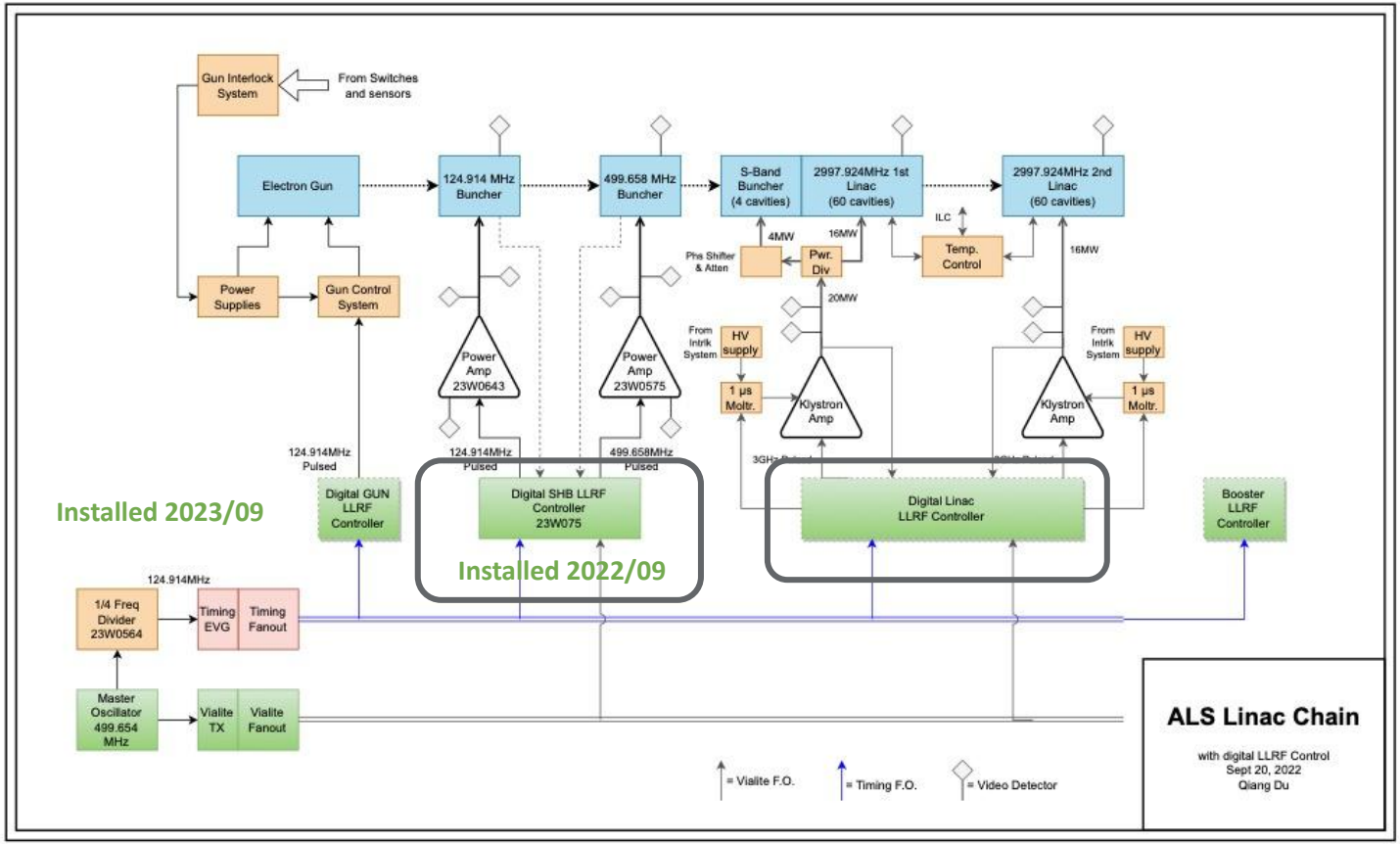
2021.7 **AR RF LLRF**
Marble FPGA carrier
2 Cavities, 60kW, 16 RF channels, 4 FPGA

2017.3 **SR RF LLRF**
KC705 FPGA carrier
2 Cavities, 42 RF channels, 3 FPGA system





Upgrade of SHB / Linac LLRF to close-loop



High Power RF system specifications

- Sub-Harmonic Buncher (SHB)
  - Frequency:
    - SHB1: 124.90 MHz (F_MO / 4)
    - SHB2: 499.64 MHz (F_MO)
  - Pulse width: about 30 microsecond
  - Trigger rate: about 0.7 Hz
  - 4 intra-pulse feedback loops:
    - SHB1: Amplitude & Phase loop
    - SHB2: Amplitude & Phase loop
    - Bandwidth: > 100kHz
  - SSA: 20kW each
  - PLC communication interface
  - EPICS control interface
  - RSS/PSS RF permits, interlocks integration

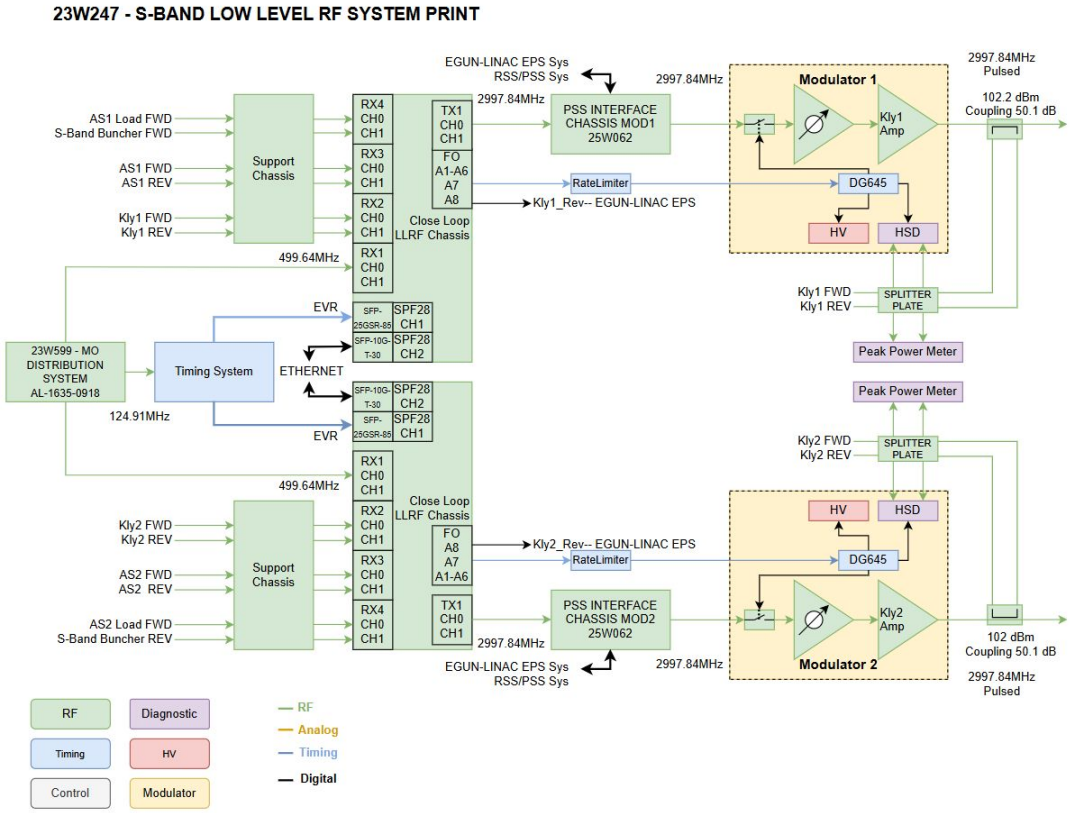
- Linear Accelerator (Linac)
  - Frequency:
    - Mod1: 2997.84 MHz (F_MO * 6)
    - Mod2: 2997.84 MHz (F_MO * 6)
  - Pulse width: about 5 microsecond
  - Trigger rate: about 0.7 Hz
  - 4 inter-pulse feedback loops:
    - Mod1: Amplitude & Phase loop
    - Mod2: Amplitude & Phase loop
    - Bandwidth: < 0.3 Hz
  - Modulator
  - PLC communication interface
  - EPICS control interface
  - RSS/PSS RF permits, interlocks integration

Low Level RF system specifications

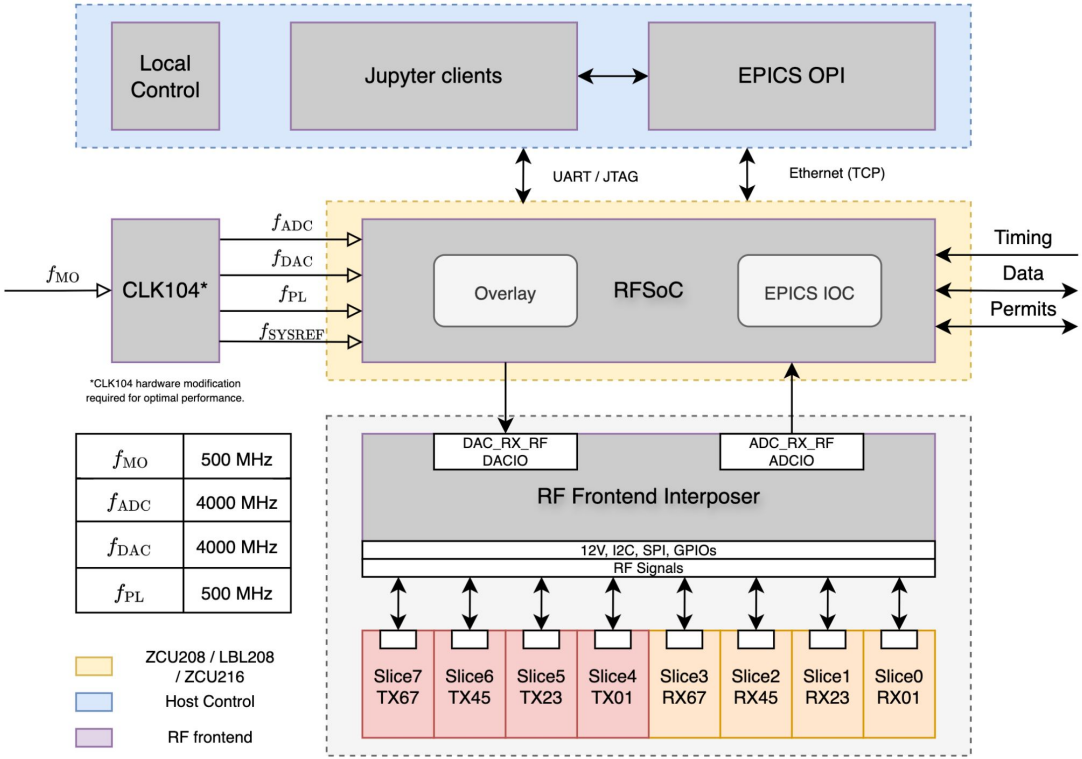
- Sub-Harmonic Buncher (SHB)
  - 8 RX channels:
    - SHB1: Forward, Reverse, Cell (Feedback)
    - SHB2: Forward, Reverse, Cell (Feedback)
    - MO1, MO2
  - 2 TX channels:
    - SHB1 Drive
    - SHB2 Drive
  - Amp stability: <0.1%
  - Phase stability: <0.02 degree
  - Interfaces:
    - Local HMI: panel display
    - Remote control: EPICS
    - Interlock: AFBR fiber-optic
    - Timing: LBNL event distribution

- Linear Accelerator (Linac)
  - 8 RX channels:
    - Mod1: Forward (Feedback), Reverse, AS Forward, AS Load
    - Mod2: Forward (Feedback), Reverse, AS Forward
    - MO
  - 2 TX channels:
    - Mod1 Drive
    - Mod2 Drive
  - Amp stability: <0.1%
  - Phase stability: <0.1 degree
  - Interfaces:
    - Local HMI: panel display
    - Remote control: EPICS
    - Interlock: AFBR fiber-optic
    - Timing: LBNL event distribution

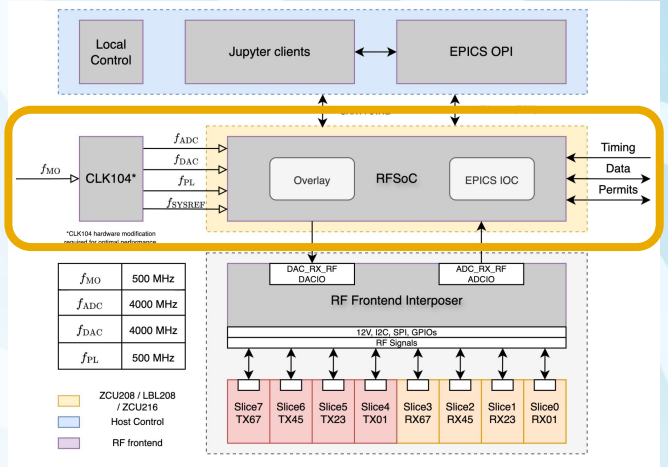
3GHz LINAC Low Level RF System



ALS RFSoC LLRF System Overview



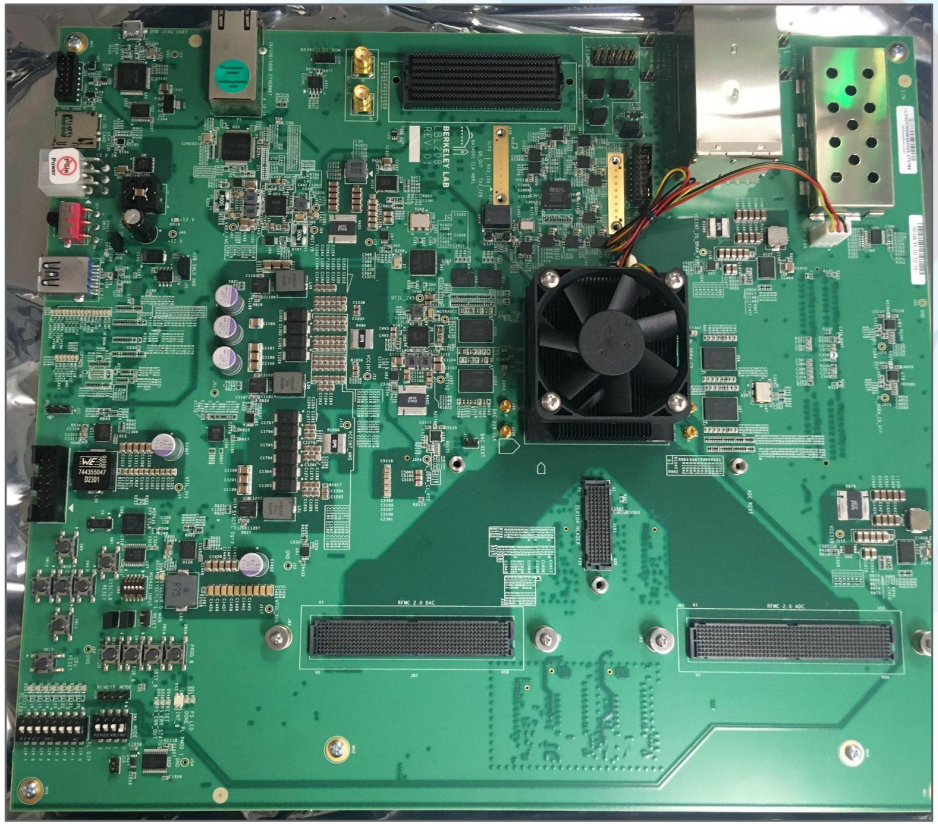
RFSoC Characterization



- Shree Murthy, et al, “Comparative Evaluation of Xilinx RFSoC Platform for Low-Level RF Systems”, Oct 14, 2025, 2:10 PM

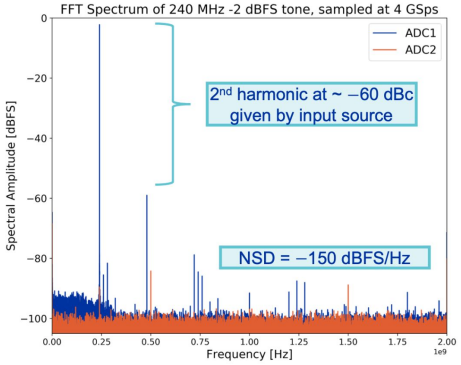
LBL208 - Ultrascale+ RFSoC Carrier

- Xilinx designed, LBL modified, Whizz Systems manufactured
- Modified to ease chassis integration and replace obsolete components
- RFSoC FPGA changed from XCZU4**8**DR-2 to XCZU4**7**DR-1 to reduce cost
- Shared platform for Ultrascale+ RFSoC LBL applications



Expected ADC Performance

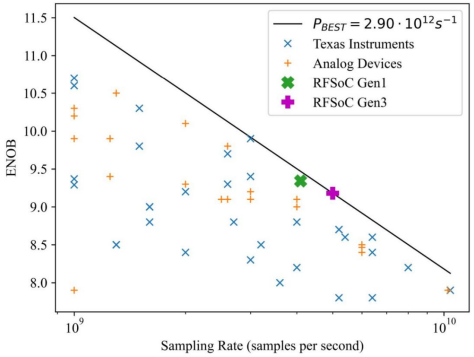
The RF System-on-Chip Technology
ADC Performance



	SNR (dBFS)	SFDR (dBFS)	ENOB
AD9208[1] (14b, 3 GSps)	60.2	78	9.7
RFSoC (12b, 4 GSps)	*58*	74[3]	*9.3*
TI 12DJ4000RF[2] (12b, 4 GSps)	57	67	9.0

1. Analog Devices, AD9208 Data Sheet link
2. Texas Instrument, ADC12DJ4000RF Data Sheet, link
3. J.E. Dusatko, "Evaluation of the Xilinx RFSoC for Accelerator Applications", in *Proc. NAPAC'19*, Lansing, MI, USA, Sep. 2019, pp. 483-486. link

The RF System-on-Chip Technology
ADC Performance



Measurement of performance

$P = 2^{\mathrm{ENOB}} \times F_s$

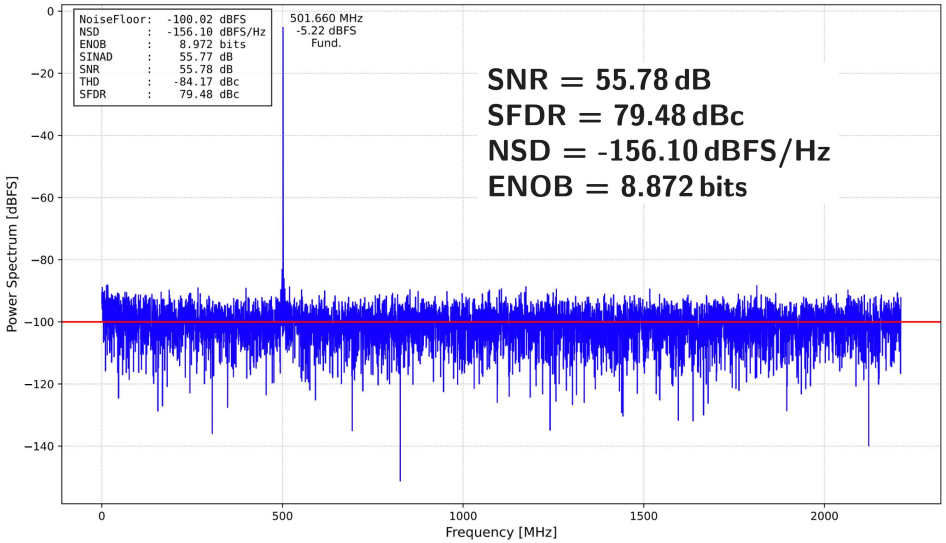
RFSoC Gen3 ADCs have **excellent P**

Credit: RFSoC-based Development for HL-LHC Beam Position Monitors
HL-LHC BPM team, 3rd CERN System-on-Chip Workshop, March 10, 2023

ADC Performance at Fs=4Gsps

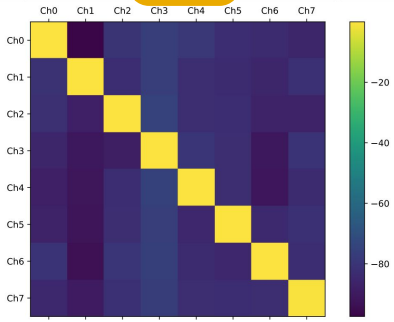
Measured on Dual Tile devices: ZCU208 (xczu48dr-2) and LBL208 (xczu47dr-1)

ADC spectrum: wide band
Fc=500 MHz, Fs=4 Gsps



ADC cross-talk: > 75.2 dB
Fc=500 MHz, Fs=4 Gsps

	C0	C1	C2	C3	C4	C5	C6	C7
C0	-0.4	-97.4	-80.5	-76.5	-78.9	-83.3	-83.4	-85.9
C1	-81.2	-0.4	-83.2	-76.7	-82.9	-83.4	-85.7	-81.6
C2	-82.5	-88.1	-0.3	-75.2	-82.7	-83.1	-86.9	-86.4
C3	-85.7	-90.9	-88.4	-0.0	-79.9	-82.6	-91.2	-80.8
C4	-88.1	-91.8	-83.1	-75.3	-0.3	-82.9	-91.5	-84.1
C5	-86.9	-92.4	-82.7	-76.7	-84.9	-0.3	-84.3	-81.5
C6	-80.9	-93.3	-80.2	-76.4	-83.7	-85.1	-0.3	-83.0
C7	-84.5	-89.7	-81.7	-77.2	-82.9	-83.2	-82.9	-0.5



DAC Performance: spectrum and crosstalk

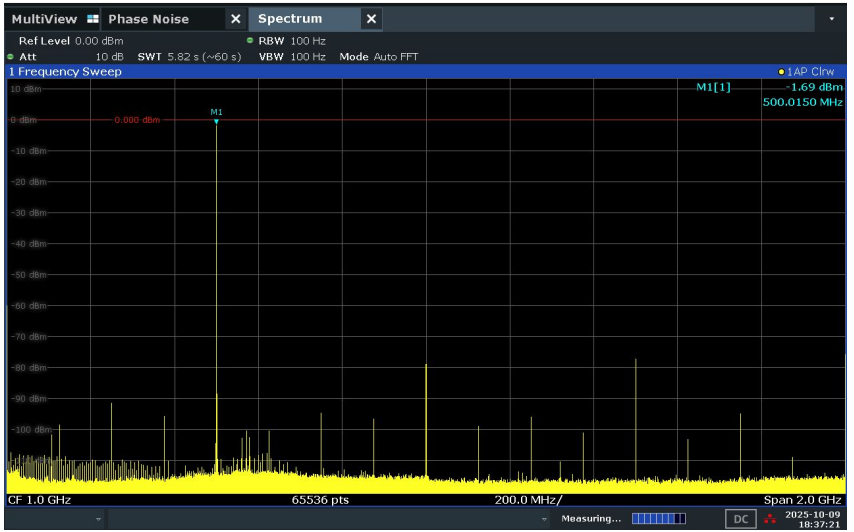
Measured on Dual Tile devices: ZCU208 (xczu48dr) and LBL208 (xczu47dr)

DAC Output spectrum narrow band

Fc=500 MHz, Fs=4 Gsps

DAC Output spectrum wide band

Fc=500 MHz, Fs=4 Gsps

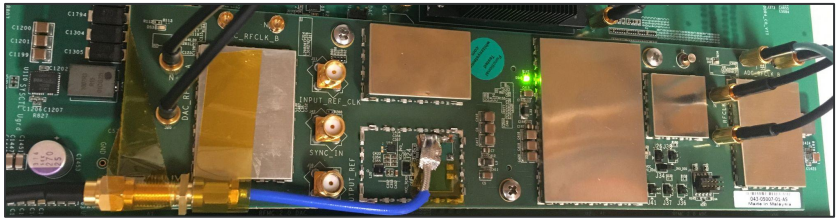


*DAC crosstalk > 80 dB per Xilinx characterization report

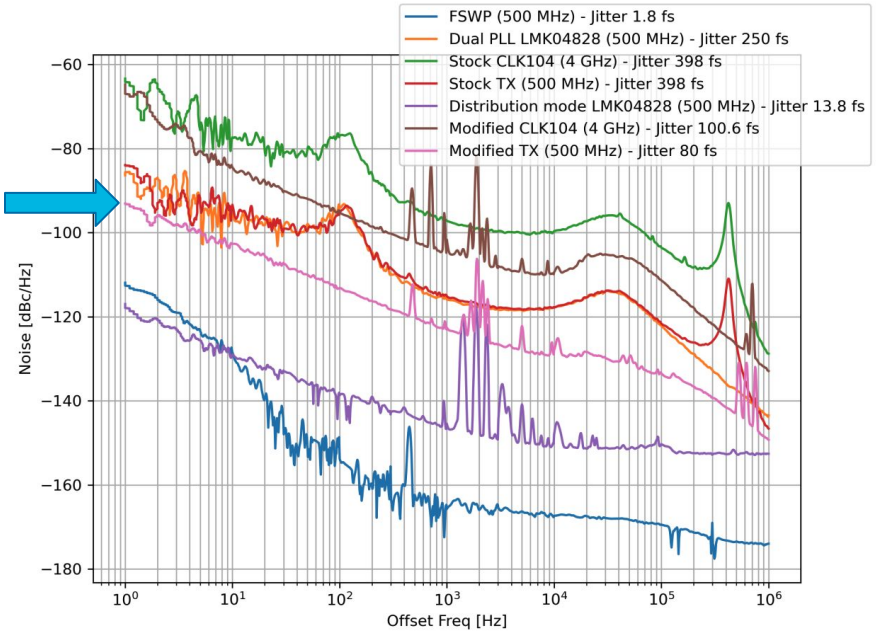
RF output Phase noise optimization

CLK104 optimization

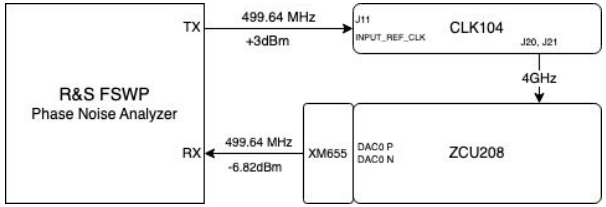
- Clocking chain analysis drive hardware and software modifications
- Initial prototyping required RF cut and jumper
- Synthesizer loop filters simulated and optimized
- Modified prototype in manufacturing



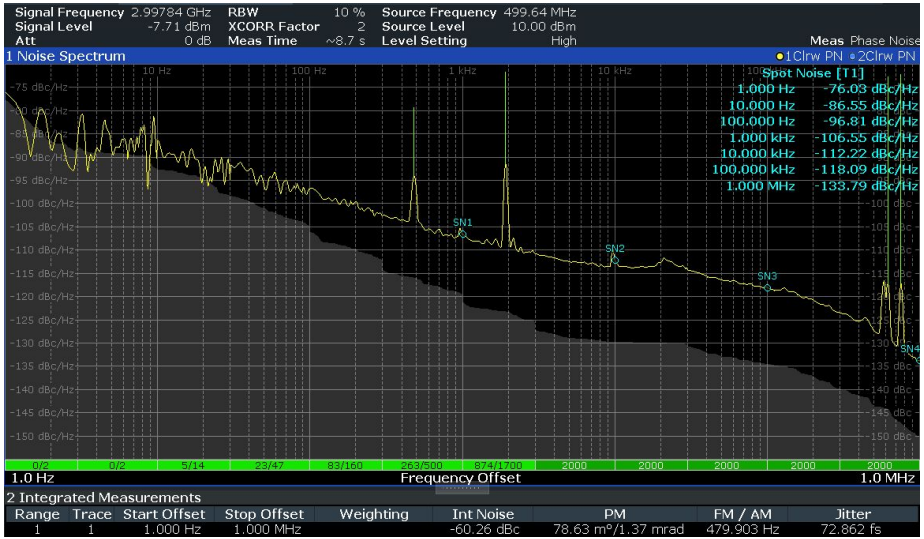
Steps towards 80 fs jitter [1Hz, 1MHz]
Fc=500MHz, Fs=4 Gsps



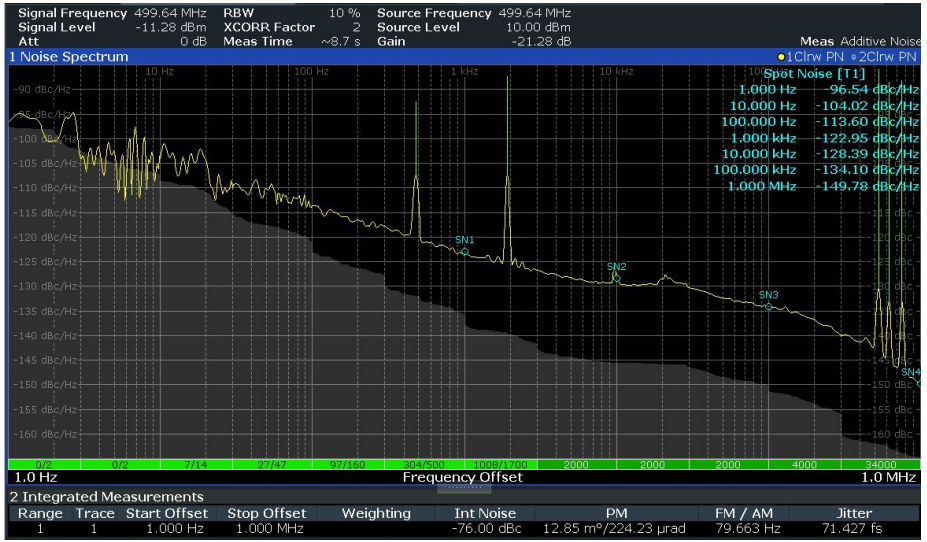
RF output Phase noise results



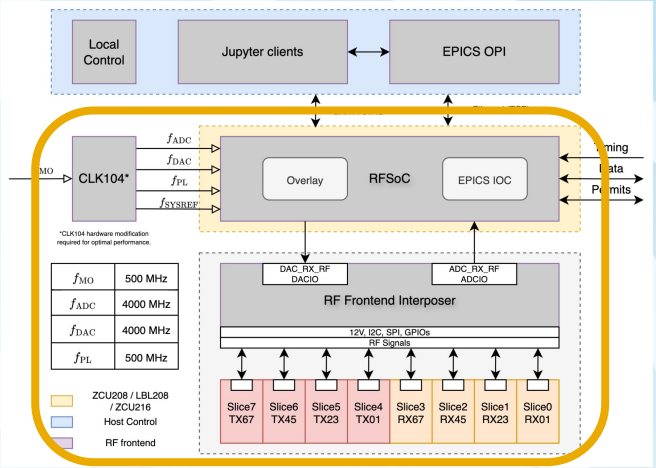
Absolute RMS Jitter: <80 fs [1Hz, 1MHz]
Fc=3000MHz, Fs=4Gsps



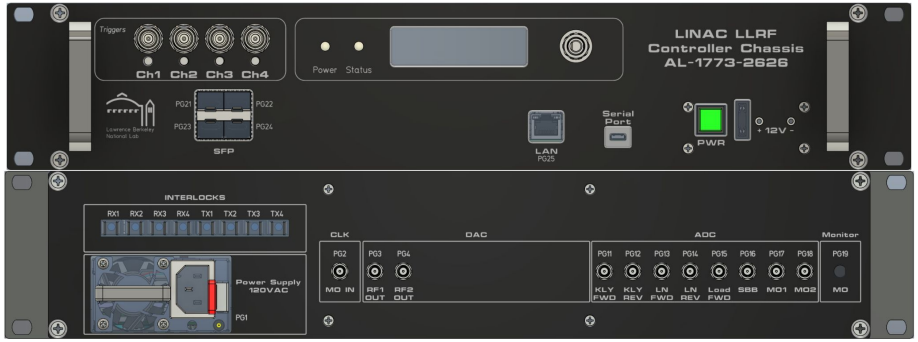
Additive RMS Jitter: <80 fs [1Hz, 1MHz]
Fc=500MHz, Fs=4Gsps

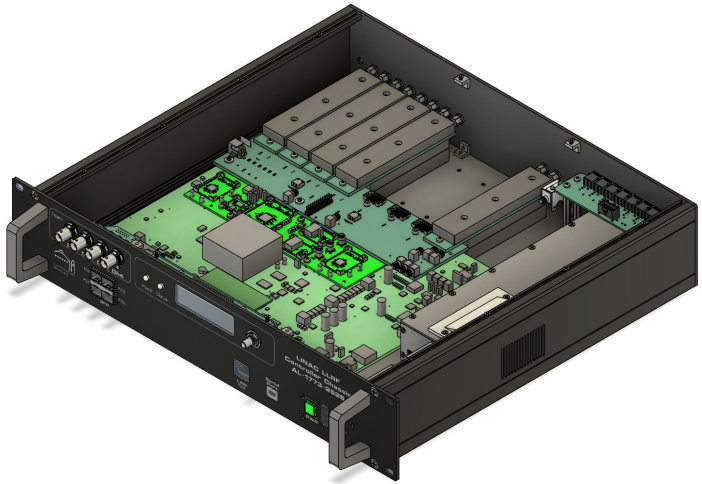


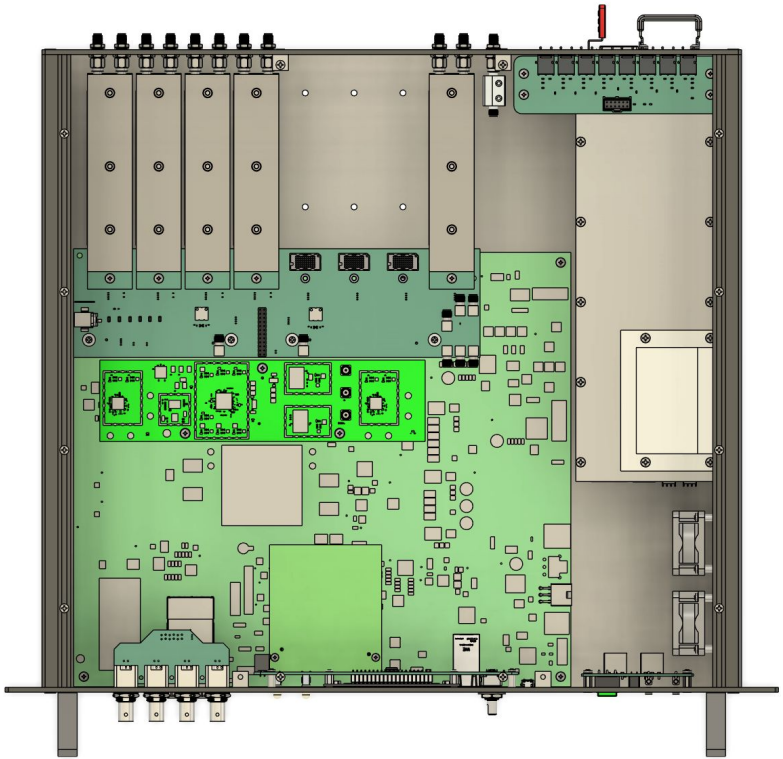
Enclosure design



Digital LLRF Controller Chassis

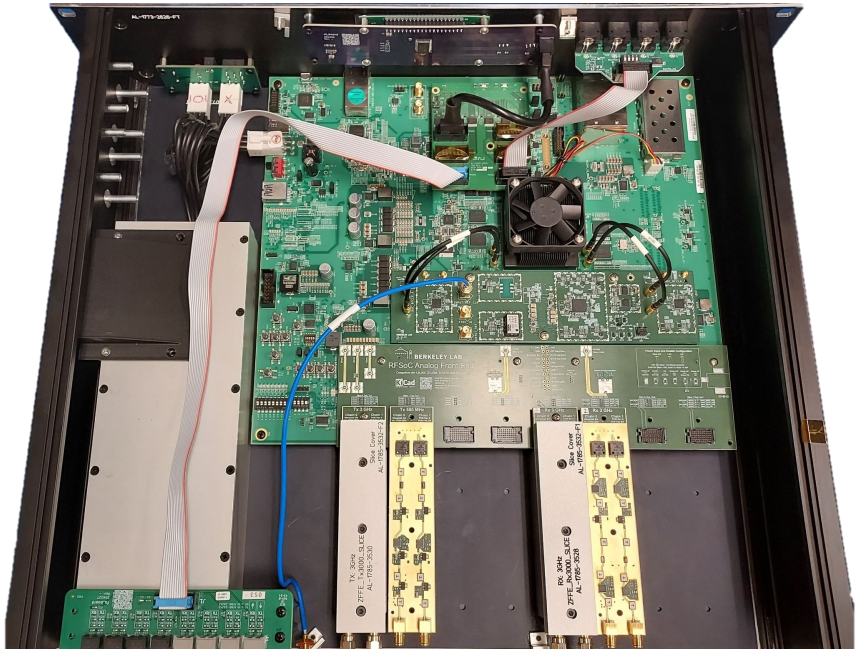


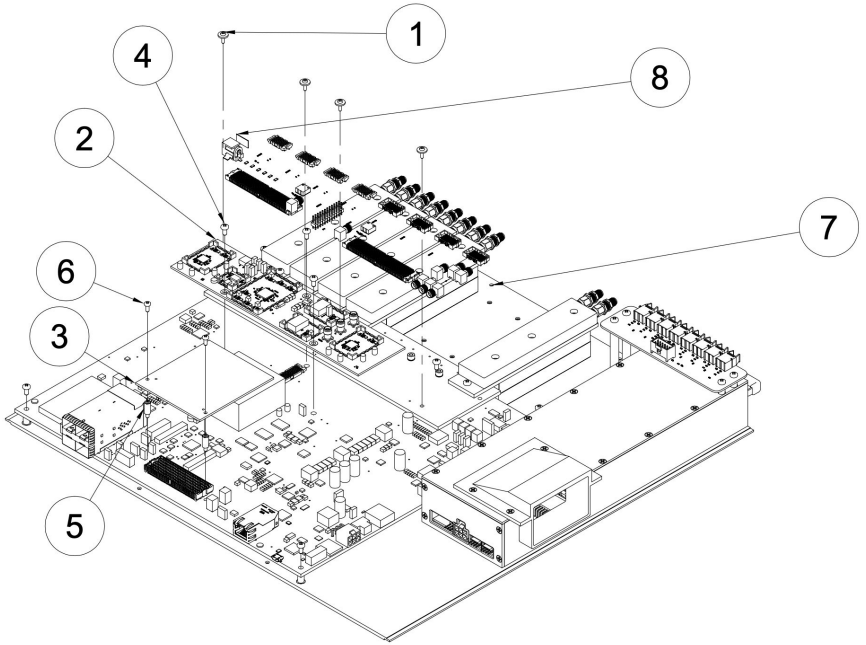


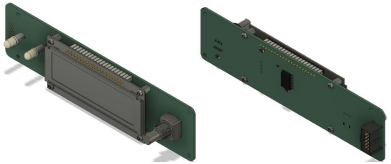


Modular enclosure assembly:

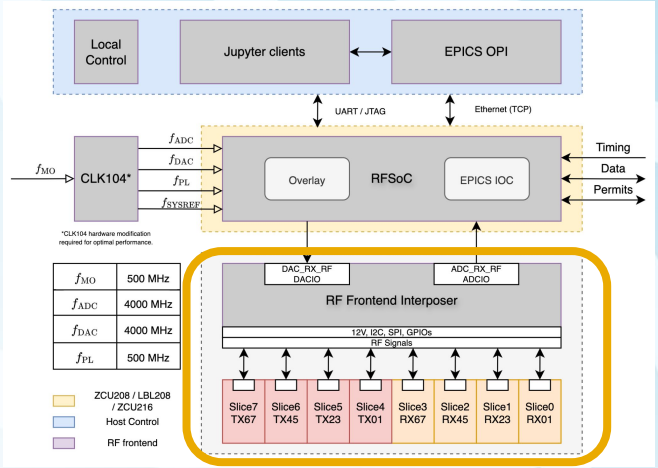
2U chassis: PMBus power supply / thermal management / Peripherals / Local display



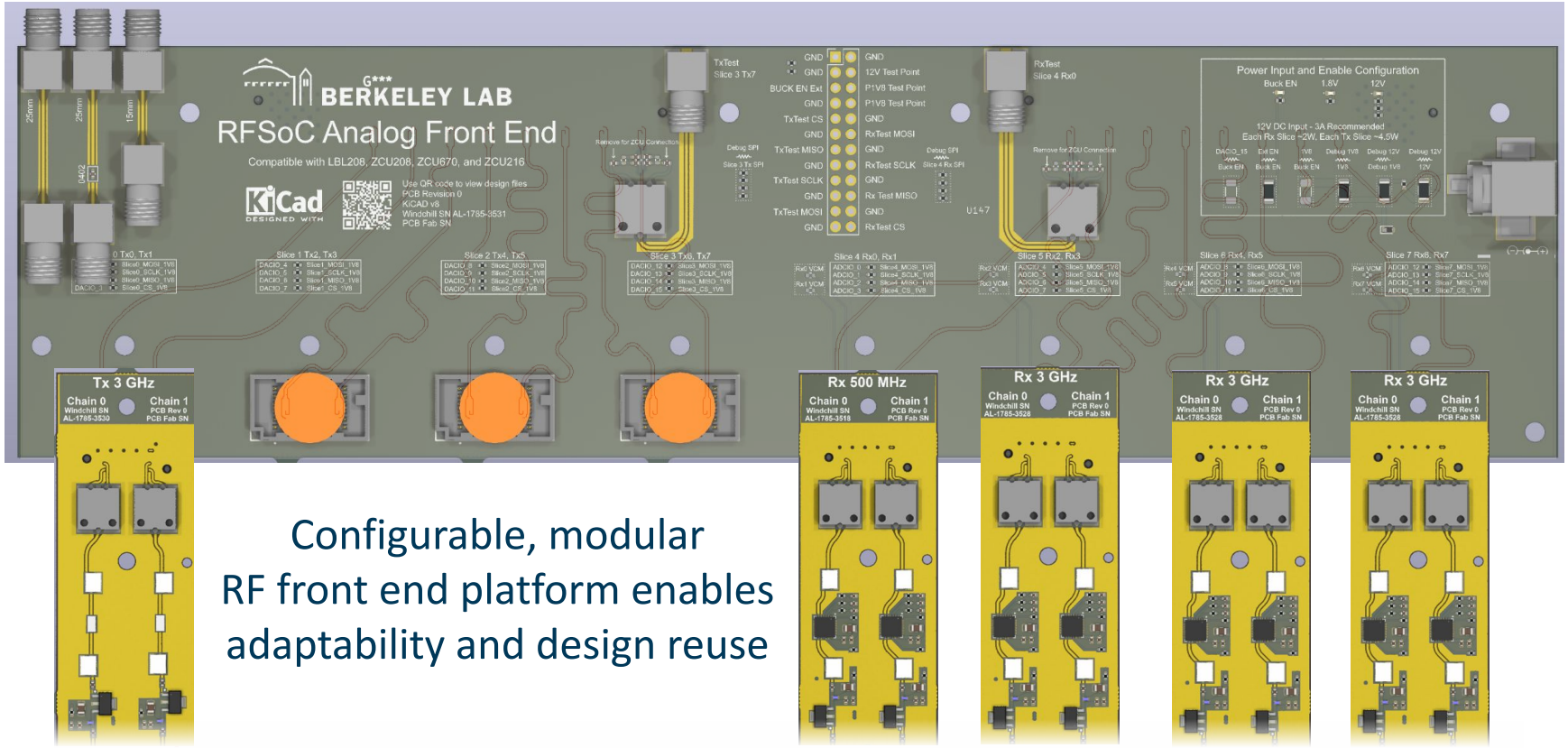




RF Front-end design

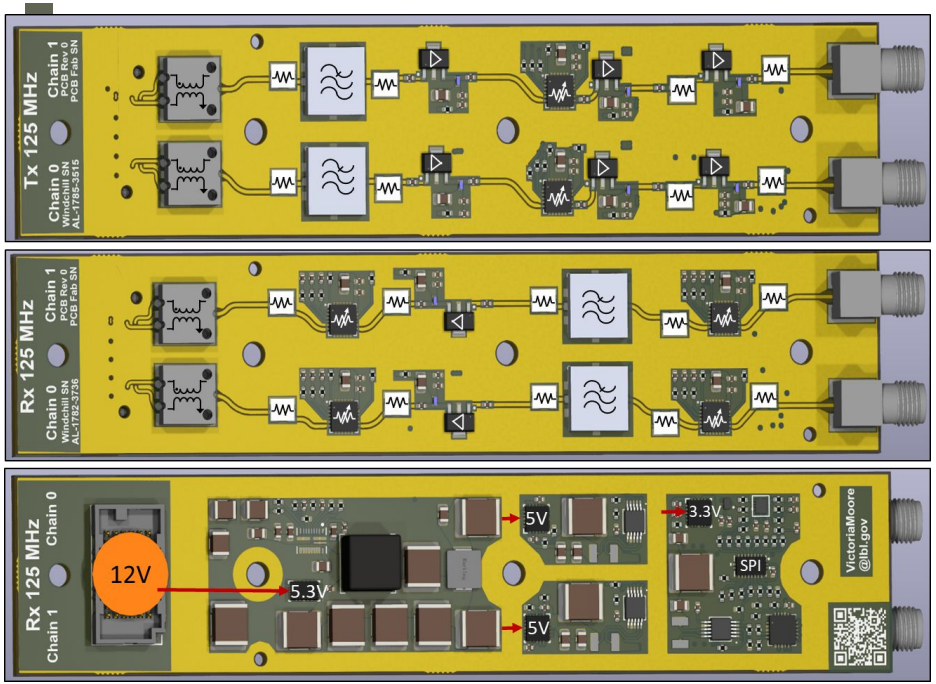


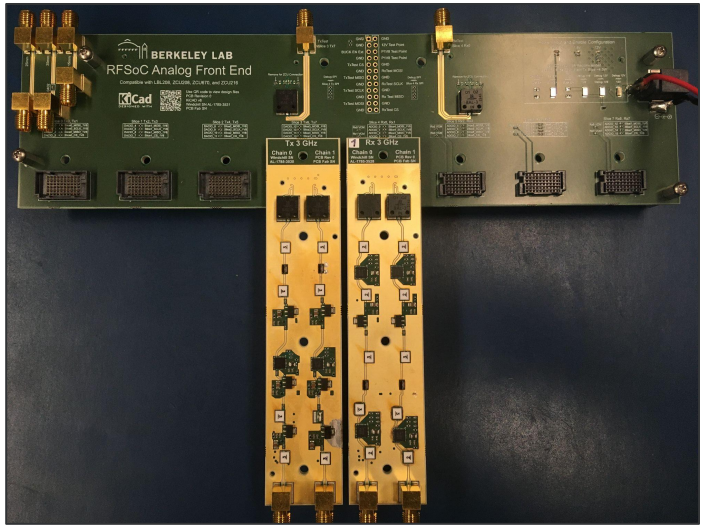
RFSoC Flexible Front End



Configurable, modular
RF front end platform enables
adaptability and design reuse

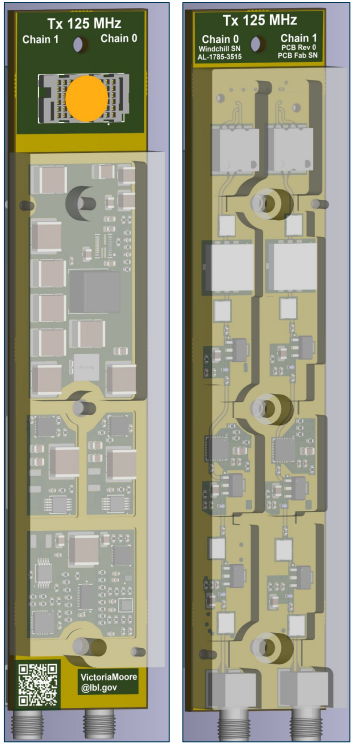
Configurable RF Slices: TX/RX dual channel modules

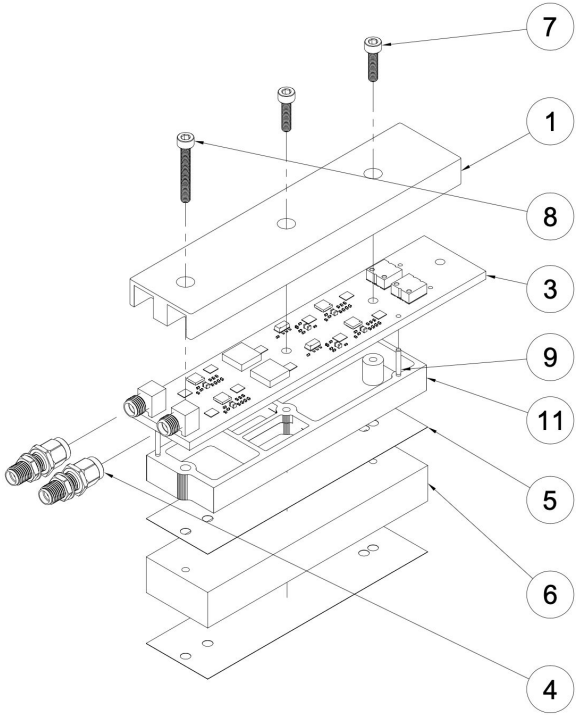


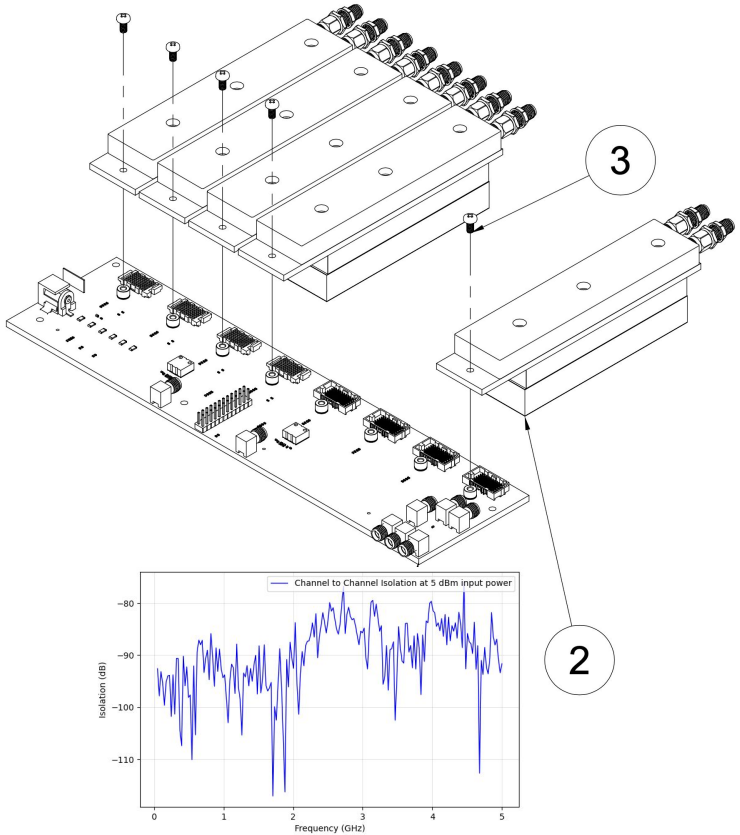


RF Slices: High Isolation Enclosures

Ensures > 80 dB Isolation (3GHz)

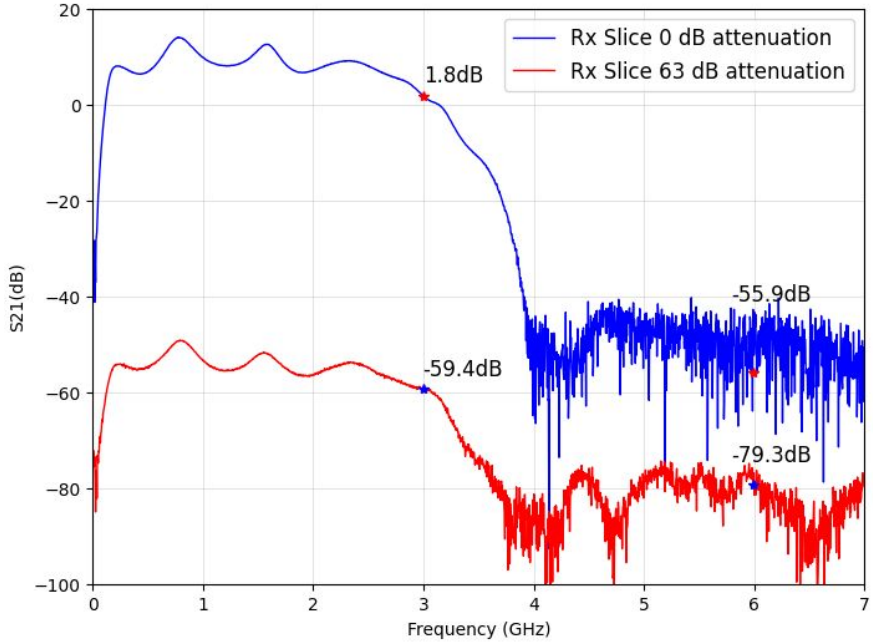


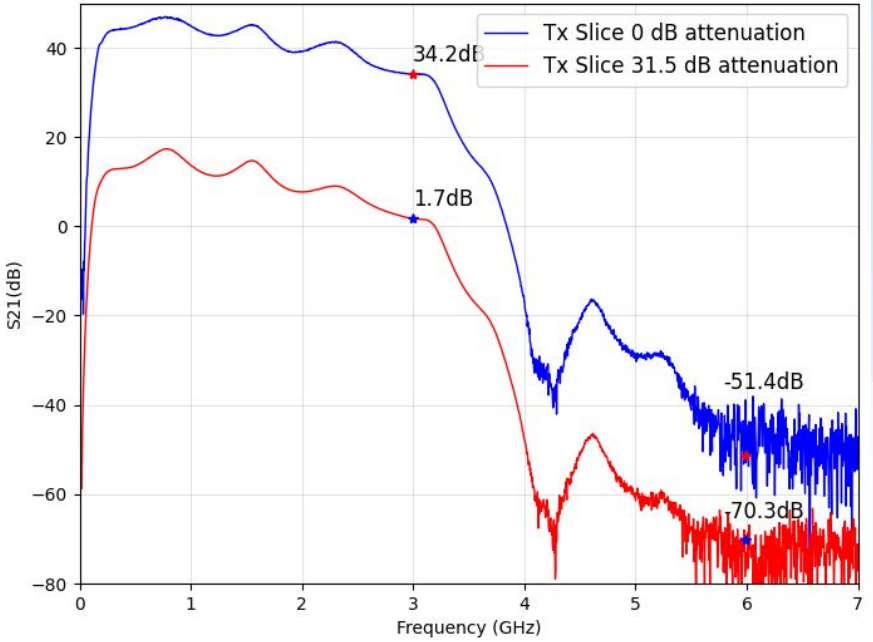




RF Slices Gain

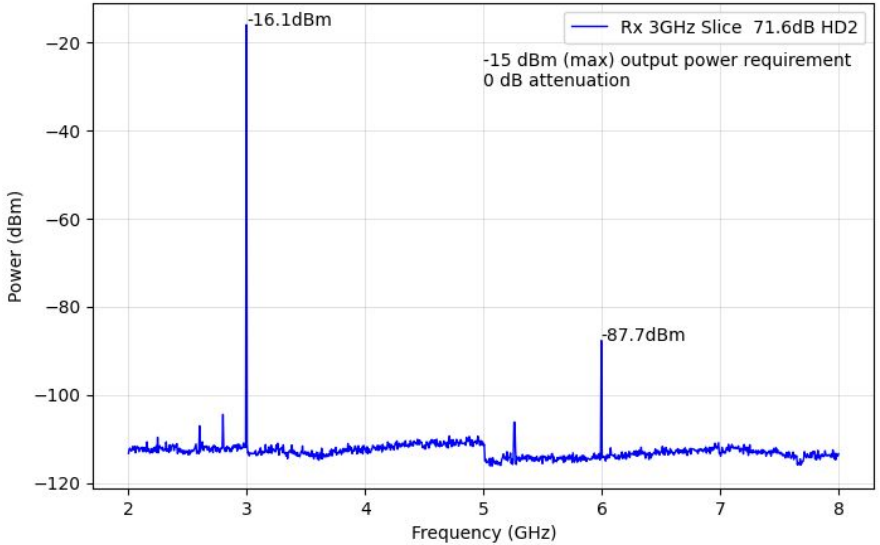
- Rx: 63 dB dynamic range, 0.5 dB resolution, second harmonic 20-50 dBc
- Tx: 31.5 dB dynamic range, 0.5 dB resolution, second harmonic 70 dBc

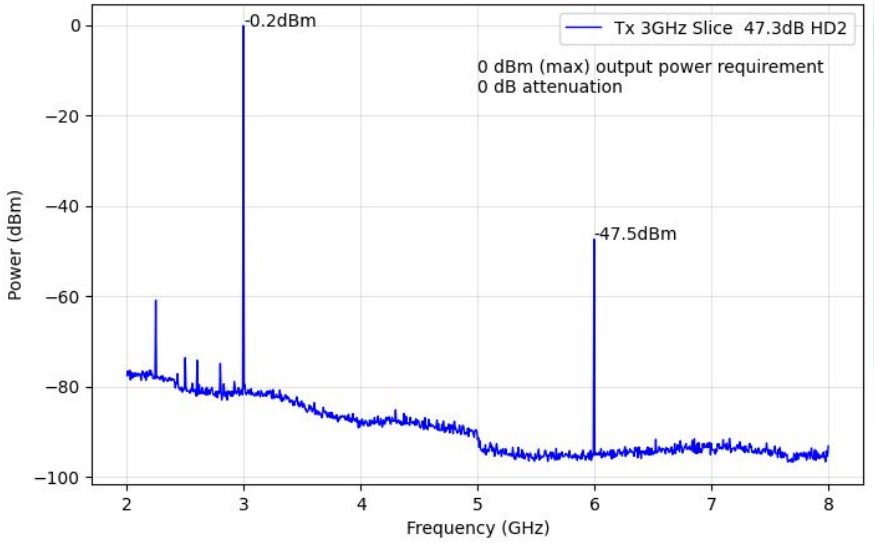




RF Slices Linearity

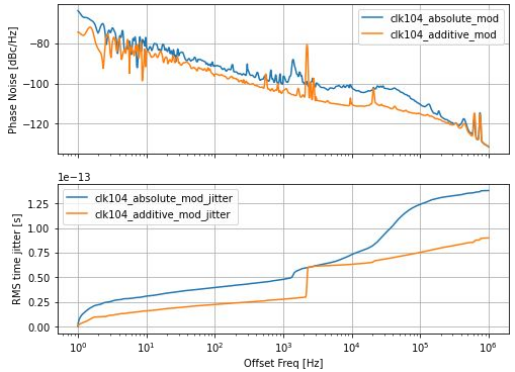
- Rx HD2 is > 20 dB better than RFSoC ADC input and will not affect linearity
- Tx HD2 is 7 dB better than Modulator pre-amplifier, < .01 dB of HD2 degradation

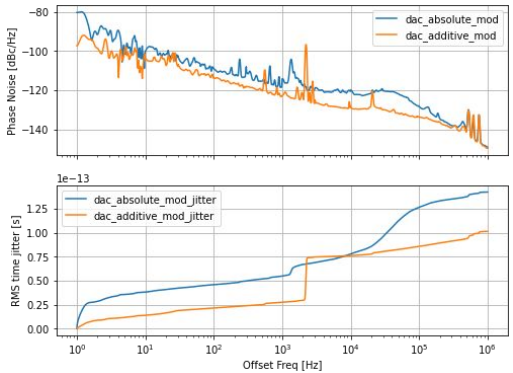




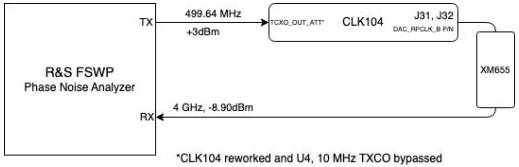
Total RF Output Phase Noise Breakdown

CLK104: **90fs**

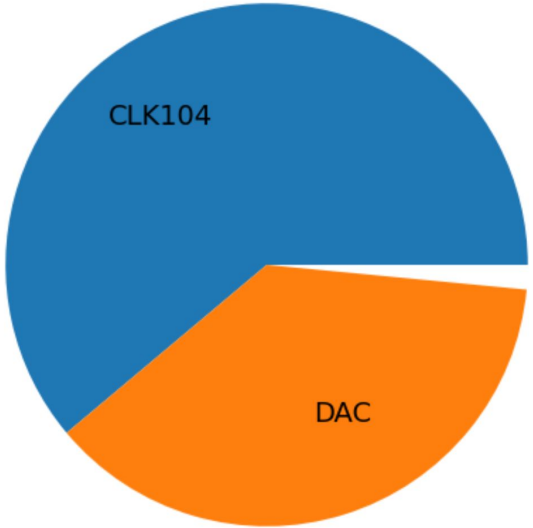


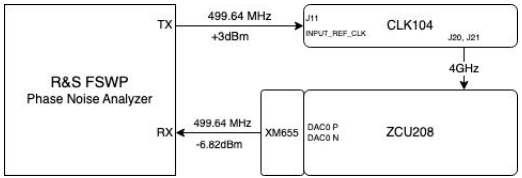


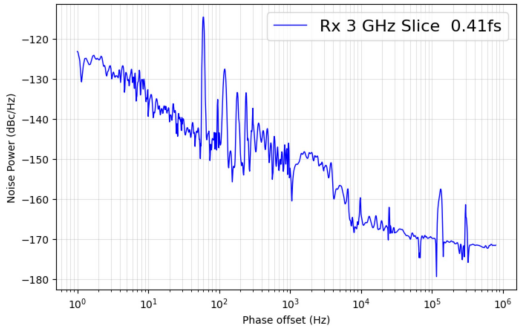
CLK104 + RFSoC: **101 fs**



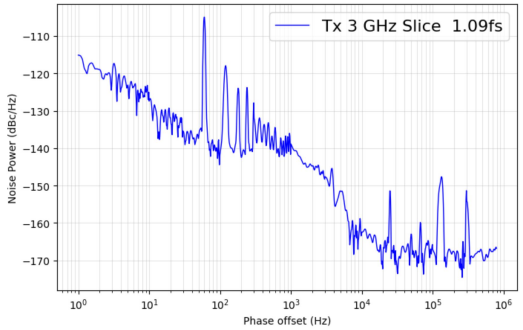
*CLK104 reworked and U4, 10 MHz TXCO bypassed





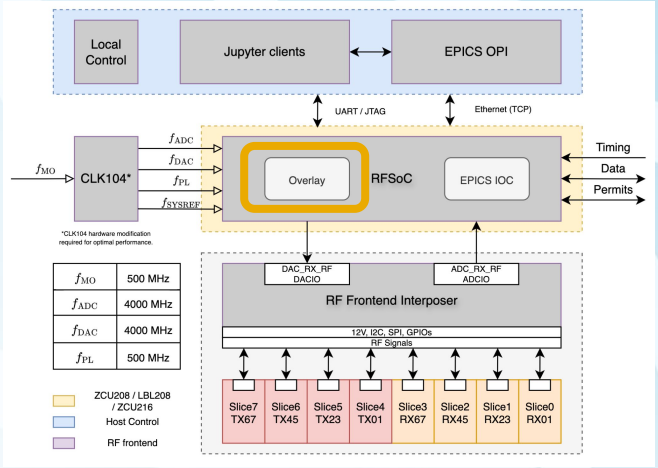


Rx Slice 0.5%
Tx Slice 1.0%

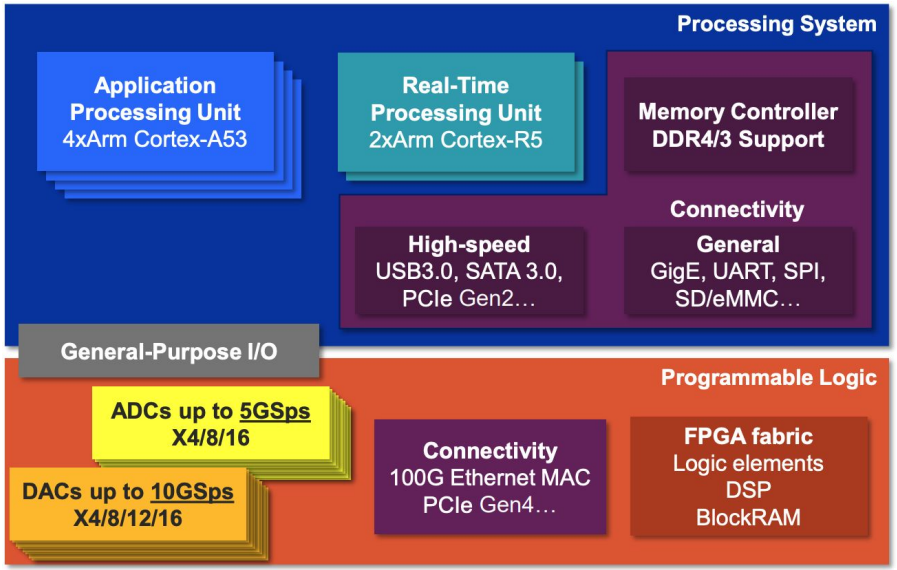


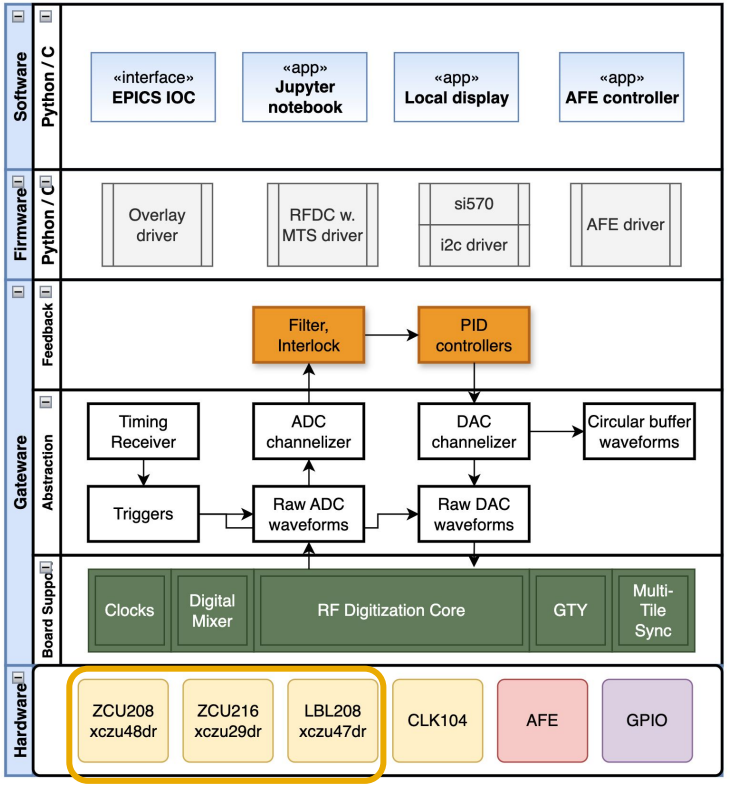
BERKELEY LAB | ALS-U

Firmware design



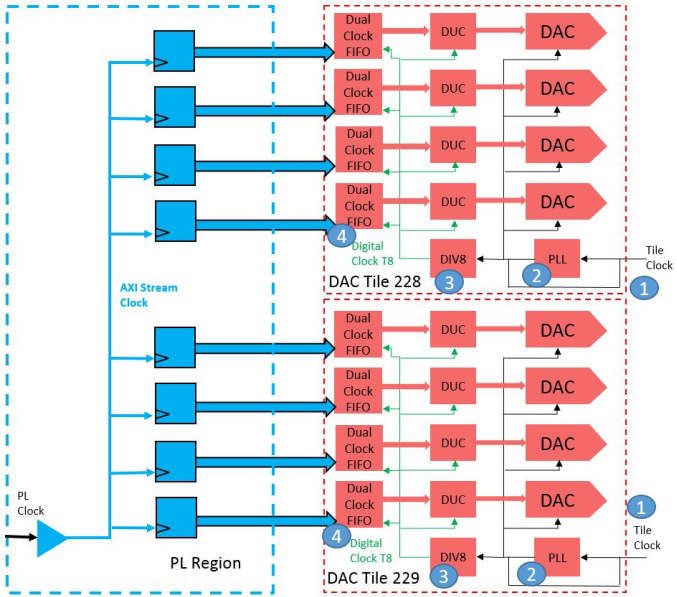
RFSoC based LLRF architecture: A unified design





Multi-Tile-Synchronization (MTS):

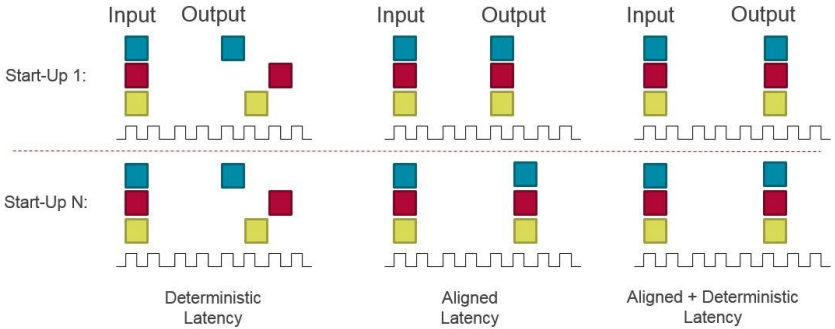
Sample-to-Sample aligned + deterministic latency

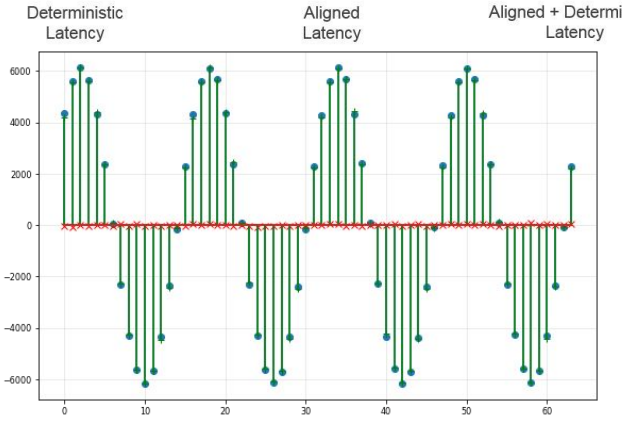


MTS

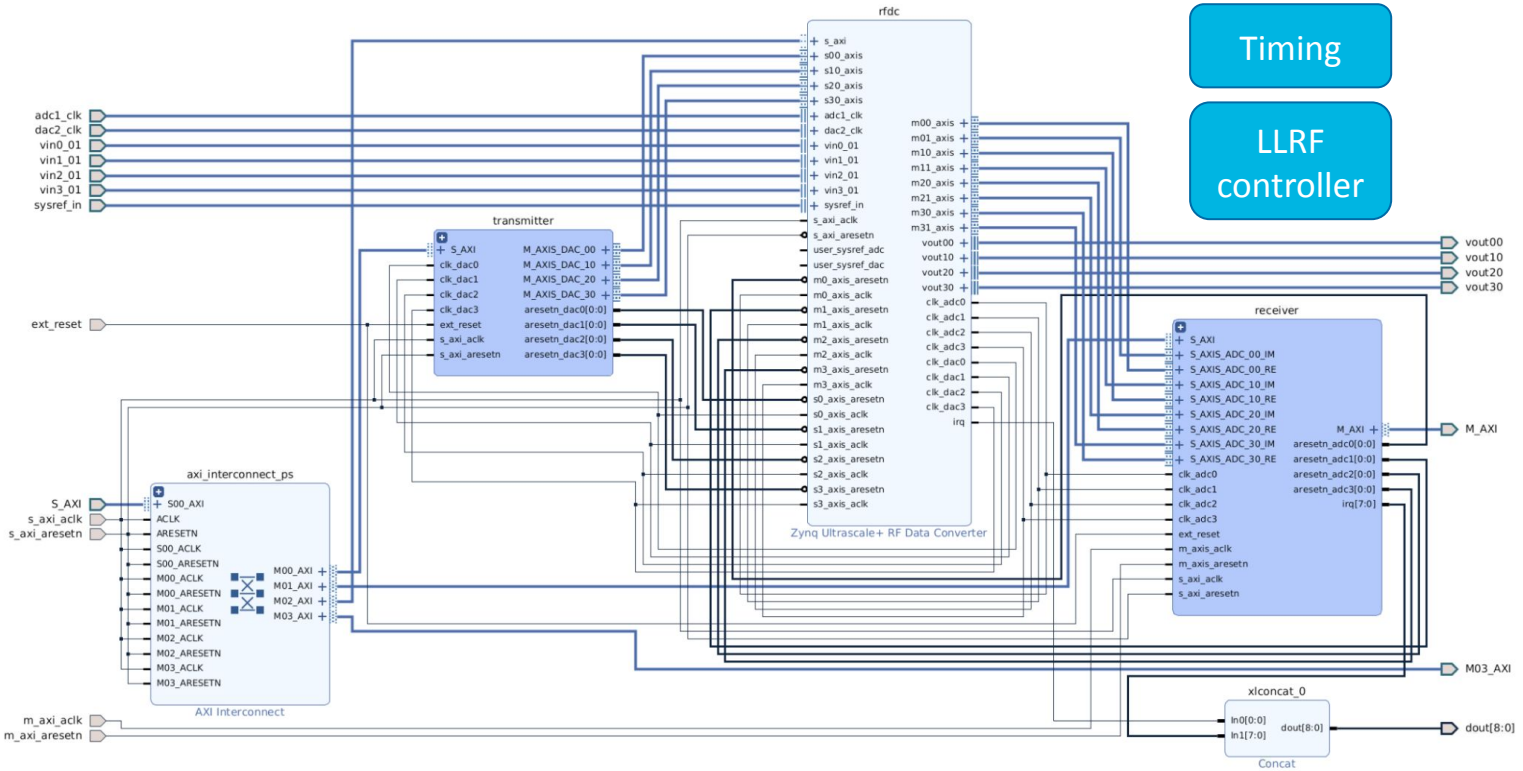
Total latency across all channels is same

Same *relative* latency across all channels





Xilinx PNYQ framework + cocotb validated RTL



Standard Baseband LLRF DSP

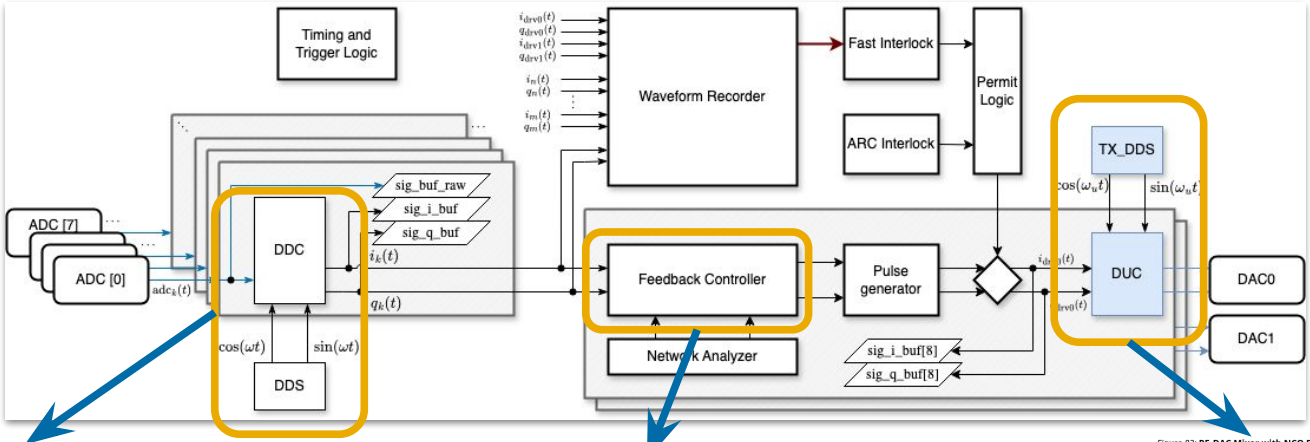
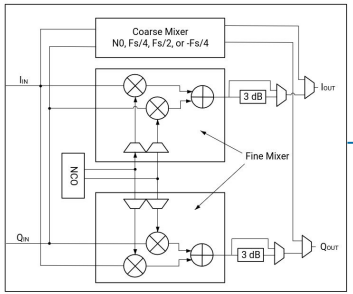
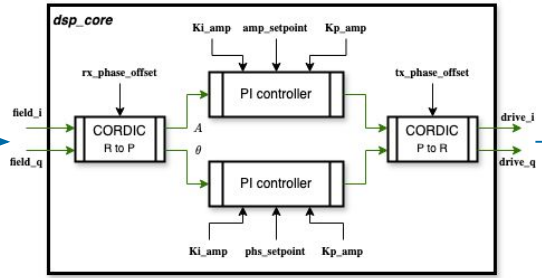


Figure 25: **RF-ADC Mixer with NCO DSP Block**





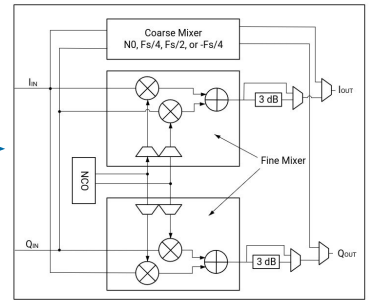
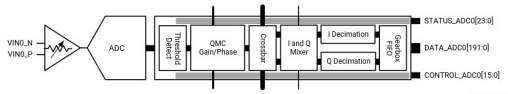
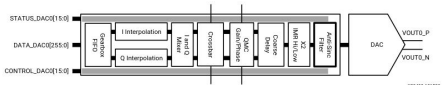


Figure 83: **RF-DAC Mixer with NCO DSP Block**

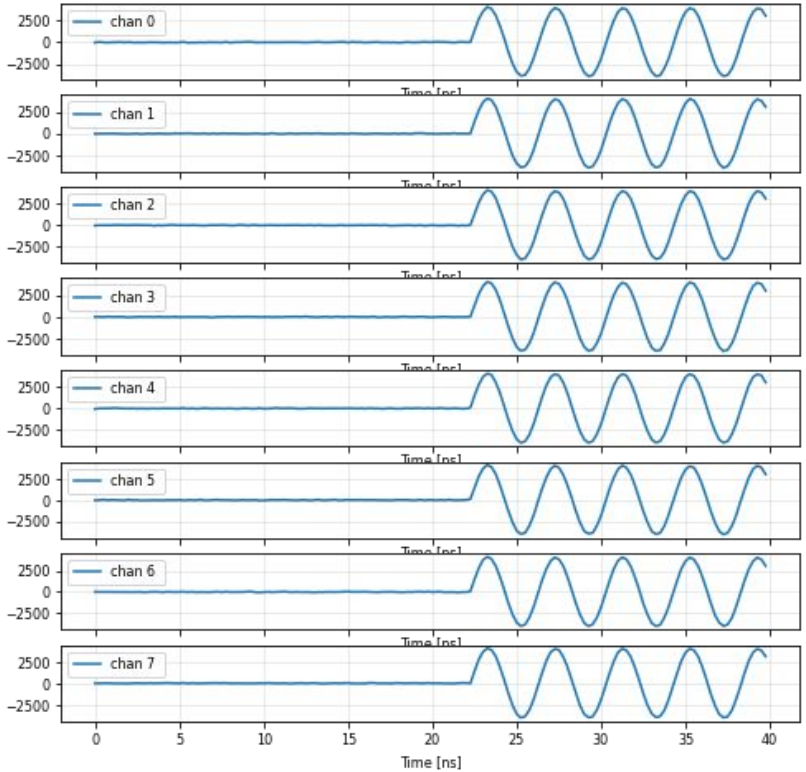
AWG



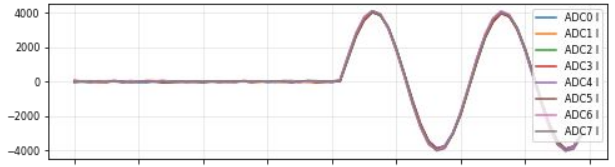


Loopback shows MTS with Latency < 300ns

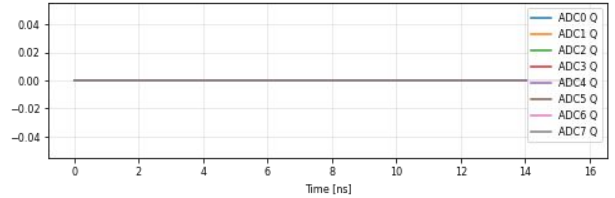
Align NCO phase as well as samples, deterministically!



I



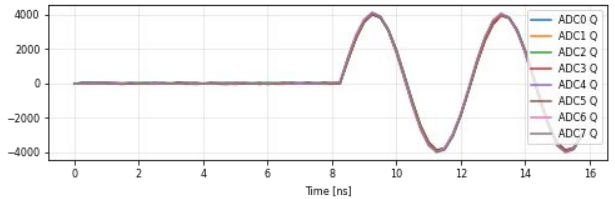
Q



LO phase 0 deg

I

Q

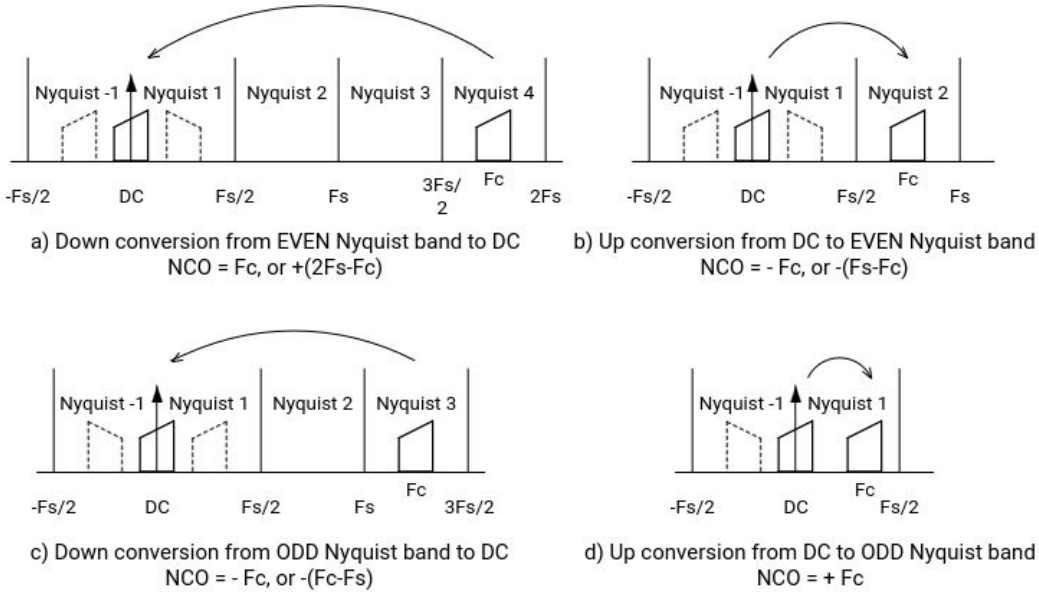


LO phase 90 deg

RF loopback latency: 287.25 ns

Digital mixer NCO settings

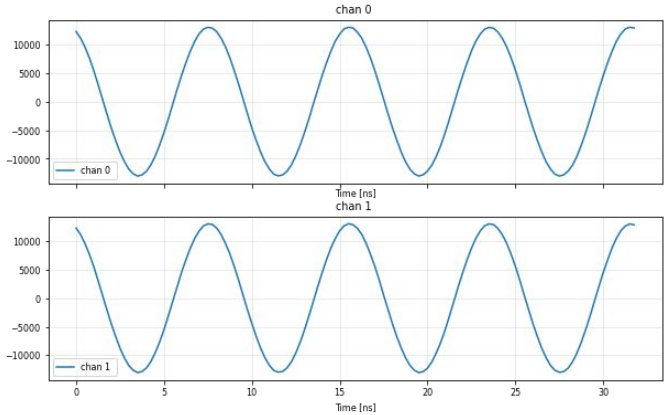
Figure 27: **NCO Setting Examples**

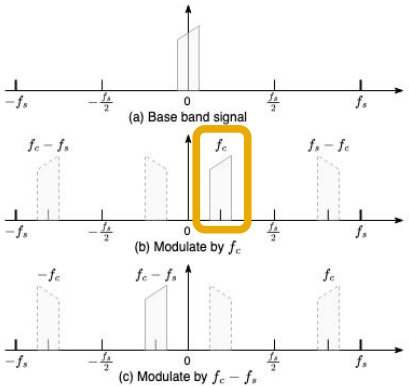


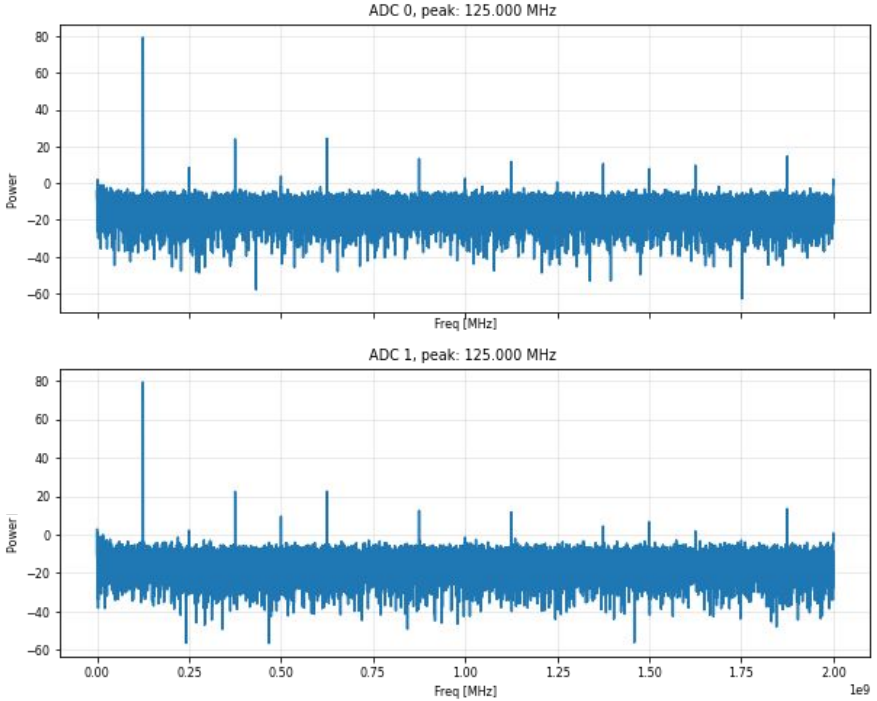
- Fine Mixer
- SHB LLRF: Nyquist 1
  - Fs = 4GHz
  - Fc = 125MHz;
  - Fc = 500MHz
  - NCO = -Fc
- Linac LLRF: Nyquist 2
  - Fs = 4GHz
  - Fc = 3000 MHz
  - NCO = Fc

Loopback test with RFDC Mixers: 125 MHz RF

First Nyquist Zone sampling at 4 Gsps

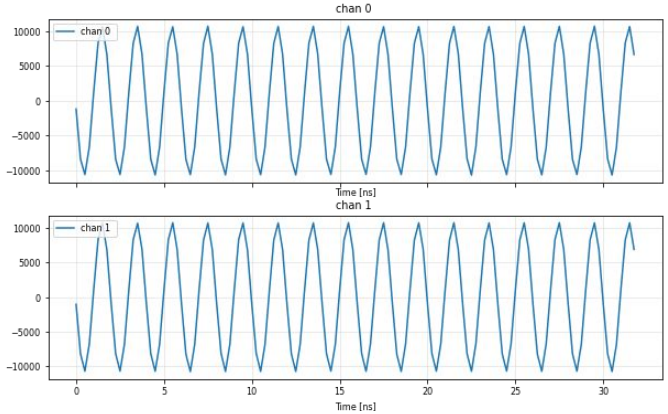


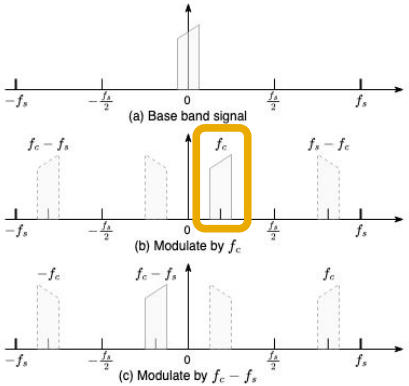


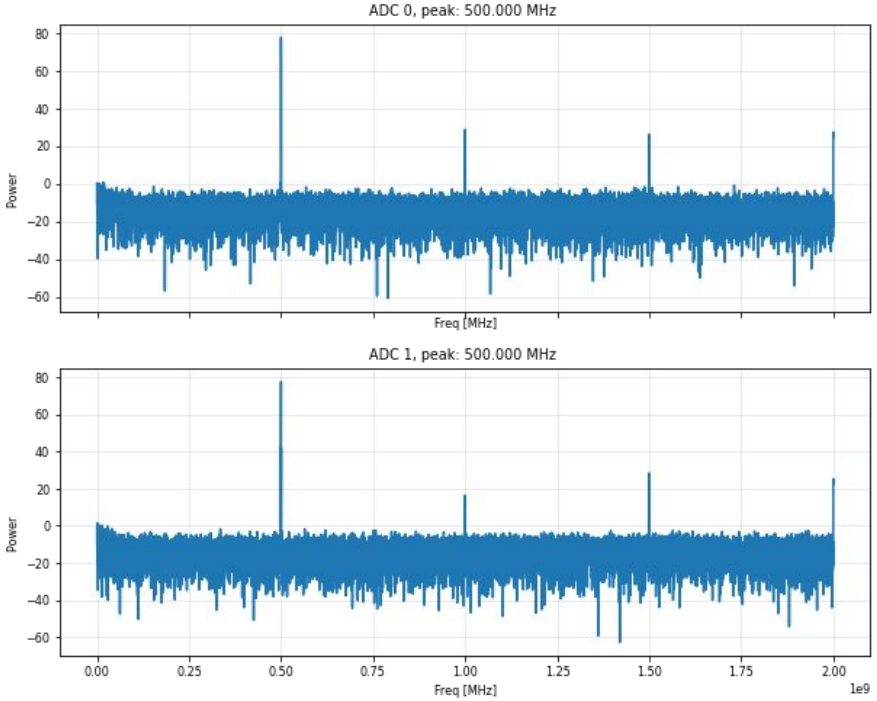


Loopback test with RFDC Mixers: 500 MHz RF

First Nyquist Zone sampling at 4 Gsps

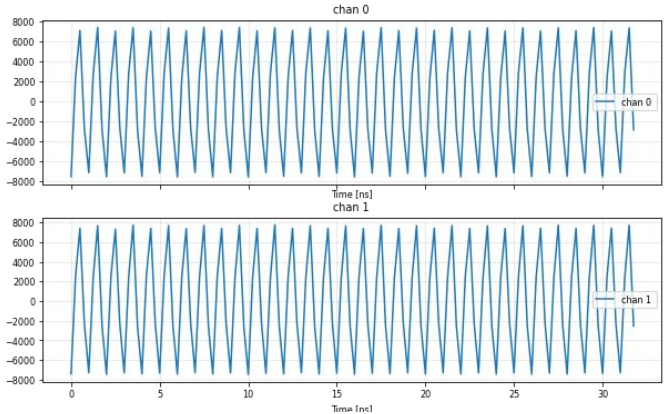


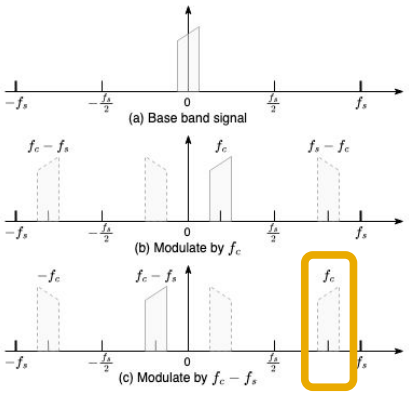


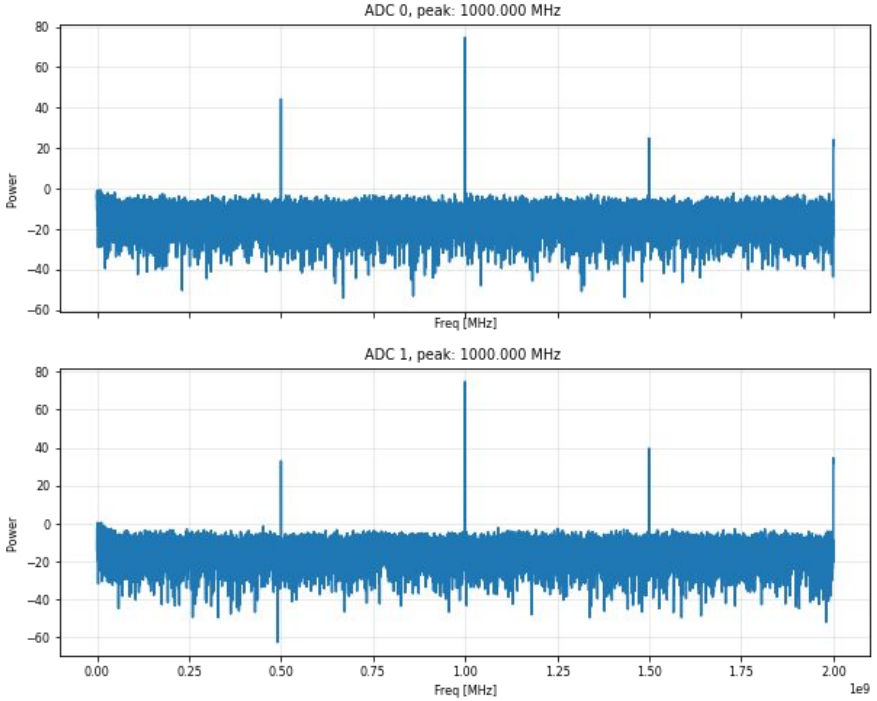


Loopback test with RFDC Mixers: 3000 MHz RF

Second Nyquist Zone sampling at 4 Gsps

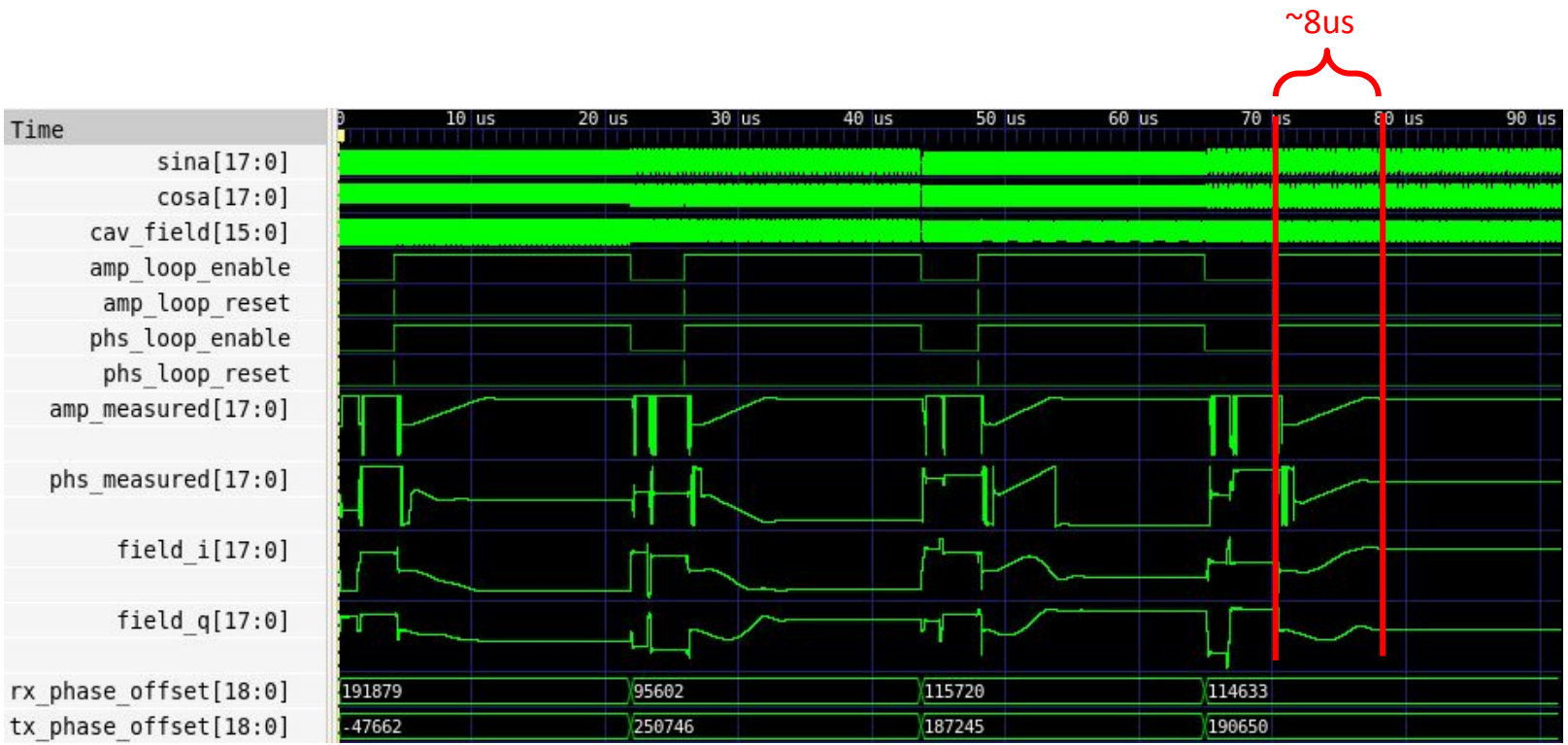






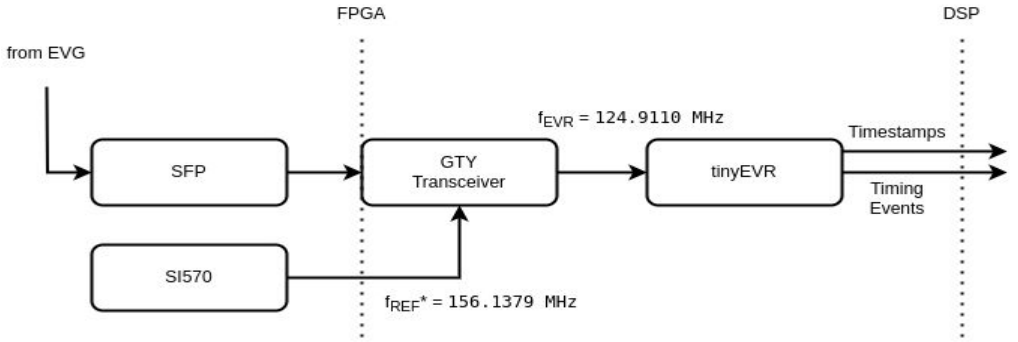
ADC spectrum shows 1GHz peak, which is folded back from Nyquist 2 zone.

In-pulse feedback is feasible thanks to low latency

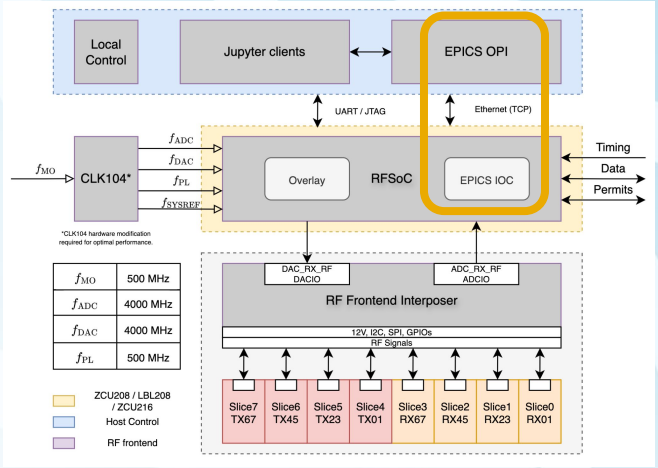


Timing support - EVR Integration

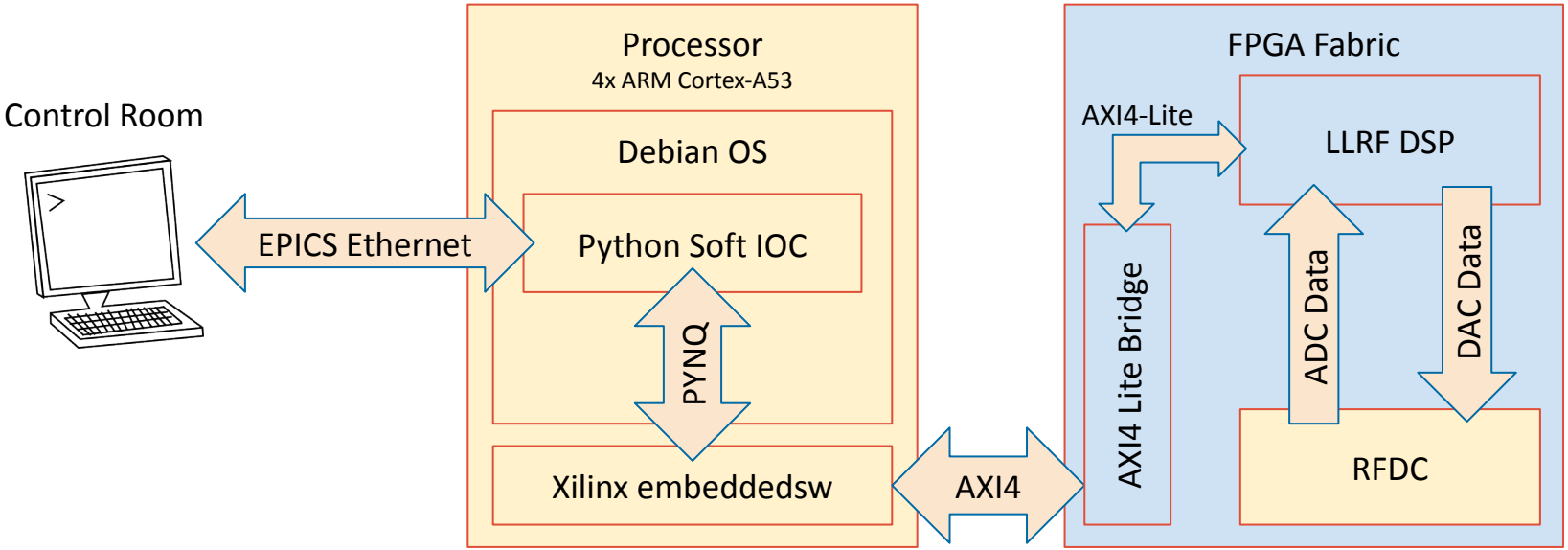
- GTY deserializes the data and recovers 124.911 MHz clock (f_{EVR}). It also recovers and realigns automatically following an unplug/replug cycle and power cycle.
- ALS Event Receiver (*tinyEVR*) code is used to decode the global timestamp and timing events
- Link lock status, alignment status, timestamp validity and debug information made available for register read/EPICS
- Enables power-cycle **deterministic** latency for events



Software design

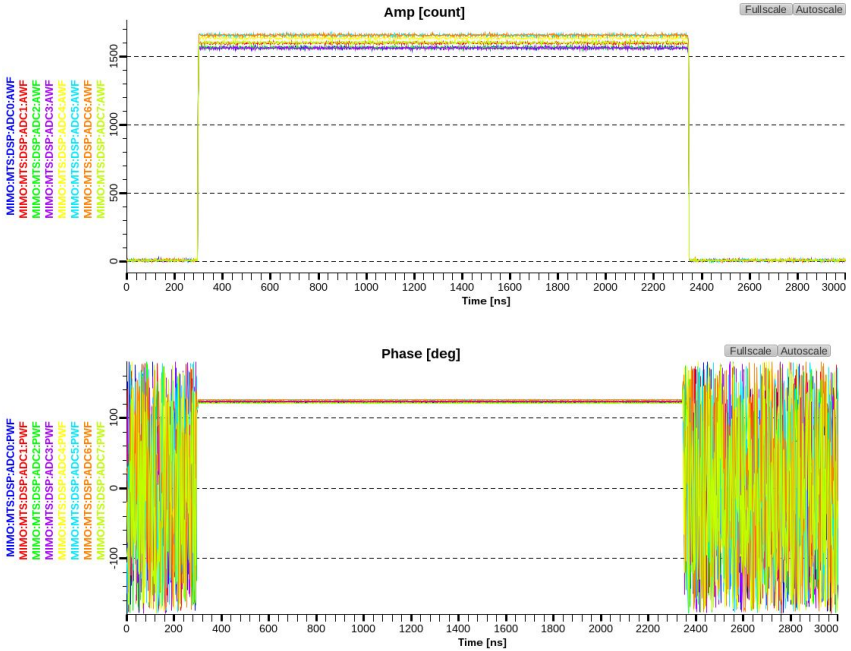


Soft EPICS IOC and Peripheral Control on Chip

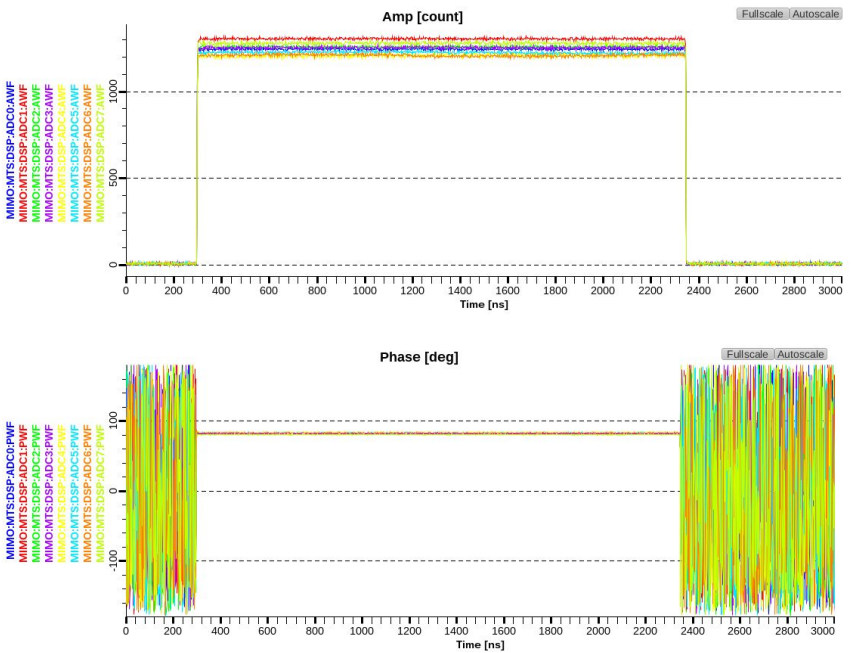


Waveforms in EPICS Phoebus screen

3000MHz RF Loopback

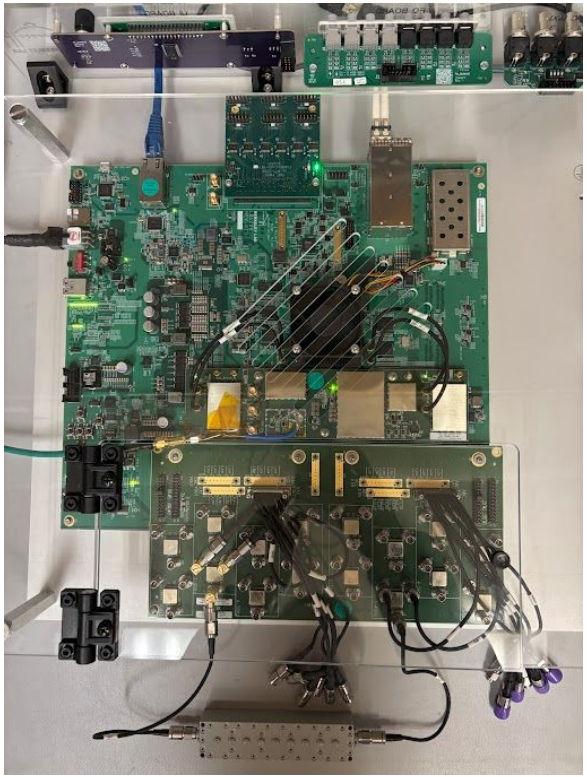


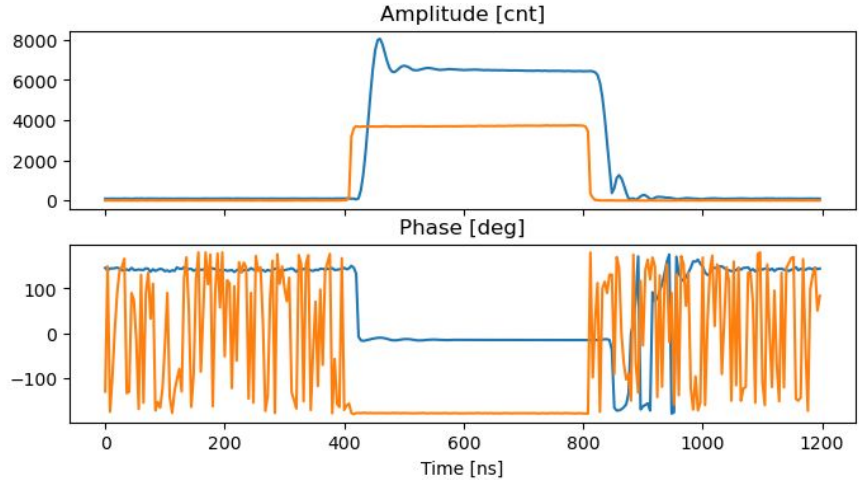
500MHz RF Loopback

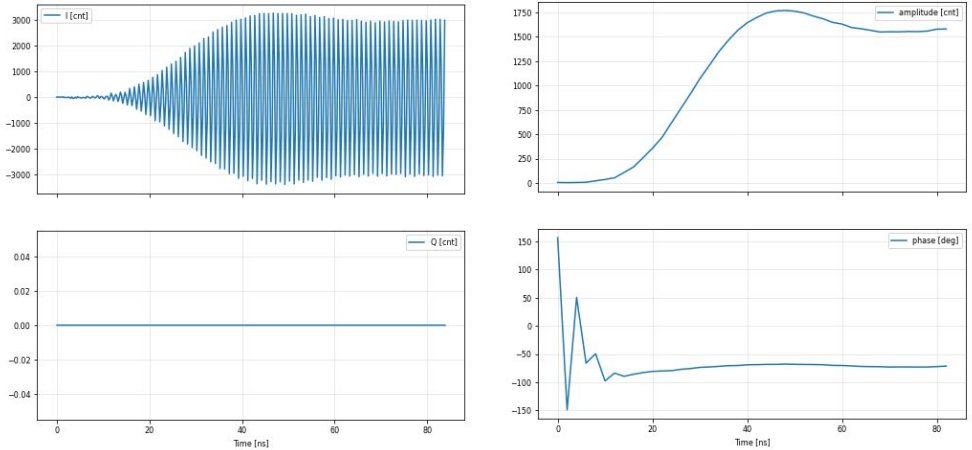


3GHz Linac bench test

Loopback; add a bandpass filter







RAW ADC I/Q

Baseband Amp/Phs

Thank you!