DIGITAL LOW-LEVEL RF SYSTEM FOR THE LINAC ELECTRONICS MODERNIZATION PLAN AT LCLS

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ABSTRACT

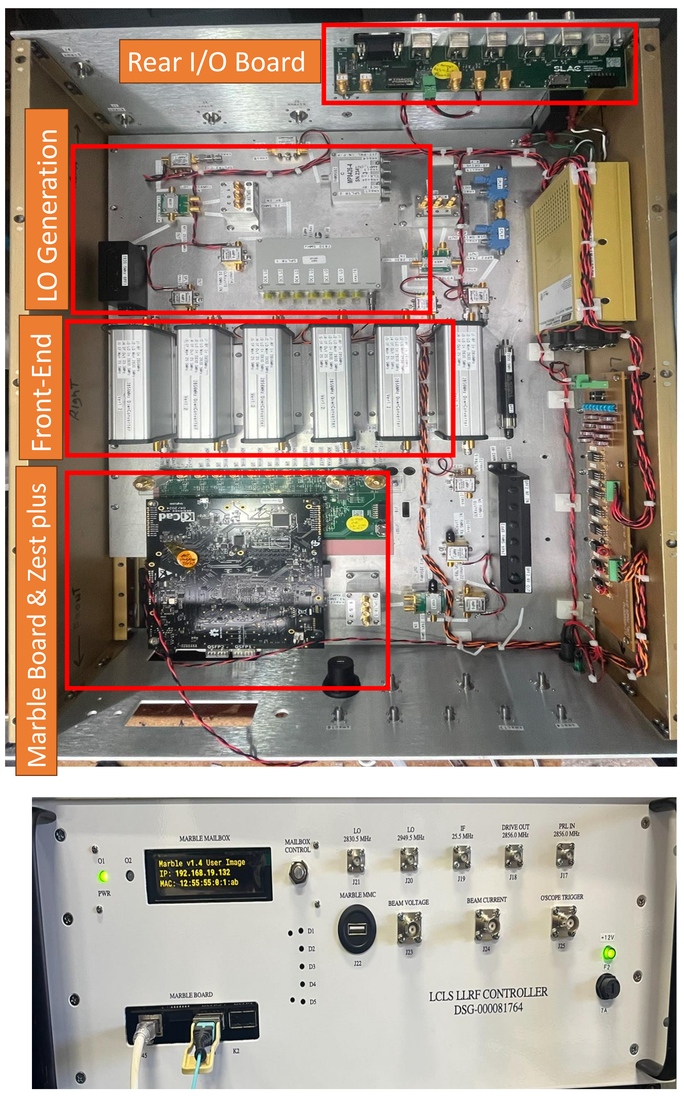
The LEMP controller replaces aging CAMAC-based LLRF controls in SLAC's NC linac. The new system is built on the open-source **Marble** FPGA carrier and **Zest+** digitizer with a custom RF front-end. A prototype has been deployed and tested at station 26-3, demonstrating RF generation/control, interlocks, and waveform capture. This poster summarizes the design, bring-up results, and planned upgrades.

HARDWARE DESIGN

Built on **open-source LBNL hardware**, the system reuses the **Marble** carrier and **Zest+** digitizer platform already deployed for **LCLS-II**, simplifying maintenance and keeping common hardware across the copper and superconducting linacs. Custom SLAC modifications for pulsed operation:

- Two ADC inputs converted to **DC-coupled** mode (LT1994) to digitize **klystron beam voltage** and **beam current**.
- New **RF front-end** down-converts 2.856 GHz to **25.5 MHz IF** for digitization.
- Compact **Rear I/O board** buffers and attenuates klystron signals and manages handshaking/interlocks with the **modulator PLC**.

All functions are integrated in a **single 4U, 26-inch, water-cooled chassis**. Only an **RF reference** is distributed along the gallery; local **SSB modulator** generates coherent up- and down-conversion LOs inside the chassis.



FREQUENCY CONFIGURATION

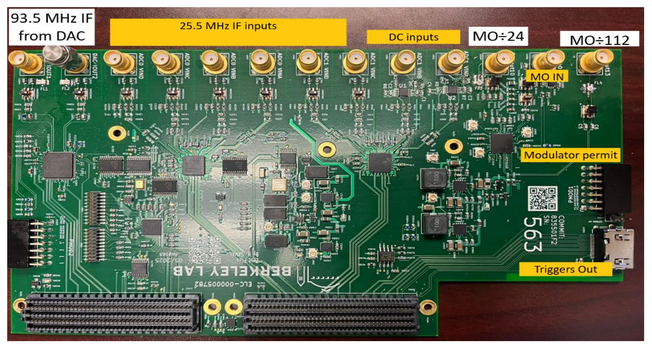
All system clocks and local oscillators are phase-locked to the 2856 MHz master oscillator (MO). Independent up- and down-conversion LOs are synthesized using single-sideband (SSB) modulation derived from the MO, see the Table 1&2

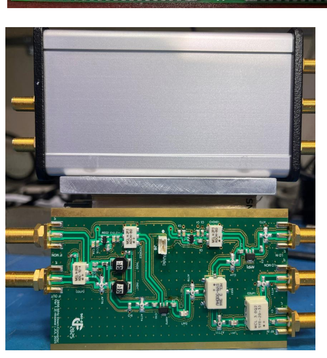
	Generation	Relationship	f [MHz]
RF			2856
MO			2856
ADC_{clk}	LMK01801	$\frac{1}{24}$ MO	119
DAC_{clk}	LMK01801	$\frac{1}{12}$ MO	238
LO_{dwn}	MO - $\frac{MO}{112}$		2830.5
LO_{up}	LO_{dwn} + ADC_{clk}		2949.5
IF_{dwn}	RF - LO_{dwn}	$\frac{3}{14}ADC_{clk}$	25.5
IF_{up}	Zest+	$\frac{11}{28}DAC_{clk}$	93.5

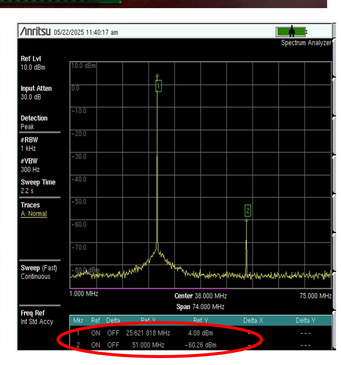
Parameter	Down LO	Up LO	Unit
LO frequency	2830.5	2949.5	MHz
Spurious-free dynamic range (SFDR)	> 90	> 81	dB
MO carrier feedthrough	≤ −80	≤ −80	dBc
RMS additive phase jitter [100Hz, 1MHz]	32	37	fs

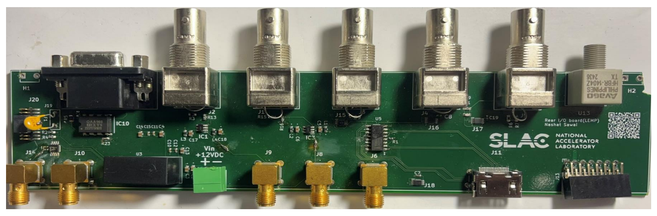
ANALOG RF FRONT-END

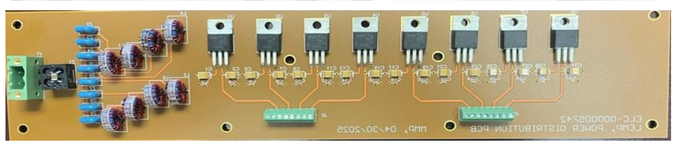
The analog front-end down-converts the 2.856 GHz RF to a 25.5 MHz IF. Each module optimized for low noise, high linearity. Single-channel modules reduce crosstalk and improving isolation. The 2×IF spur at 51 MHz is 64 dB below the fundamental.
Two digitizer inputs were modified from transformer-coupled to DC-coupled using single-to-differential amplifiers to monitor beam voltage and beam current.





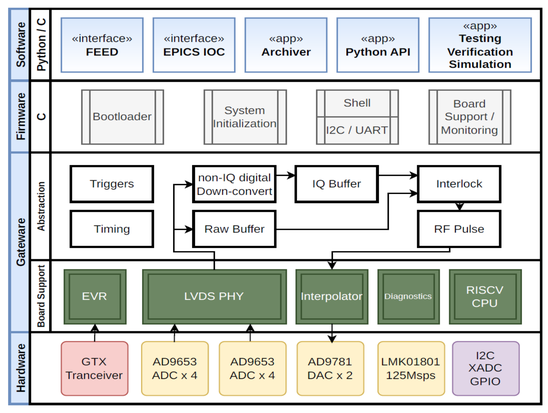






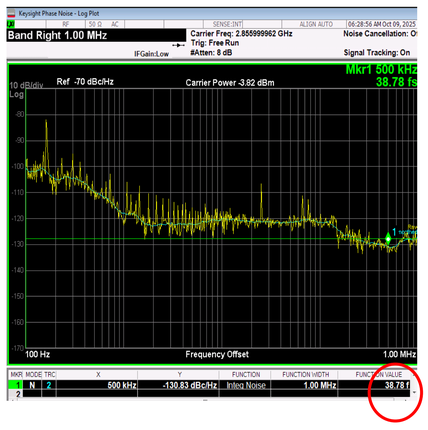
FIRMWARE DESIGN

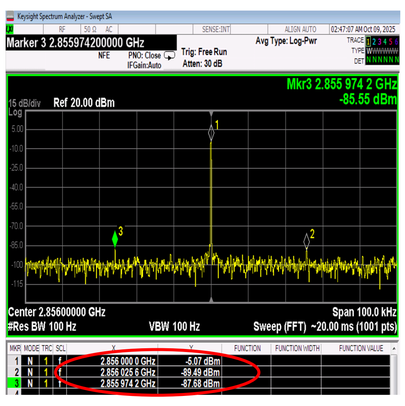
Firmware is based on the **open-source Bedrock** library (LBNL) and adapted at **SLAC** for pulsed LEMP operation. A lightweight **RISC-V (PicoRV32)** core handles initialization, configuration, and monitoring. Firmware controls **ADC/DAC timing**, **trigger generation**, and **interlocks**. Bedrock's **Packet Badger** provides high-speed access to **EPICS** for waveform capture and diagnostics. Closed-loop simulation uses a calibrated cavity model

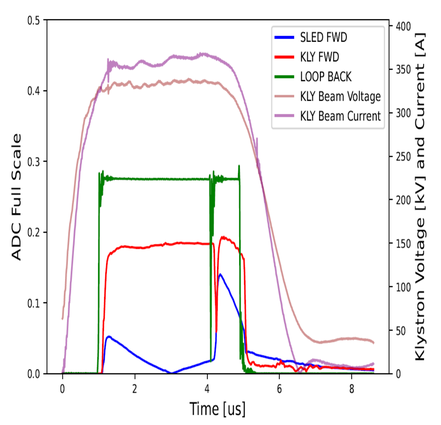


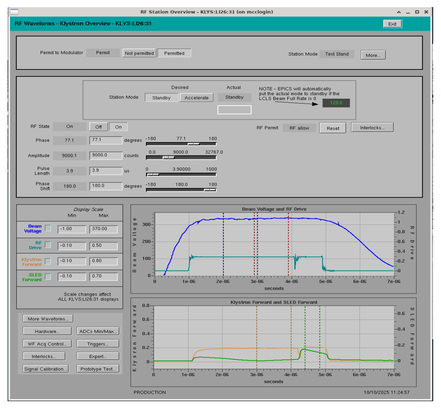
PROTOTYPE TEST

The prototype LLRF chassis was tested at station 26-3 in klystron gallery .The 2.856 GHz RF drive achieved ≈ 82 dB SFDR. Integrated phase noise over 100 Hz–1 MHz corresponds to ≈ 38 fs RMS jitter. Screenshots show the jitter integration measured spectra, waveform acquisition during 5 µs RF pulse and EPICS control interface.









SUMMARY

A prototype chassis for the LEMP project has been designed, tested and deployed at station 26-3,based on previous LLRF projects. After successful verification of the main functionality, the station was aligned to the accelerate event and the phase setpoint was optimized. The system has been in operation for hundreds of hours, mostly in standby mode. Future work includes finalizing the design and building more chassis to upgrade more stations.