# Obvious and Non–Obvious Aspects of Digital Self–Excited–Loops for SRF Cavity Control

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## Abstract

In 1978, Delayen showed how Self-Excited Loops (SEL) can be used to great advantage for controlling narrow-band SRF cavities. Its key capability is establishing closed-loop amplitude control early in the setup process, stabilizing Lorentz forces to allow cavity tuning and phase loop setup in a stable environment.

As people around the world implement this basic idea with modern FPGA DSP technology, multiple variations and operational scenarios creep in that have both obvious and non-obvious ramifications for latency, feedback stability, and resiliency.

This paper will review the key properties of a Delayen-style SEL when set up for open-loop, amplitude stabilized, and phase-stabilized modes. Then the original analog circuit will be compared and contrasted with the known variations of digital CORDIC-based implementations.

## Cavity State Space Equation

$$\frac{dV}{dt} = aV + bK + cI$$

Would be LTI if $a$, $b$, and $c$ were constant.
But in SRF, the imaginary part of $a$ (detuning) varies with time!
Not LTI! For frozen $V$ and ignoring $cI$, the correct drive is

$$K = K_0\left(1 + j\frac{\Im(a)}{\Re(a)}\right)$$

Controller's main job is to stabilize cavity phase by adjusting reactive drive.

## Delayen (1978)

PHASE AND AMPLITUDE STABILIZATION
OF SUPERCONDUCTING RESONATORS

Thesis by
Jean Roger Delayen

In Partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy

California Institute of Technology
Pasadena, California
1978
(Submitted August 8, 1977)

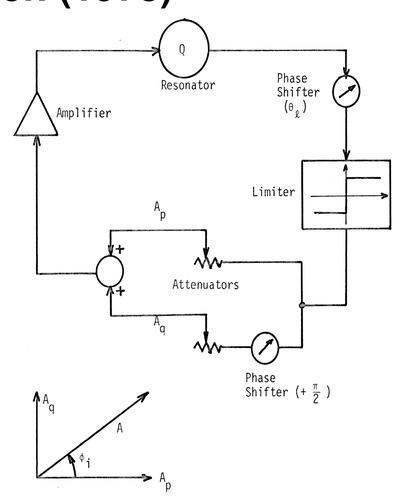
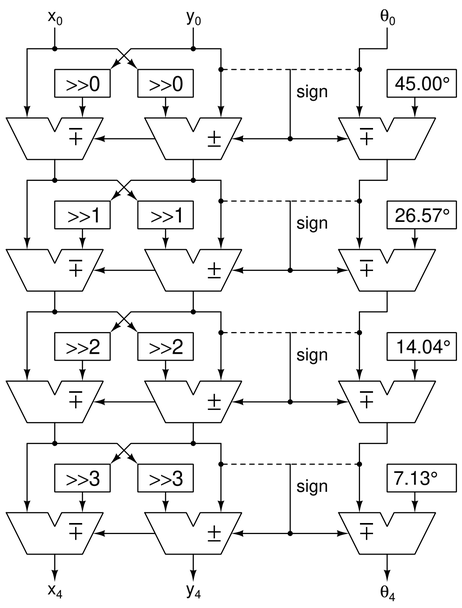
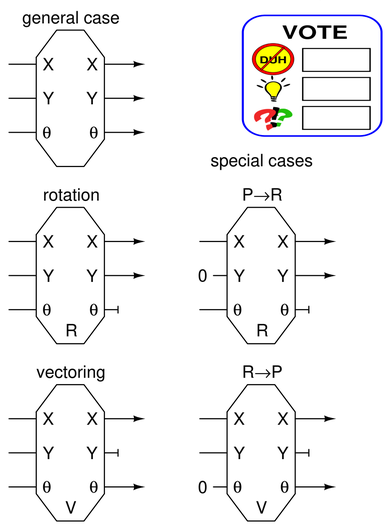



Fig. 2.3 Principle of stabilization of a self-excited loop by addition of a signal in quadrature

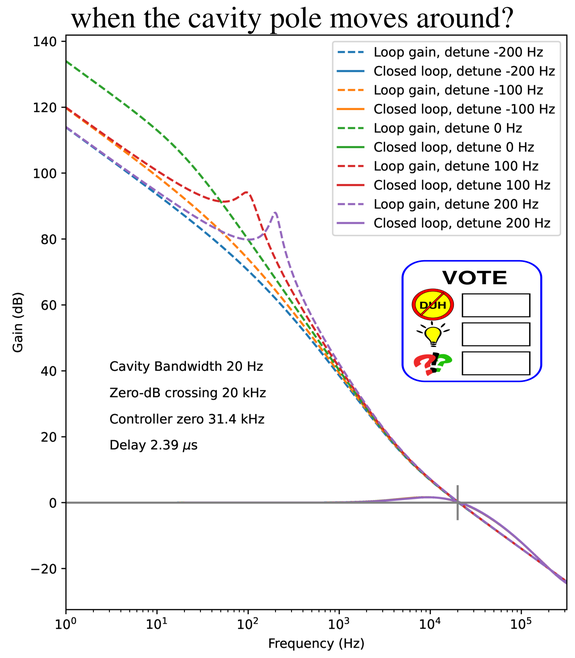
## CORDIC (1959)



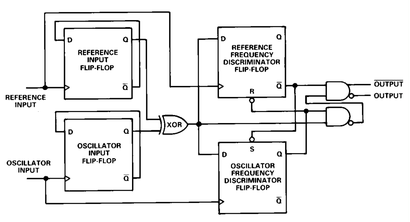




CORDIC blocks in an FPGA are "big". Designs from JLab and LBNL, at least, time–slice multiple CORDIC tasks onto a single CORDIC hardware instance.

## What happens to the control loop stability when the cavity pole moves around?




## Phase Chatter (1996)




Phase detectors in a PLL are notorious for chattering when loop is unlocked.

LBNL takes inspiration from AD9901 and adds Stateful Phase Resolver at input of PI loop.

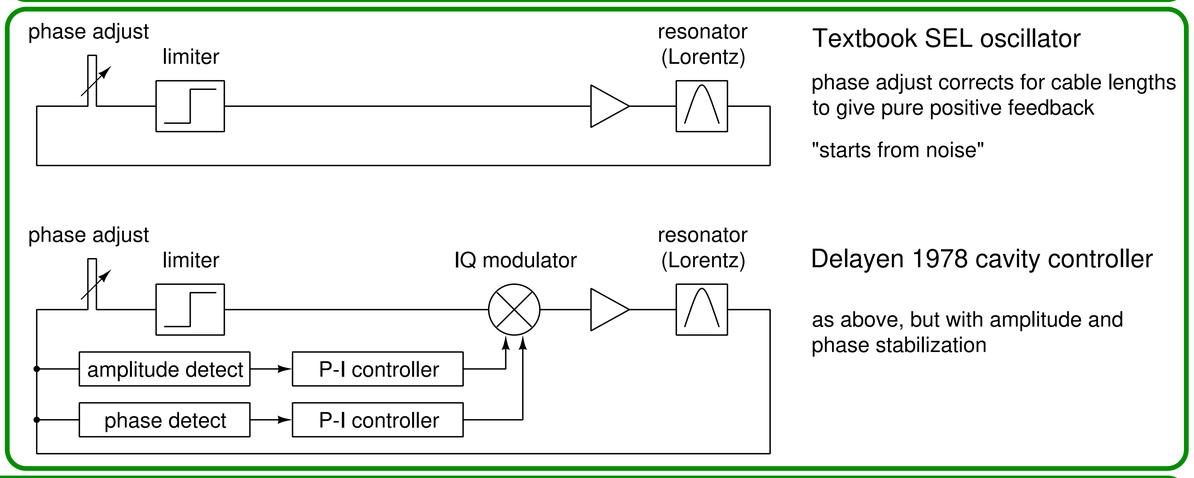
## Turn–on Sequence

Freezes Lorentz forces!

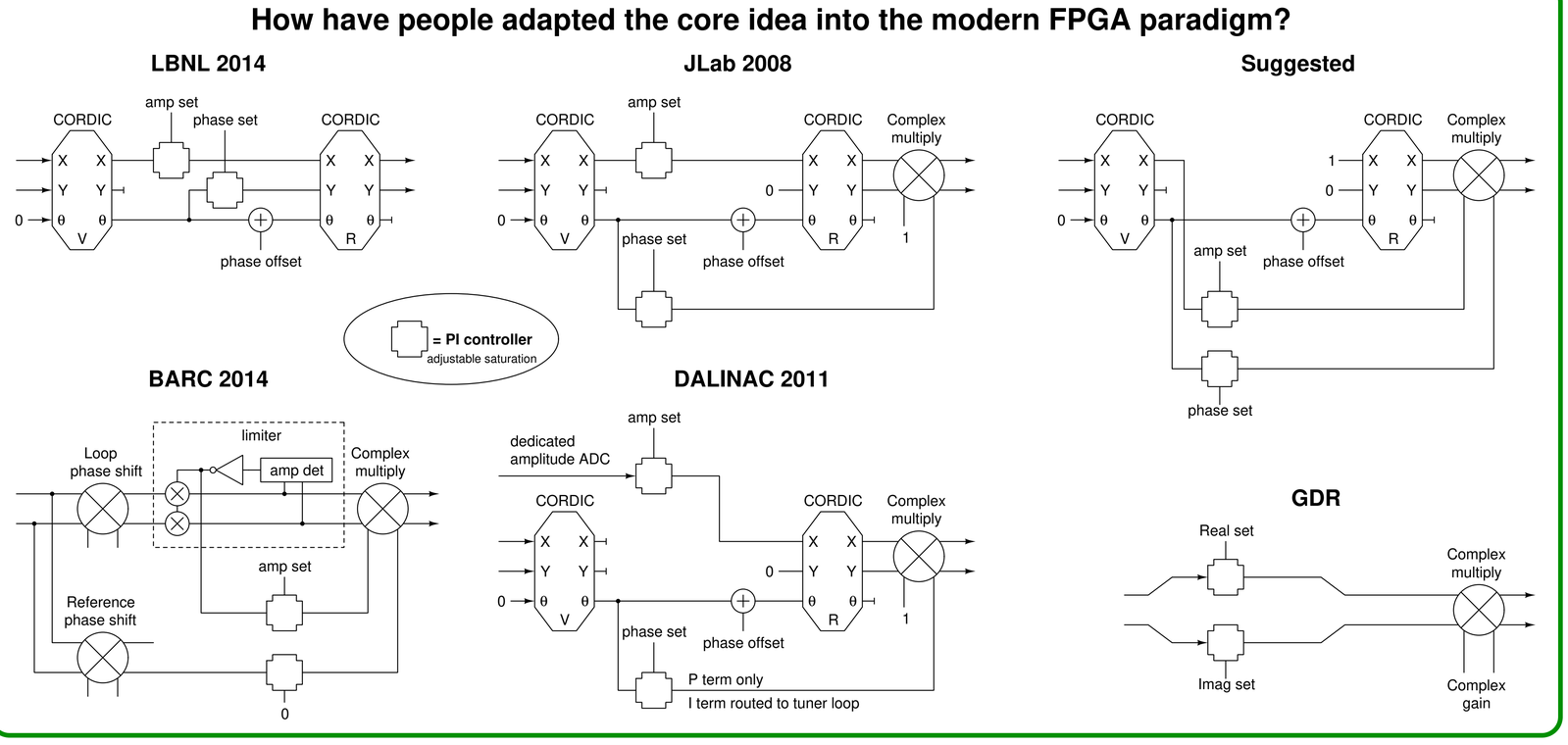
Breaks open the loop

that can lead to ponderomotive instability!

| GDR | SEL |
|---|---|
| 1 Fine tune cavity | 1 Coarse tune cavity |
| 2 Find negative feedback phase | 2 Find SEL phase offset |
| 3 Turn on at low gradient | 3 Turn cavity on and up to gradient |
| 4 Engage frequency tracking loop | 4 Apply amplitude feedback |
| 5 Gradually raise gradient | 5 Engage frequency tracking loop |
| 6 On over-detuning event, go to 1 | 6 Apply phase feedback |
| | 7 Over-detuning events self-heal |



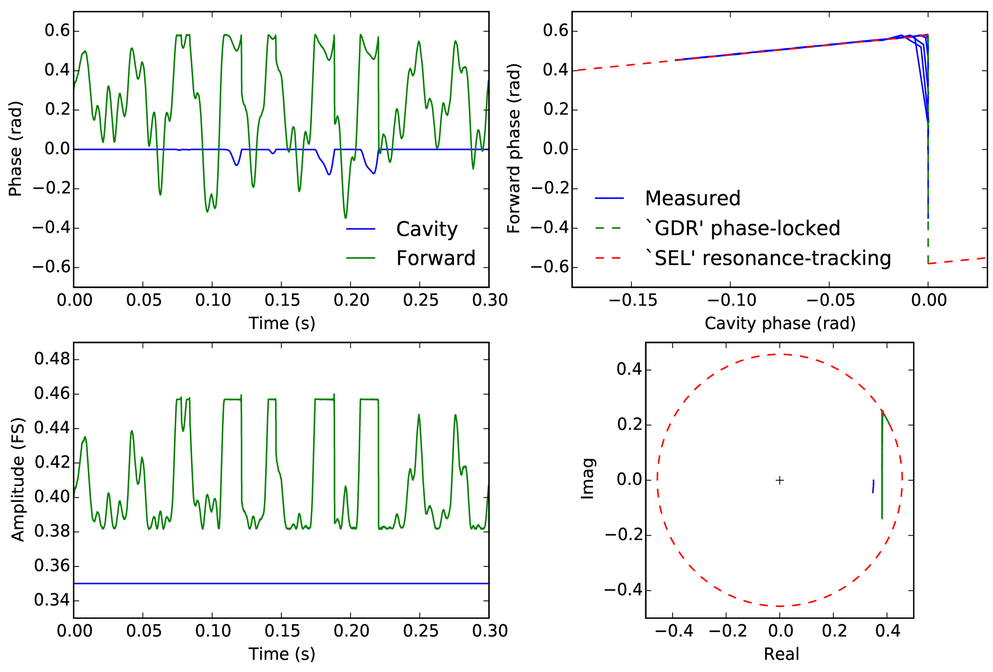

## How have people adapted the core idea into the modern FPGA paradigm?



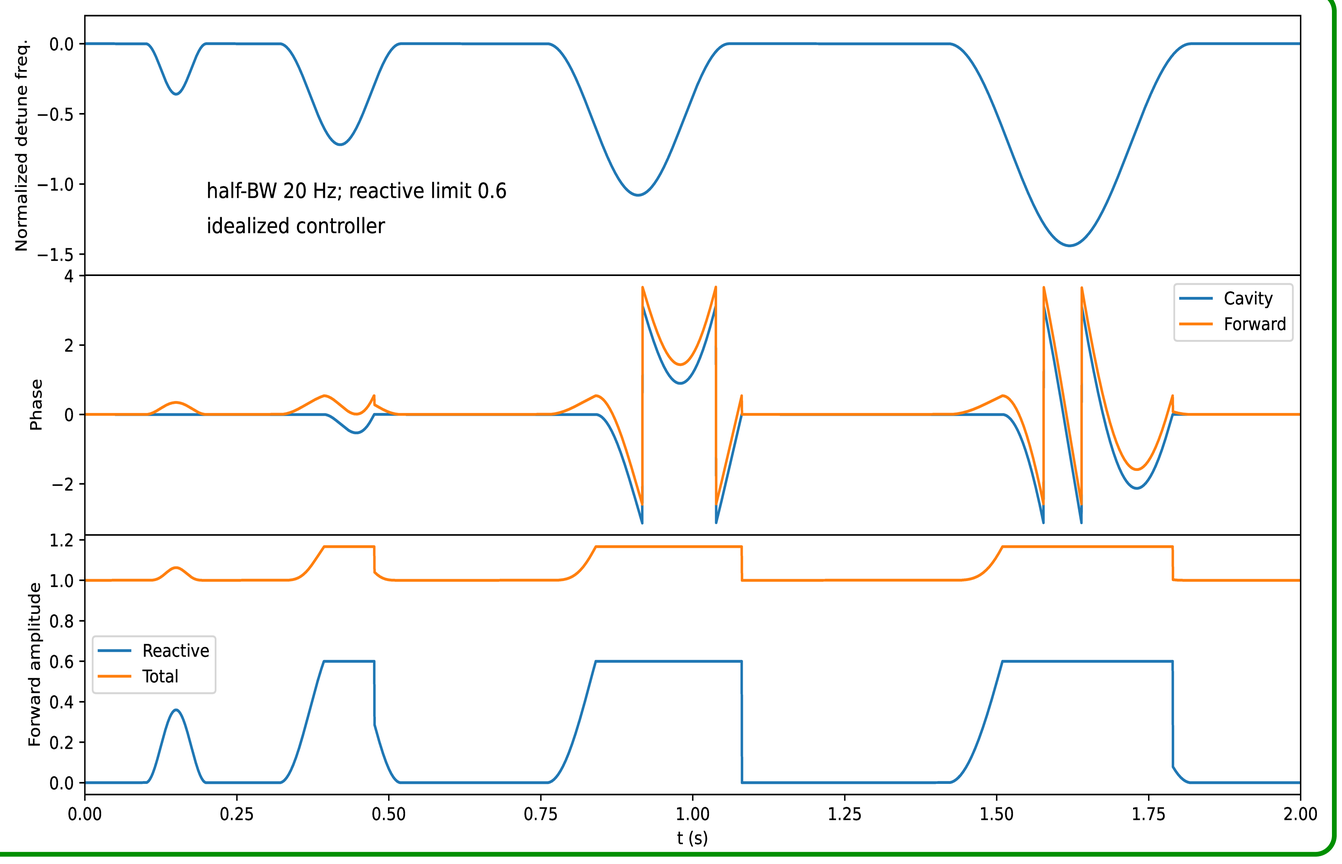

All the same, but all different! Code reuse would be ideal.
Could 'we' at least learn how to mix–and–match implementations and test benches?

## How does the system react when the reactive drive limit is reached?

Phase-locking SEL with clip limits on Q component works as intended




Data taken at Fermilab CMTF, June 27, 2017

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