Update on PIP-II Beam Pattern Generator Upgrade

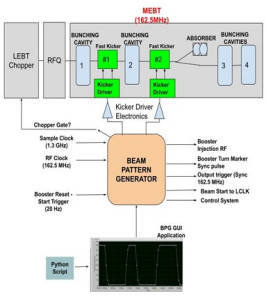
P. Varghese*, S. Raman, M. Guran, L. Reyes, D. Klepec, Fermilab, Batavia, IL, USA
J. Dusatko, D. Chabot, SLAC, Menlo Park, CA, USA

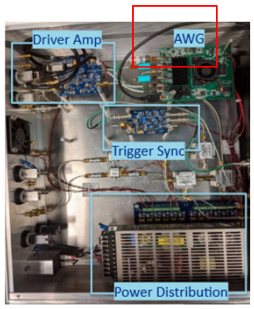
ID 21

Introduction

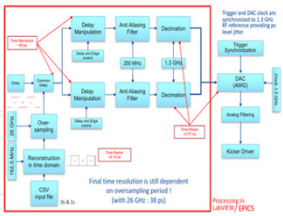
The beam pattern generator enables the transfer of beam pulses from the PIP-II linac to the Booster ring, the two RF systems being non-harmonically related. It is synchronized to the timing system to provide beam arrival information to the downstream accelerator subsystems. The design is being upgraded with COTS components and is being developed with a collaboration with SLAC.The pattern generation, digital signal processing and the user interface to an external EPICS server are integrated onto the ARM processor of the SOCFPGA. The progress of the system development is described.

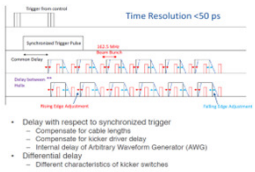
BPG Prototype



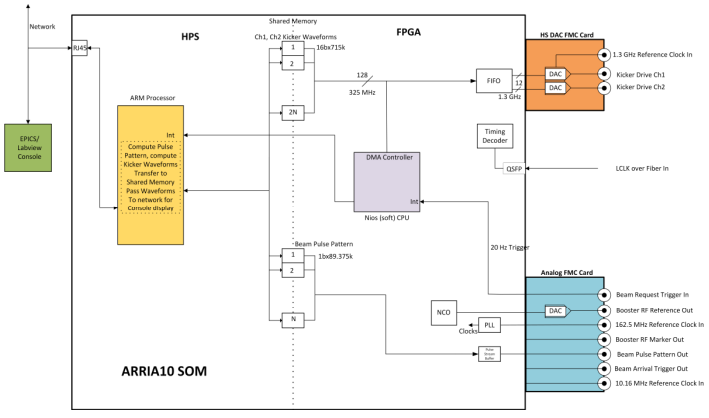


Signal Processing and Delay Adjustment





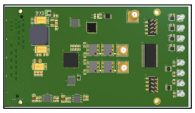
BPG Upgrade Architectuure



Hardware Components

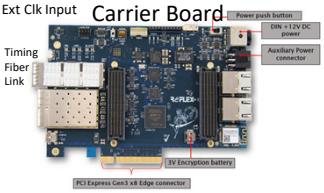
HS DAC Board
DAC12DL3200EVM
12-bit, 3.2 GSPS, Ext Clk Input

Arria10 SOM

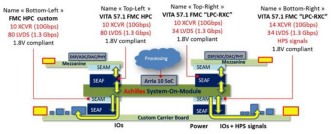


FMC Analog PCB

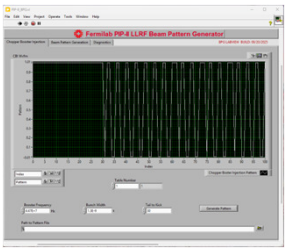
Carrier Board

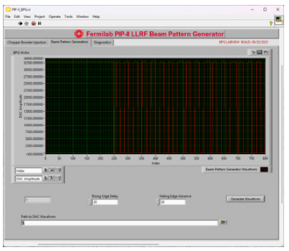


Hardware Configuration

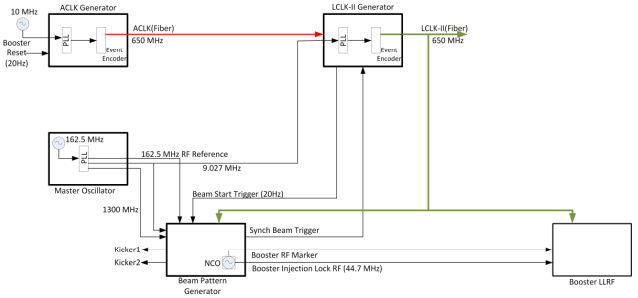


Pattern Generation and DSP in ARM SOC





Timing signals



Summary

- Pattern generation and signal processing software complete in ARM software.
- Analog FMC board being manufactured
- EPICS interface development is in progress. IOC architecture will be hardware based(ARM)

*varghese@fnal.gov