EIC Resonance and Interlocks Control

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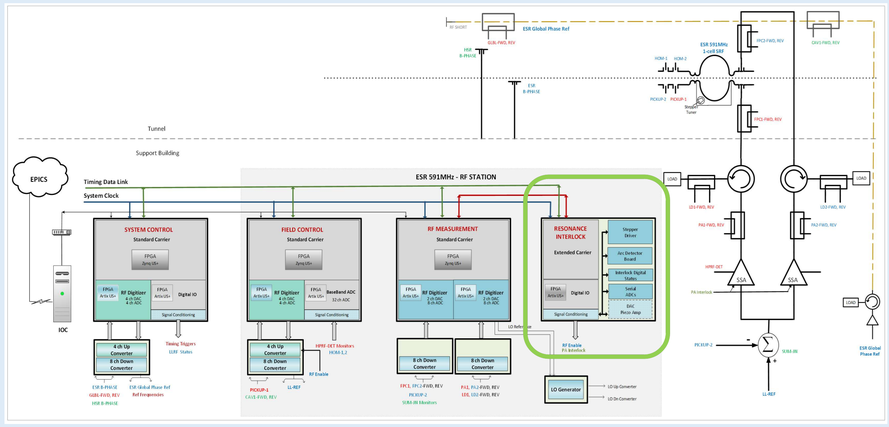
Abstract

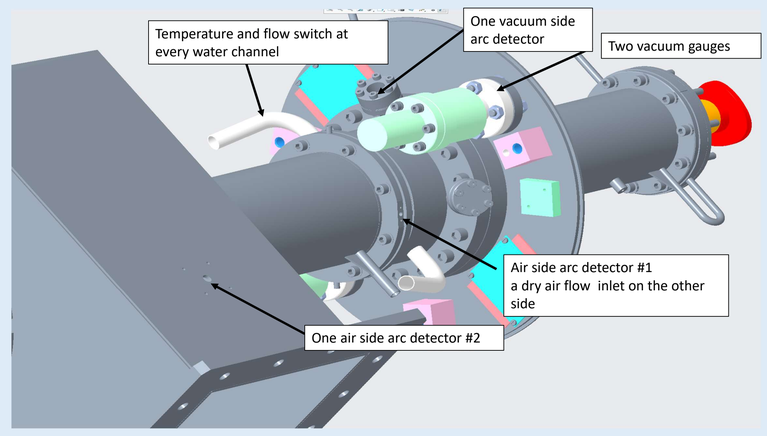
The Resonance and Interlocks Chassis is an important part of any RF control design. When leveraged correctly it will afford the user the ability to tune a given cavity to machine reference frequency, correct for microphonics or slow drifts and provide all the necessary safety interlocks which will reduce the risk of equipment being damaged during operations. Furthermore, it will provide signals which can be used to diagnosis operational problems and overall system health. With regards to controllability and system protection it is one of the most important investments that can be made. The EIC project posses a very interesting problem as there are a dozen different types of cavity designs planned, each with their own interlock and resonance control needs. Furthermore, the physical distance between cavities is large, necessitating 'single cavity' controllers geographically distributed over a wide area. Rather than planning on a dozen unique designs (relative to each cavity), the needs of each cavity were distilled into a common scalable design which is planned to address all the needs of both superconducting and normal conducting LLRF systems for the EIC project.

Much of the design experience form the CEBAF LLRF team, regarding resonance and interlocks control systems, comes from the development of CEBAF's LLRF 3.0 system [1], the collaboration for the LCLS-II Design [2, 3], and the collaboration for the PIP-II RCC design [4]. This design experience is being leveraged into the resonance and interlocks controls development for EIC.

This work being presented at the LLRF 2025 conference hopes to address the scope of this project and highlight some of the solutions to the challenges of this complex and highly integrated system. At the end of this poster, a summary is provided with the next steps for this project as well as tentative PDR and FDR dates.

At the time of writing this document, several of the key PCBs have been prototyped and are being tested (DIO, and Generic Slot) however the extended carrier and power interface board are still being designed by BNL's controls group. All firmware is to be documented and formatted in accordance with Desy FWK.





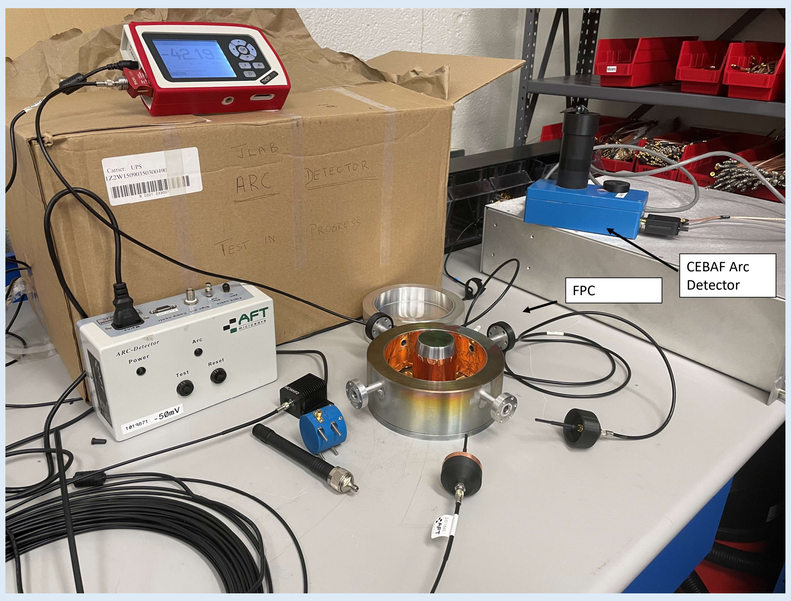
System Block Diagram

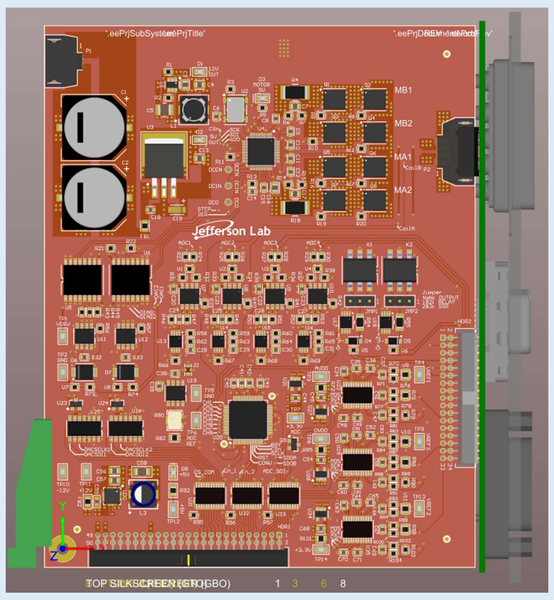
It always useful to see where a subsystem fits into the big picture. One of the dozen cavity types that the Resonance and Interlocks chassis will be used in is the ESR system. Above is an artist's rendition of this which is intended to reveal the overall system integration in a digestible format. Highlighted in green, is the scope of this chassis. This subsystem will rely on communication with BNL's Extended Carrier and Digital Input Output FPGA board (DIO).

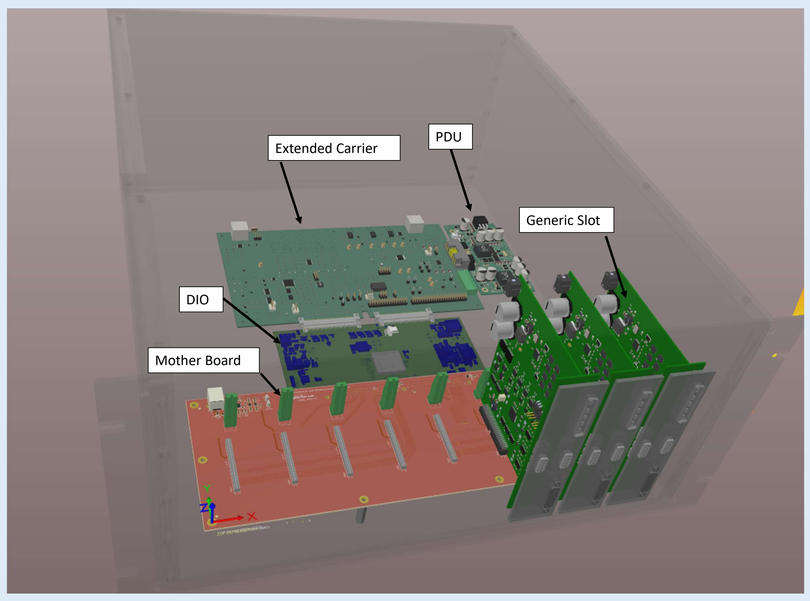
This is one of many complex SRF designs which have varied but similar interlock needs. Though there are a wide variety of cavity types, there will be one common, scalable resonance and interlock chassis. Rather than a dozen customized designs, there will be one unified design which will cover all cavity types.

System Needs

Above is a 3D model of the ESR Fundamental Power Coupler (FPC) which is one of many devices that will be interfaced with this chassis. This model was chosen to help visualize the real-world interface for several key interlocks; here Arc detectors, RTDs and several analog sensor. In addition to these, the subject chassis will also be required to interface with PLC equipment via dry relay contacts to various external systems such as cryogenics and high-power RF systems. It will also need to handle resonance control such as driving stepper motors or providing a low-level signal for controlling external piezo and fast ferrite drivers.







Arc Detector Testing with FPC

An effort lead by Kyle Fahey at BNL was to test various arc detectors with the planned ESR FPC [5]. Several varieties of arc detectors were evaluated, including CEBAF's tried and true PMT Arc Detector (shown above enclosed in a blue box). This is an example of some of the collaboration between BNL and CEBAF engineers to help refine the scope of the interlock requirements for this design, evaluate the planned light pipe designs, and use CEBAFs existing interlocks system to help establish a baseline for performance.

Combining forces leverages abilities from both labs to help reach our common goal. BNL's elegant fiber-optic to SMA design is shown above connected to the CEBAF PMT. A 3D printed adapter was needed for this test setup.

Generic Slot Design

The backbone of the subject chassis is to use a board to board connected generic slot PCB. This approach greatly increases the input/output density available at the front of the chassis without introducing a bird's nest of wiring (and the intermittent failures associated with wiring failures). Each of these slots has a stepper motor driver, several ADC channels, several DACs, several RTD ADCs, and several generic IO. This allows the chassis to be scalable to the individual cavity needs. Some systems will only need two slots installed some will need 6 (ex. ESR, the most demanding system).

This chassis can house up to 8 total slots, so there is additional room for expansion if necessitated by cavity design changes. Furthermore, slot specific cards may be designed for future BNL needs, thus these spare slots give room for future growth.

Chassis Layout

This chassis will follow the design convention of BNL which is to have the communication and power enter through the back of the chassis and for signal IO to come out of the front of this 5U chassis. The DIO is the brain of this chassis which will run firmware to control and monitor all generic slots. The extended carrier is essentially a feed through which will accept a fiber signal from an upstream carrier chassis and provide this communication link to the DIO.

The generic slot PCB has already been described elsewhere; however, this orientation better reveals the connector interface on the front panel. This is also a common but customizable PCB which will allow connector styles to be customized for any given cavity type.

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LLRF team involved in EIC: (L to R) Plawski, Settle, Bachimanchi, Latshaw

Summary

The Resonance and Interlocks design has been a very exciting and challenging project but also a rewarding one. We look forward to having our PDR (part 2) in November 2025 followed by the FDR in March 2026. We look forward to continuing to be a part of the EIC project and help to advance the mission of science together.

References

[1] R. Bachimanchi et all., "JLAB LLRF 3.0 Development and Tests"
[2] L. Doolittle et al., "The LCLS-II LLRF System" in Proceeding of IPAC2015, Richmond, VA, USA, 2015.
[3] R. Bachimanchi et al., "LLRF Resonance Control System for LCLS-II Cavities" in Proceeding of LLRF2017, Barcelona, Spain, 2017.
[4] J. Latshaw et all., "PIP-II Resonance Control System"
[5] BNL team, private communications.