2025 EIC User Group Early Career Workshop

Prototype Testing of AstroPix Sensors and System Integration for BIC at ePIC

Bobae Kim (bobae.kim@anl.gov)

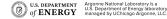
Argonne National Laboratory





Contents

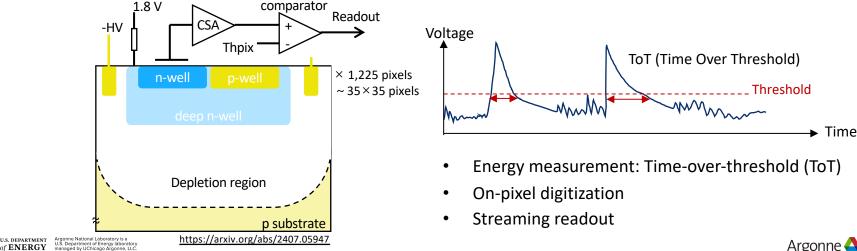
- Introduction
 - Astropix
 - Barrel Imaging Calorimeter (BIC)
 - Structure of Imaging Layer with AstroPix in BIC
 - AstroPix and BIC Timeline
- Testing Setup
- AstroPix Testing Result and Status
 - AstroPix v3 Single chip
 - StroPix v3 Quad chip
 - Multilayer of AstroPix v3 Quad chips
 - AstroPix v3 9-chip Module: The smallest unit of imaging layer at BIC!
 - AstroPix v4 Single chip
- System Testing for Integration
- Summary & Plan



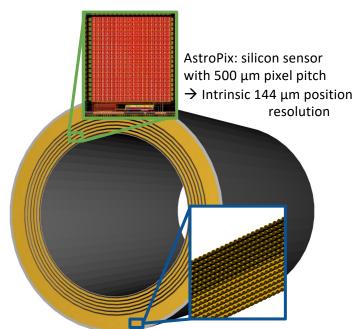


Overview of AstroPix

- New silicon pixel sensor: High-voltage CMOS monolithic active pixel sensor (HV-CMOS MAPS)
 - Developed based on the experience from ATLASpix and MuPix
 - For space-based missions, specifically for gamma-ray astrophysics
 - NASA sounding rocket mission (End of March 2026), ComPair2 balloon mission, and AMEGO-X space mission
 - Use as the imaging layers in the barrel imaging calorimeter for nuclear physics applications.
- Charge collection/signal processing (Charge Sensitive Amplifier → Comparator for ToT) on each pixel
 - →low noise and low power consumption!



Overview of Barrel Imaging Calorimeter at EIC detector



- Hybrid lead/scintillating fiber calorimeter with silicon tracking layers to precisely measure electromagnetic shower profile
- Requirements for Barrel EM Calorimeter [Yellow Paper]
 - Energy resolution < 10%/√(E) + (2-3)%
 - Photon measurements in energies of 100 MeV 50 GeV
 - Electron ID up to 50 GeV and down to 1 GeV and below
 - e/π separation for energies of 1 GeV 50 GeV
 - γ/π⁰ separation up to 10 GeV
- 4(+2) layers of AstroPix sensors interleaved with the first 5 Pb/SciFi layers, and a large section of Pb/ScFi section
- Total radiation thickness [~] 17.1 X₀ at η=0
- Sampling fraction ~ 10%

Pb/SciFi Layers with two-sided SiPM readout

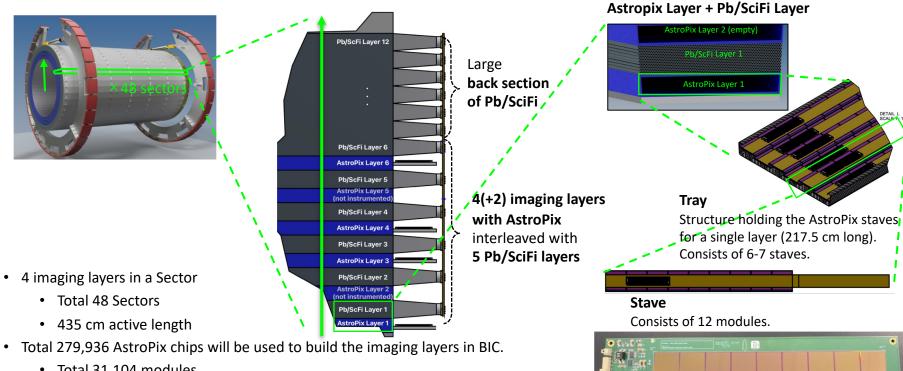
 \rightarrow 1.1cm/VE position resolution in z by Δ t measurement [NIMA 596 (2008) 327]

- Energy resolution Primarily from Pb/ScFi layers (+ AstroPix energy information)
- Position resolution Primarily from imaging layers (+ 2-sided Pb/ScFi readout and φ-R segmentation)





Structure of Imaging Layer with AstroPix in BIC



- Total 31,104 modules
- All Trays will be built using same modules, standardizing the loading procedure
- The first prototype module, built with v3 sensors for initial testing.
 - \rightarrow v5 will be used for 9-chip module after fabrication is complete.

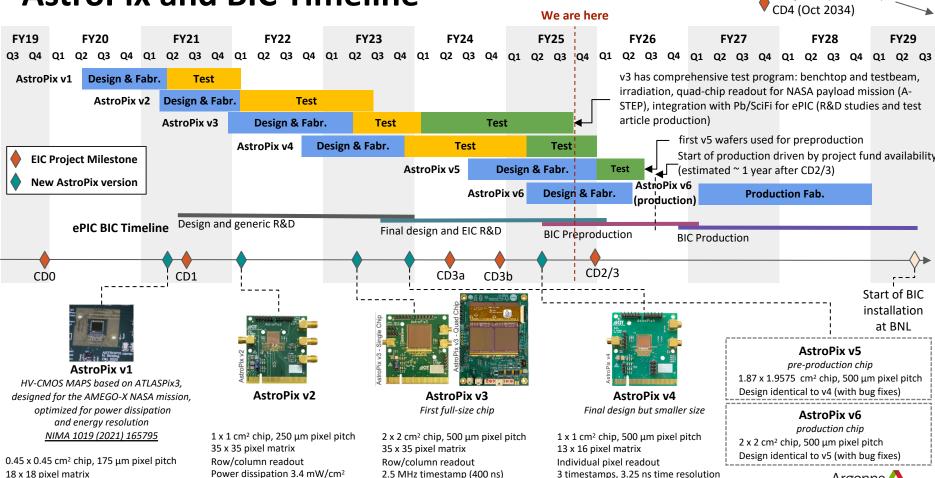


AstroPix Module

9 AstroPix sensors daisy-chained together on PCB.



AstroPix and BIC Timeline



200 MHz ToT (5 ns)

TuneDAC for pixel-by-pixel thresholds

Not shown:

Early CD4 (Oct 2032)

Power dissipation 14.7 mW/cm²

Test Setup







9-chip daisy-chained Prototype Module



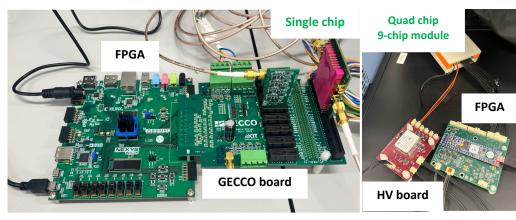
Bench test

- Noise scan (w.r.t thresholds)
 - → Masking noisy pixel
- Injection test (w.r.t different injection voltages)
 - → ToT response vs injection voltages
- Radiation source test
 - → Calibration curve each pixel

Beam test

- 120 GeV Proton beam @FNAL (June.2024)
 - → MIP response
 - → Depletion depth

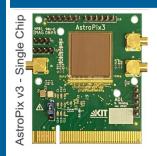
Two testing setups for AstroPix



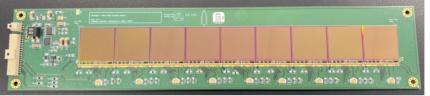
ASTEP-HW board



Test Setup







9-chip daisy-chained Prototype Module



Bench test

- Noise scan (w.r.t thresholds)
 - → Masking noisy pixel
- Injection test (w.r.t different injection voltages)
 - → ToT response vs injection voltages
- Radiation source test
 - → Calibration curve each pixel

Beam test

- 120 GeV Proton beam @FNAL (June.2024)
 - → MIP response
 - → Depletion depth

Test Results

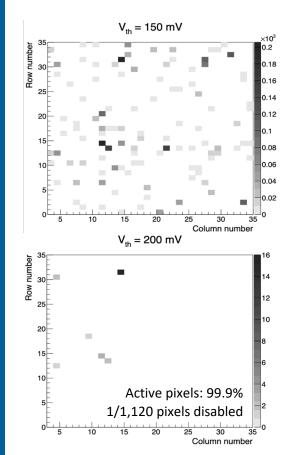
	Single chip	Quad chip	Three layer of Quad-chips	9-chip Module [<mark>##</mark>]	V4 Single chip
Noise scan	V	~		V	~
Injection test	V	V		✓	~
Source test	V	V	V		V
Beam test	V				

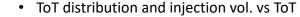


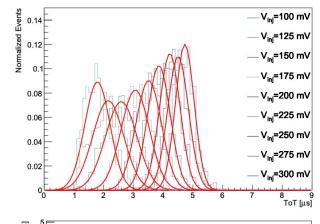


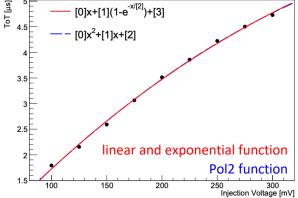
v3 Single Chip: Performance Test Results (1)

Bench Test: Noise Scan, Injection scan and source test

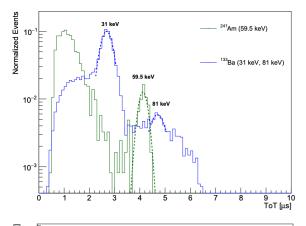


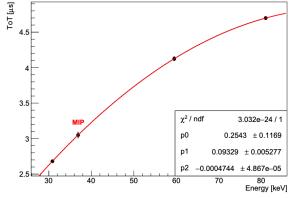






Calibration curve (Am241 and Ba133)

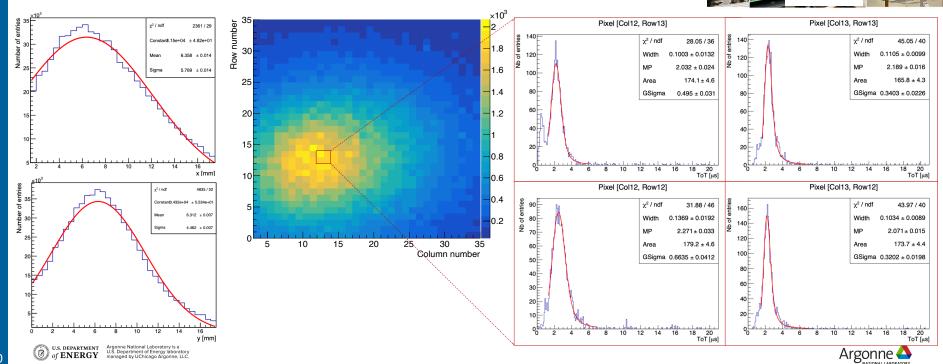




v3 Single Chip: Performance Test Results (2)

Beam Test: 120 GeV Proton Beam

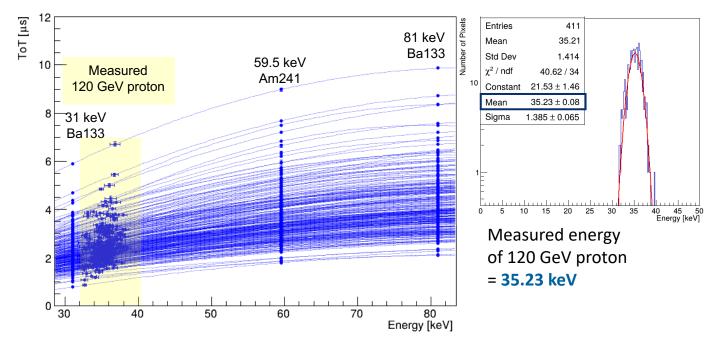
- The hit map reveals the proton beam profile: $\sigma_x \times \sigma_v = 5.8 \text{ mm} \times 4.5 \text{ mm}$
- ToT Histograms with MIP response → Fit with Landau convoluted with gaussian function
- Behaves well in the particle rates of 13 kHz



v3 Single Chip: Performance Test Results (3)

Beam Test: 120 GeV Proton Beam

- Calibration curve as a function of energies for selected pixels
- First 120 GeV proton response: 35.23 keV for MIP which sits well within dynamic range (25 keV 200 keV) in AstroPix v3
- → The corresponding depletion depth: 132.4 um



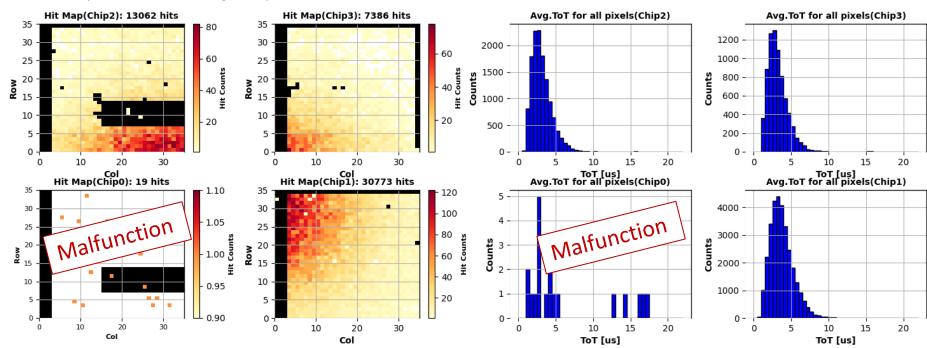


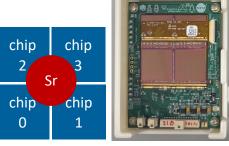


v3 Quad chip: Performance Test Results (1)

Bench Test: Source test with Sr90

- The hit map aligns well with the source position at the center of the quad chip.
- The ToT distribution is well-described by a Landau convoluted with a Gaussian function.
- Comparable with v3 single chip results





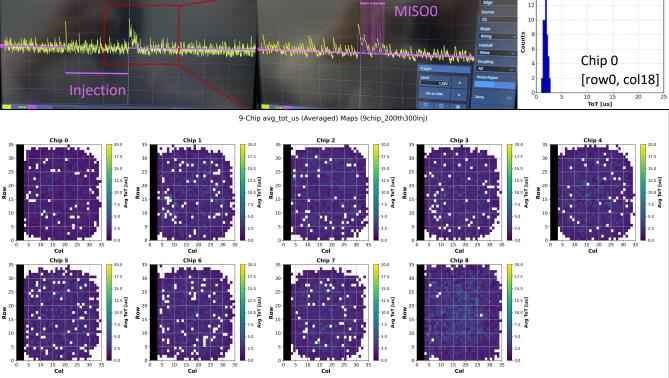
Readout 4858, Timestamp 173, Laver 3 v3 Quad chips: Functional Test Results (2) Bench Test: Cosmic test using three layers of quad-chips To verify that the software and firmware under development operate properly Display of a representative event where all three layers share the same timestamp 1 TimeStamp = 400 ns Readout 4858, Timestamp 173 → Validated the capability to read data from all quad chips. Laver 1 Layer 2 Readout 4858, Timestamp 173, Layer 2 → Successfully merged the feature branch for quad-chip Laver 3 testing into main: https://github.com/AstroPix/astep-fw 3 Readout 4858 Timestamn 173 Laver **ASTEP-HW** Chip3 **FPGA** 60 PC Chip1 20 50 70

9-chip prototype module: Functional Test Results

- Initial functionality confirmed power stable and DAQ communication OK.
- Moise/Injection scan (10s for each pixel)
 - Observed unexpected maximum buffer values ideally, only 0/22 or 44 bytes were expected.
 - Analog signal height is lower compared to single- or quad-chip setups







ASTEP-HW

FPGA

v4 single chip: Performance Test Results

81 keV (Ba133)

- Optimized the configuration for v4 testing
- ✓ Injection scan (HV = -200 V, threshold = 130 mV)
- Noise scan w.r.t thresholds

U.S. DEPARTMENT
of ENERGY

Argonne National Laboratory is a
U.S. Department of Energy laboratory
managed by Uchicago Argonne, LLC.

- Source test with Am241/Ba133
- 🊧 Plan to perform the irradiation test at FNAL (Fall, 2025)



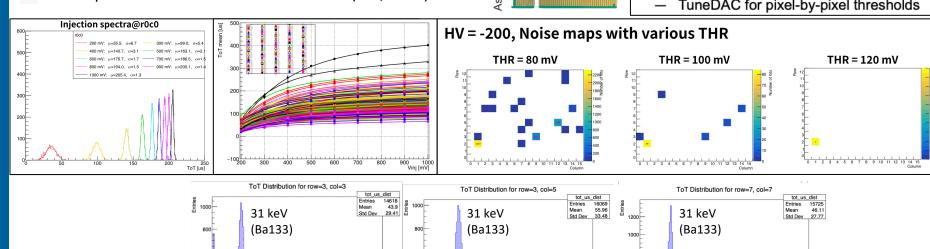
*Final version for BIC, similar design to v4 spec.

Astropix v4 single chips

- 1 x 1 cm² -size with 13 \times 16 pixel matrix
- 500 µm pixel pitch

81 keV (Ba133)

- Individual pixel readout
- 3 timestamps, 3.25 ns time resolution
- TuneDAC for pixel-by-pixel thresholds



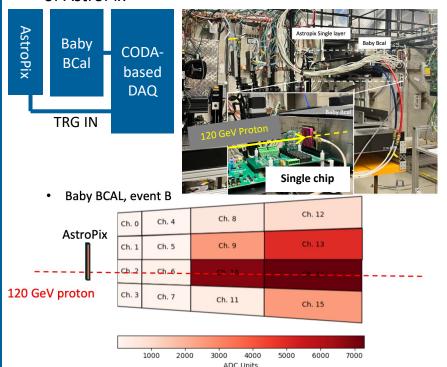
81 keV (Ba133)



System Testing for Integration (1)

AstroPix+BabyBCAL @Beam test (June 2024)

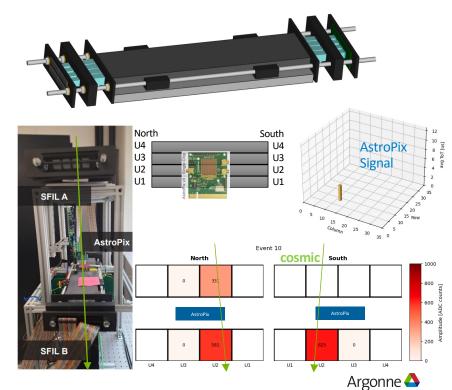
 Baby BCAL triggered by analog signal from one pixel of AstroPix



^{*}Example plot of 120 GeV proton event display from an integrated system of Baby BCAL and a single-layer AstroPix v3 chip by Henry Klest

AstroPix+SFILs @Bench test

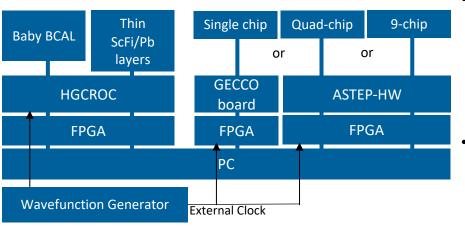
 Thin Pb/SciFi layers with new SiPMs and optical cookies commissioned on bench.



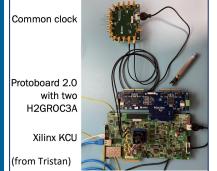
System Testing for Integration (2)

Synchronization Plan between AstroPix DAQ and HGCROC for Pb/SciFi

Provide 40 MHz external clock to HGCROCs and AstroPix DAQ



- AstroPix single chip+
 GECCO board + Nexys + ASTEP sw/fw
 - LVDS external clock used
 - Both 10MHz Timestamp and the FPGA timestamp external (10MHz+40MHz)
 - Bit file exists but needs debugging;
- AstroPix quad-chip / 9-chip module +
 ASTEP HW board + CMOD + ASTEP sw/fw
 - single-ended clock required
 - FPGA Timestamp external (40 MHz)









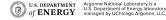
Summary & Plan

Testing and characterization of AstroPix is underway:

- First 120 GeV proton response: 39.41 keV for MIP which sits well within dynamic range (25 keV 200 keV) in v3 single chip
- Several configurations involving a successively increasing number of AstroPix sensors have been successfully tested and are ongoing.
 - Single chip in a beam-like environment
 - Multi-layers of quad-chips
 - 9-chip prototype module
- The v5 chip, intended as a pre-production prototype, is currently being fabricated.

For the upcoming PDR,

- Continue to test 9-chip prototype module
- Integration and synchronization of AstroPix & Pb/SciFi with HGCROC (CALOROC)







Key Performance and Parameters Metrics

For Final Chip Version in BIC

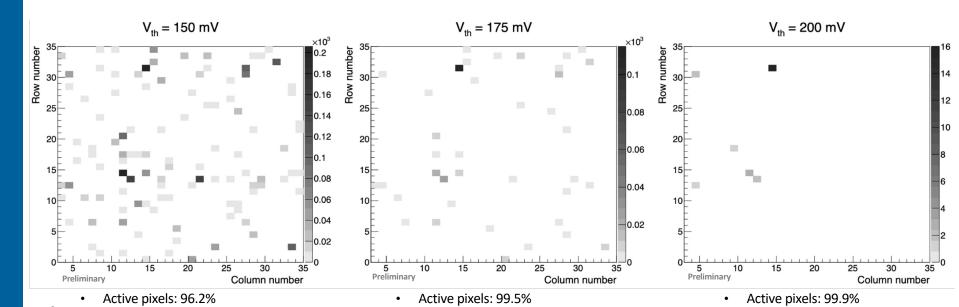
	AstroPix for AMEGO-X requirements [arXiv:2208.04990]	BIC requirements	
Pixel pitch	500 μm x 500 μm		
Power usage	< 1.5 mW/cm ²	~ 2 mW/cm² in v5 acceptable	
Energy resolution	< 10% (FWHM) @ 59.5 keV		
Dynamic range	25-700 keV		
Passive material	< 5% on the active area of Si		
Time resolution	25 ns	3.125 ns (in v5)	
Si Thickness	500 μm Fully depleted		

v3 single chip: Performance Test Results (1)

Bench Test: Noise Study

43/1.120 pixels disabled

- Determine the percentage of pixels which are sensitive to the dynamic range and record intrinsic noise rates lower than the set threshold (plots below show 5s of data taking)
- The AstroPix dynamic range floor (25 keV) allows for threshold values of more than 200 mV above baseline.
- < 0.5% of pixels (1 pixel/array) have a noise rate > 2 Hz for data collection and are masked
- Fulfills BIC requirements on low energy threshold (25 keV tested in simulations), and yield of masked pixels.



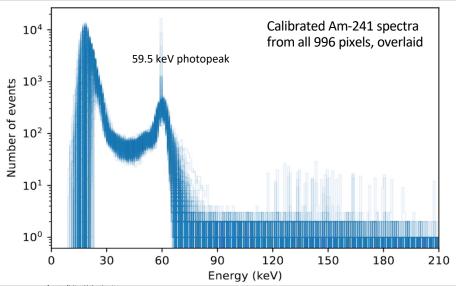
6/1.120 pixels disabled

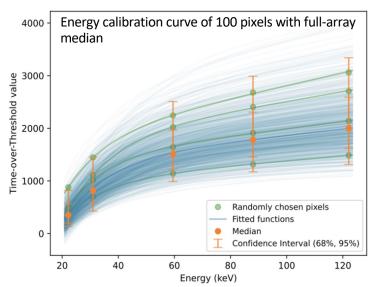
1/1.120 pixels disabled

v3 single chip: Performance Test Results (2)

Bench Test: Radiation Source Test

- Energy resolution/calibration: Cd-109, Ba-133, Am-241, and Co-57; from 22.2 keV to 122 keV
- Dynamic range: 25-200 keV (v5 will test 700 keV dynamic range, required for BIC)
- 44% of pixels meet the energy resolution requirement of 10% at 59.5 keV with a median full-width half-maximum of 6.2 keV (10.4%).
- **92.4% of pixels achieve the low-energy floor requirement** of 25 keV sensitivity, required for BIC.

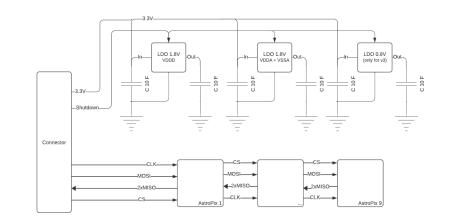


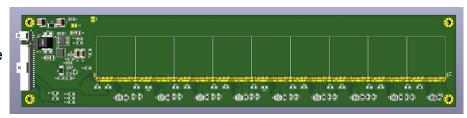




AstroPix 9 Chip PCB Test Module

- Similar design to quad chip board (no busbar required)
- Nine AstroPix Chips, Daisy-chained on the Module
- Each Module plugs into its adjacent Module
- All Modules will be controlled by the End-of-Tray Card
- The broadcast commands/data readout through SPI protocol
- One main HV line (~500V) and one (or 2) LV line (3.3V)
- Voltage Regulators (LDO) to regulate power on each Module
 - Analog and digital power of 1.8V at Module
- 4 differential data SPI (Clk, MOSI, 2MISO) common for stave
- One single-ended Chip-select SPI per Module
- Approximately 24 I/O + GND Pins per Stave
 - Exploring connector options (radiation hard, smaller size)













U.S. DEPARTMENT of ENERGY