Fermilab

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FCFD Status

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U.S. DEPARTMENT of ENERGY

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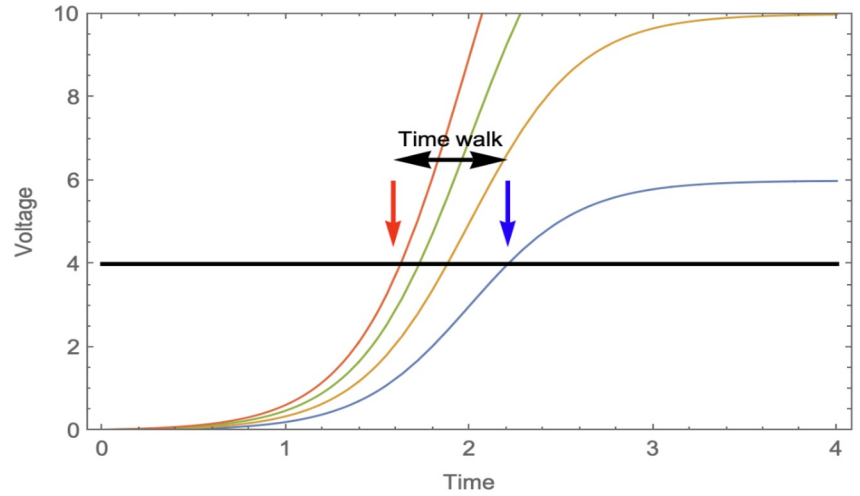
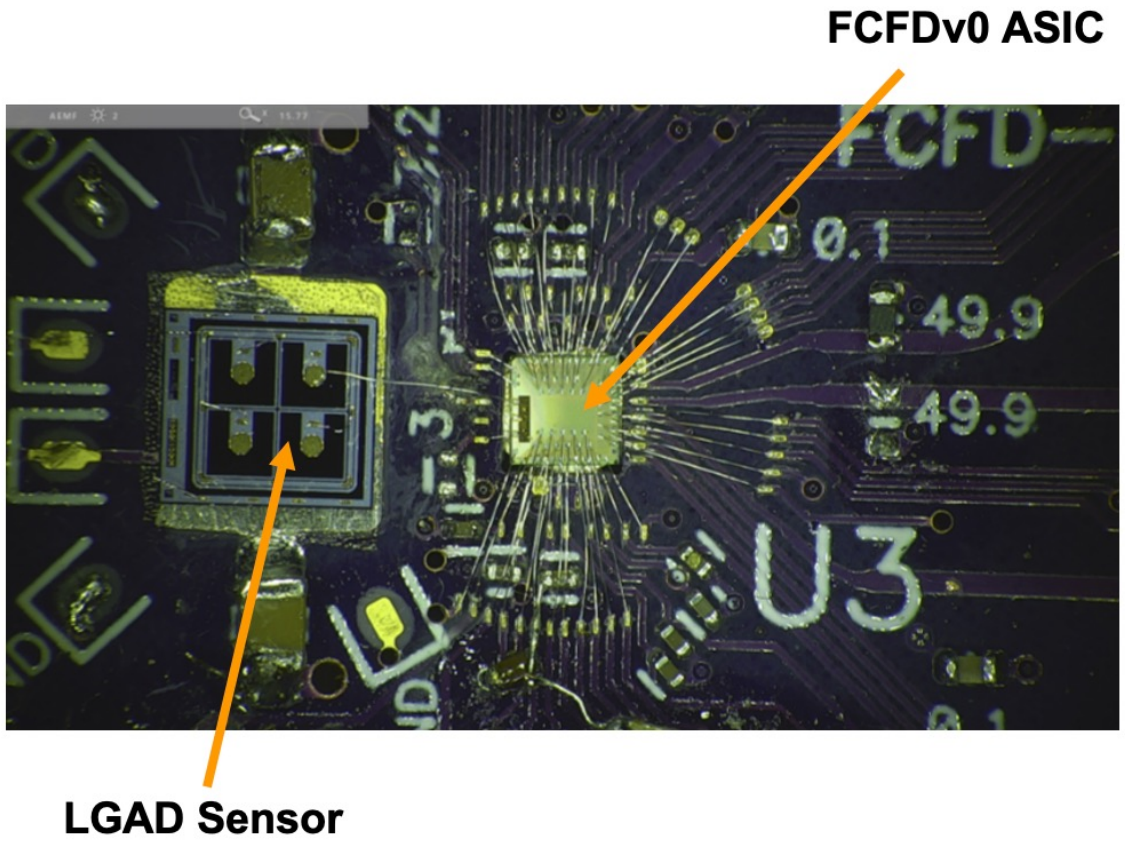
Introduction

- A robust fast-timing measurement technique for LGADs
- CFD approach achieves excellent performance, especially for low S/N systems, such as LGADs (NIM A 940 (2019), pp 119-124)
  - CFD-based readout is much simpler in operation and maintenance
  - No need to maintain the calibration and monitoring system, computing workflows, database maintenance, payloads, etc…
- Time-walk effect is well known & must be corrected for best performance
- A hardware-enabled correction via CFD built into the readout ASIC design offers much simpler solution

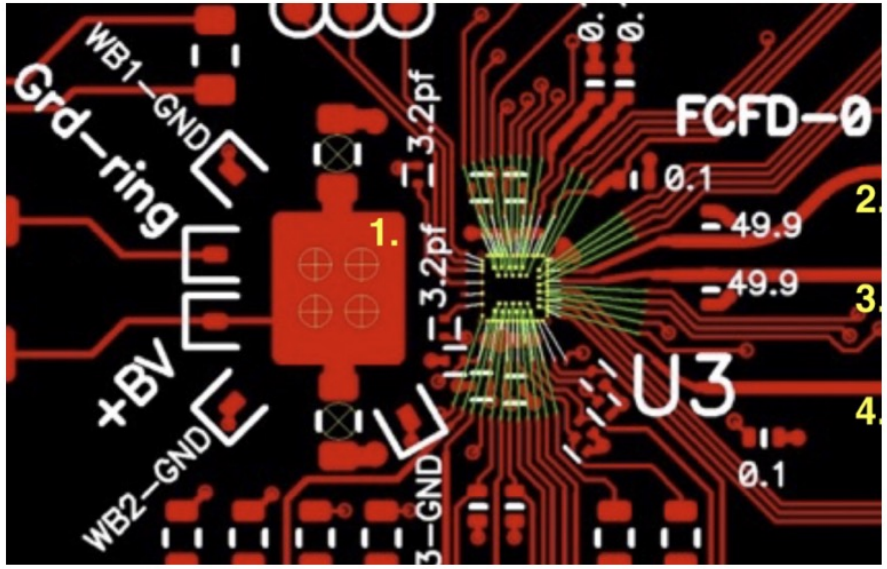


FCFD Chip Prototype v0

- First prototype designed and fabricated in 2021 & tested in 2022

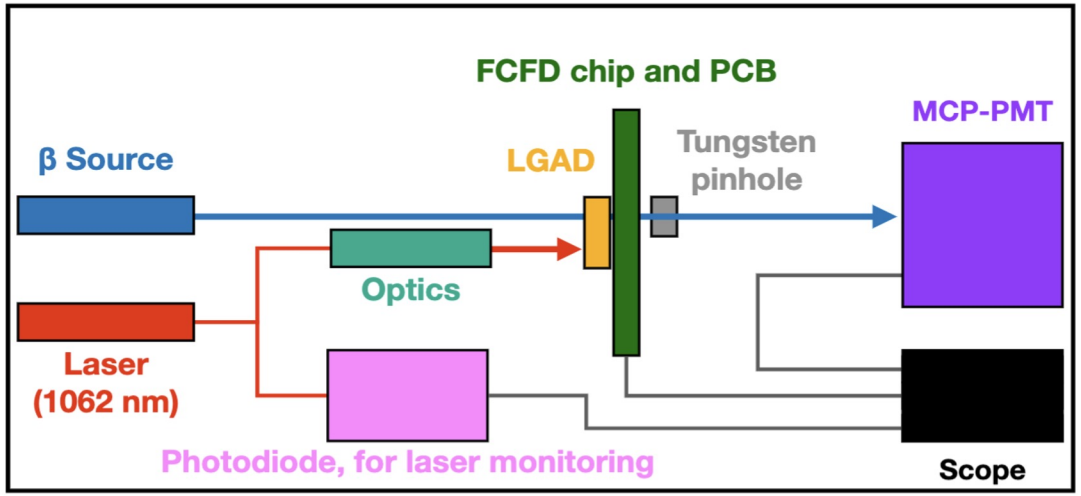


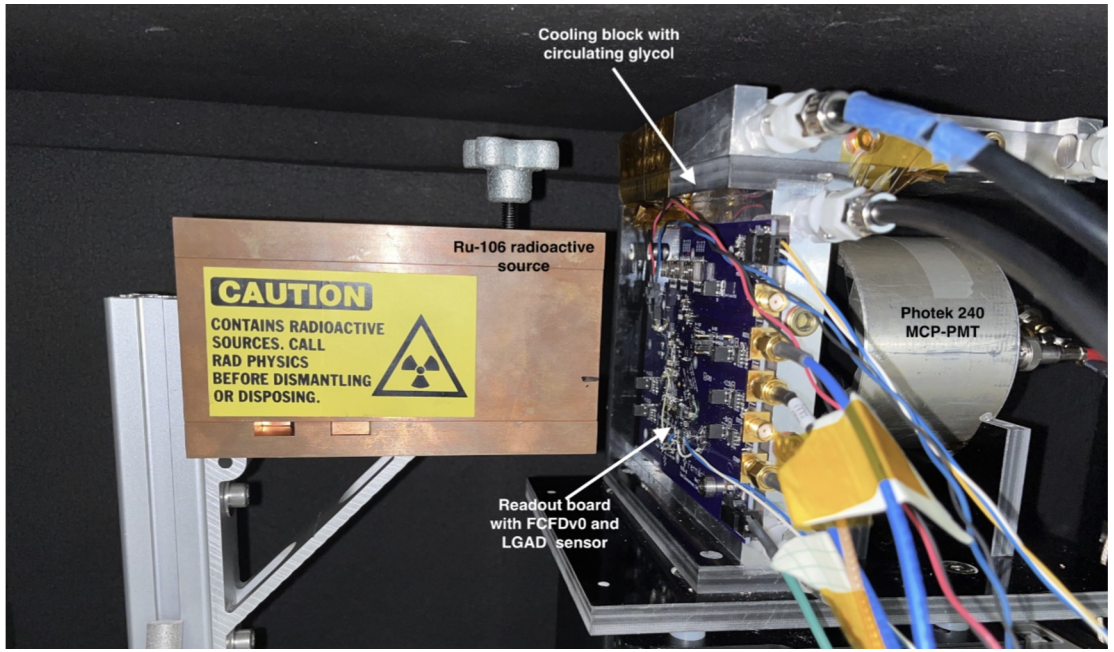
Schematic Diagram



Picosecond Laser & Beta Source Setup

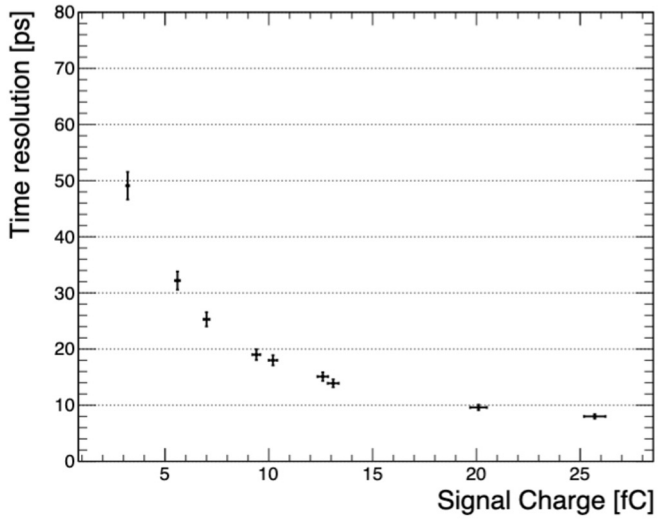
- Dark box with motorized stages, enabling laser injection and beta source
- Picosecond Laser trigger signal serves as time reference
- Collimator and MCP time reference detector ensures straight trajectories: get beta rates of about 2-3Hz at best alignment
- Temperature maintained at 20C by chiller and cooling block



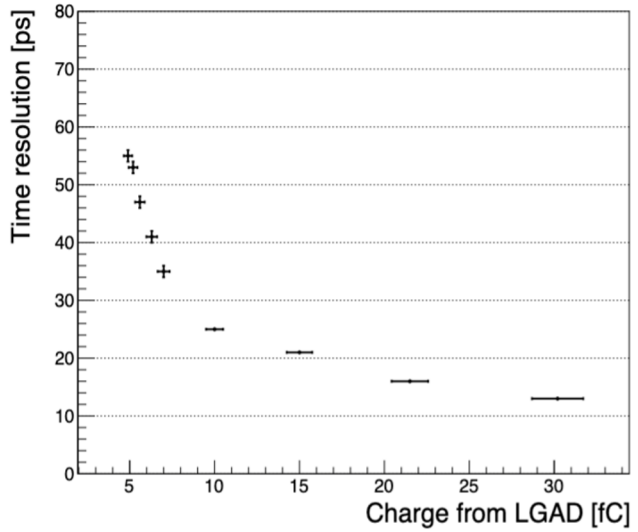


Multi-Source Signal Testing Setup

- FCFD v0 performance evaluated using multiple types of signals:
  - Charge-injected signal
  - Picosecond Laser signal
  - Radioactive Source signal
  - Proton Beam signal

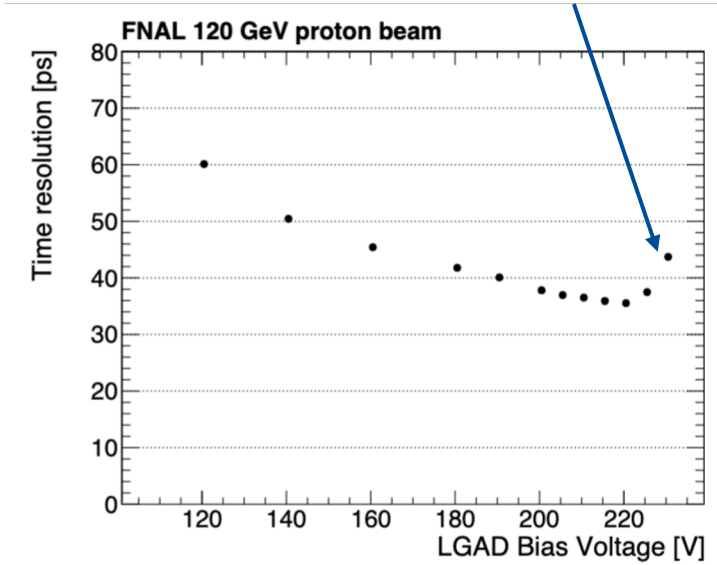


Charge Injection: intrinsic jitter



Laser signal on LGADs

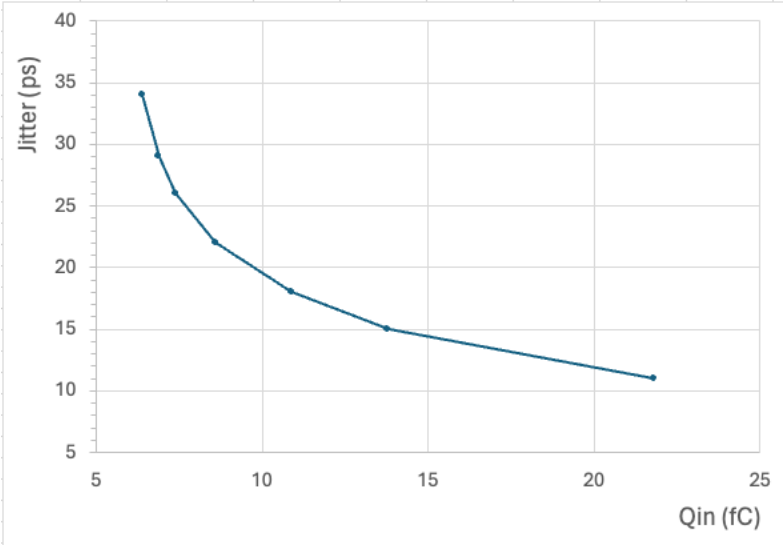
Saturation here again
Addressed with v1 chip



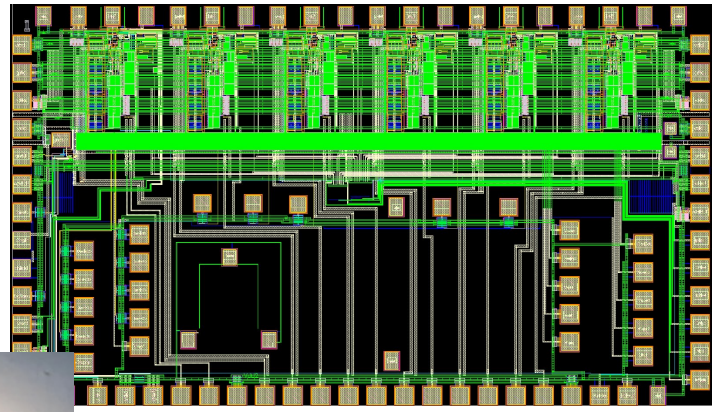
Test beam in FNAL

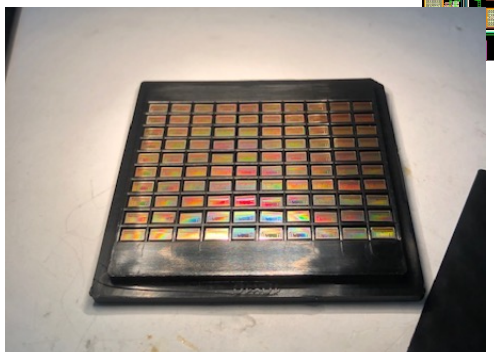
FCFDv1

- Six-channel FCFDv1 submitted Sep. 2023
  - Wider dynamic range,
  - Sensitivity to smaller signals
  - Includes signal amplitude measurement for position measurement
- Received the chip back from TSMC in Jan 2024
- Internal charge injections with an LGAD-like signal
  - Measure around 11 ps time resolution
  - The analog output works linearly over the range from 7 fC to 60 fC,
  - the discriminator flip time output stays constant around 10 pS



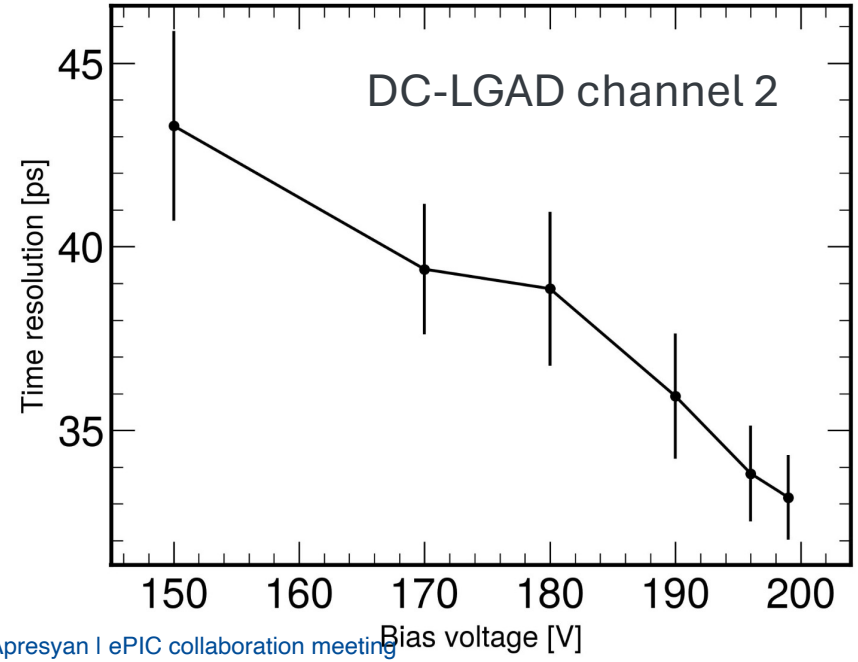
Jitter measurements with 3.5 pf input capacitance and charge injection

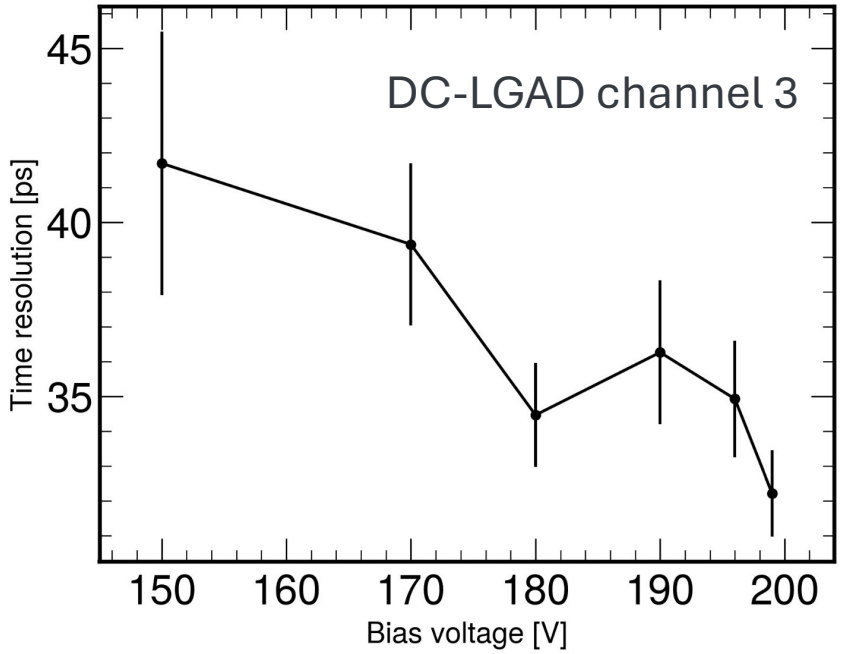




FCFDv1 testing in proton beams: DC-LGADs

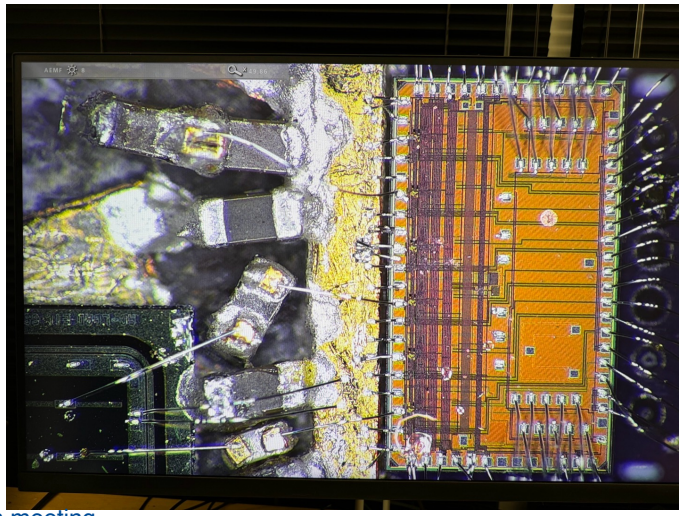
- Performed bias scan BV = 150V, 170V, 180V, 190V, 196V and 199V (breakdown above 200 V)
- Achieve time resolution around 32 ps
  - No time-walk observed, no time-walk correction applied
  - Signal amplitudes around 300 mV
  - Chip performs well for sensors with expected characteristics

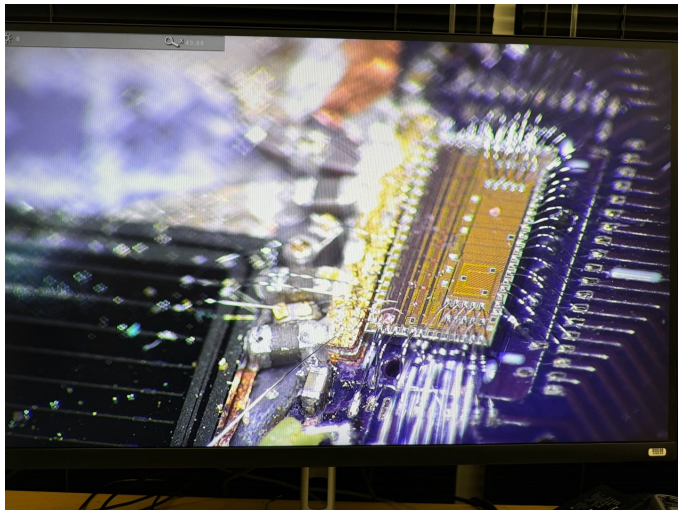




FCFDv1 testing in proton beams

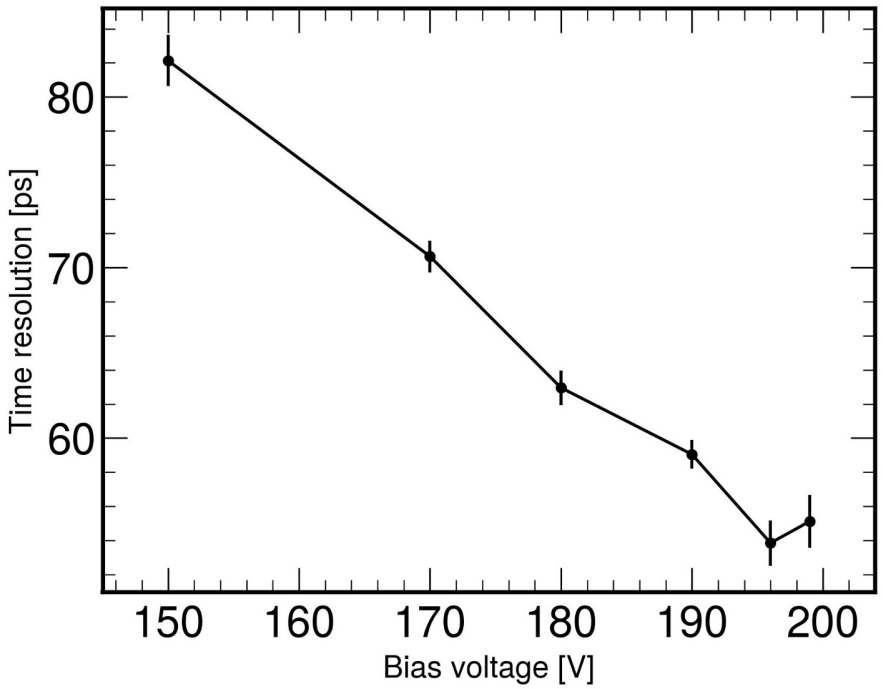
- Measurements with AC-LGAD strip sensors showed higher noise and unexpected behavior
  - Our measurements of the AC-LGAD strip sensors showed the complex RC-network which complicates operation of the ASIC, and larger capacitance than expected
- Modified the readout board for test beam in June 2024
  - Added a 7-pF capacitor in series to the AC-LGAD sensor, to reduce the noise and avoid fake hits, and reduce input capacitance
  - Fake hits are reduced, but also signal size was reduced by half

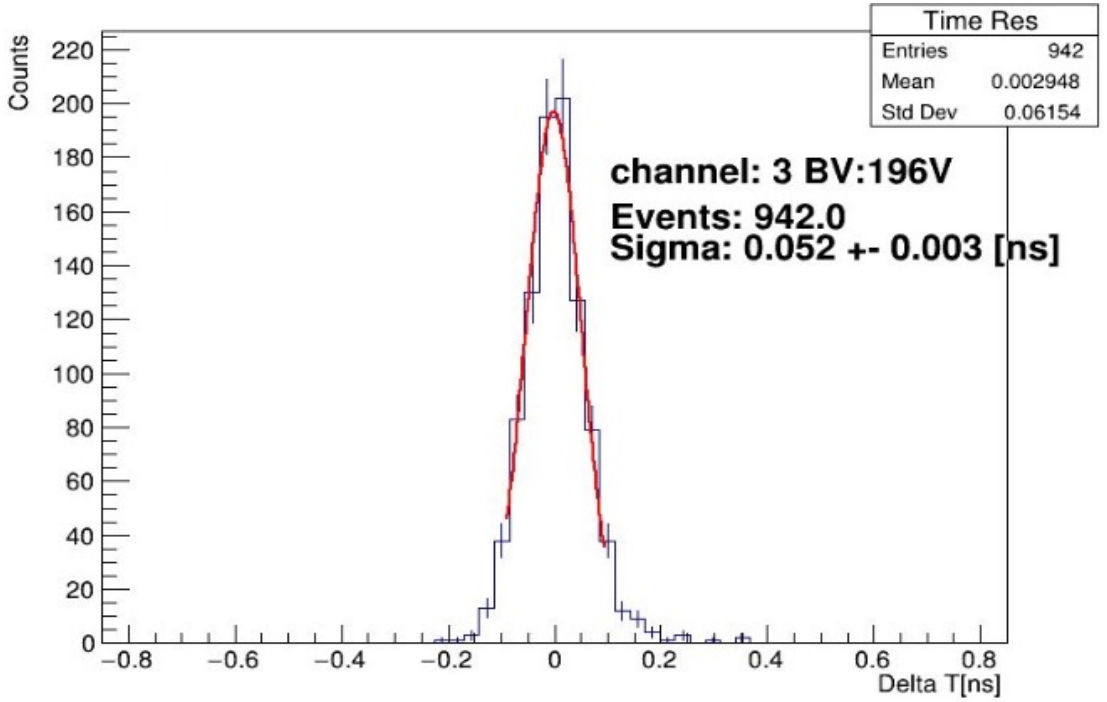




FCFDv1 testing in proton beams: AC-LGADs

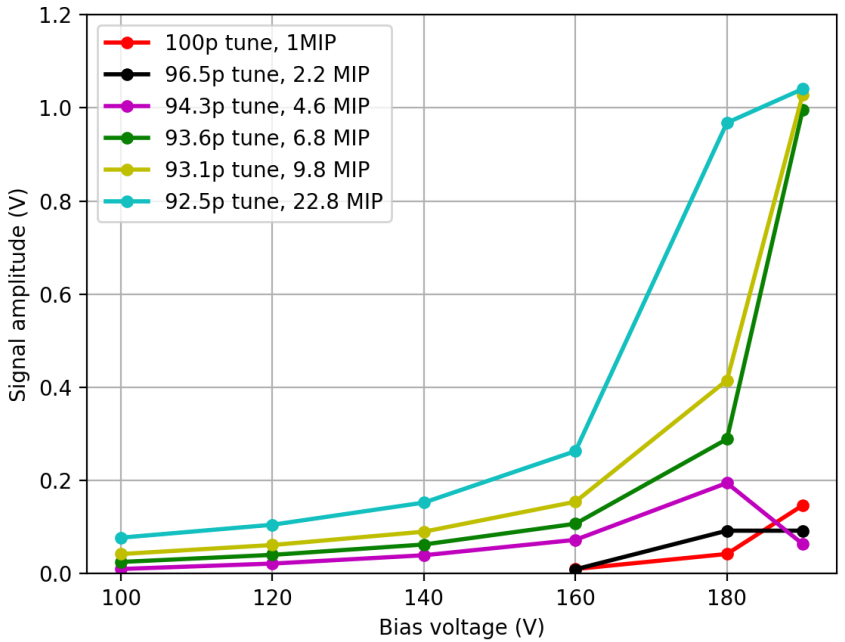
- Time resolution on the AC-LGAD channel achieves around 52 ps
  - Due to series capacitor, MPV signal size of strip reduced by more than half: ~130 mV (AC-LGAD) compared to 300 mV (DC-LGAD)



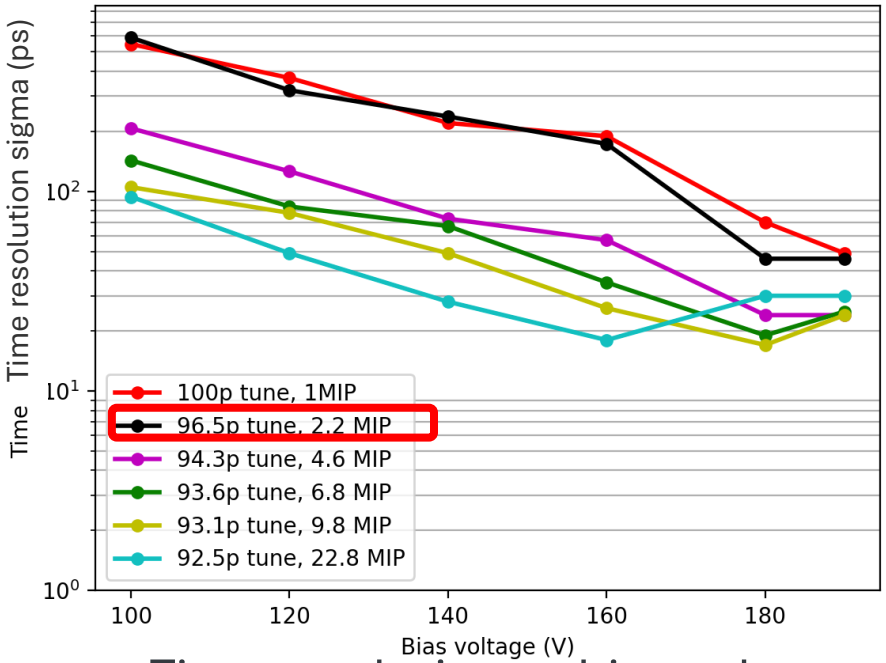


Testing with IR-laser

- Verified with IR-laser that if we correct the signal size to match MIP, performance is recovered
  - Observe around **~40-45 ps** for input signals of around 1MIP (2MIP laser intensity)



signal amplitude vs bias voltage



Time resolution vs bias voltage

Deriving sensor specifications

- We proposed to use this specific HPK sensor, with its design and measured RC-properties as the specifications to optimize the FCFD v1.1
- We also defined the input charge, dynamic range, and required amount of charge sharing
- These specs were presented and agreed within the Electronics and barrel TOF groups
  - **Hamamatsu 1 cm long strips, 50 µm thick sensor**
  - **500 µm pitch, 50 µm wide metal strips**
  - **Sheet resistance 1600 Ω/square**
  - **Dynamic range:10 - 70 fC**
  - **Signal MPV : 25 fC**
  - **Jitter at MPV : around 20 ps**

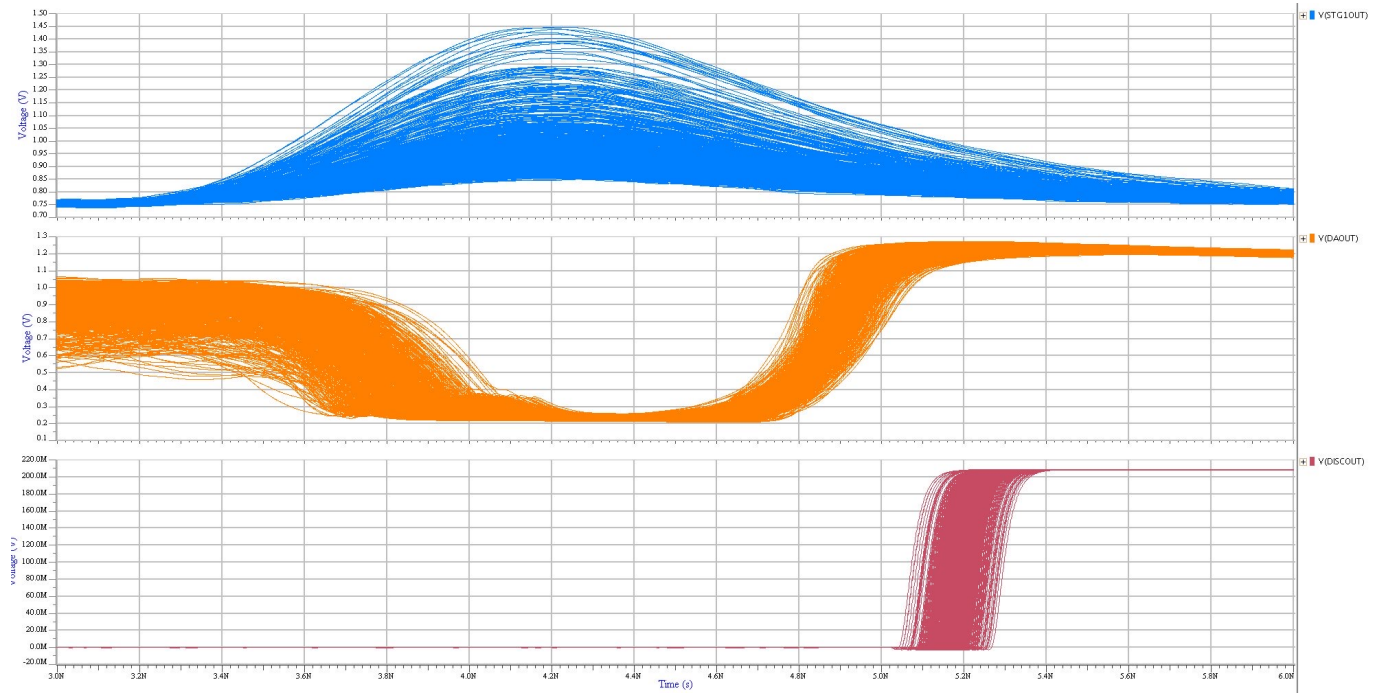
Re-optimization of the FCFD

- Based on the sensor specs on previous page, we designed a new version of the CFD chip, FCFDv1.1
  - Optimized the pre-amp, and arming comparator

- Three power settings tried during the optimization of v1.1:
  - In high power mode:
    - Doing transient noise runs with the 1000 LGAD pulses gives a jitter of 31.9 ps
  - In low power mode:
    - Transient noise runs with the 1000 LGAD pulses gives a jitter of 33.1 ps
  - In very low power mode
    - Transient noise runs with the 1000 LGAD pulses gives a jitter of 35.1 ps

Simulation results

- Using 1,000 LGAD simulated signals
  - With transient noise added in the simulation
  - Signal MPV simulated to be 20 fC
  - The jitter on Discriminator output is of 33.1 ps



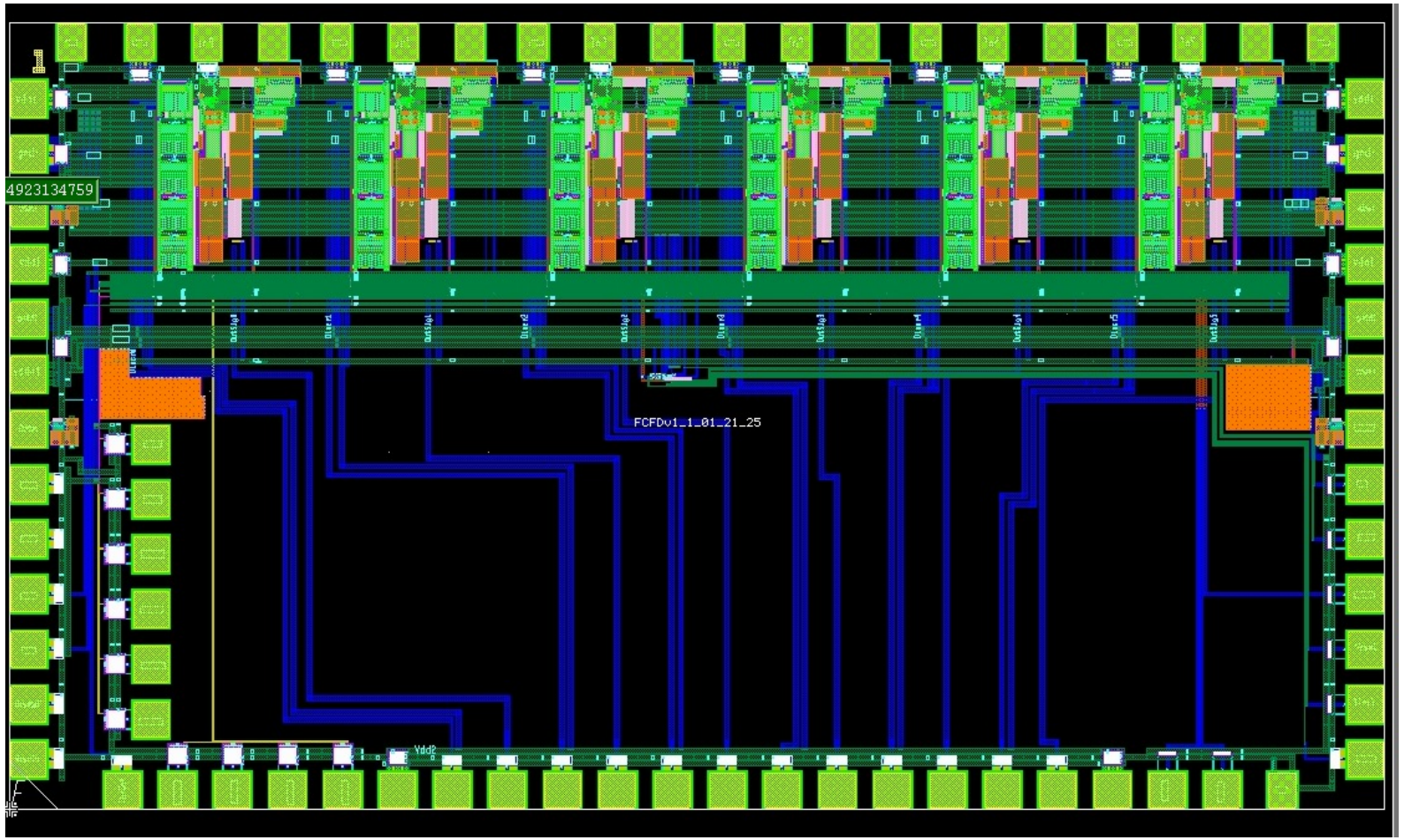
Stage1 output

High Gain Diffamp output,

Discriminator output

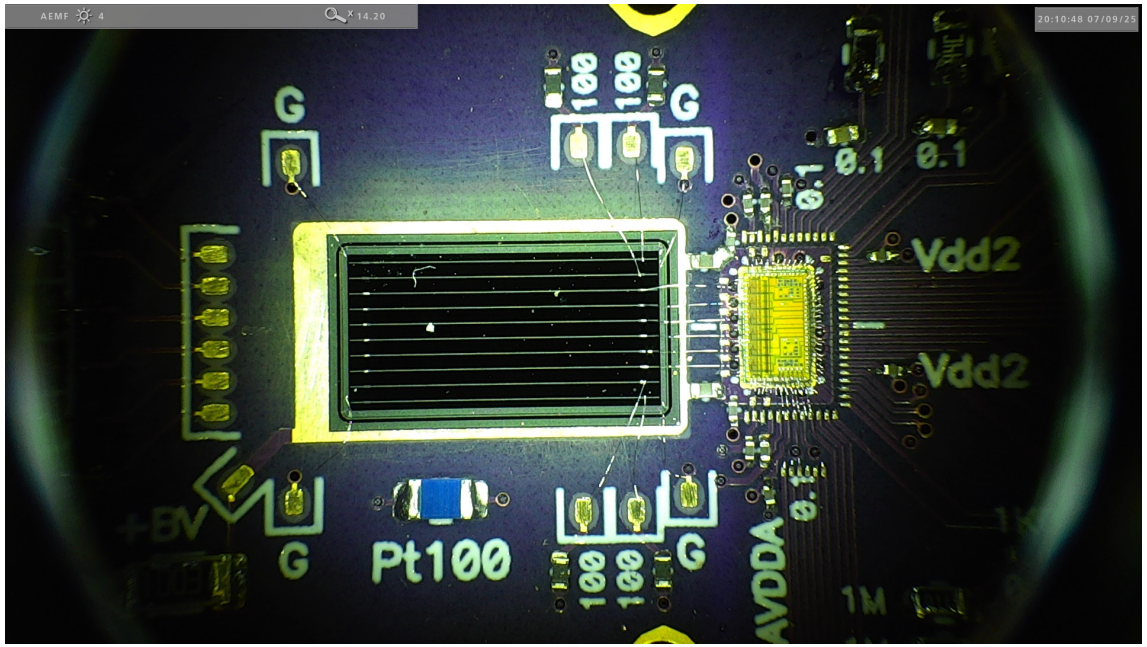
FCFDv1.1 ASIC design

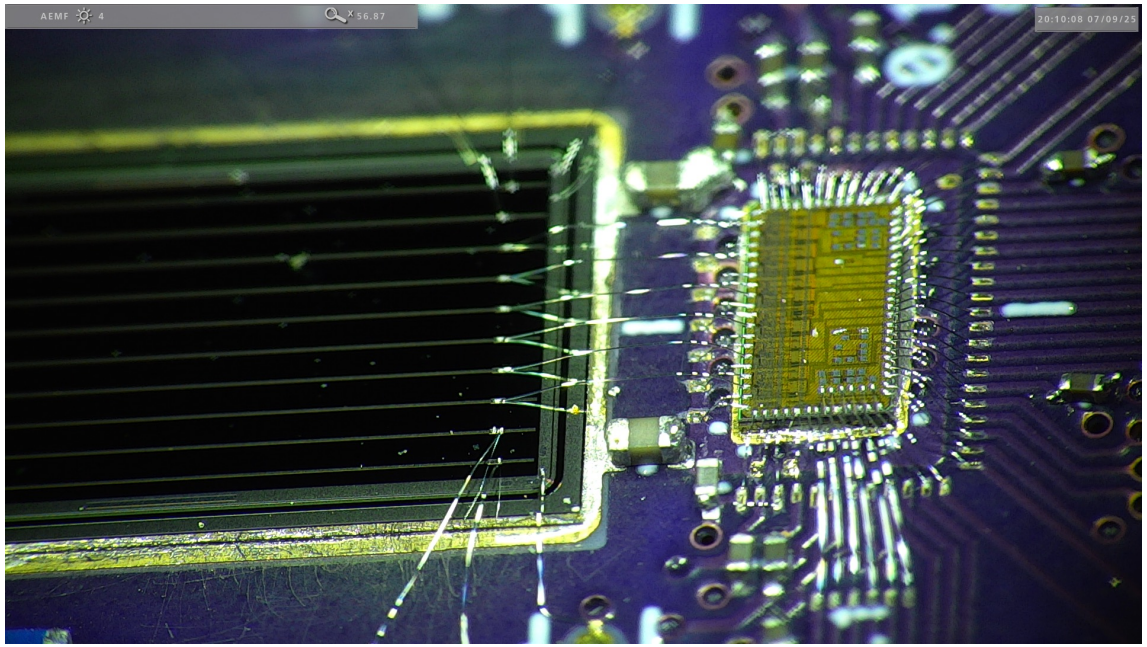
- The design was completed, and chip **submitted on Feb 19, 2025**



FCFDv1.1 status

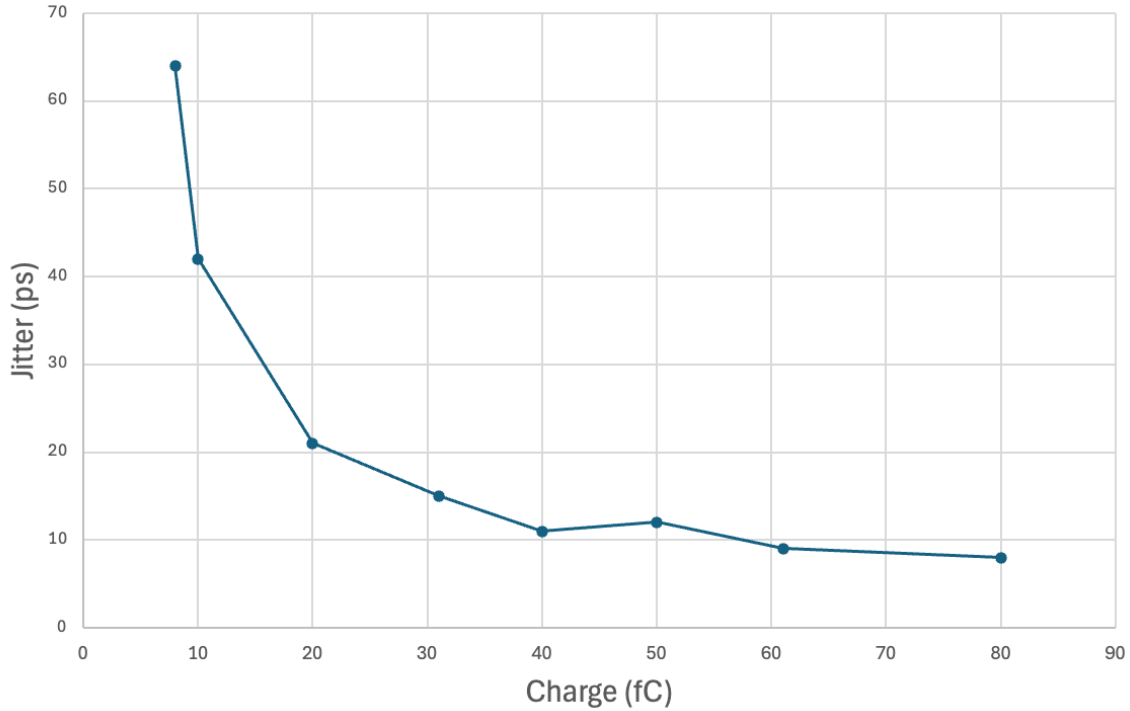
- Chip was received in Fermilab in June.
- Mounted on testing board and testing started immediately
  - Wirebonded to a HPK 1-cm strip sensors, 6 strips connected
  - Sensor specs as we agreed in the previous presentations





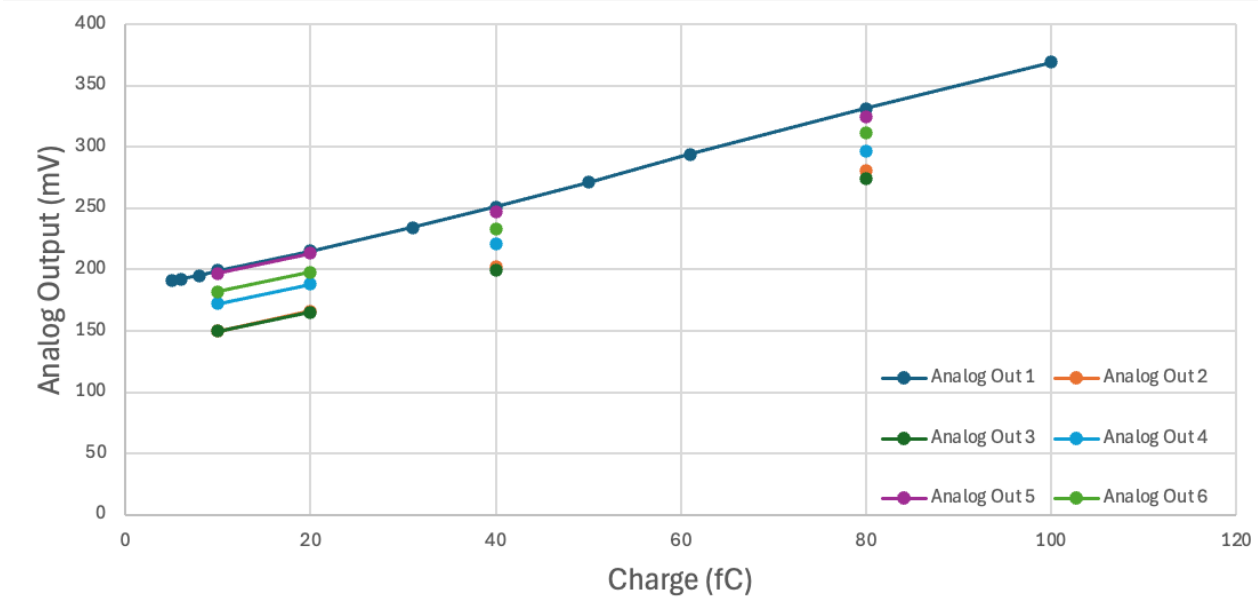
Preliminary results

- Charge injections measurements
  - No anomalous noise that was observed in the previous version!
  - Tunable arming comparator, and CFD threshold work well
  - Jitter measurements consistent with simulation and the specs
  - All channels behave well and consistent among with each other



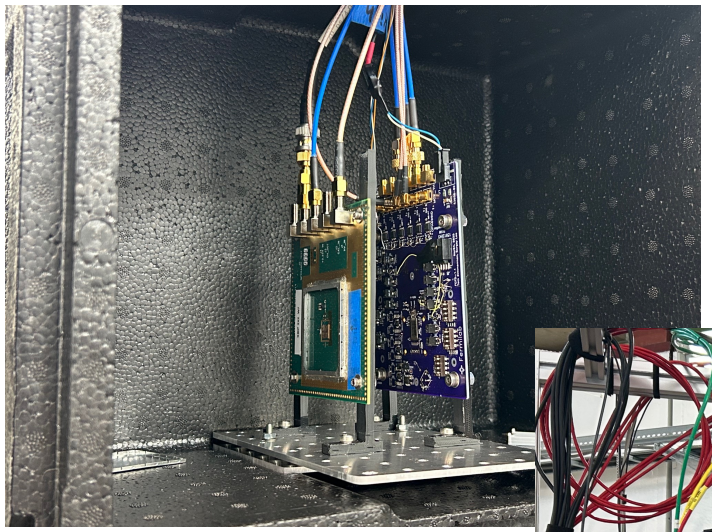
Preliminary results

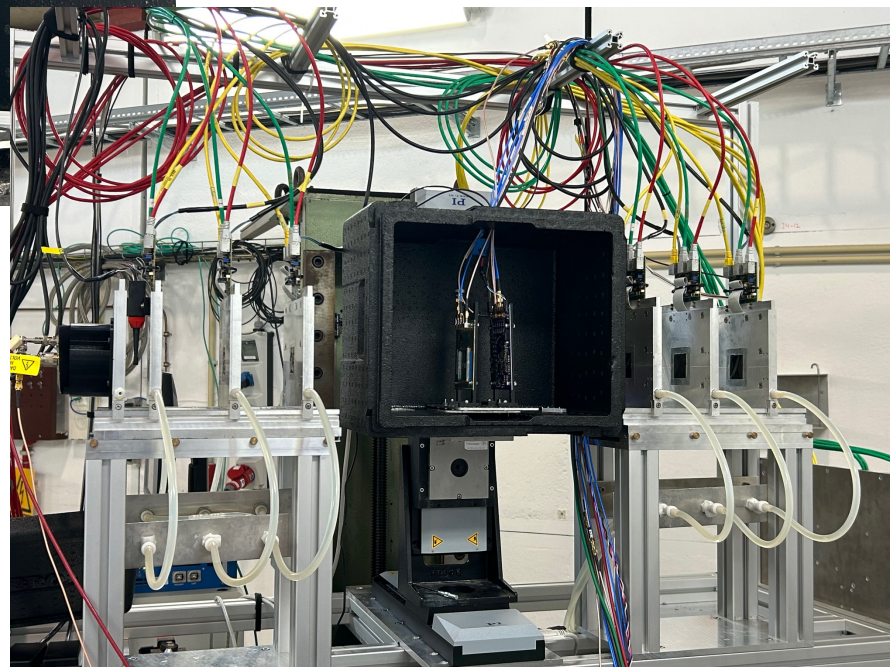
- Charge sharing
  - Injected 80 fC in Ch2, measure signals in Ch1 and Ch3
    - σ_1 and σ_3→ 32 ps, σ_2→ 9 ps
    - Measured analog signal about 20 fC to Ch1 and Ch3, as expected
- Analog output measurements all channels behave as expected, performance very linear in the range



Preliminary results

- Installed the board in the laser setup
- Prepared 3 boards to be taken to DESY test beam this week





DESY test beam this week:

A. Apresyan, S. Wu, Z. Ye, T. Zenger

Towards the full readout chip

- We recently started working towards the full readout chip

- Team of physicists and engineers working on the design
  - Physicists: A. Apresyan, C. Pena, S. Wu, S. Xie, Z. Ye
  - Engineers: C. Gingu, D. Gong, J. Hoff, N. Kharwadkar, S. Los, C. Syal, T. Zimmerman

Timing and Position Resolution Specifications

- Let's review the components that go into overall timing:
  - $\sigma_T^2 = \sigma_{LGAD}^2 + \sigma_{Internal\ Clock}^2 + \sigma_{System\ Clock}^2 + \sigma_{TDC}^2$

Component	Spec
σ_{LGAD}	~40 ps
$\sigma_{Internal\ Clock}$	< 10 ps
$\sigma_{System\ Clock}$	< 10 ps
σ_{TDC}	< 10 ps
Total	~ 45 ps

- Time resolution **$\sigma_T \sim$ 45 ps**

- Position resolution:
  - 30 μm in polar angle**: is an 9-bit ADC for amplitude measurement sufficient?**

Total power

- Target power per channel:

Circuit Component	Power per Channel [mW]	Power per ASIC[mW]
Preamp + Discr (low-*high power*)	2.1 - 3.8	269 - 486
TDC+ADC	0.2	26
Supporting Circuitry	0.2	26
Global Circuitry		*200**
Total (*high power*)		521 - 738

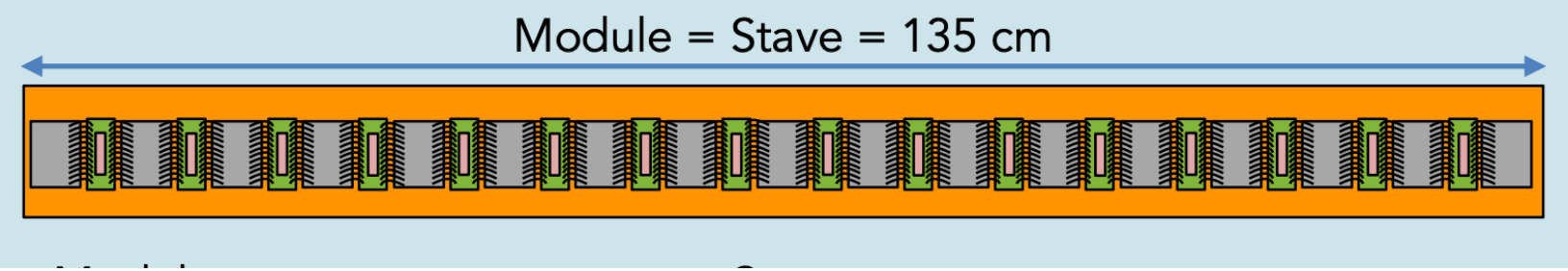
Assumptions : FCFD is 128 channels

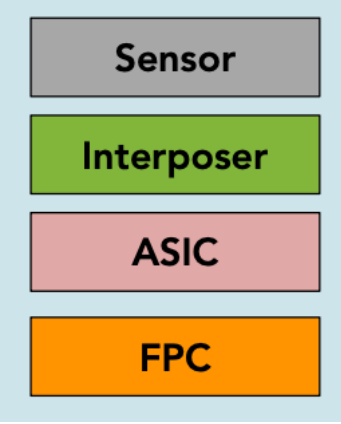
*** Based on ETROC, may be an overestimate**

- Total power:
  - The estimate above : **9.8-14 kW**
    - As a reference ETROC (3.4 pF per pixel) power for Preamp + Discr: ***1.9-2.4 mW***
    - Much smaller capacitance in ETROC, while about the same power consumption!

Physical interfaces and constraints

- Each sensor has 64x2 sets of strips, with 500 µm pitch
- Constrain from the system-side is to use single data line per sensor
- The dimensions of the Interposer are not clear yet: **seem to be around 1-2 cm?**
- **What is the distance between ROCs and lpGBT?**
  - **How far do the data need to be transmitted?**
  - **The transmission lines need to be carefully designed**
- **Current plan is 1VTRX and 4 lpGBT per stave?**



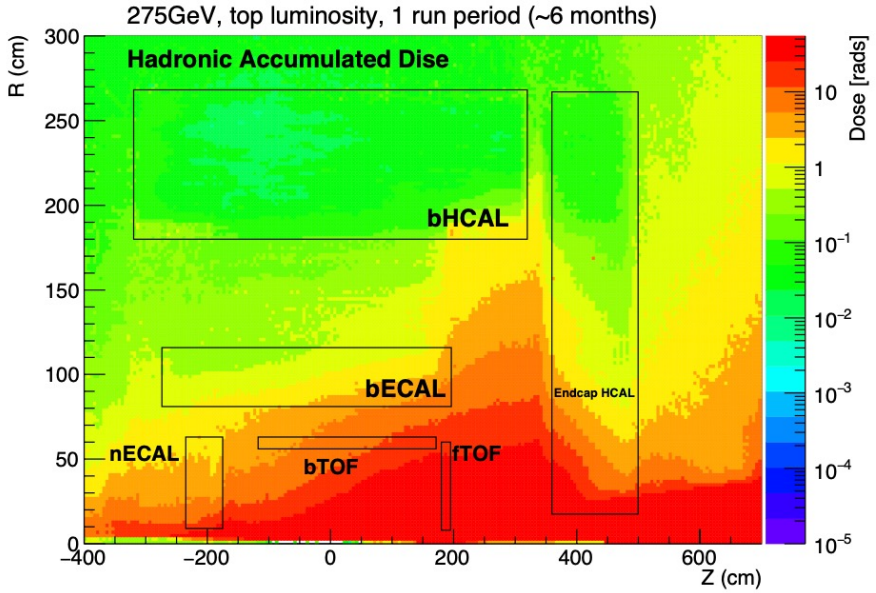


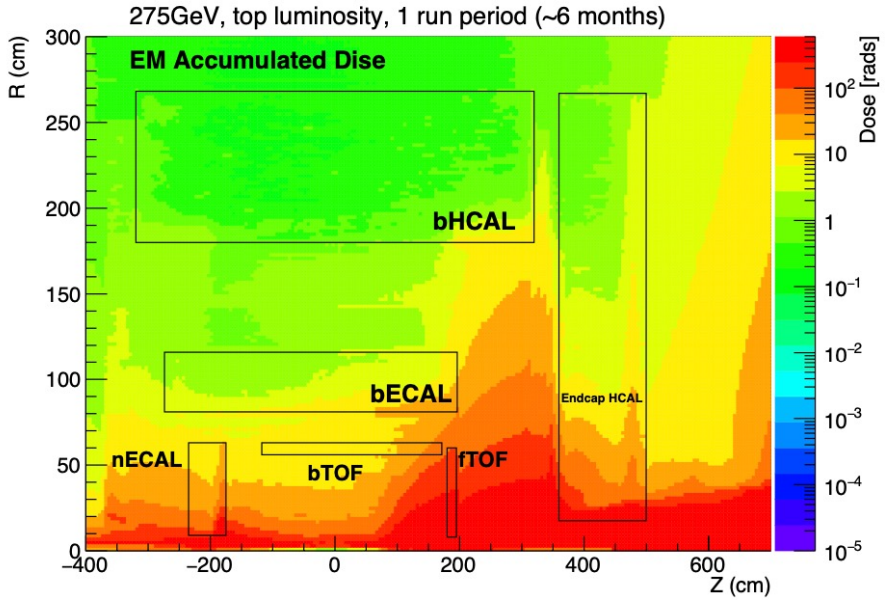
Physical interfaces and constraints

- Signal occupancy: **O(10) Hz per channel**

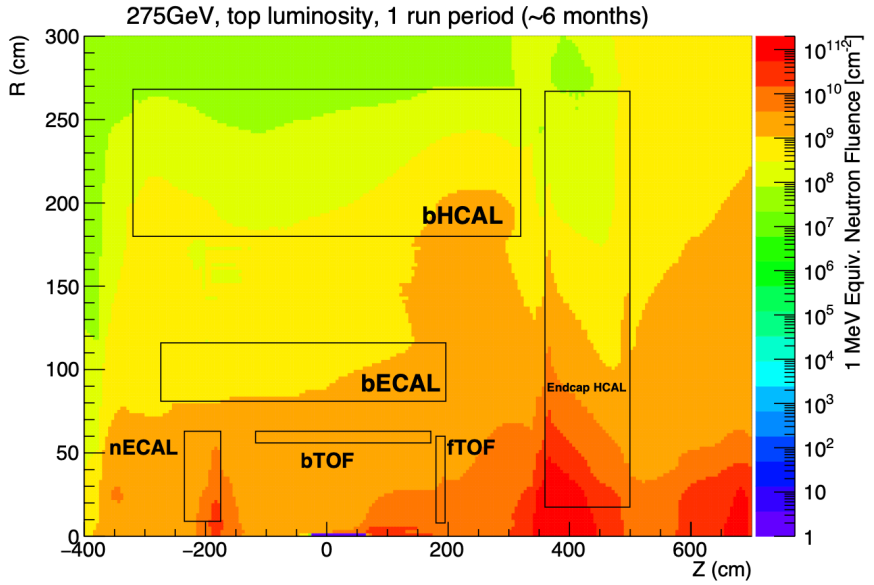
- **Voltage and current requirements**
  - **Need 2.5 and 1.2 V voltages for the operation of analog**
  - **Need 1.2 for digital**

Radiation environment

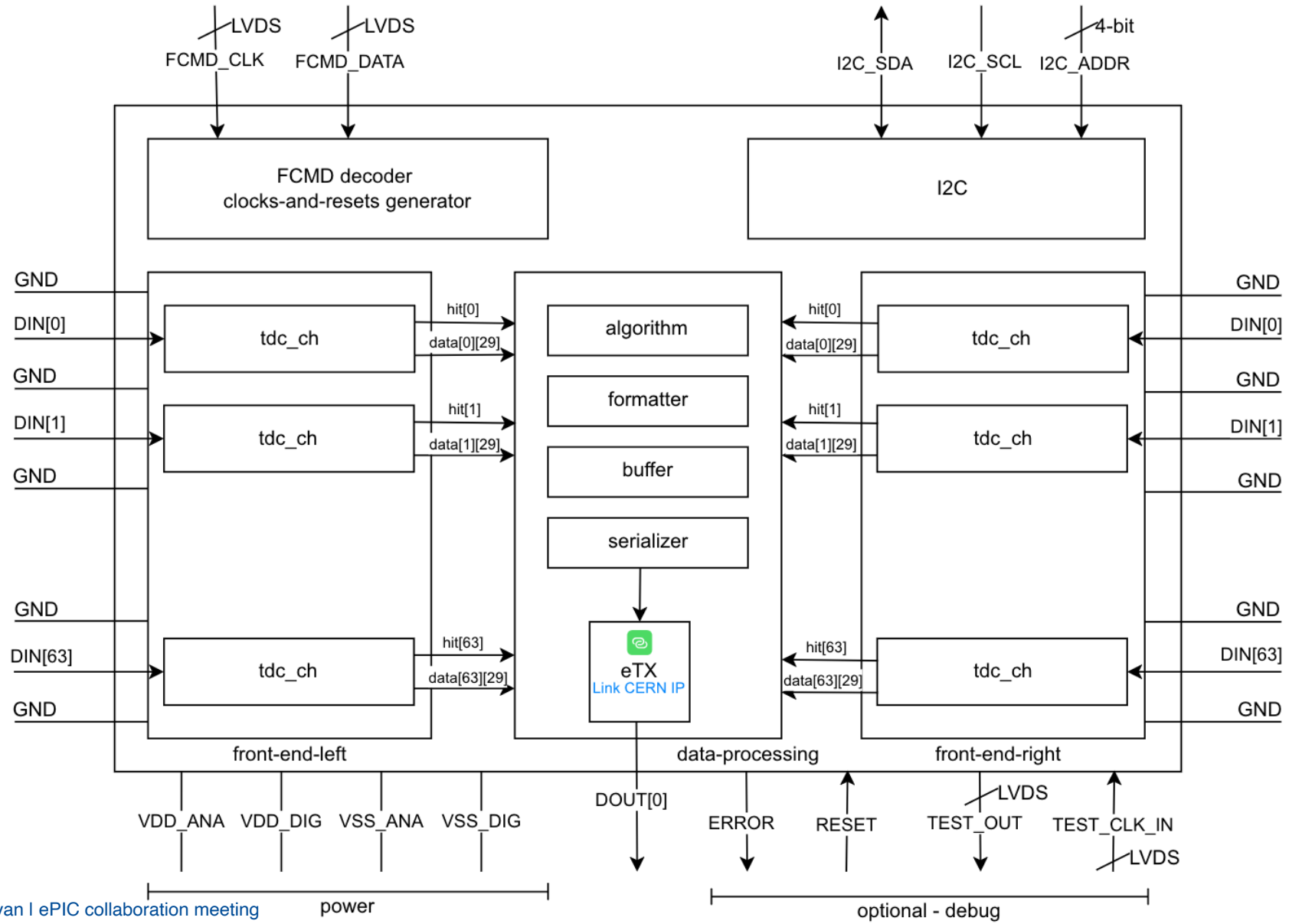




- Radiation environment after 10 years of running (plots show the sum of collision and beam + gas)
  - **TID: 1 krad**
  - **1 MeV neutron: 3×10^{10} n_{eq}/cm^2**



Preliminary block diagram



Status of various blocks

- TDC
  - Needs to be redesigned starting from ETROC version.
    - However, ETROC TDC is only active for ~12 ns.
  - For FCFD, we need to have TDC active at all times.
  - Will be designed as a fully digital module that can be easily verified
- I2C
  - Will reuse/adapt from ECON, using CERN IP module
  - Can have up to 16 FCFD per I2C bus
  - The 7-bits I2C chip address assignment on I2C bus is done like this for ECON-T/D
- Readout
  - Take as much as possible from ECON for CMS HGCal

Anticipated timeline

- Optimization of the analog front-end to reduce footprint, and add ADC
  - Estimate around 2-3 months
- Design of the TDC and FCD
  - Estimate around 2-3 months each, total ~6 months
- Design of the I2C
  - Estimate around 3 months
- Produce a small test chip to verify design changes and testing
  - Small chip will test the new front-end and new ADC, new TDC
  - To be submitted **by the end of 2025**

Anticipated timeline

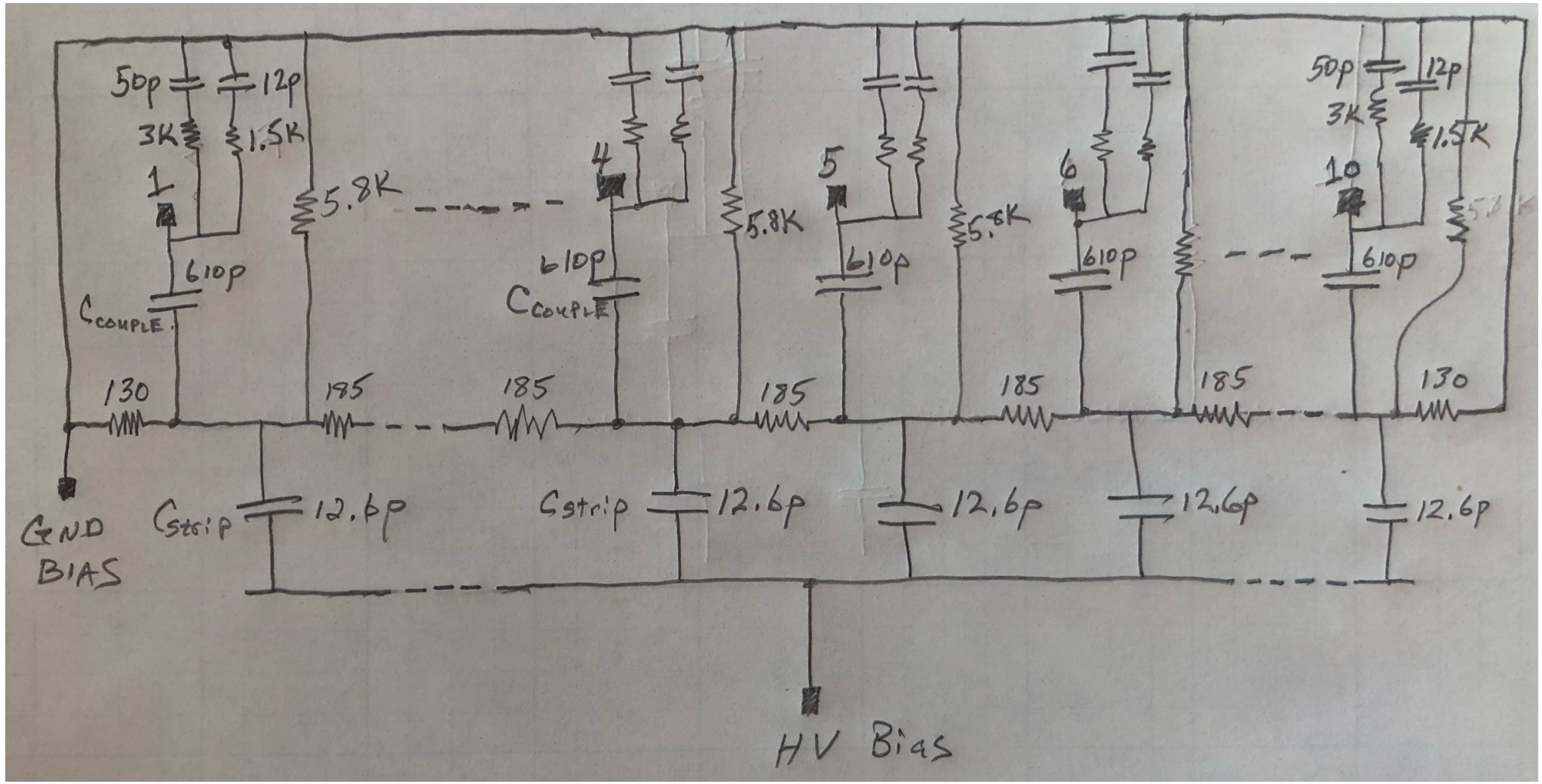
- Design of the clock and power distribution
  - Estimate about 2-3 months
- Readout
  - Estimate 5-6 months
- Integration and Verification:
  - Estimate about ~6 months, will go in parallel as blocks are developed
- Submission of the first prototype full chip : **around 10-12 months**

- Proposal is to design a 32-channel prototype as a next version
  - First full ROC, with many new components
  - Demonstrate all components of the chip, power and clock distribution, overall performance
  - Can be tested with the full system, build modules, integration, etc
  - An economical solution which allows to test most of the main questions

Summary

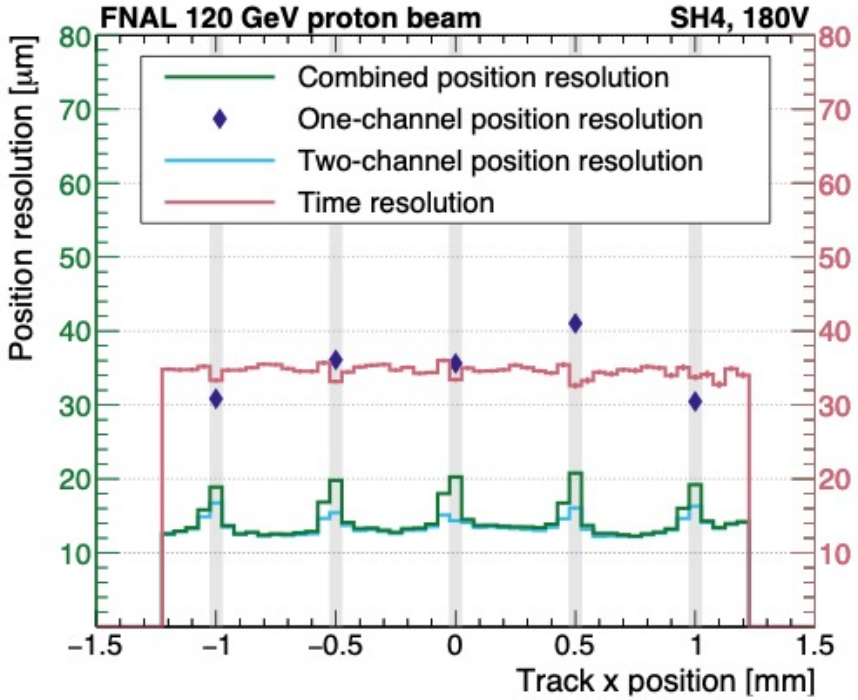
- Design of the readout chip for the AC-LGAD strip sensors for bTOF is well advanced
- Strong, experienced team has been assembled, we are working now towards the next version of the chip
- We need to specify performance parameters, and fix interfaces to the rest of the system
  - Working on the specifications and interfaces document, we should review them with the group

Measurements of AC-LGAD sensors parameters

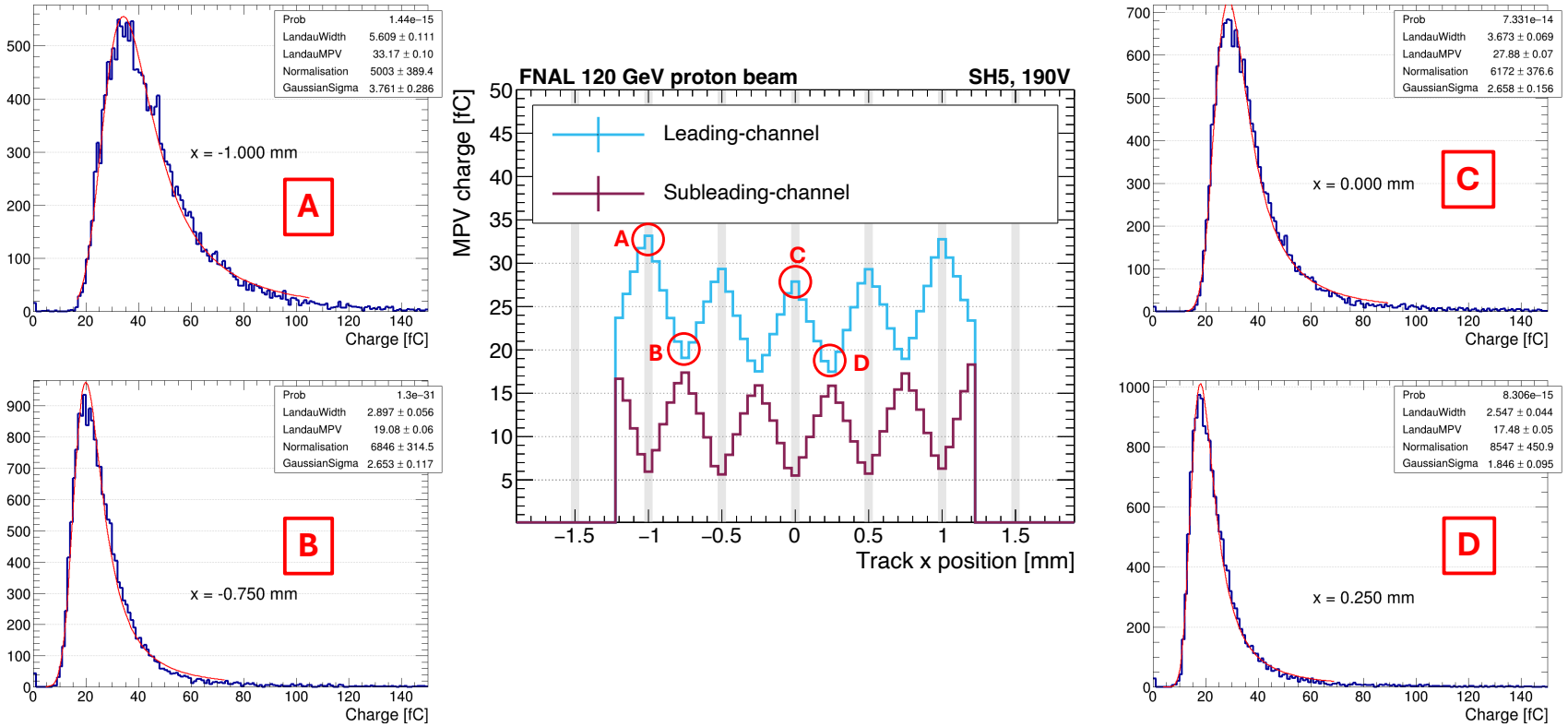


Time resolution measured in test beam

- Time resolution is measured by combining leading and sub-leading channels
- Measurements performed on dedicated readout boards using commercial amplifiers and with full waveform analysis
- More details in the paper: arXiv:2407.09928



Signal characteristics



- Signal characteristics that went into plot on previous page
  - Dynamic range:10 - 70 fC
  - Signal MPV : 25 fC
  - Jitter at MPV : around 20 ps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