BTOF FPC and Interposer

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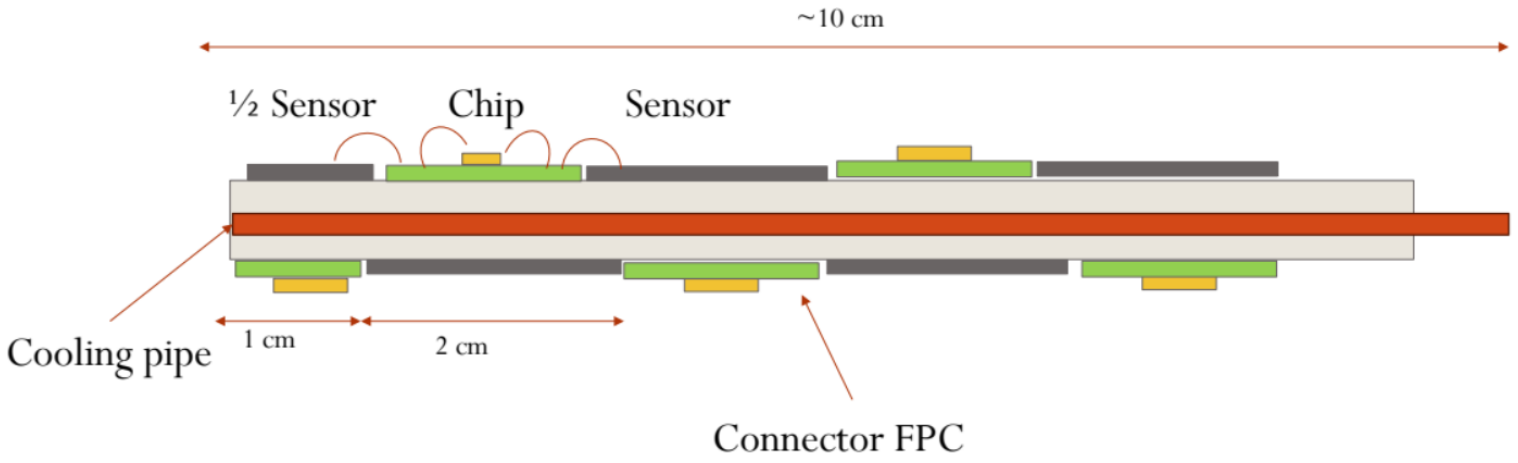
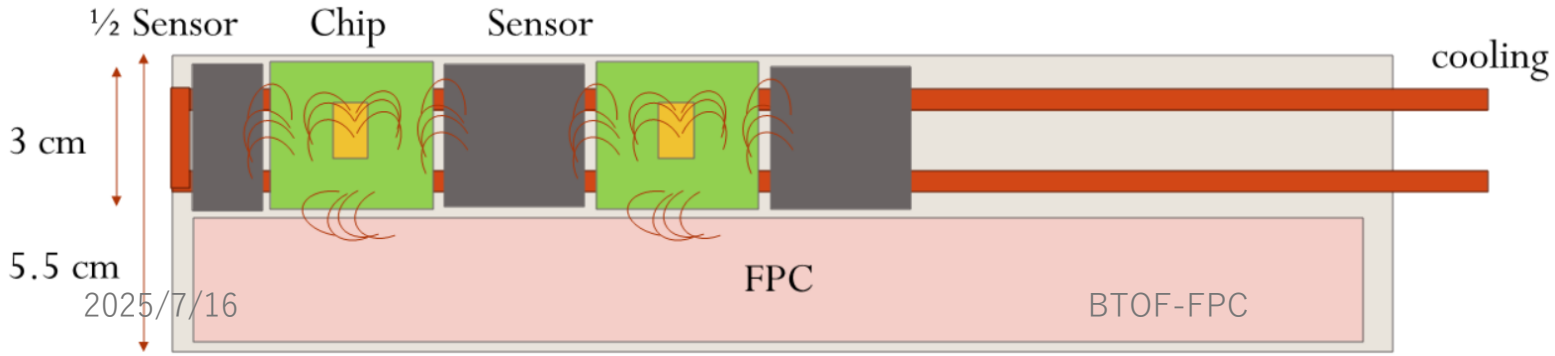
ePIC collaboration meeting

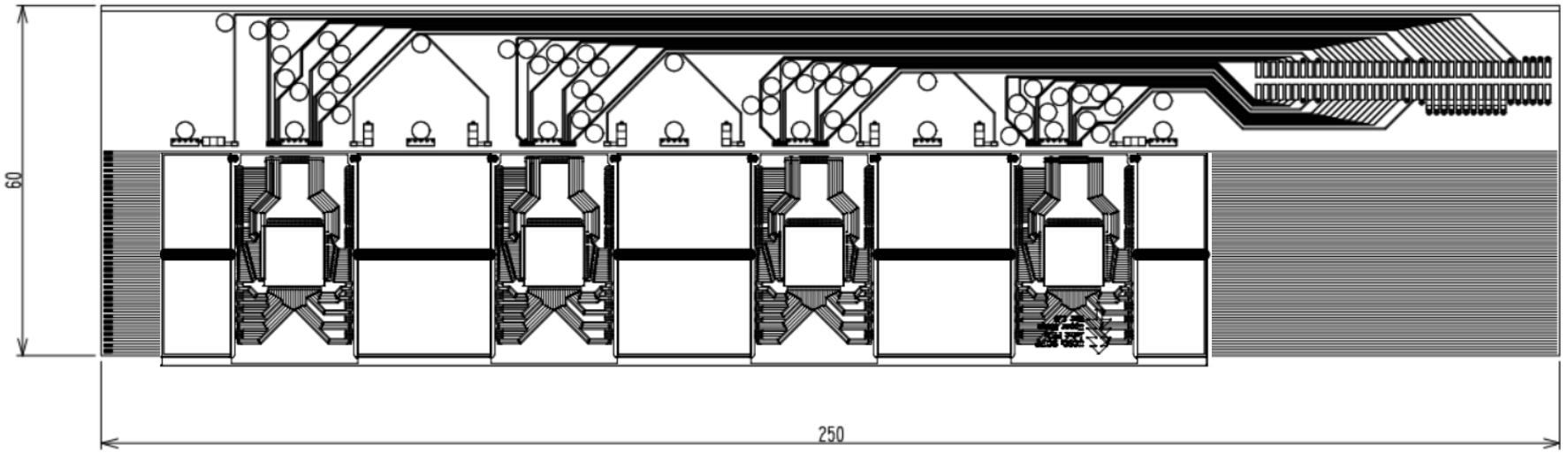
FPC for the demo-project

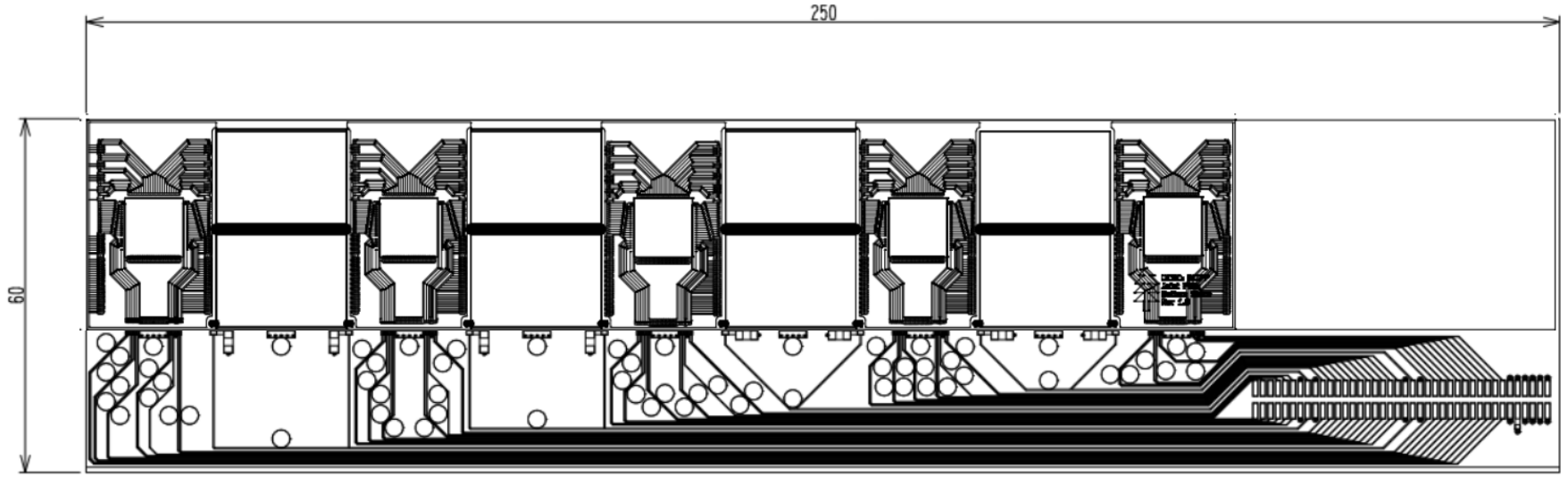
- Ladder design: Sensor/ASIC/FPC at both sides
- Demo project Goal: build a thermo-mechanical stave demonstrator to:
  - Test assembly procedure
  - Test thermal proprieties of the stave, e.g. temperature gradient





FPC design w/ test pads (and lines under the interp.)

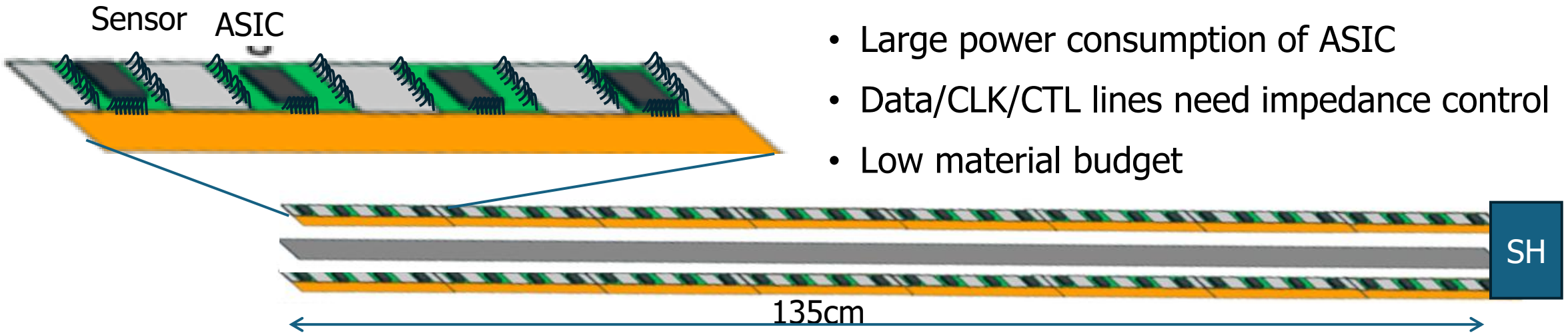


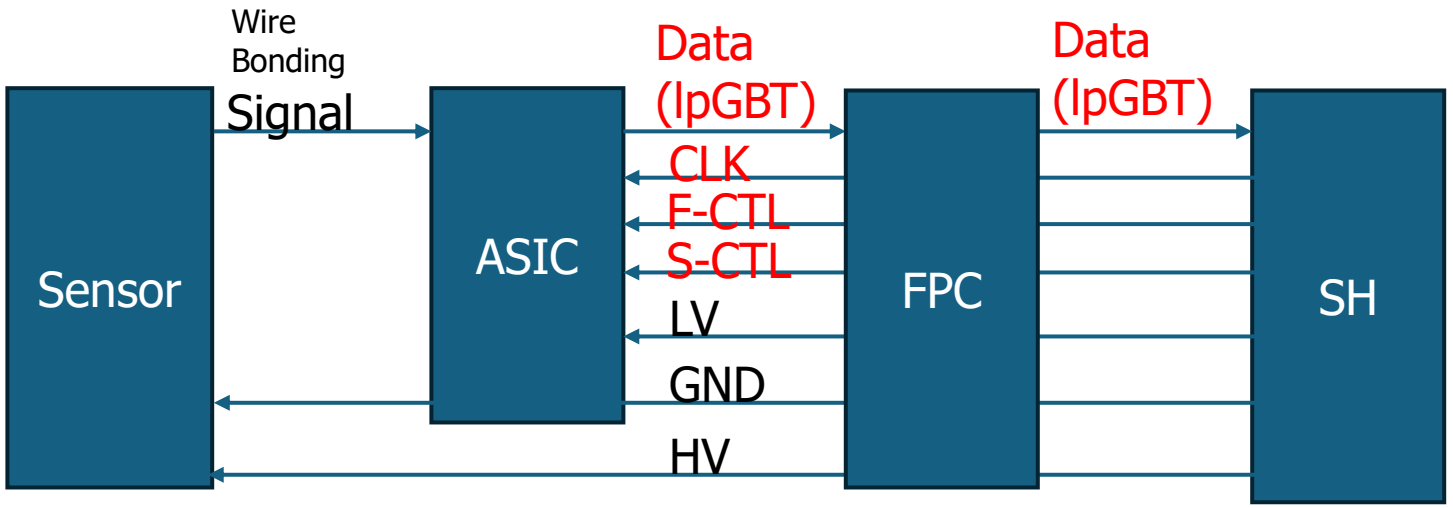


- FPC has 2 layers (top/bottom)
  - HV, signal lines at top
  - GND plane at bottom
- All lines lead to the connector at the side
- HV and GND has pads for the bypass capacitors.
- Test pads as much as possible
  - TPsize = 3mmϕ
  - See next page which ch has TP
  - Adding TP for GND around the connector since
- Thick bonding pads for wire bonding: 6um
- Will be delivered by early Aug.
  - 5 FPCs for each were ordered

Recap : B-TOF ladder structure

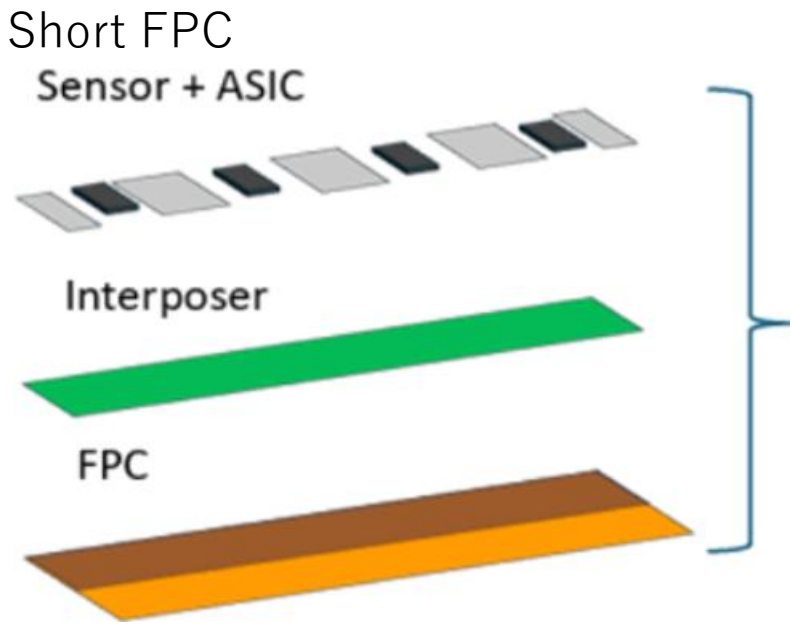
- Long FPC, both side
- Large power consumption of ASIC
- Data/CLK/CTL lines need impedance control
- Low material budget

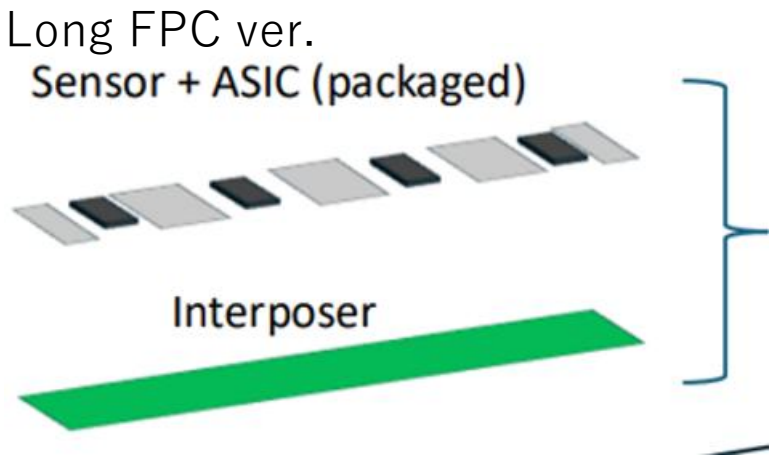




FPC and interposer is technically challenging

Module

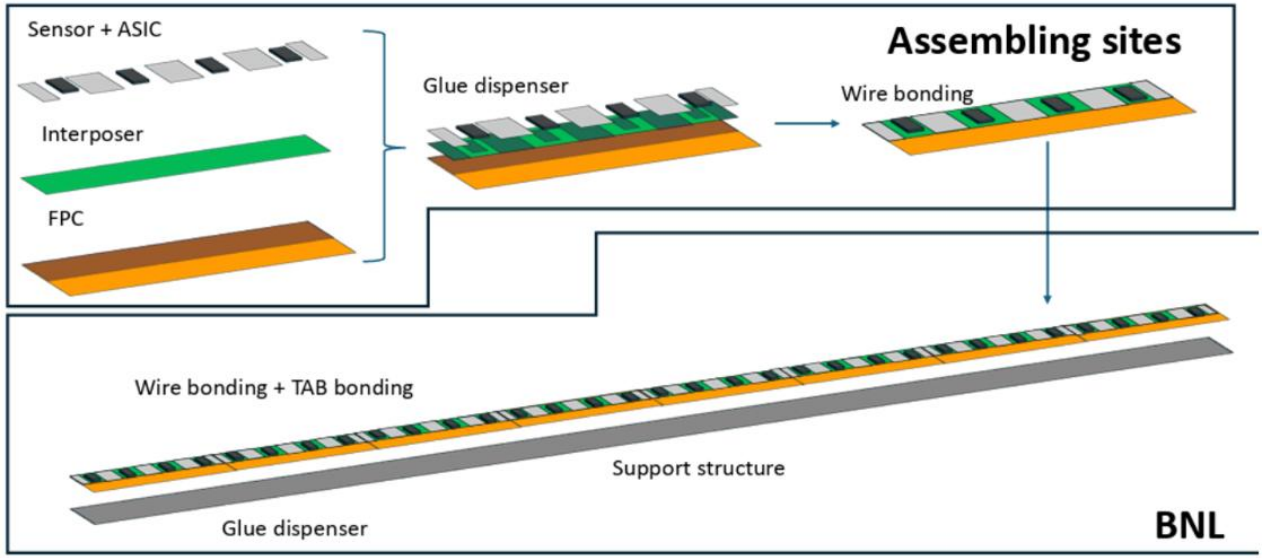


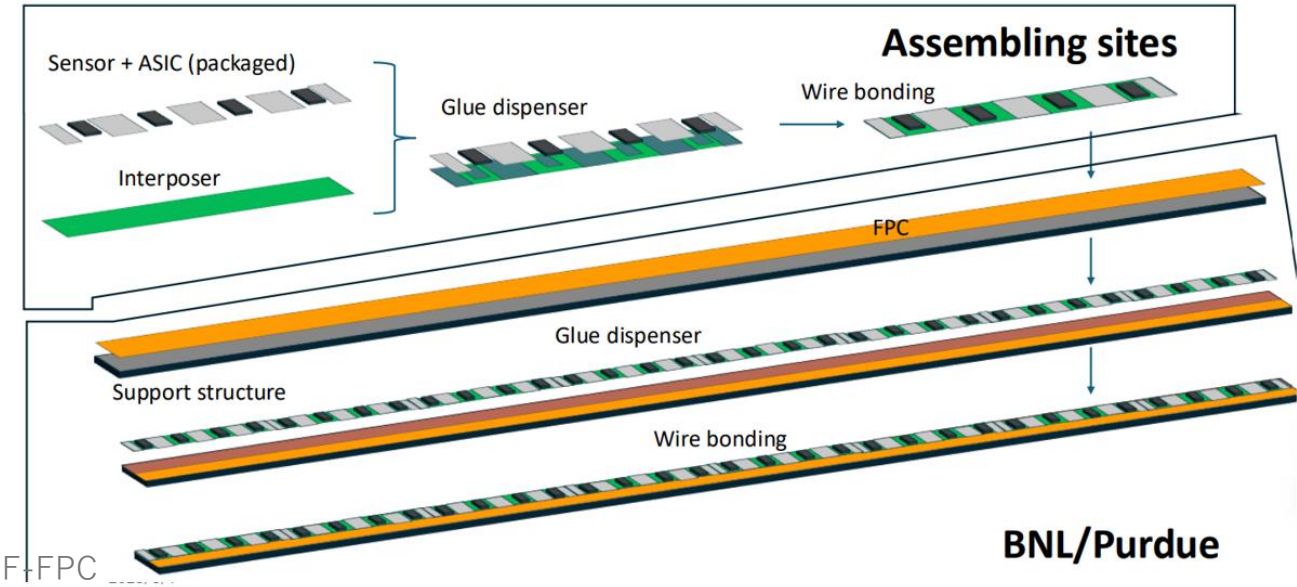


- Sensor + ASIC on interposer (+ FPC) is built as a module
  - The interposer is expanded under the sensor
  - Good for heat spread through Cu layer in FPC
  - Additional but small material under sensor(if a few Cu 10um = 0.07% X0)

Things to make very long FPC & interposer

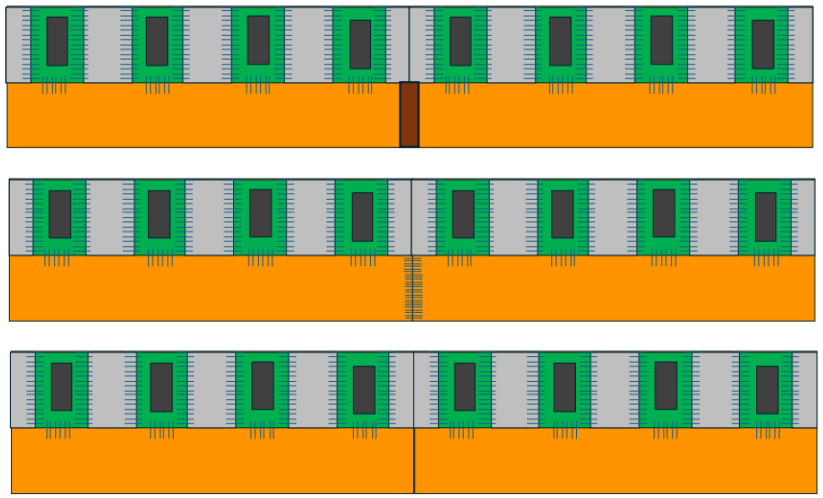
- **Length : 135cm x 6 cm**
  - The structure is similar with INTT's bus extender (max 130 cm), ATLAS-ITK FPC (135cm)
  - How to make it?　Is it feasible?
    - One large FPC? Connecting short FPC?
    - If connected, how? What about TAB bonding?
    - If long, can we make it?
- **All in FPC**
  - Signal lines/HV/LV/GND in FPC
- **N signal lines in FPC?**
  - Depends on ASIC, ~200 lines from 32 ASICs ?
  - N layers of FPC？, Based on our experience from the INTT, signal layer should be one for the yield rate
- **Signal transmission quality**
  - 640Mbps by lpGBT-> impedance control necessary



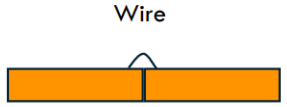


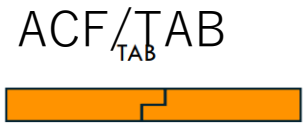
Option 1: Connecting Short FPCs

Module Connection Method

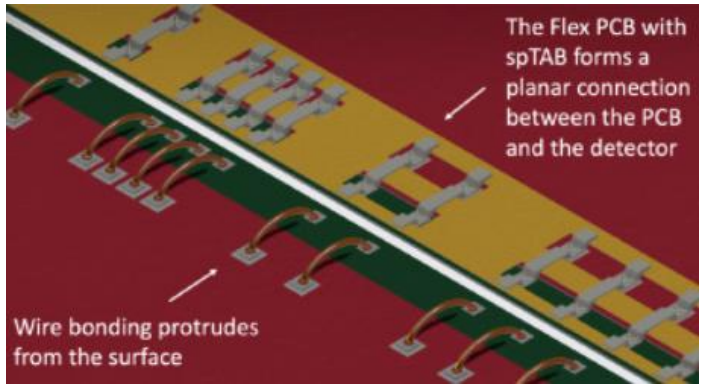


ACF/TAB + mini-FPC

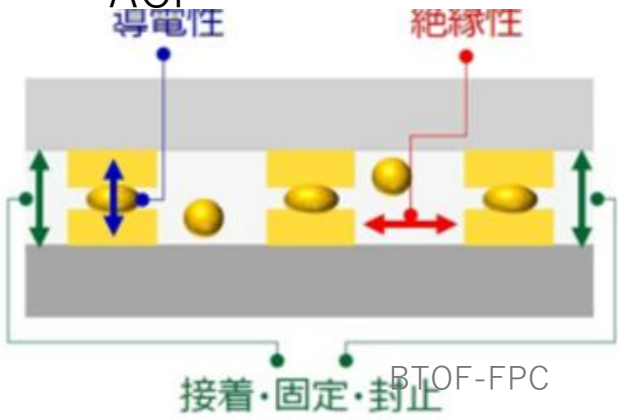




spTAB



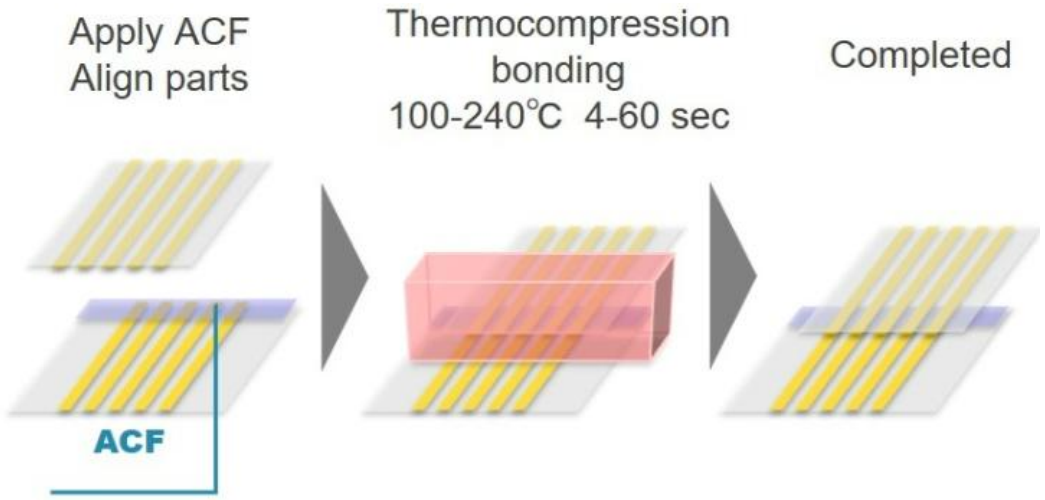
ACF

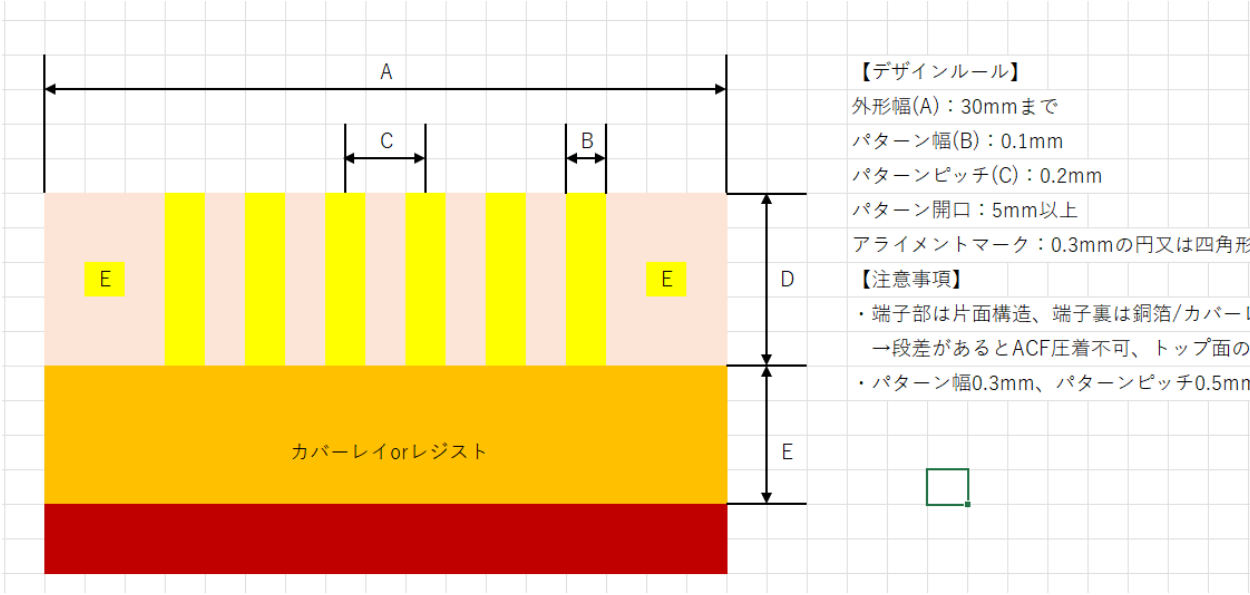


- spTAB, ACF, wire bonding is possible methods to connect FPCs
- spTAB :
  - Widely used but not commercially available (at least in Japanese companies)
- ACF : anisotropic conductive film
  - Some limitations
  - Need more info
- No impedance control at the bonding region
  - Signal quality get worse at each bonding place. Reflection..

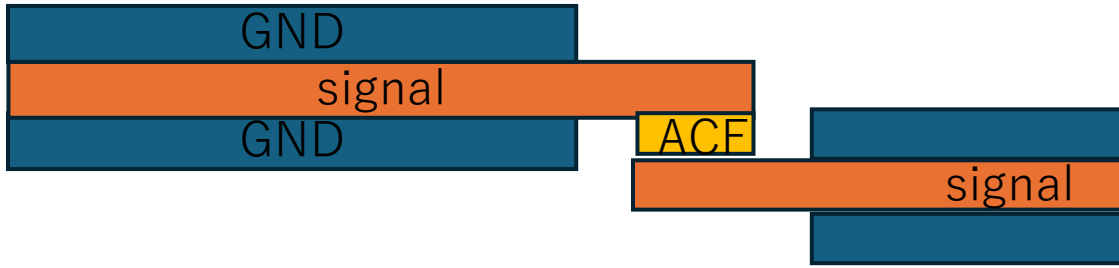
ACF : Anisotropic Conductive Film

- Modern technology to gang bonding (multi-point bonding)



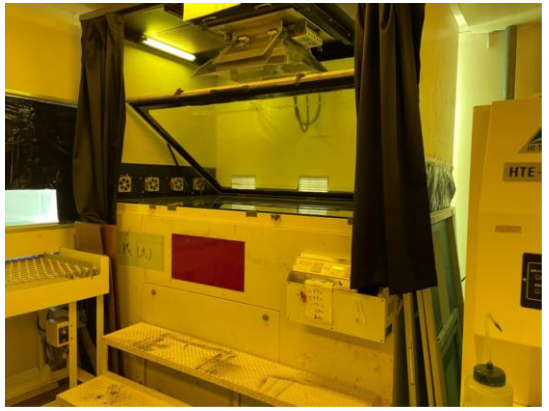


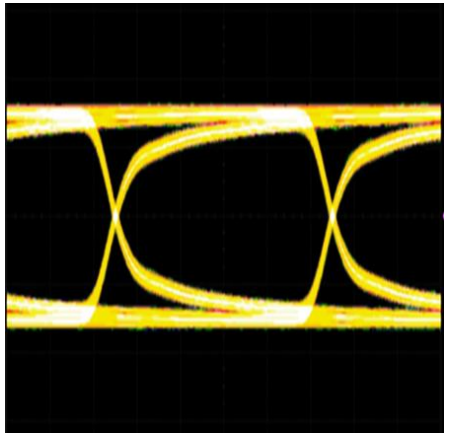
- Several parameter limitations
  - Only single layer supported
    - No impedance control at the connection
  - Width, length : 2mm, 60mm as maximum
    - FPC may shrink by heat/pressure

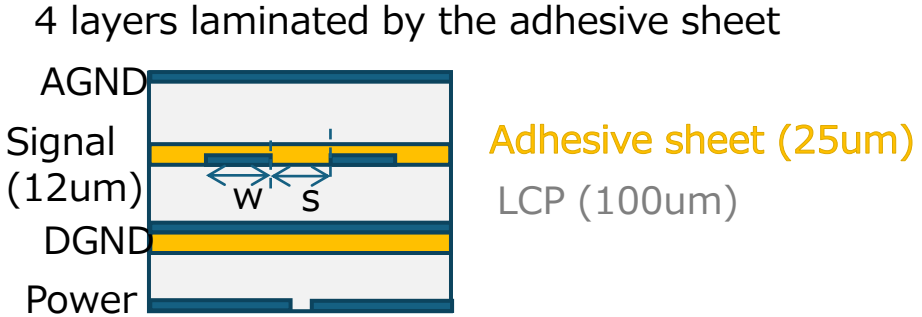


Long FPC

- sPHENIX-INTT experience: 130cm long FPC w/ 4 layers
  - Fabrication is done in Japan
  - Line & Space : 130 x 130 um (min), N-lines: 124
  - FPC width 3.5cm, one signal layer (good for yield rate)
  - QA procedure available

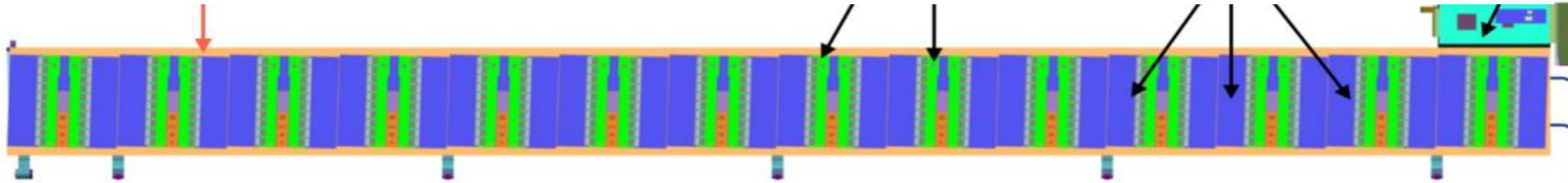




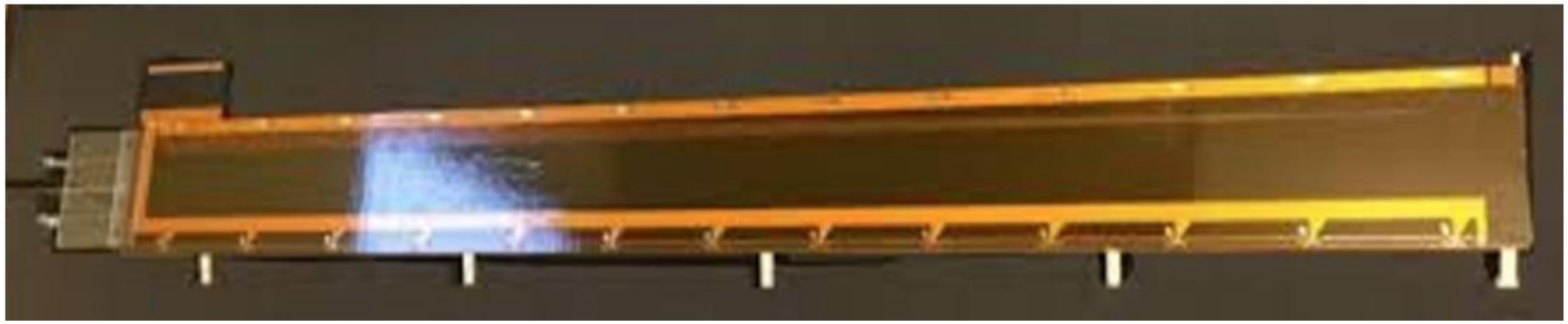


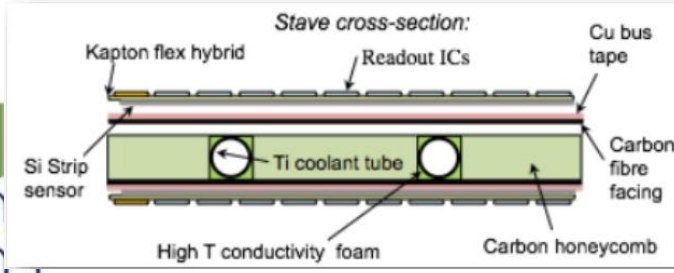
- Our Korean colleague has a fabrication machine for long FPC
  - Smaller line & space available : 100 x 100 um or smaller (70um)
  - They made the machine and a company operated it

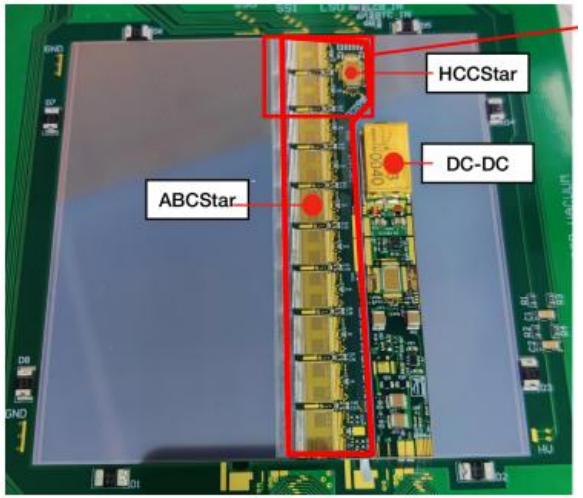
ATLAS ITK bus-tape as reference



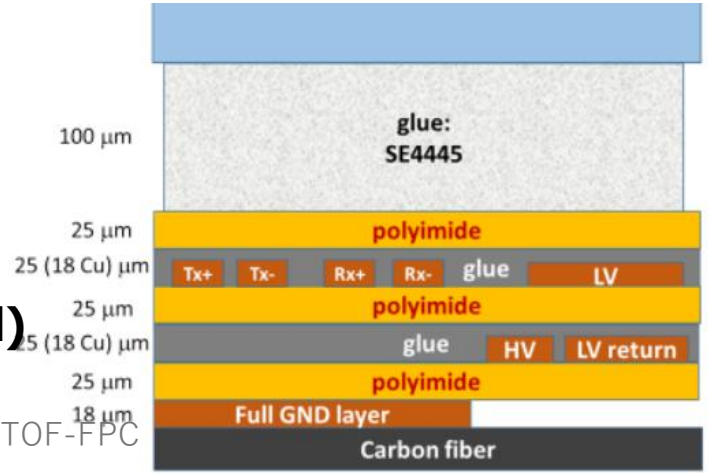
1400 mm

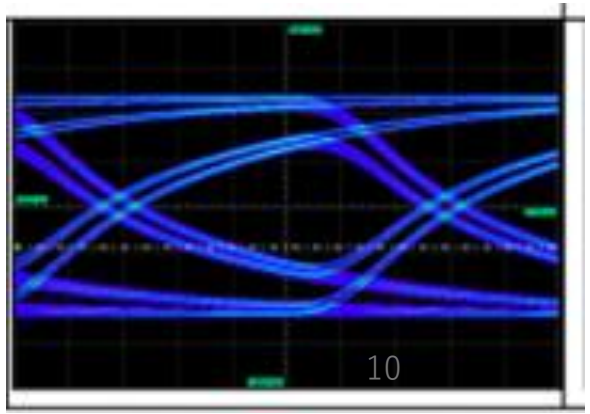






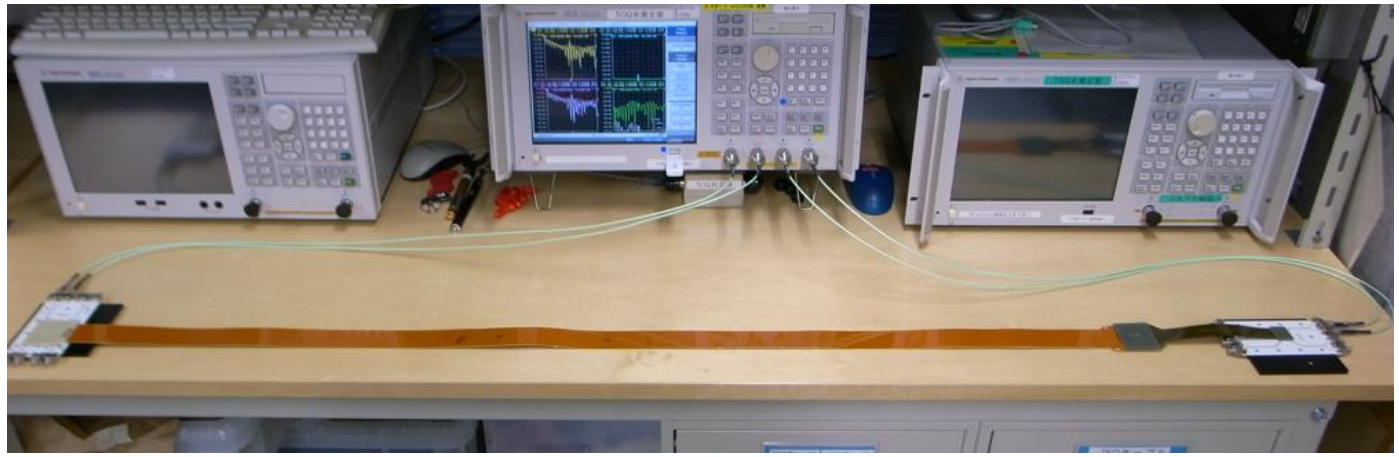
- 1.4 m FPC(bus-tape) is manufactured at CERN
  - **N-lines : 44~** (22~ pairs), lpGBT : 640Mbps
    - Line & space : 100x100um
  - **One signal layer** (good for yield rate)
  - One PWR line
  - **Microstrip line structure(No Cu shield installed)**
  - Similar with BTOF, good to refer it

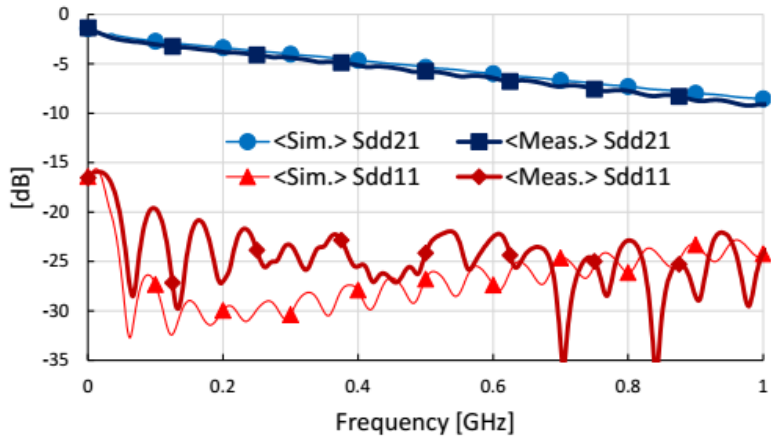


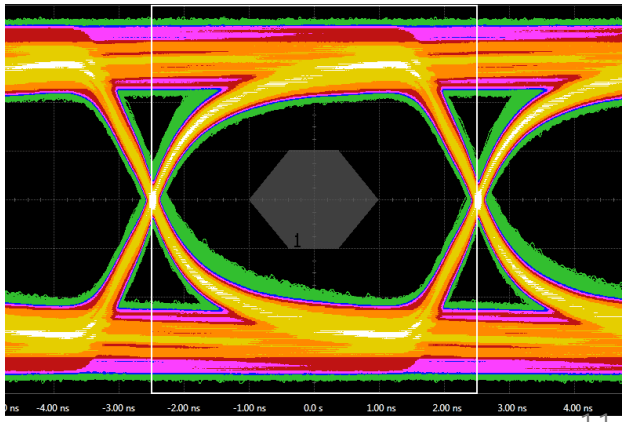


Next for long FPC: Test production

- Our Korean colleague has a fabrication machine in Korea which can make long FPC
  - Long: 1.3m (1.4m?) with INTT-design since BTOF FPC design is not available yet
  - Testing different line & space : 100 x 100 um or 70x70um
  - Measuring S-parameters (Signal loss), TDR for impedance, Eye-diagram
    - Should be similar with the INTT-bus extender
- Measure the transmission loss and other parameters
  - Data rate is faster (INTT 200Mbps -> lpGBT 640Mbps)
  - T-loss at 1000~1500MHz should be checked (300~500MHz for INTT)
  - We have a test equipment for this measurement

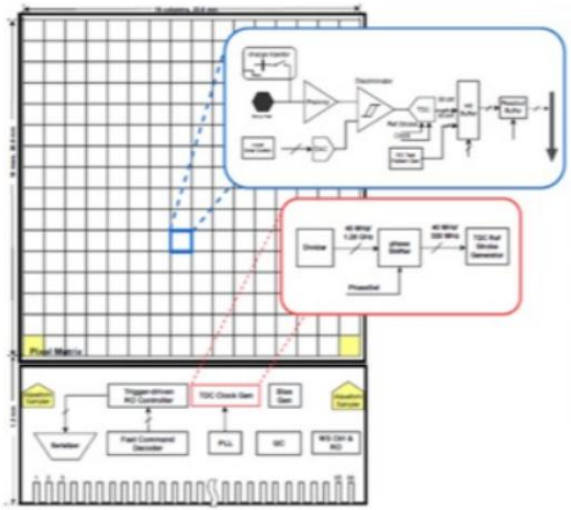




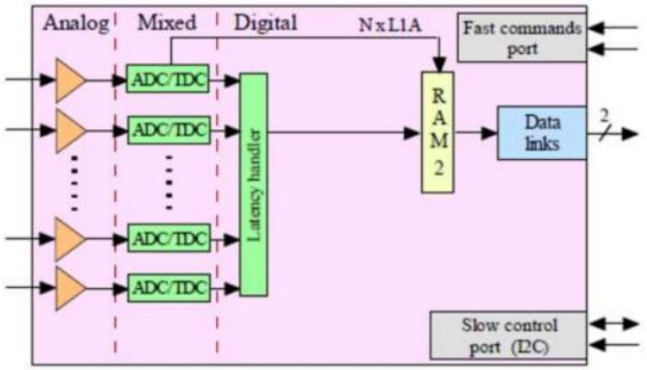


ASIC: ETROC vs EICROC

- ETROC : ROC for CMS ETL (DC-LGAD pixel)
  - Tx: 2x DataOut (DS)
  - Rx: ***CLK40 (DS)***
  - Rx: ***FastCom (DS)***
  - Rx: **I2C**
  - Rx: **RSTn (1 line)**
  - Analog : 1 line (Vtemp)



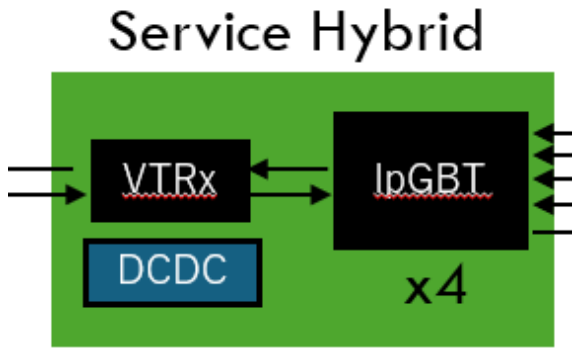
- EICROC: EPIC-FTOF (AC-LGAD pixel)
  - Tx: 2x DataOut (DS)
  - Rx: ***CLK (DS)***
  - Rx: ***FastCom (DS)***
  - Rx: **I2C**
  - Rx: **RSTn (1 line)**



- From the digital part point of view, both ETROC and EICROC have similar N-inputs/outputs
  - 2x DataOut could be reduced to one pair because of small multiplicity
  - Multiple lines can be tied as bus for Fast Com, I2C, RSTn
    - Fast Com = each 4 ASICs, Slow Com= half of ASICs, RST= 1 or 2 for all ASICs
- N-lines for 32 ASIC : Digital ~150, Analog ~ 34 → 180 total

Connecting to Service Hybrid

- Service Hybrid design for BTOF is not started yet
- Connector also depends on the size of SH



Summary

- 25cm FPC for demo-project was ordered and delivered by early August.

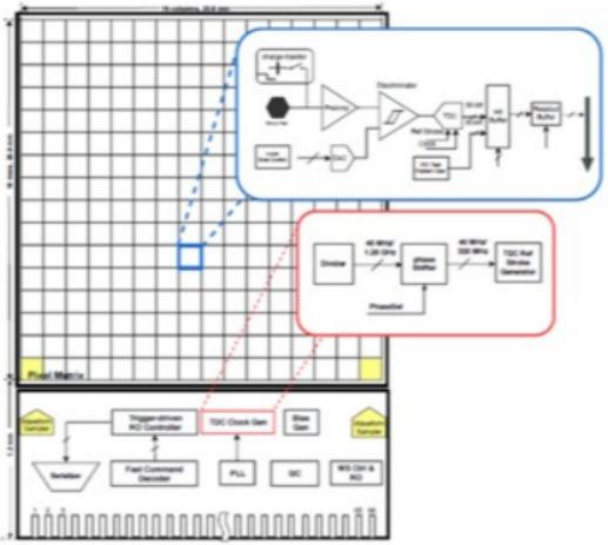
- Long FPC is technically challenging
  - Connecting multiple FPCs is technically difficult. Need more investigation
  - INTT-BEX and ITK-bustape are helpful to design BTOF-FPC.
  - 1.35m long FPC will be made as a test and measure its performance

- Designing the connection to SH is started

Signal lines based on ETROC2

- Size : 21x23mm^2 (Box shape) since 2D for the pixels
  - Bump bonding for pixel (CMS)
- Npads : 124 w/ wire bond
  - CMS Digital lines: 13 lines
    - Tx: 2x DataOut (DS)
    - Rx: ***CLK40 (DS)***
    - Rx: ***FastCom (DS)***
    - Rx: **I2C (2 lines, SCK, SDA)**
    - Rx: **RSTn (1 line)**
    - Rx: I2C addr (5bits)
  - Analog : 1 line (Vtemp)

ETROC for BTOF FPC
→ BTOF FPC ~5 or 6 lines
→ 1x DataOut (DS) = 2 lines
→ ***p2p = 2 lines***
→ ***bus w/ 4 chips (not p2p) = 2 /4 lines***
→ ***bus w/ 17 chips = 2/17 lines***
→ **bus for all chips = 1 / 34**
→ 5 or 6 bits (depending on FPC conf.)
→ ***1 line***



https://etl-rb.docs.cern.ch/Specifications/etroc-test-card/#Specifications

- 135 cm FPC = 33 or 34 ASICs/FPC (x2 FPC x 2cm/sens)
  - **33 or 34** sensors are necessary
- If 34 ASIC's are in a FPC, 34 x {2+2 + 2/4+ 2/17 + 1/34+1} = 194 lines in total
  - INTT: 124 lines w/ 3.5cm width (1.5 times more than INTT,)
  - If use INTT technology, Thickness is ~0.8 % X0 / FPC

We use 2 FPC for a ladder ~ 1.6%X0

EICROC2 : 32x32 with EIC backend

- EICROC2 needs to address EIC digital architecture
  - Auto-trigger
  - Data driven zero-suppressed readout
  - Only readout hit channels and neighbours
  - Will depend a lot on the (low?) occupancy
  - Triplication and SEE tolerance

- Several EIC functions will be tested in CALOROC
  - Sparsified readout
  - Output links 160-1280 Mb/s

- Foreseen submission mid-2026