TOF Electronics Status

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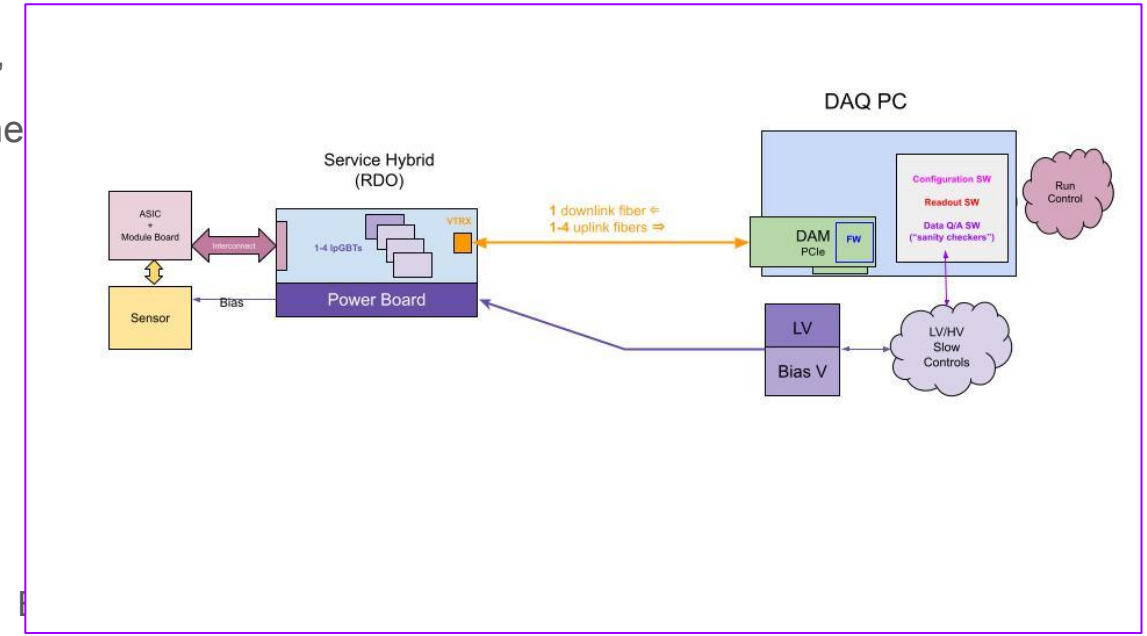
for the TOF Electronics Team

Reminder

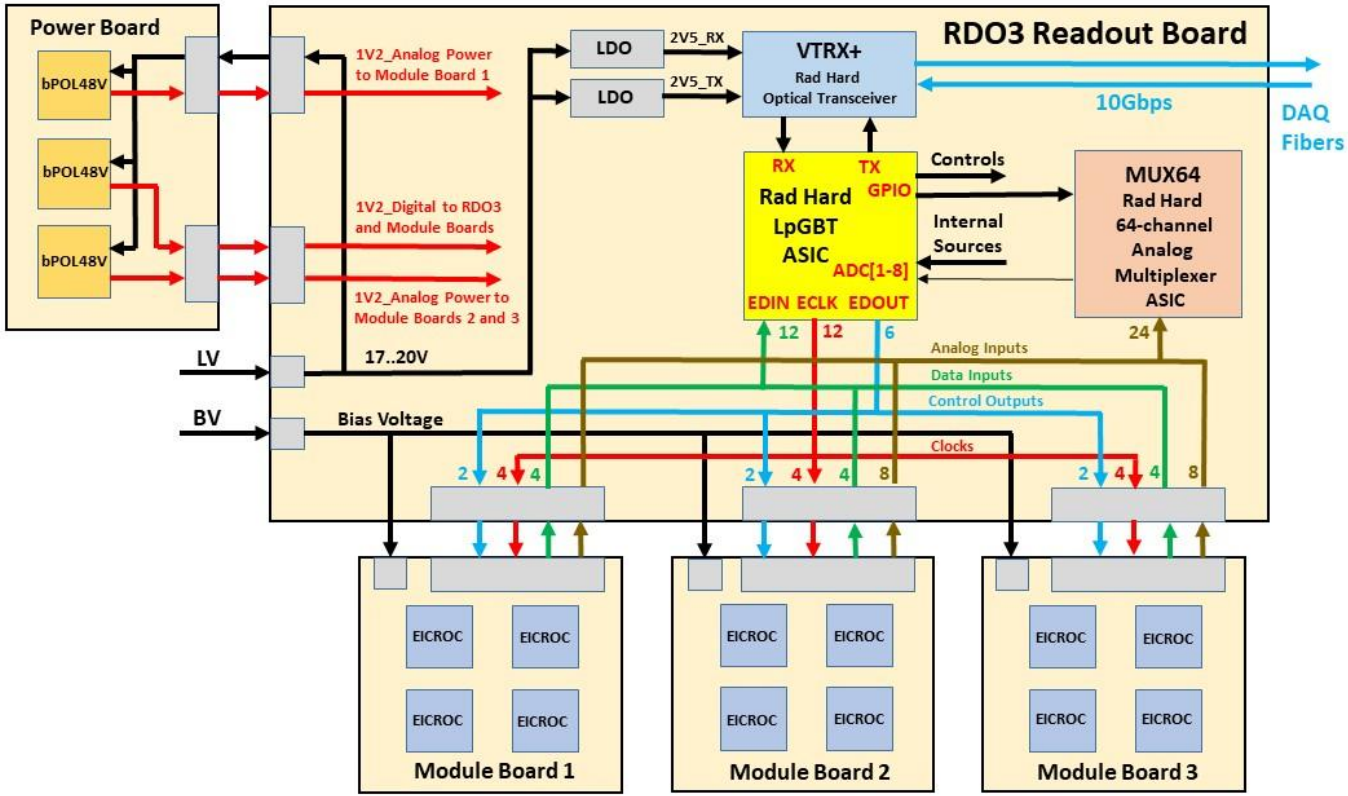
- we submitted a PED request “AC-LGAD Readout Electronics“
- aim is to prototype the readout chain
  - ASIC ⇒ RDO(w lpGBT & VTRX+) ⇒ DAM Board (w streaming firmware) ⇒ DAQ PC (w streaming software)
  - together with a “Power Board” which provides LV power to the ASICs (separate analog and digital) and to the RDO
- …by end of calendar 2025



Overview

- FTOF Readout Board 1st prototype – **RBv1** (Rice U)
- FTOF Power Board 1st prototype – **PBv1** (BNL)
- FTOF ASIC Module (ORNL, Rice, …)
  - using the EICROCx ASIC
- BTOF RDO Developments (Rice, …)
  - using the FCFD ASIC
- TOF Readout and DAQ (Rice, …)
- Short-term Future
- Mid-term Future

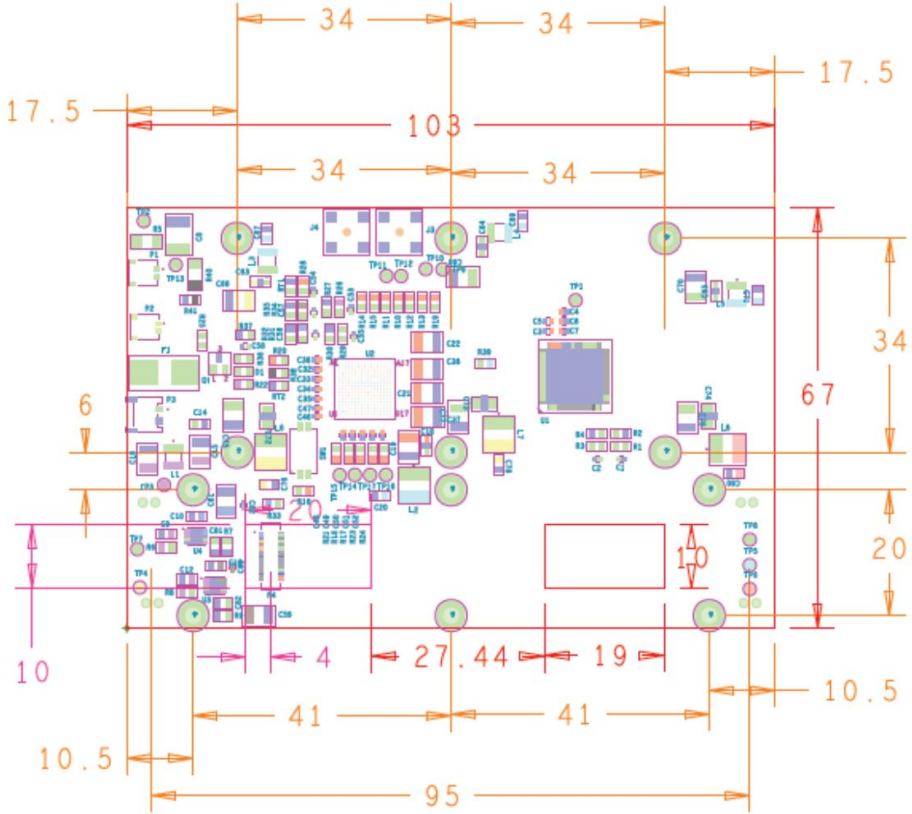
Scheme


Power Board
bPOL48V
bPOL48V
bPOL48V
1V2_Analog Power to Module Board 1
1V2_Digital to RDO3 and Module Boards
1V2_Analog Power to Module Boards 2 and 3
17..20V
LV
BV
Bias Voltage
RDO3 Readout Board
LDO
LDO
2V5_RX
2V5_TX
VTRX+
Rad Hard Optical Transceiver
10Gbps
DAQ Fibers
RX
TX
GPIO
Rad Hard LpGBT ASIC
ADC[1-8]
EDIN ECLK EDOUT
Controls
Internal Sources
MUX64
Rad Hard 64-channel Analog Multiplexer ASIC
12
12
6
24
Analog Inputs
Data Inputs
Control Outputs
Clocks
2 4 4
2 4 4 8
2 4 4 8
EICROC
Module Board 1
Module Board 2
Module Board 3

FTOF Readout Board (RBv1)

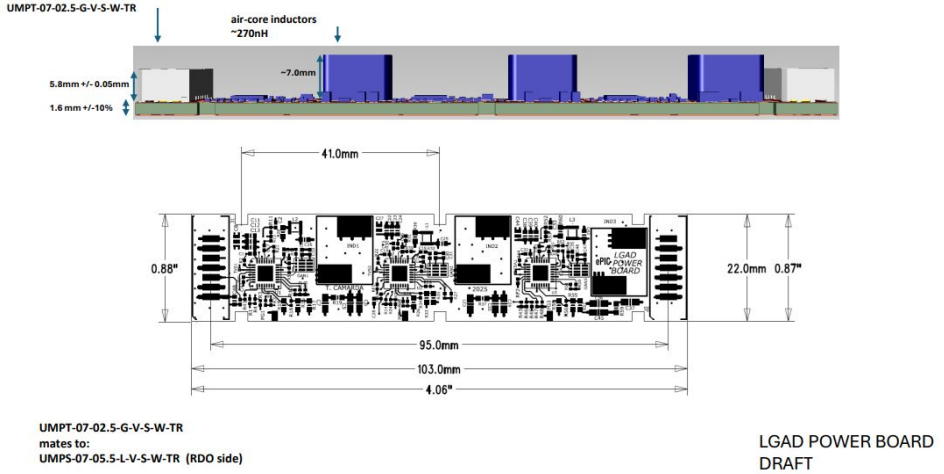
- Status
  - Schematics completed ✔
  - PCB design completed✔
  - PCB being manufactured (2 weeks)
  - Parts ordered
  - Assembled boards expected in 1 month (mid-Aug)
  - Testing (Aug,Sep,Oct)
- we used the CMS ETL Readout Board (very similar to ours) to already complete: ✔
  - DAM Streaming Firmware using our “FELIX-lite” candidate PCIe FPGA board (Alinx AXAu15)
  - develop and debug lpGBT configuration & control
    - lpGBT was in the FEC12/10Gbs mode running at the EIC-type clock of 315.2 MHz
      - 39.4 MHz recovered at lpGBT
  - develop and debug a “typical ASIC” interface to lpGBT using the CMS ETROC ASIC
- ⇒ we are ready to start debugging our RBv1 as soon as it arrives from the assembly house

RBv1 PCB Layout



FTOF Power Board (PBv1)

- PBv1 designed and started by Tim Camarda (BNL)
  - responsibility moved to Steve Boose (BNL) but with Tim's continuing help
- Recent Status from Tim
  - The power board PCBs are scheduled to ship out **in a few days.**
  - Instrumentation has the solder stencil and they say they can start when we get the boards and parts in.
  - The parts are on order.
  - We will populate **one circuit first** for testing/ evaluation.



FTOF ASIC Module

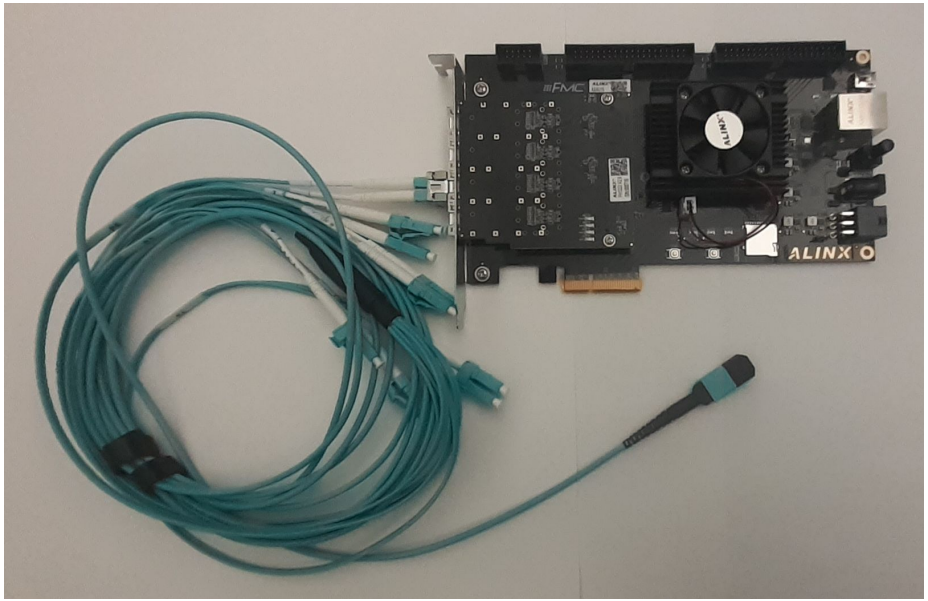
- We are designing a 2x2 (“a quad”) EICROC ASIC Module
- ASIC Module connects to the RBv1 via a single connector
  - connector decided, pinout decided
- See Mathieu’s presentation
- Note that we will need this module to continue testing the entire readout chain

BTOF RDO Evolution (and Power Board?)

- What we know now
  - RDO will have **1 Master lpGBT** and **3 Slave lpGBTs** connected to **1 VTRX+**
  - each lpGBT will use the VTRX's TX channel
  - Master lpGBT will additionally use VTRX's RX channel for configuration and clock recovery
  - **we will connect 16 FCFD ASICs to each lpGBT** ⇒ total 64 ASICs per RDO
- What we assume now
  - FCFD ASIC: **320 Mbs data rate, 1 differential data link per ASIC**
- What we need to know
  - **external constraints on the size of the RDO**
  - other BTOF groups which are willing to contribute (apart from Rice)?
  - how are the ASICs connected? **Connector?**
    - this contributes to the size/footprint of the BTOF RDO
- Issues
  - **funding???**
  - long (~1.4m) signal traces to/from ASICs and lpGBT
    - this is something we should start testing **now**
      - clock jitter
      - signal/data integrity
      - even I2C might be problematic
  - power distribution is unknown (and Tim is gone)

DAQ

- We use the AXAU15 PCIe FPGA board as the “FELIX-lite”
  - we purchased 4 kits each with AXAU15, Alinks 4-channel SFP FMC, 1 SFP+
    - 2 will stay at Rice
      - 1 for development
      - 1 for possible beam tests?
    - 1 for BNL testing [Prithwish et al]
    - 1 for LBLN testing [Zhenye et al)
  - first verision of the DAM firmware complete
- The AXAU15 is housed in a “DAQ PC” with DAQ software [TL]
  - currently simple: initialize lpGBT, read internal ADC, set/get GPIO, VTRX I2C, read data etc.etc.etc.
- We added 3 Lemo inputs/outputs to the AXAU15 [Mike]
  - **1 will be used for the external trigger while still using non-streaming chips**
  - 2 are for scope debugging



Short-term (up to end of 2025)

- EICROC1 ASIC “Characterization Board” interface to RBv1 [Mike, TL, …]
  - the Test Board needs to be available first (?) as well as the ASIC (?) [Omega Group]
  - and later with 32x32 pixel sensor [Mathieu et al]
- Possibly also the FTOF-specific EICROC1 ASIC Module Board? TBD…
- William’s SFP FMC with the GTU interface fiber and clocking [William, TL]
  - with GTU emulation in AXAU15
  - this enables the final clock distribution mechanism ⇒ important step
  - (I am unsure about the status – need to check)
- **TClink:** CERN’s Temperature Controlled Link ⇒ required for TOF [TL]
  - CERN-developed FPGA firmware for Xilinx Ultrascale FPGAs
  - I’d like to use our FELIX-lite first to gain experience and to measure performance
- “User-quality” DAQ software [TL, others?]
  - with GUI etc

Mid-term (early 2026+)

- Start the BTOF RDO and PB
  - strongly depends on funding as well as a person in charge of the Power Board (was Tim)
  - we can start now with the CMS ETL board which is very similar: 1 Master lpGBT, 1 Slave lpGBT
- FELIX use and commissioning with RBv1
  - we need DAQ-wide decision on how to do this?
  - I am willing to contribute but see line above
- Test Beams ⇒ TBD
  - of course, we need the ASIC and the sensor

Summary

- We are aiming for a full readout chain by the end of calendar 2025
  - ASIC is hoped to be EICROC1
    - possibly first versions of FCFD with digital backend?
- We would like to start with the BTOF RDO and Readout chain
  - funding??