Intro & DSC Requirements

EIC UGM 2025, Software Interface for Test Beams/Benches

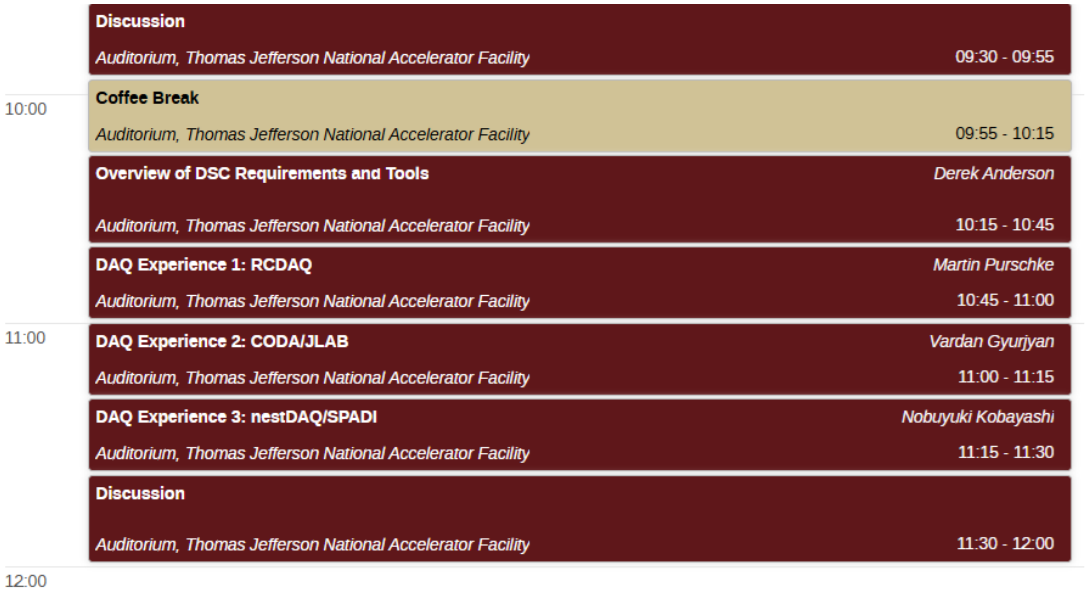
Martin Purschke, Dmitry Kalinkin, Derek Anderson

Introduction | Software to Readout Interface

- **Workfest goal:** prepare a demonstrator analysis chain going from data readout to final chain using our software ecosystem

- Important exercise for several reasons
  1) We want **to support users at test beams,**
  2) This helps us **practice using our software in real data taking**
  3) And **encourages users to start practicing with software**

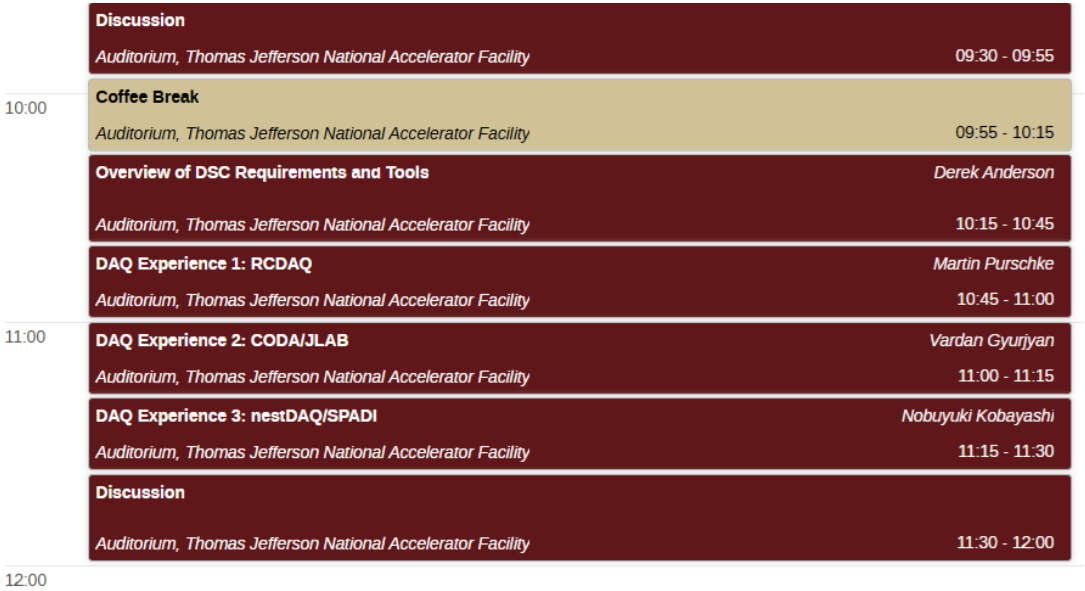
- The earlier we can start with these, the better!



Introduction | Software to Readout Interface

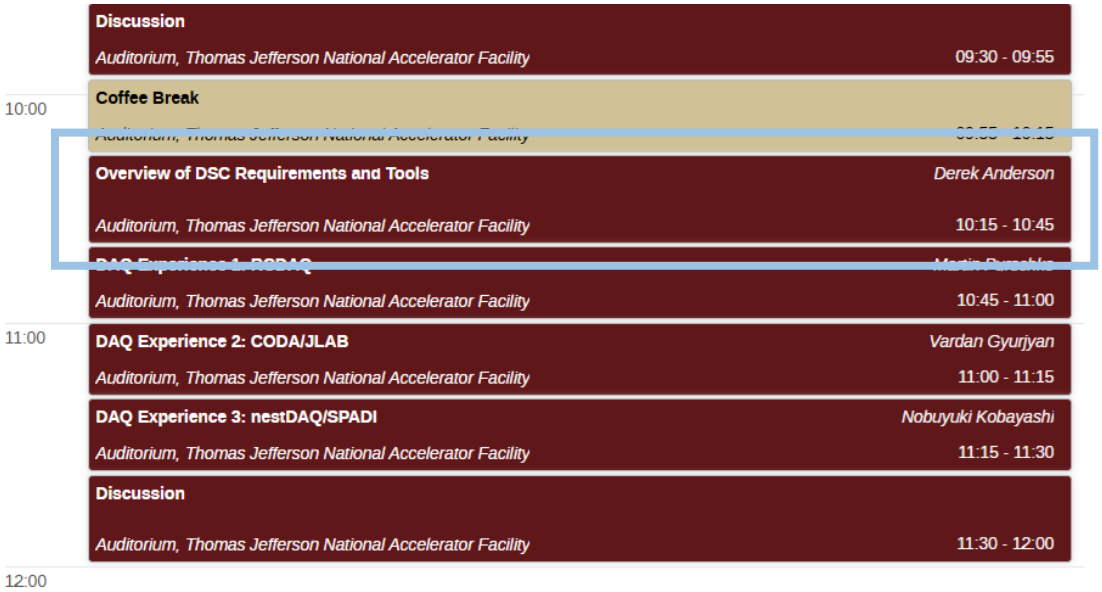
- Two halves to workfest:
  1) **Morning session of talks (see right):** to gather input on demonstrator requirements
     - Input from DSCs (this talk)
     - And experience using past DAQ frameworks
  2) **A hackathon at 6 pm tonight in the CEBAF Center lobby:** to code up demonstrator

- **Pizza will be provided at the hackathon!**



Introduction | This Talk

- **This talk:** review & discuss setups used by DSCs
  - What DAQ frameworks were used?
  - What software tools were used?
  - Did (or do) they have any software requirements?
- **Received Input from 3 DSCs:**
  - BIC
  - LFHCAL/EEEMCal
- Open discussion afterwards
  - **We want to hear from you!**



Electronics and DAQ I: PICO-DAQ and RDO status, joint with Software Interface to Readout for Test Beams and Benches

Input from BIC

Bobae Kim and Maria Żurek
Argonne National Laboratory

Choice of tools

Hardware

What tools **have been used so far**:

- Calorimeter prototype (Baby BCAL) readout with SiPMs and 250 MHz fADC (JLab style) with CODA-based readout.
- Current tests of the AstroPix-SciFi integration (see slide 3)
  - AstroPix setup with GECCO board and Xilinx FPGA, synchronized with Baby BCAL through the LVDS MISO signals that generated from AstroPix used as trigger IN for CODA-based DAQ (challenging for many reasons)
  - Baby BCAL triggered by analog signal from one pixel of AstroPix
- **Integration with the HGCROC planned (see slide 8)**

Software

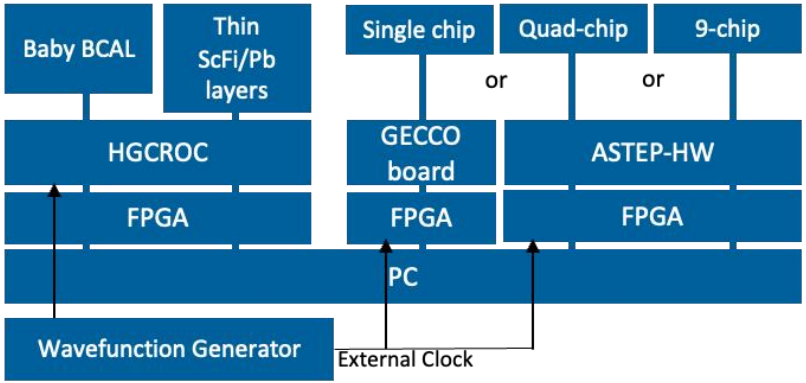
Our FTBF prototype geometry implemented in dd4hep. Currently in the fork: https://github.com/richardsj-anl/epic Geometry implementation

System Testing for Integration (2)

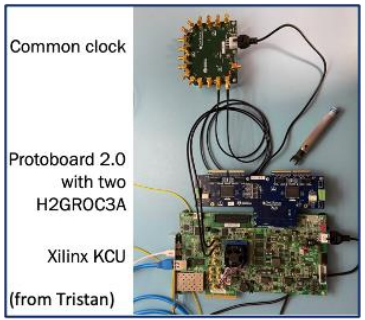
PLANS

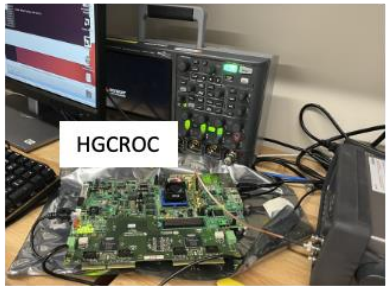
Synchronization Plan between AstroPix DAQ and HGCROC for Pb/SciFi

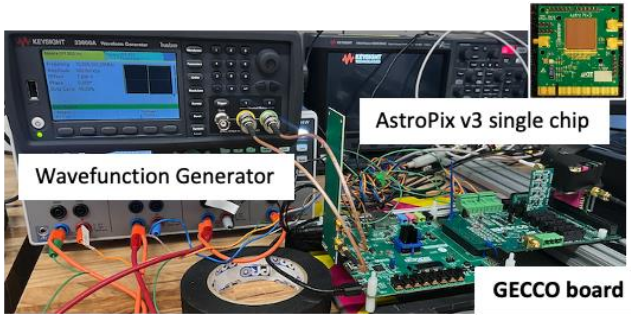
- Provide 40 MHz external clock to HGCROCs and AstroPix DAQ

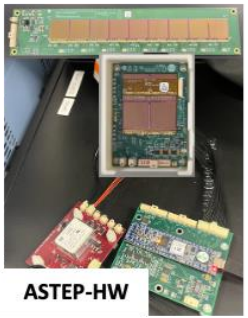


- **AstroPix single chip+ GECCO board + Nexys + ASTEP sw/fw**
  - LVDS external clock used
  - Both 10MHz Timestamp and the FPGA timestamp external (10MHz+40MHz)
  - Bit file exists but needs debugging;
- **AstroPix quad-chip / 9-chip module + ASTEP HW board + CMOD + ASTEP sw/fw**
  - single-ended clock required
  - FPGA Timestamp external (40 MHz)







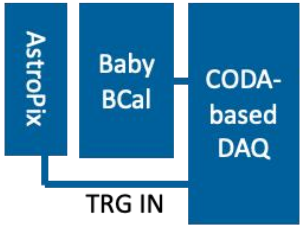


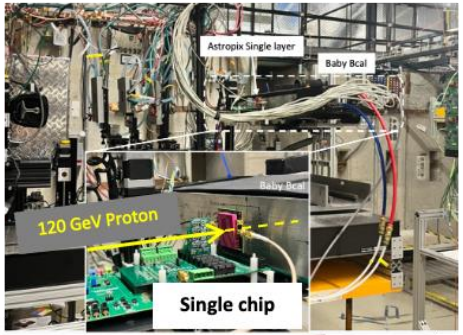
System Testing for Integration (1)

WHAT HAVE WE TRIED SO FAR

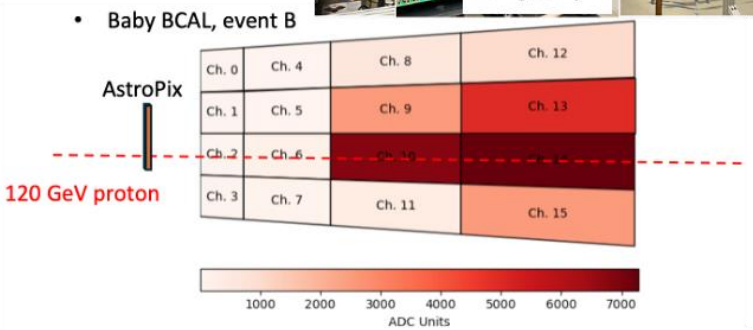
AstroPix+BabyBCAL @Beam test (June 2024)

- Baby BCAL triggered by analog signal from one pixel of AstroPix





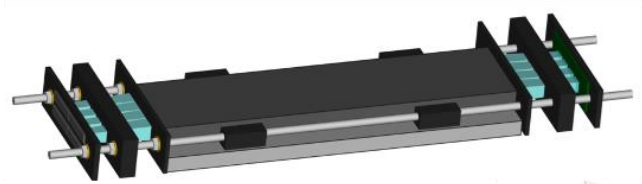
- Baby BCAL, event B

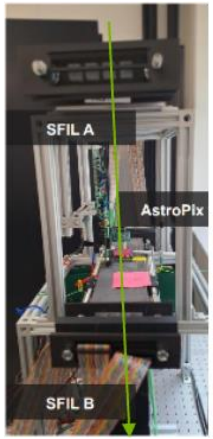


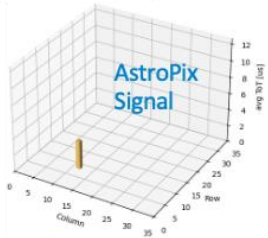
*Example plot of 120 GeV proton event display from an integrated system of Baby BCAL and a single-layer AstroPix v3 chip by Henry Klest

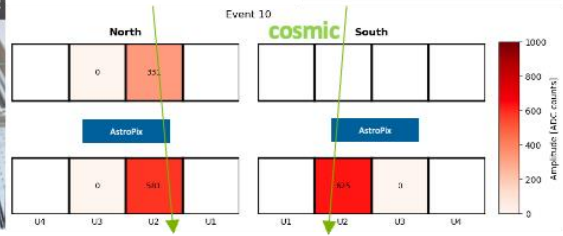
AstroPix+SFILs @Bench test

- Thin Pb/SciFi layers with new SiPMs and optical cookies commissioned on bench.









DSC Needs

Hardware

- Switching to HGCROC: initial studies done, work on AstroPix-HGCROC (Baby BCAL) sync in progress
- Challenge: from our experience CODA is not very well documented, lots of “internal” knowledge needed, that makes setting up DAQ challenging

Software

- How do we want to maintain the prototype geometries in the ePIC repo? We can dedicate workforce to move the baby BCAL implementation, but it would be useful to have an example.

Electronics and DAQ I: PICO-DAQ and RDO status, joint with Software Interface to Readout for Test Beams and Benches

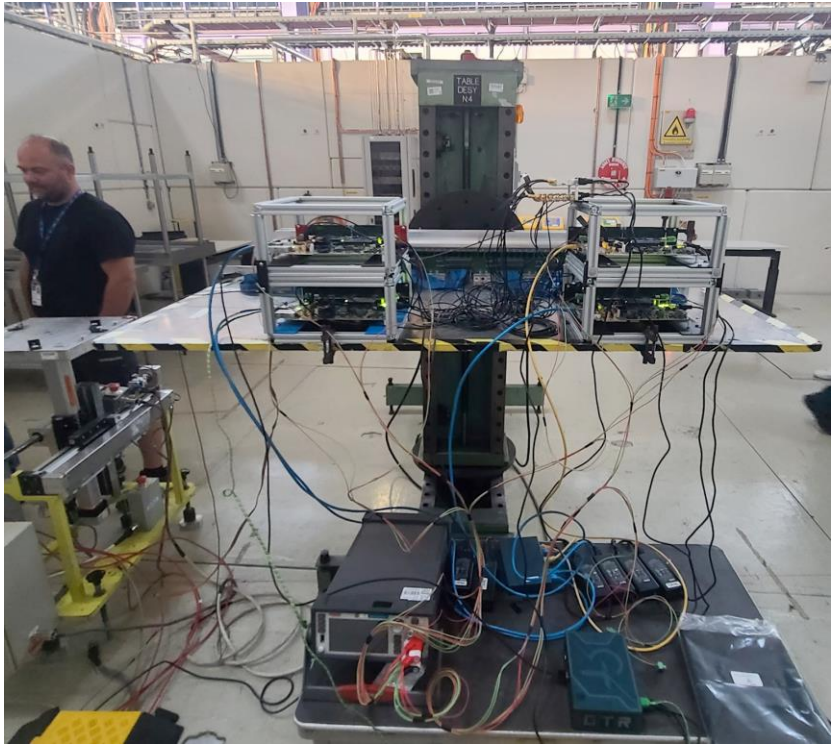
Input from LFHCAL/EEEMCal

Tristan Protzman, Lehigh University

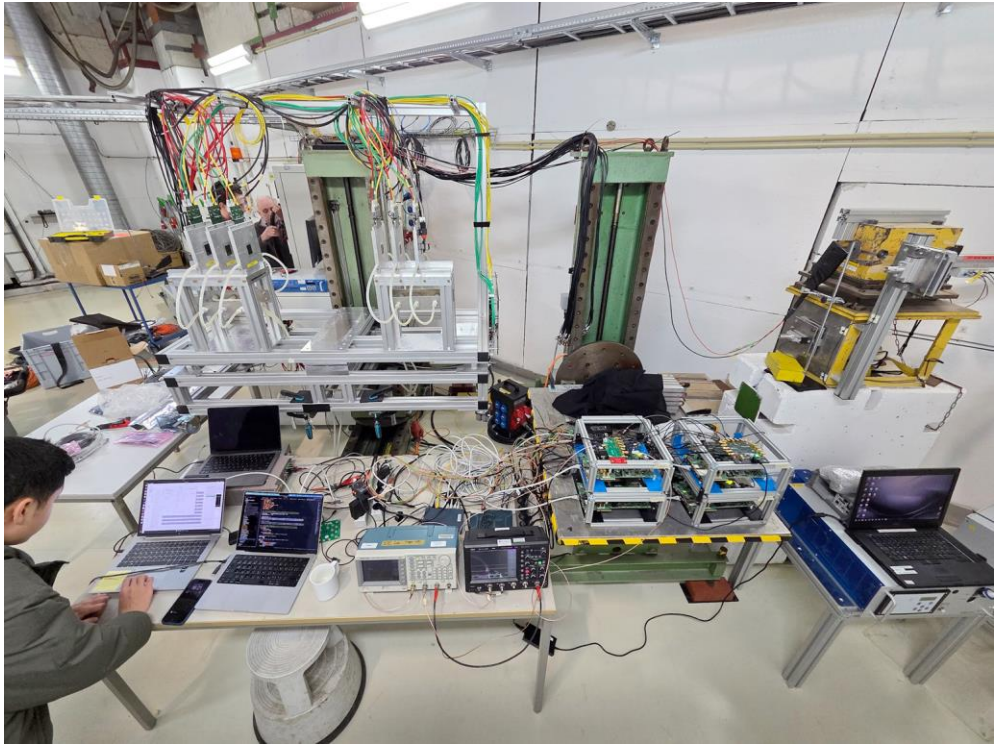
NSF

LEHIGH UNIVERSITY

Test beam setup



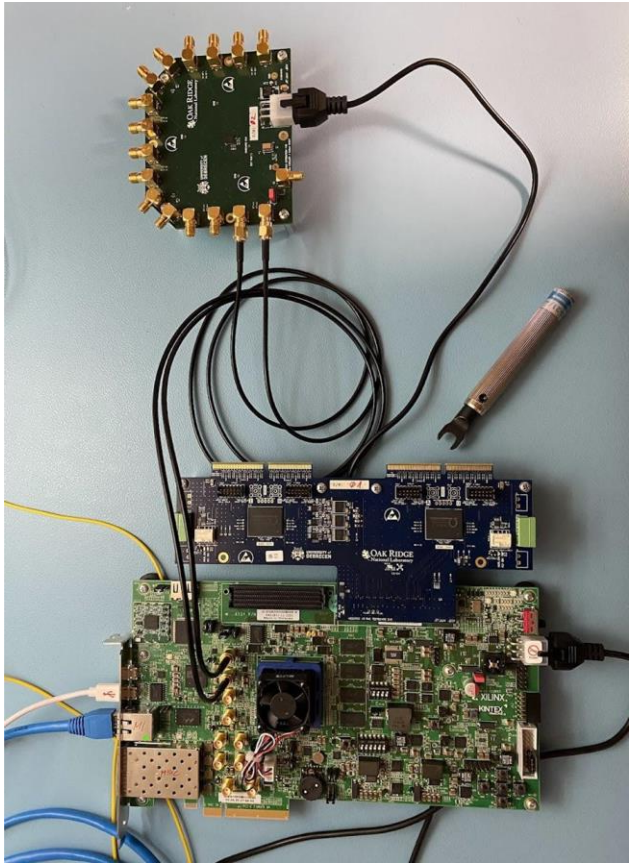
LFHCal @ CERN PS



EEEMCal @ DESY II

Basic setup

- Xilinx KCU
  - FPGA to interface between between DAQ/slow controls and ASIC
- Protoboard
  - Contains 2 ASICs, breaks out IO
- Clock
  - 40 MHz dual edge clock
  - Common to all KCU used in test beam
- Trigger board (Not shown)
  - Duplicates and distributes trigger to all KCU



Software

- FPGA Programming: Vivado
- DAQ: H2GDAQ
- Configuration: H2GConfig
- Calibration: H2GCalib
- Online Monitoring: H2G Online Monitoring
- Decoding: H2G Decode
- Analysis (LFHCAL): epic-lfhcal-tbana

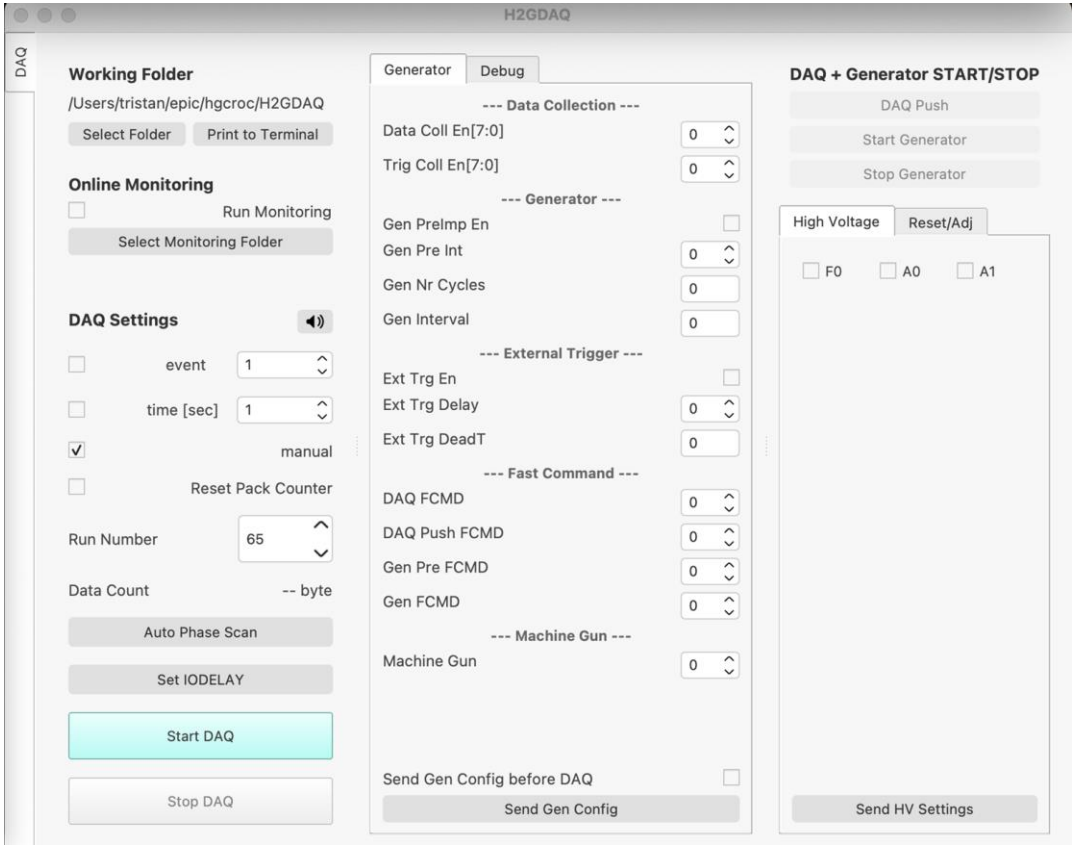
Shihai Jia

Tristan Protzman

Friederike Bock (+ several others)

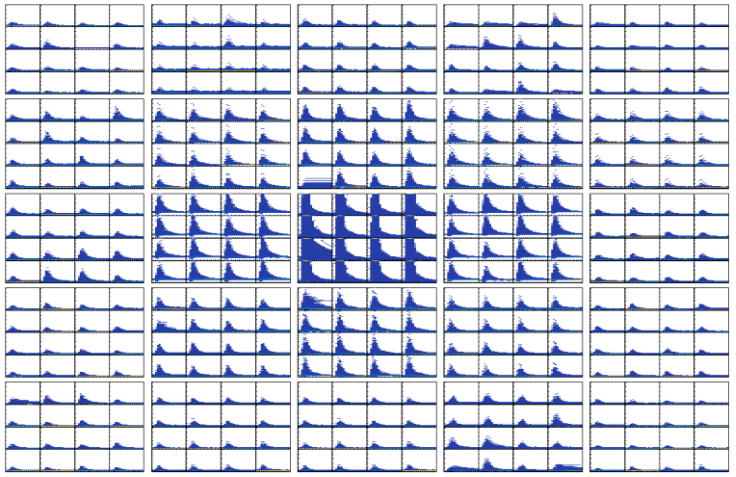
Running the DAQ

- Enable/disable bias from High Voltage tab
- Select external trigger, delay, and number of samples
- Three run modes
  - Number of events
  - Duration
  - Manual start/stop
- Can automatically start the online monitoring
  - Check the box and select the folder with the compiled code

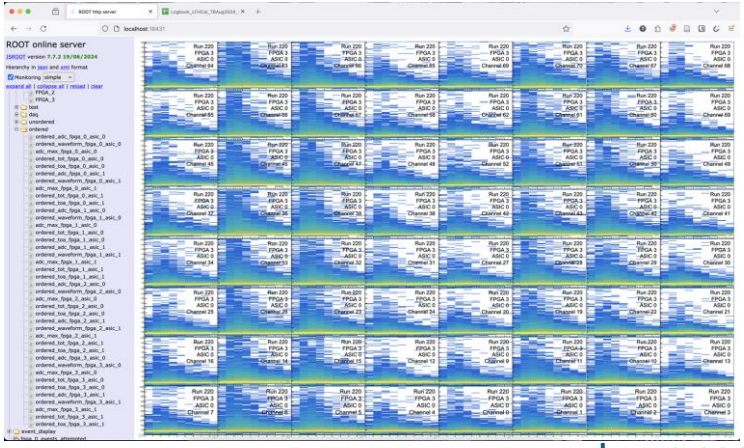


Online monitoring

- Real time decoding of events
- Implemented as webserver accessible from any browser
- Easy-ish to develop detector specific visualizations
- ADC, ToA, ToT spectra
  - Very helpful to make sure pedestals look correct
- Tracks events and packets from each ASIC
- Does **not** do event alignment
  - I could be convinced to add this though



EEEMCal @ DESY II



LFHCal @ CERN PS

DSC Needs

Hardware

- Will same DAQ be used for the 2025 CERN test beams?
- Event alignment was (is) a significant challenge

Software

- Where does processing with EICrecon begin? Raw data? Data after some processing?

Questions/Discussion?