

RDO concept

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Goals for the Readout Board

- **Design a versatile Readout Board to be used in all detectors:**
 - Collection of the data from FEB's
 - Aggregation of data
 - Suitable for the streaming data acquisition
 - Adaptable for all detectors
 - Design and support will be kept in the collaboration
- **Constraints:**
 - Price, based on the Artix Ultrascale+ family
 - Scalable to larger systems
 - Size for some of the detectors

FPGA choices

Basic choice is the Artix Ultrascale+ family:

- ~300-500\$
- Long-term availability (in the next decade)
- Scalability of the system:
 - From Artix even up to the Kintex capability

UltraScale Architecture Migration Table

Footprint	Artix™ UltraScale+™					Kintex™ UltraScale™							Kintex UltraScale+						Virtex™ UltraScale								
	AU7P	AU10P	AU15P	AU20P	AU25P	KU025	KU035	KU040	KU060	KU085	KU095	KU115	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P	VU065	VU080	VU095	VU125	VU160	VU190	VU440	VU3P	
A289	■																										
A368		■	■																								
B484		■	■																								
C484	■																										
A784							■	■																			
B784				■	■								■	■													
A676							■	■					■	■													
B676		■	■	■	■								■	■													
A900							■	■																			
D900													■	■		■											
E900															■		■										
A1156						■	■	■	■		■						■	■									
A1365																											
A1517								■	■		■																
C1517											■								■	■	■					■	
D1517												■								■	■	■	■				
E1517															■	■		■									
A1760																		■									
B1760								■	■	■										■	■	■					

The footprints of the selected FPGA's are the same:

- B676 - 1mm pitch
- B784 - 0.8mm pitch

The pitch correlates with the size and cost (complexity) of the PCB

The large FPGA family coverage in the footprint enables to have interchangeable designs

FPGA consideration

B676 Package, 1mm pitch

#	Part Number	Unit Price \$	Logic Cells	DSP	36K	HP	HD	GTH GTY	PCIe Gen/Lane
11	XCAU10P-1FFVB676E	185	96 250	400	100	156	72	12	4/4, 3/8
13	XCAU10P-2FFVB676E	259	96 250	400	100	156	72	12	4/4, 3/8
15	XCAU15P-1FFVB676E	231	170 100	576	144	156	72	12	4/4, 3/8
17	XCAU15P-2FFVB676E	324	170 100	576	144	156	72	12	4/4, 3/8
19	XCAU20P-1FFVB676E	334	238 437	900	200	156	72	12	4/8
21	XCAU20P-2FFVB676E	467	238 437	900	200	156	72	12	4/8
23	XCAU25P-1FFVB676E	398	308 437	1200	300	208	72	12	4/8
25	XCAU25P-2FFVB676E	557	308 437	1200	300	208	72	12	4/8
27	XCKU3P-1FFVB676E	1 405	355 950	1368	360	208	72	16	4/8
29	XCKU3P-2FFVB676E	2 054	355 950	1368	360	208	72	16	4/8
31	XCKU5P-1FFVB676E	2 055	474 600	1824	480	208	72	16	4/8
33	XCKU5P-2FFVB676E	2 731	474 600	1824	480	208	72	16	4/8

B784 Package, 0.8mm pitch

#	Part Number	Unit Price \$	Logic Cells	DSP	36K	HP	HD	GTY	PCIe Gen/Lane
19	XCAU20P-1SFVB784E	305	238 437	900	200	156	72	12	4/8
21	XCAU20P-2SFVB784E	428	238 437	900	200	156	72	12	4/8
23	XCAU25P-1SFVB784E	388	308 437	1200	300	208	96	12	4/8
25	XCAU25P-2SFVB784E	543	308 437	1200	300	208	96	12	4/8
27	XCKU3P-1SFVB784E	1 466	355 950	1368	360	208	96	16	4/8
29	XCKU3P-2SFVB784E	2 054	355 950	1368	360	208	96	16	4/8
31	XCKU5P-1SFVB784E	1 976	474 600	1824	480	208	96	16	4/8
33	XCKU5P-2SFVB784E	2 768	474 600	1824	480	208	96	16	4/8

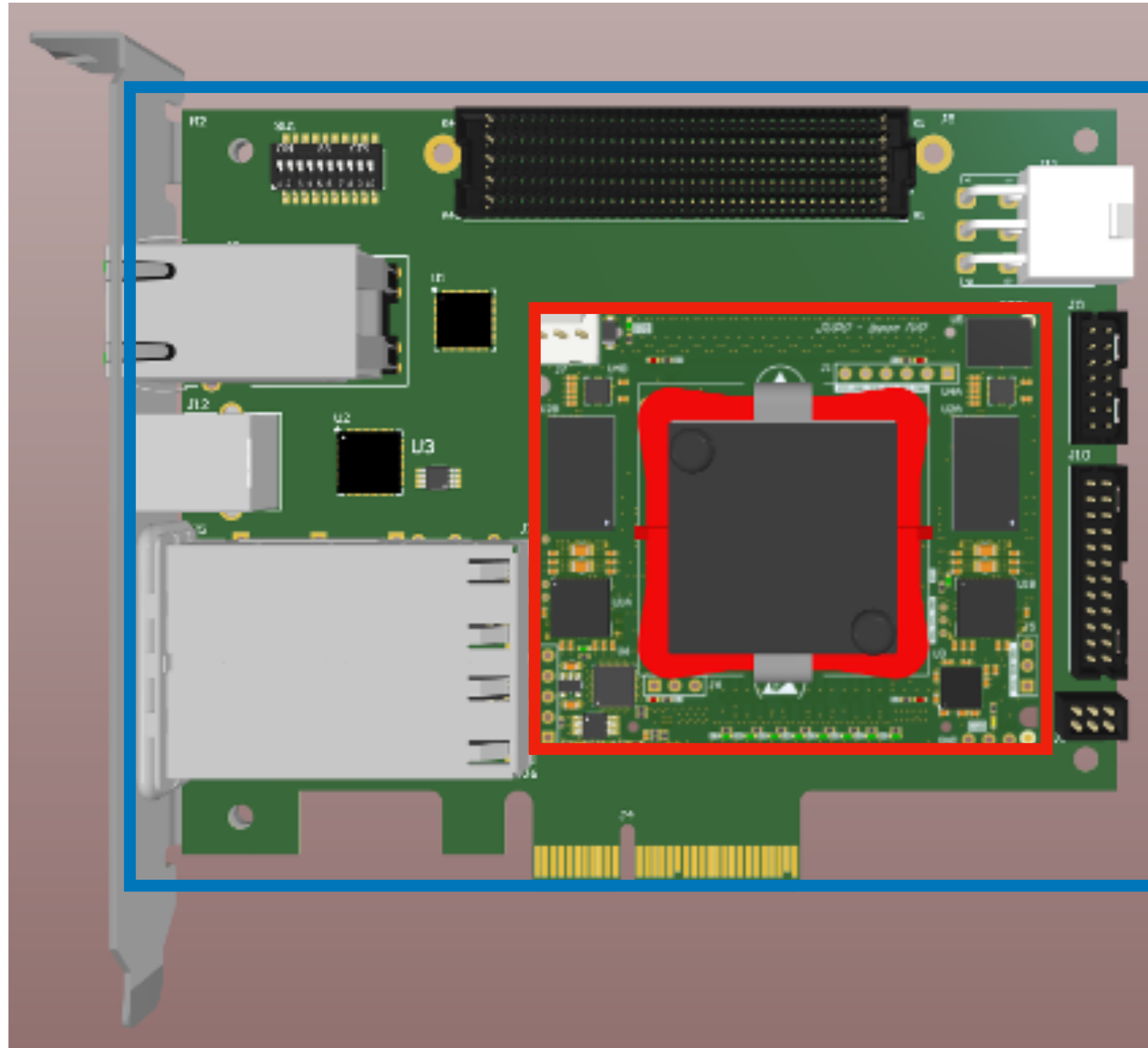
- Difference is in the number of logic cells
 - Depends on the application, e.g. CALOROC we plan the XCAU20P-2...
- DSP capabilities, buffering, clocking
- GTH/GTY = 16.3 Gbps/32.72 Gbps
- Availability:
 - Xilinx/AMD is trusted and long lasting. Typical availability is ~15 years (Ultrascale+ extended 2045)
- 100+ HP/HD pins enables interfacing many different FEB options
- High speed GTx pins would be for LpGBT communication (10Gbps)

Conclusion:

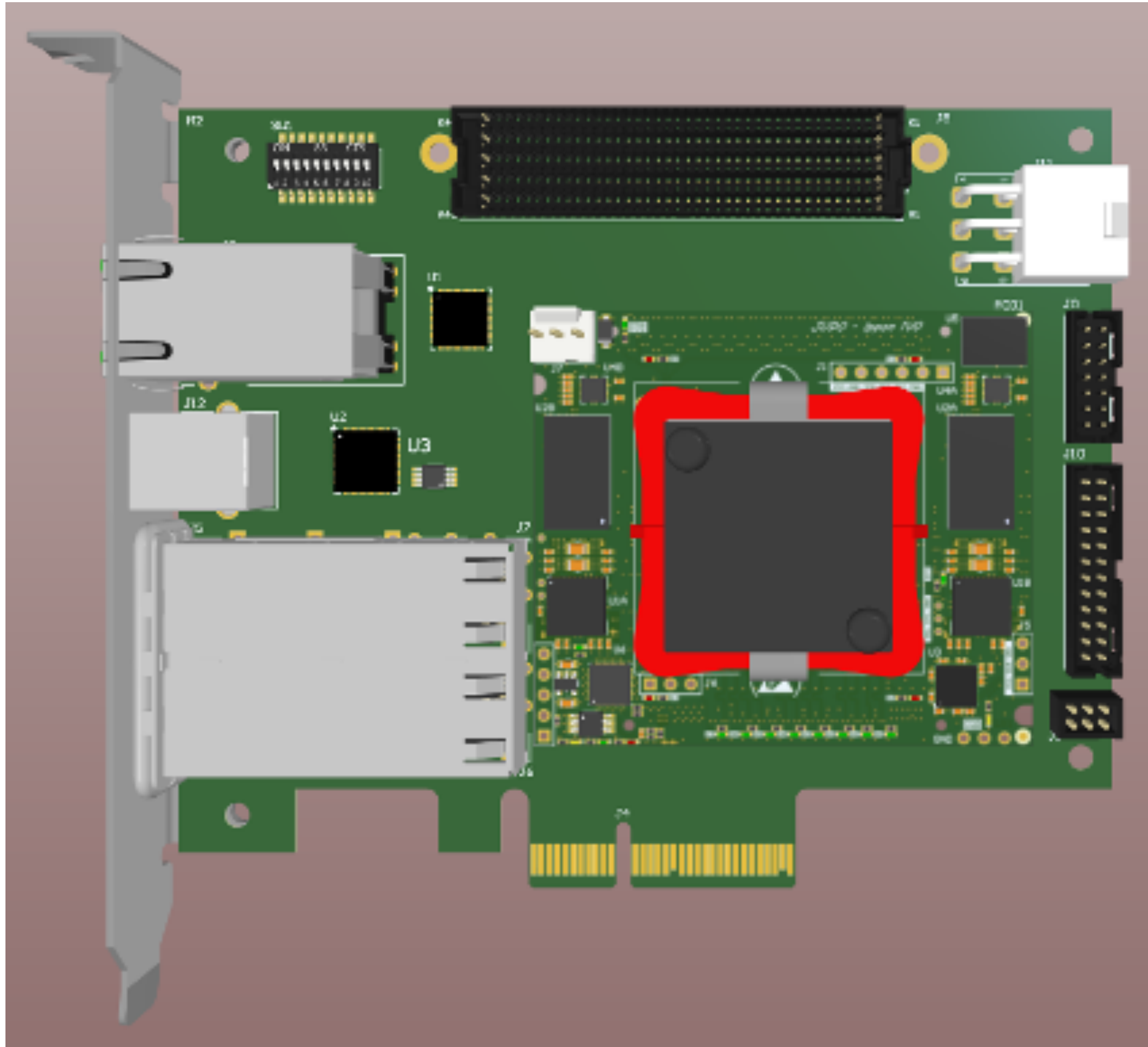
- B676 footprint would be the winner (unless space is a constraint), 1mm pitch helps with the PCB price also and easier production

- AMD UltraScale+ GTH (16.3Gb/s): Low power & high performance for the toughest backplanes
- AMD UltraScale+ GTY (32.75Gb/s): Maximum NRZ performance for the fastest optical and backplane applications;
33G transceivers for chip-to-chip, chip-to-optics, and 28G backplanes
- <https://www.amd.com/en/products/adaptive-socs-and-fpgas/technologies/high-speed-serial.html>

Basic idea - mother/daughter boards



Basic idea - mother/daughter boards



Mother board:

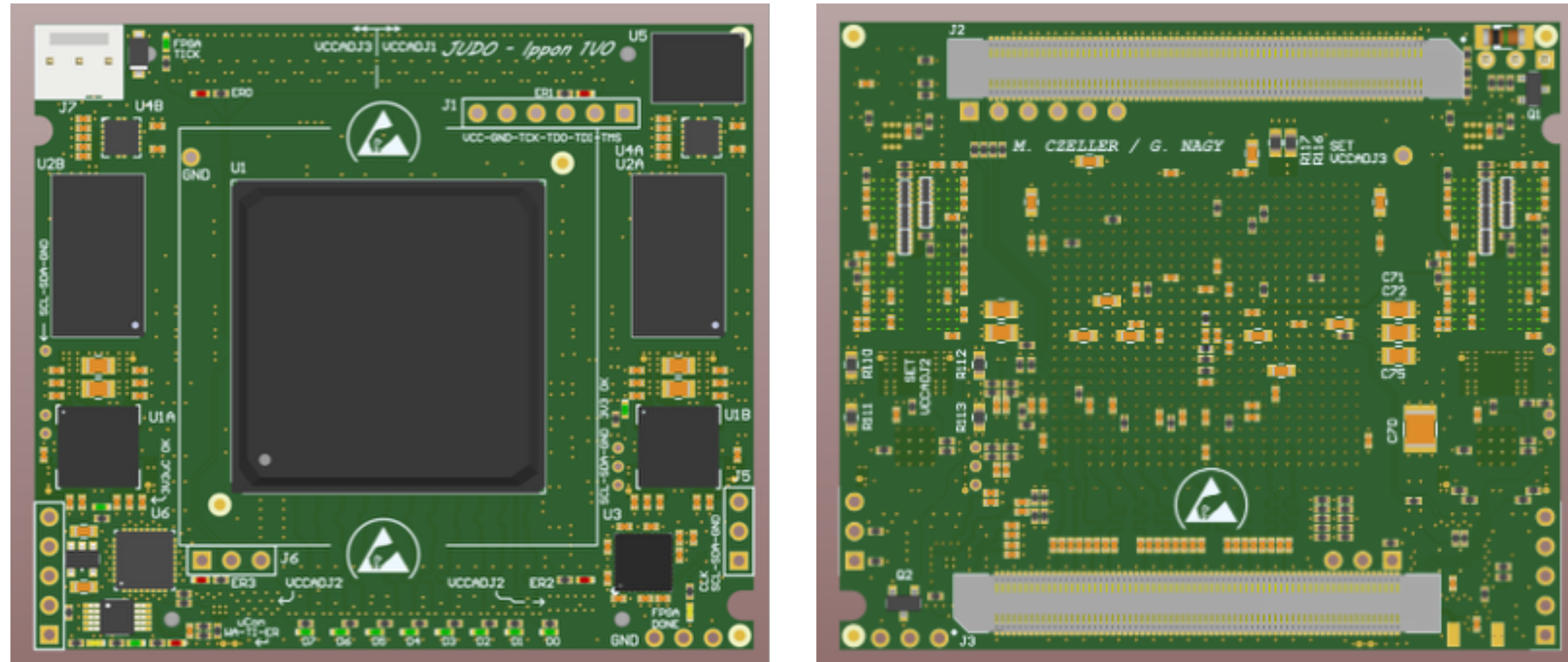
- User specific (or detector specific)
 - Depends highly on the need of a detector
- All connections to the FEB
- All connections to the DAM boards
 - SFP+, firefly or FMC with module
- Power distribution
- Low and high complexity on the clock distribution
- Compatible with the daughter cards

Daughter board:

- Same for every card, interchangeable with different FPGA
- 676 pin package
- 12-16 GTx
- 50+ differential pairs, HP
- 20+ single ended wire, HD
- On board memory (DDR4, optional)
- System controller on the board
- 12 V power input

Proposed daughter boards

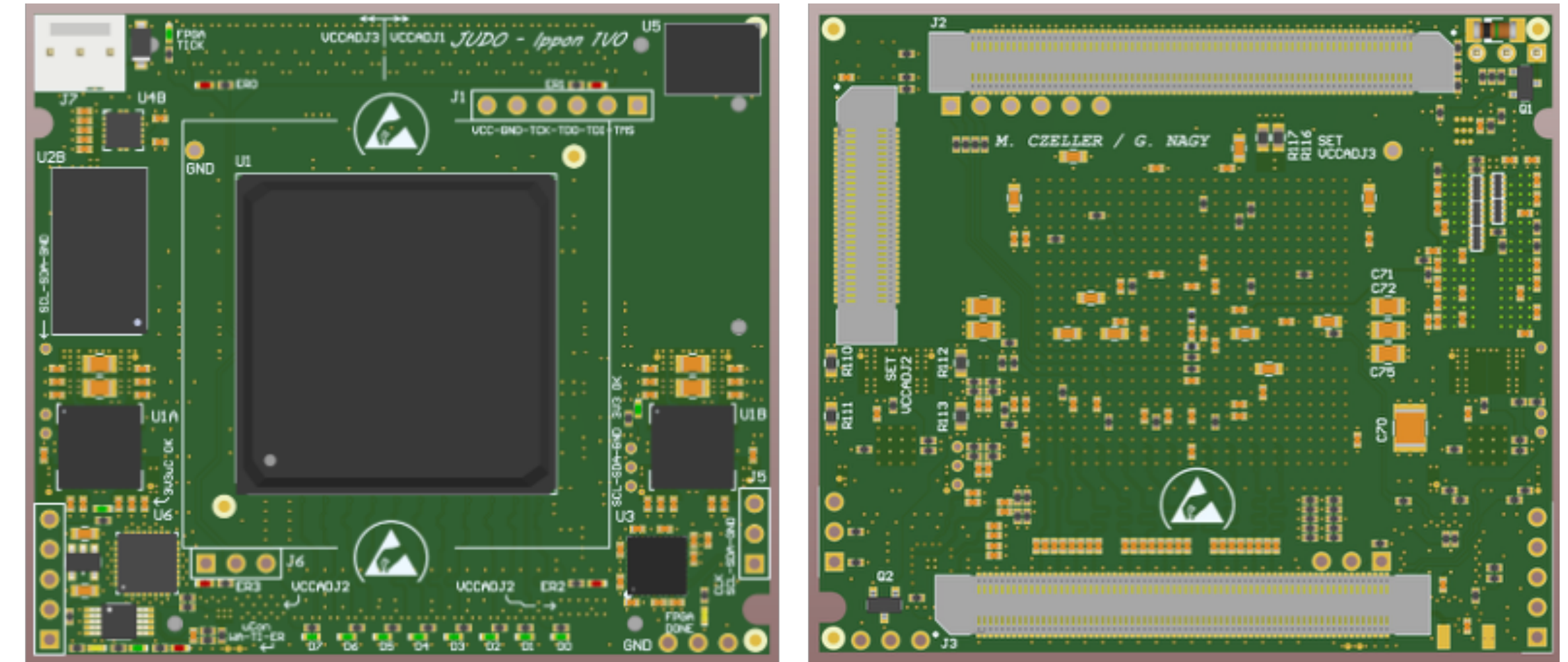
Version A - two connector design 62x54mm



2 connector version, contains 2x independent DDR4 memory chips

46 HP differential pairs, 46x max 1250Mbps
12 MGT, 12x 16.3 Gbps
Ideal for aggregation tasks

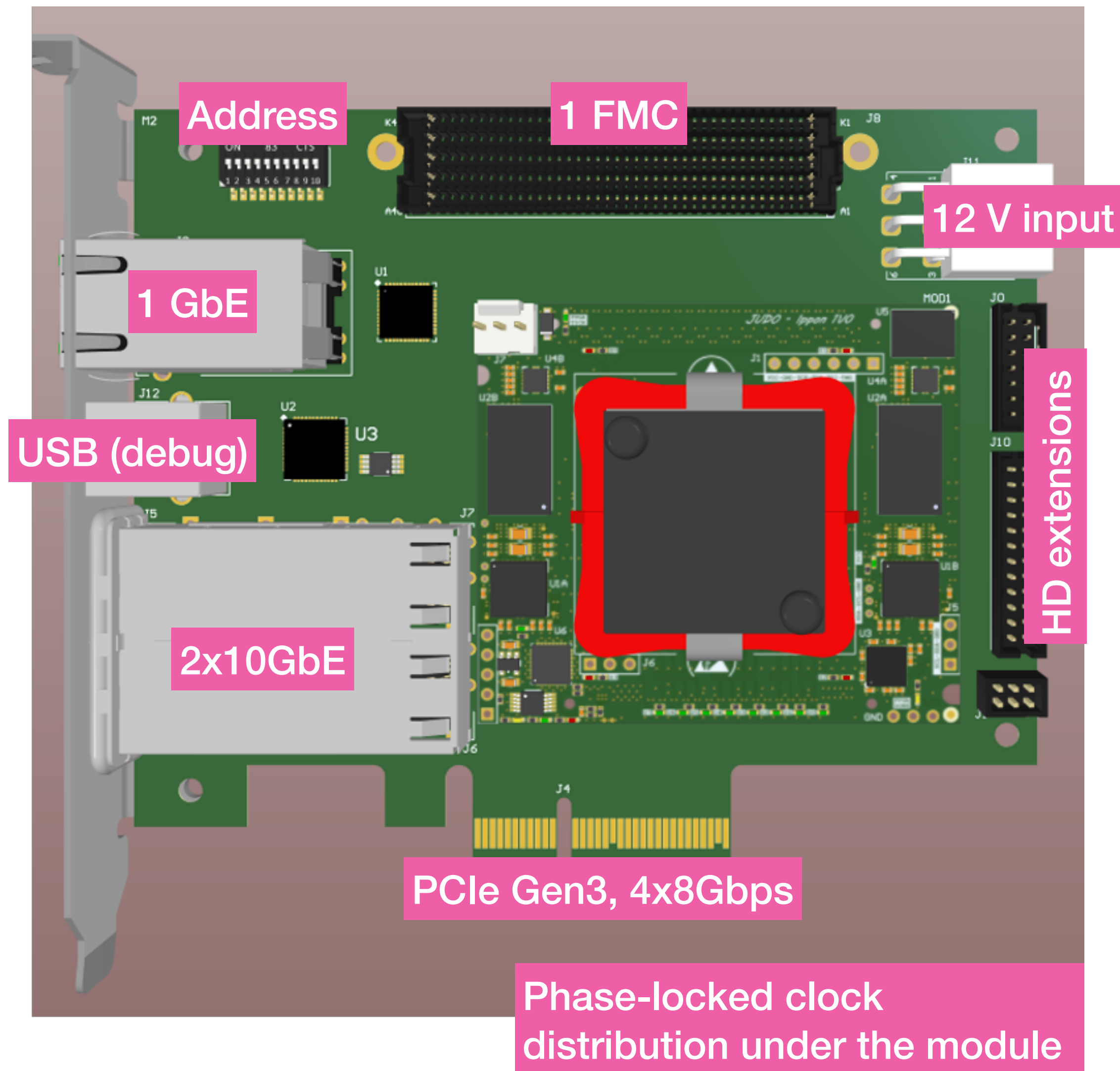
Version B - three connector design 62x54mm



3 connector version, contains 1 independent DDR4 memory chips

46+24 HP differential pairs, 70x max 1250Mbps
12 MGT, 12x 16.3 Gbps
Ideal for interfacing with ASICs

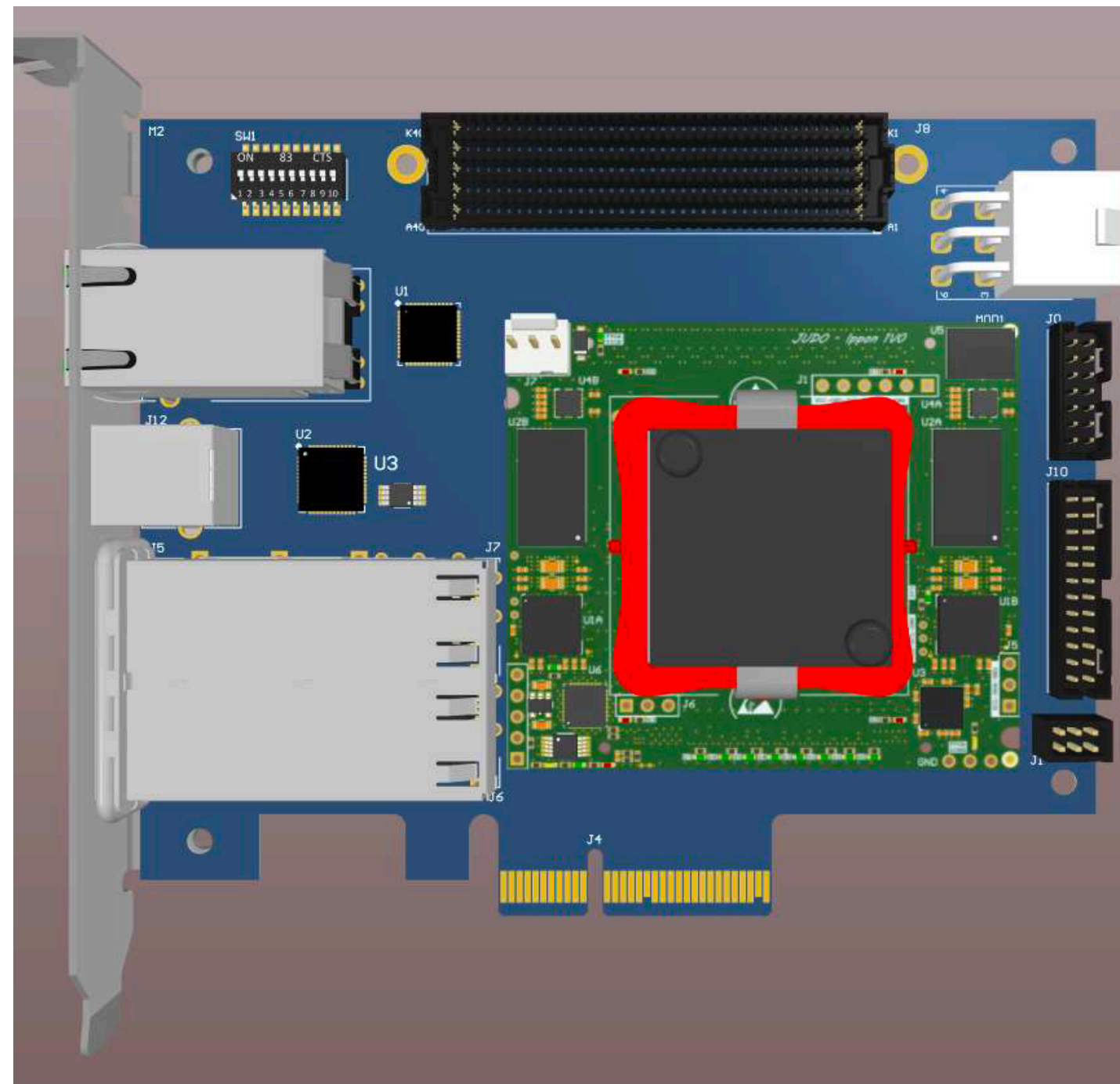
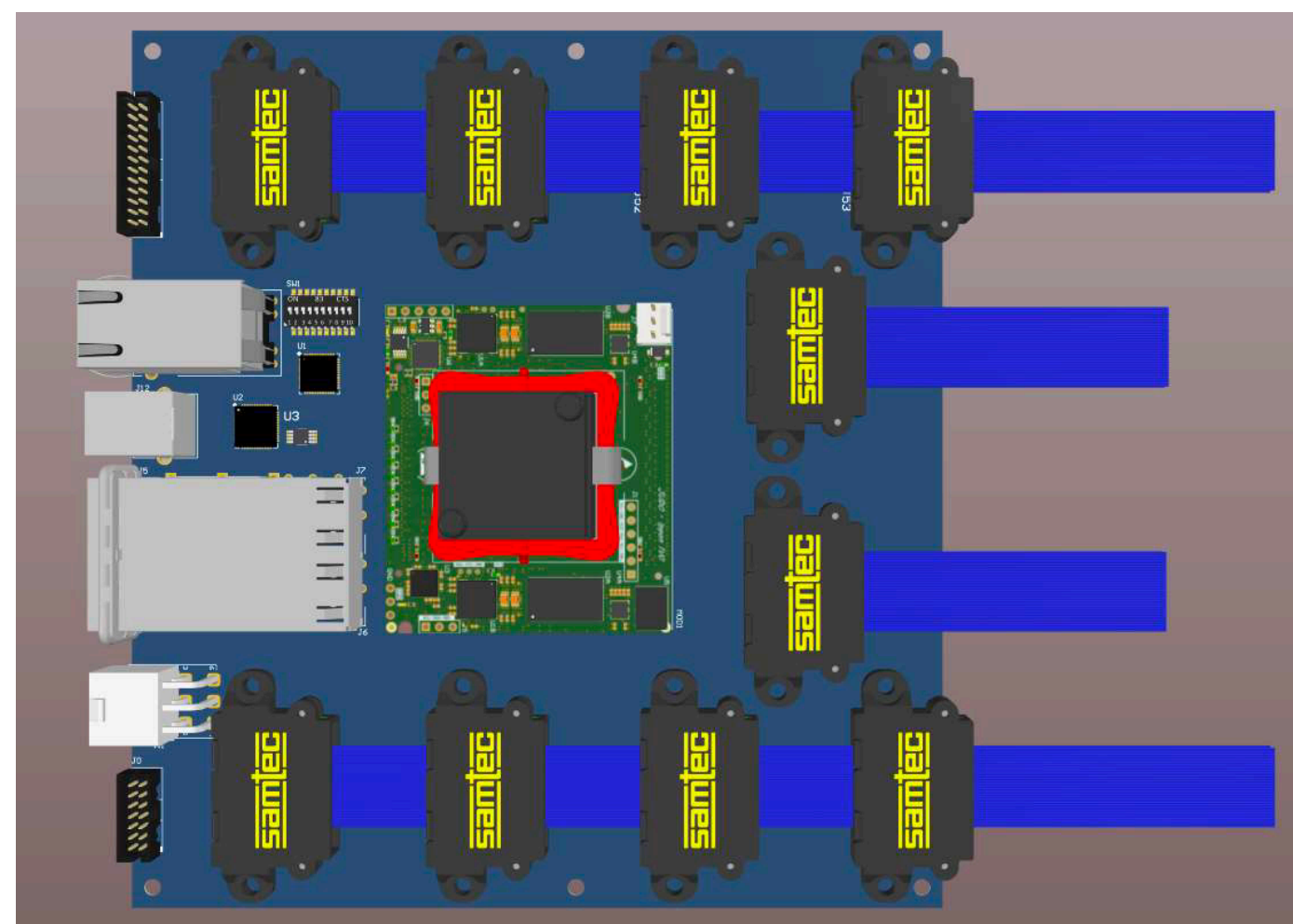
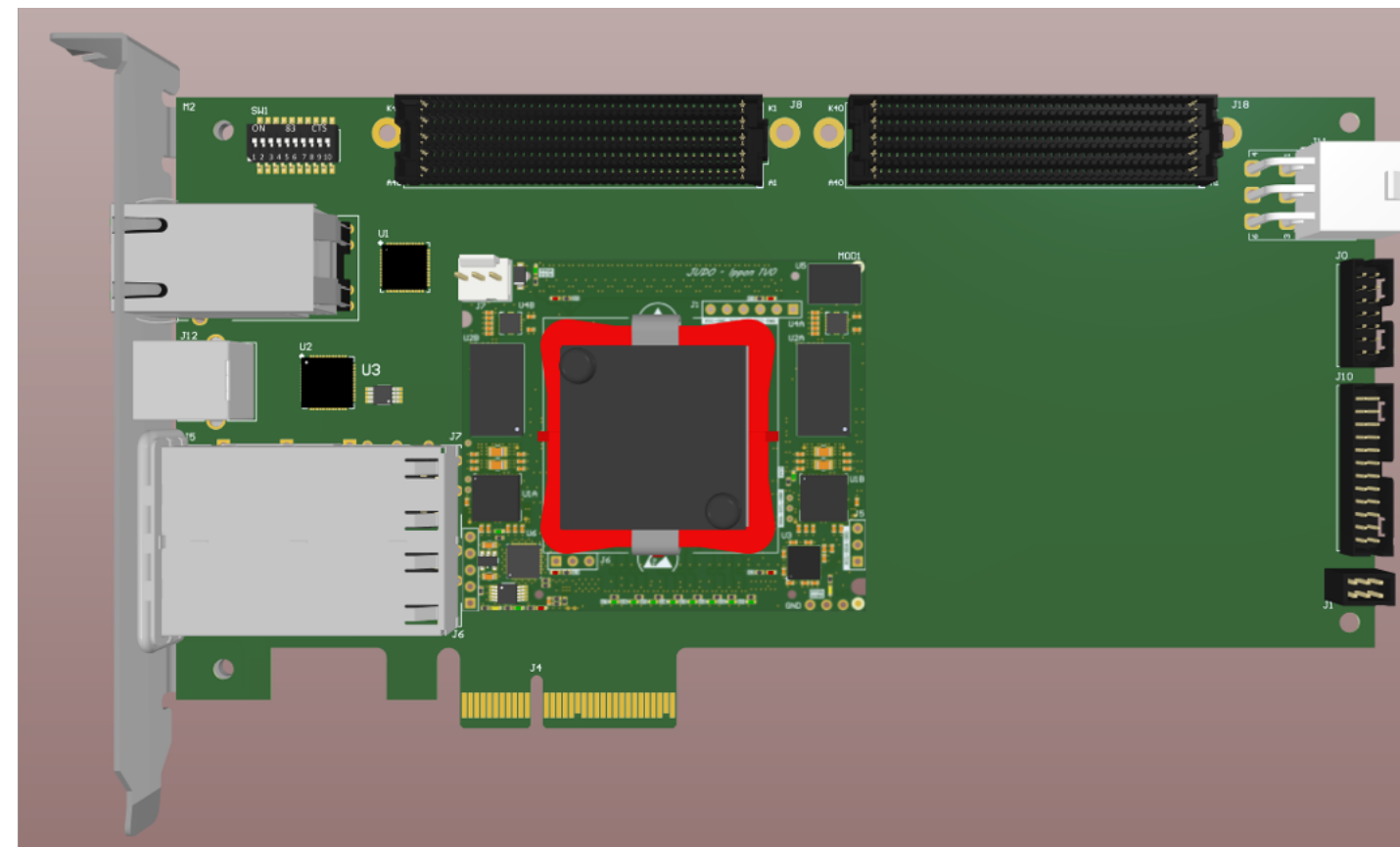
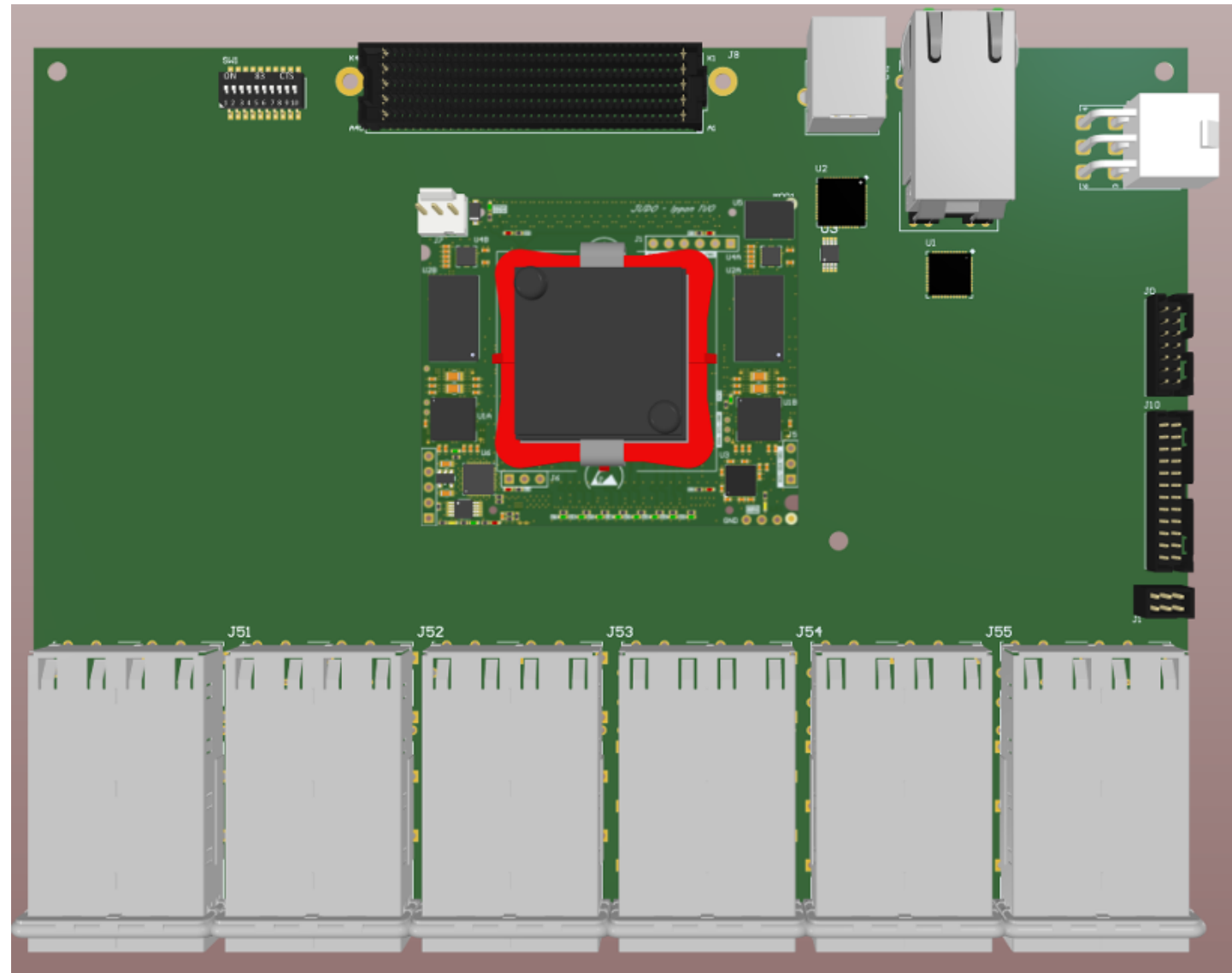
First version of the RDO



This version of the board is the first test article:

- Compatible with all the DB previously
- Develop the required DAM-RDO interface IP
- User IP can be developed by all the detector groups:
 - We could provide support
- Fast production (can be readily available soon)
- Cost effective board to start real detector applications

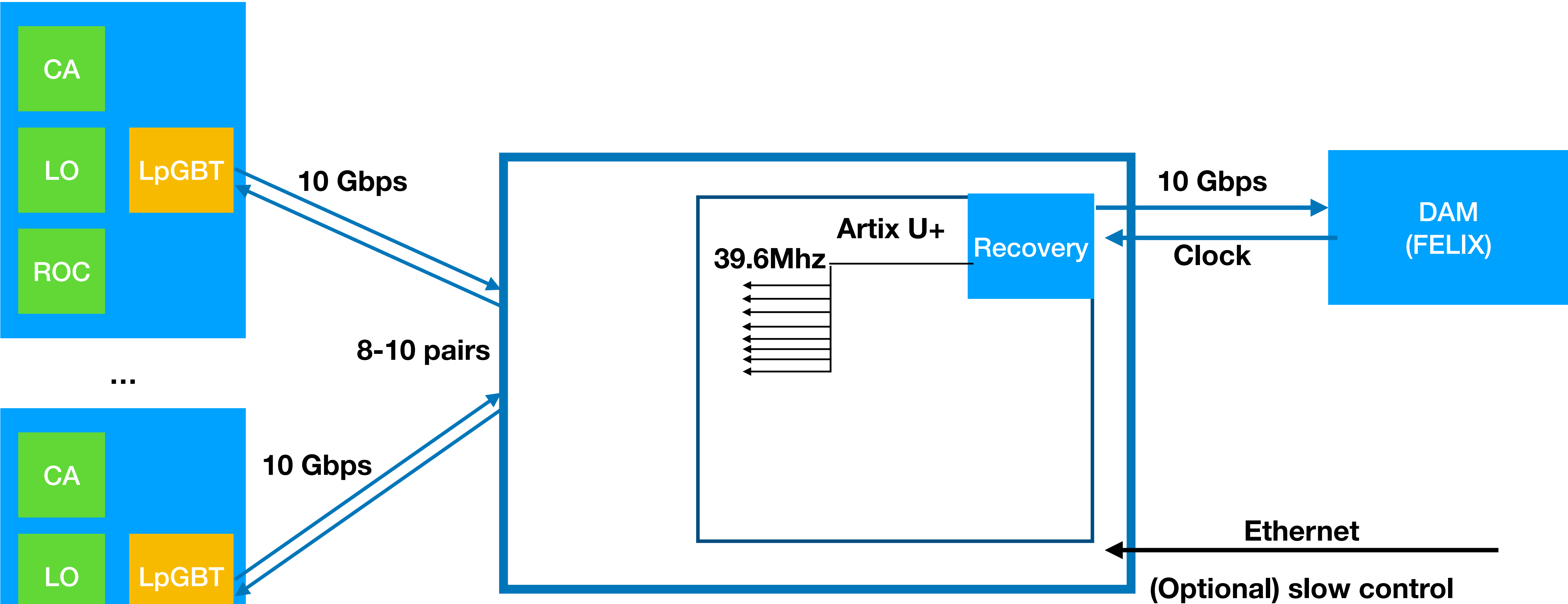
Different daughter board proposals



Some other ideas of the mother boards, these are just conceptual

We would leave the mother board in the hand of the detector people, depending what FEB they are connecting to

Specific proposal for Calorimetry (using the CALOROC)



Configuration	2 Con. Version	3 Con. Version
-	46 HP Diff.	70 HP Diff.
H2GCROC (Full)	5	8
H2GCROC (Full), Ext CLK	6	10
H2GCROC (Full), TC9	7	11
H2GCROC (Full), Ext CLK, TC9	9	14

Slow Control (Software)

FPGA 0

ASIC 0

ASIC 1

Robot Mode

Human Mode

-- Top Register --

Top

-- Global Analog Register

Global_Analog_1

Global_Analog_0

-- Reference Voltage Regi

Reference_Voltage_1

Reference_Voltage_0

-- Master TDC Registers -

Master_TDC_1

Master_TDC_0

-- Digital Half Registers

Digital_Half_1

Digital_Half_0

-- Channel Wise Registers

CM_2

CM_3

Channel_36

Channel_37

Channel_38

Channel_39

Channel_40

Channel_41

Channel_42

Channel_43

Channel_44

Channel_45

Channel_46

Channel_47

Channel_48

Channel_49

Channel_50

Channel_51

Channel_52

Channel_53

Channel_54

Channel_55

Channel_56

Channel_57

Channel_58

Channel_59

Channel_60

Channel_61

Channel_62

Channel_63

Channel_64

Channel_65

Channel_66

Channel_67

Channel_68

Channel_69

Register: Channel_54

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte Gain_conv<1>	Gain_conv<0>	Inputdac<5>	Inputdac<4>	Inputdac<3>	Inputdac<2>	Inputdac<1>	Inputdac<0>	
0	0	0	0	0	0	0	0	0
Byte trim_toa<5>	trim_toa<4>	trim_toa<3>	trim_toa<2>	trim_toa<1>	trim_toa<0>	sel_trig_t oa	mask_toa	
1	0	0	0	0	0	0	0	0
Byte trim_tot<5>	trim_tot<4>	trim_tot<3>	trim_tot<2>	trim_tot<1>	trim_tot<0>	NA	NA	
2	0	0	0	0	0	0	0	0
Byte trim_inv<5>	trim_inv<4>	trim_inv<3>	trim_inv<2>	trim_inv<1>	trim_inv<0>	probe_noinv	probe_inv	
3	0	0	0	0	0	0	0	0
Byte probe_toa	probe_tot	mask_tot	sel_trig_t ot	Channel_off	HighRange	LowRange	probe_pa	
4	0	0	0	0	0	0	1	0
Byte mask_adc	NA	DAC_CAL_CT DC_TOT<5>	DAC_CAL_CT DC_TOT<4>	DAC_CAL_CT DC_TOT<3>	DAC_CAL_CT DC_TOT<2>	DAC_CAL_CT DC_TOT<1>	DAC_CAL_CT DC_TOT<0>	
5	0	0	0	0	0	0	0	0
Byte HZ_inv	HZ_noinv	DAC_CAL_CT DC_TOA<5>	DAC_CAL_CT DC_TOA<4>	DAC_CAL_CT DC_TOA<3>	DAC_CAL_CT DC_TOA<2>	DAC_CAL_CT DC_TOA<1>	DAC_CAL_CT DC_TOA<0>	
6	0	0	0	0	0	0	0	0
Byte NA	NA	DAC_CAL_FT DC_TOT<5>	DAC_CAL_FT DC_TOT<4>	DAC_CAL_FT DC_TOT<3>	DAC_CAL_FT DC_TOT<2>	DAC_CAL_FT DC_TOT<1>	DAC_CAL_FT DC_TOT<0>	
7	0	0	0	0	0	0	0	0
Byte NA	NA	DAC_CAL_FT DC_TOA<5>	DAC_CAL_FT DC_TOA<4>	DAC_CAL_FT DC_TOA<3>	DAC_CAL_FT DC_TOA<2>	DAC_CAL_FT DC_TOA<1>	DAC_CAL_FT DC_TOA<0>	
8	0	0	0	0	0	0	0	0
Byte NA	NA	IN_FTDC_EN CODER_TOA<5>	IN_FTDC_EN CODER_TOA<4>	IN_FTDC_EN CODER_TOA<3>	IN_FTDC_EN CODER_TOA<2>	IN_FTDC_EN CODER_TOA<1>	IN_FTDC_EN CODER_TOA<0>	
9	0	0	0	0	0	0	0	0
Byte DIS_TDC	NA	IN_FTDC_EN CODER_TOT<5>	IN_FTDC_EN CODER_TOT<4>	IN_FTDC_EN CODER_TOT<3>	IN_FTDC_EN CODER_TOT<2>	IN_FTDC_EN CODER_TOT<1>	IN_FTDC_EN CODER_TOT<0>	

-- Current Config --

FPGA selection: FPGA 0

ASIC selection: ASIC 0

-- Register Selection --

☐ Use half-wise registers

☒ Use channel-wise registers

-- Config File Info --

/home/epical/PythonCodes/
NewGit/H2GDAQ

f0a0.json

Synced to File

Load

Save

Save As

-- Link Info --

IP Address: 10.1.2.208

Port: 11000

Ping FPGA

Send Current ASIC Config

Send All Configs

DAQ

Working Folder

/home/epical/PythonCodes/
NewGit/H2GDAQ

Select Folder

Print to Terminal

DAQ Settings

☐ event 100

☐ time [sec] 1

☒ manual

Run Number 35

Data Count 8.46 MB

Set IODELAY

Start DAQ

Stop DAQ

Generator

Debug

--- Data Collection ---

Data Coll En[7:0] 3

Trig Coll En[7:0] 0

--- Generator ---

Gen PreImp En ☒

Gen Pre Int 16

Gen Nr Cycles 1000

Gen Interval 100000

--- External Trigger ---

Ext Trg En ☐

Ext Trg Delay 0

Ext Trg DeadT 255

--- Fast Command ---

DAQ FCMD 75

DAQ Push FCMD 75

Gen Pre FCMD 45

Gen FCMD 75

--- Machine Gun ---

Machine Gun 10

Send Gen Config before DAQ ☐

Send Gen Config

DAQ + Generator START/STOP

DAQ Push

Start Generator

Stop Generator

High Voltage

Reset/Adj

☒ F0 ☒ A0 ☒ A1

Send HV Settings

We already have a H2GCROC/DAQ setting software working with the KCU (RDO+DAM) and H2GCROC protoboards

- We can also adopt this software (based on python3) on the new RDO (+DAM also) and other ASICs too.

Summary

The RDO would be based on Artix Ultrascale+, with possible upgrade to Kintex Ultrascale+ (lower end) if there are some specialized needs

- Mother/daughter card design
 - All designs will be kept within the 'house'
- Mother card are detector specific:
 - In case of calorimeters (CALOROC LpGBT aggregator), it should be unified
 - Other detectors we could help with engineering
- Daughter card
 - Plan to have several of them, interchangeable depending on the scale of the detector and performance needed
 - Support for the RDO-DAM firmware communication
 - Help in RDO-FEB communication if needed

Time line:

- 80h of engineering time already went in to the daughter board, est. 80h more needed
- 80-100h for the first iteration of the daughter board
 - This can be an evaluation platform for many detectors (testbeam support)
 - Can help with more specialized daughterboard (e.g. two FMC for TOF)
- How many should we produce - PED request