OAK RIDGE National Laboratory

RDO concept

Miklos Czeller, Gabor Nagy

Norbert Novitzky

Goals for the Readout Board

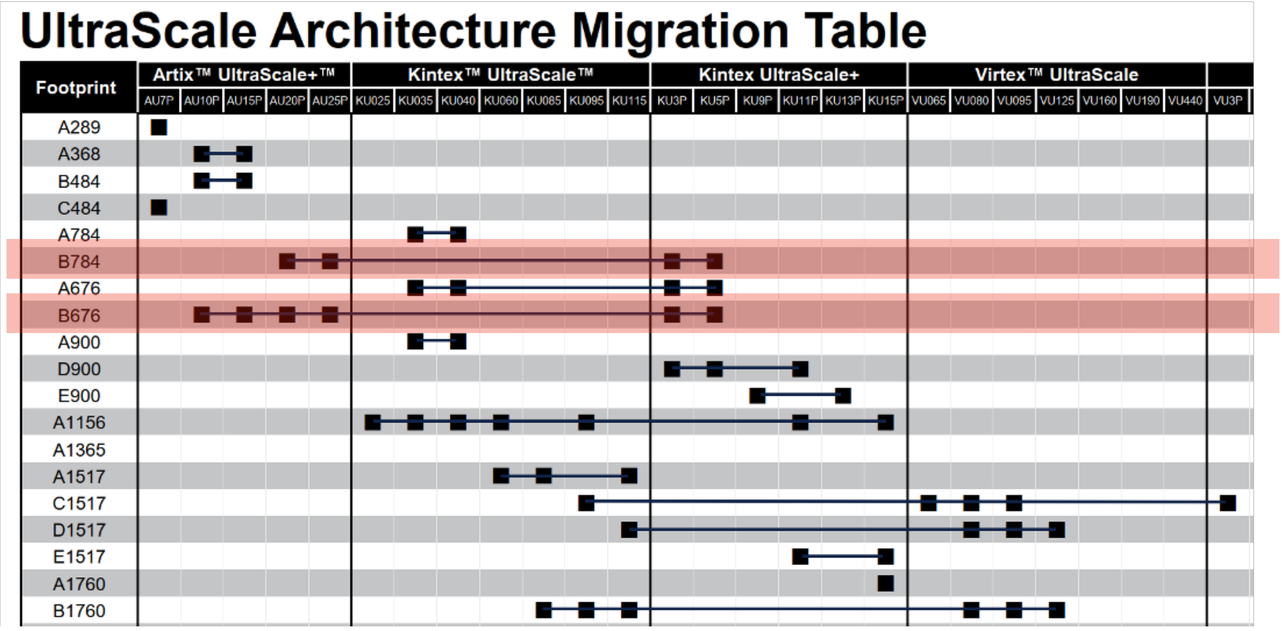
- **Design a versatile Readout Board to be used in all detectors:**
  - Collection of the data from FEB's
  - Aggregation of data
  - Suitable for the streaming data acquisition
  - Adaptable for all detectors
    - Design and support will be kept in the collaboration

- **Constraints:**
  - Price, based on the Artix Ultrascale+ family
  - Scalable to larger systems
  - Size for some of the detectors

FPGA choices

Basic choice is the Artix Ultrascale+ family:

- ~300-500$
- Long-term availability (in the next decade)
- Scalability of the system:
  - From Artix even up to the Kintex capability



The footprints of the selected FPGA's are the same:

- B676 - 1mm pitch
- B784 - 0.8mm pitch

The pitch correlates with the size and cost (complexity) of the PCB
The large FPGA family coverage in the footprint enables to have interchangeable designs

FPGA consideration

B676 Package, 1mm pitch

#	Part Number	Unit Price $	Logic Cells	DSP	36K	HP	HD	GTH GTY	PCIe Gen/Lane
11	XCAU10P-1FFVB676E	185	96 250	400	100	156	72	12	4/4, 3/8
13	XCAU10P-2FFVB676E	259	96 250	400	100	156	72	12	4/4, 3/8
15	XCAU15P-1FFVB676E	231	170 100	576	144	156	72	12	4/4, 3/8
17	XCAU15P-2FFVB676E	324	170 100	576	144	156	72	12	4/4, 3/8
19	XCAU20P-1FFVB676E	334	238 437	900	200	156	72	12	4/8
21	XCAU20P-2FFVB676E	467	238 437	900	200	156	72	12	4/8
23	XCAU25P-1FFVB676E	398	308 437	1200	300	208	72	12	4/8
25	XCAU25P-2FFVB676E	557	308 437	1200	300	208	72	12	4/8
27	XCKU3P-1FFVB676E	1 405	355 950	1368	360	208	72	16	4/8
29	XCKU3P-2FFVB676E	2 054	355 950	1368	360	208	72	16	4/8
31	XCKU5P-1FFVB676E	2 055	474 600	1824	480	208	72	16	4/8
33	XCKU5P-2FFVB676E	2 731	474 600	1824	480	208	72	16	4/8

B784 Package, 0.8mm pitch

#	Part Number	Unit Price $	Logic Cells	DSP	36K	HP	HD	GTY	PCIe Gen/Lane
19	XCAU20P-1SFVB784E	305	238 437	900	200	156	72	12	4/8
21	XCAU20P-2SFVB784E	428	238 437	900	200	156	72	12	4/8
23	XCAU25P-1SFVB784E	388	308 437	1200	300	208	96	12	4/8
25	XCAU25P-2SFVB784E	543	308 437	1200	300	208	96	12	4/8
27	XCKU3P-1SFVB784E	1 466	355 950	1368	360	208	96	16	4/8
29	XCKU3P-2SFVB784E	2 054	355 950	1368	360	208	96	16	4/8
31	XCKU5P-1SFVB784E	1 976	474 600	1824	480	208	96	16	4/8
33	XCKU5P-2SFVB784E	2 768	474 600	1824	480	208	96	16	4/8

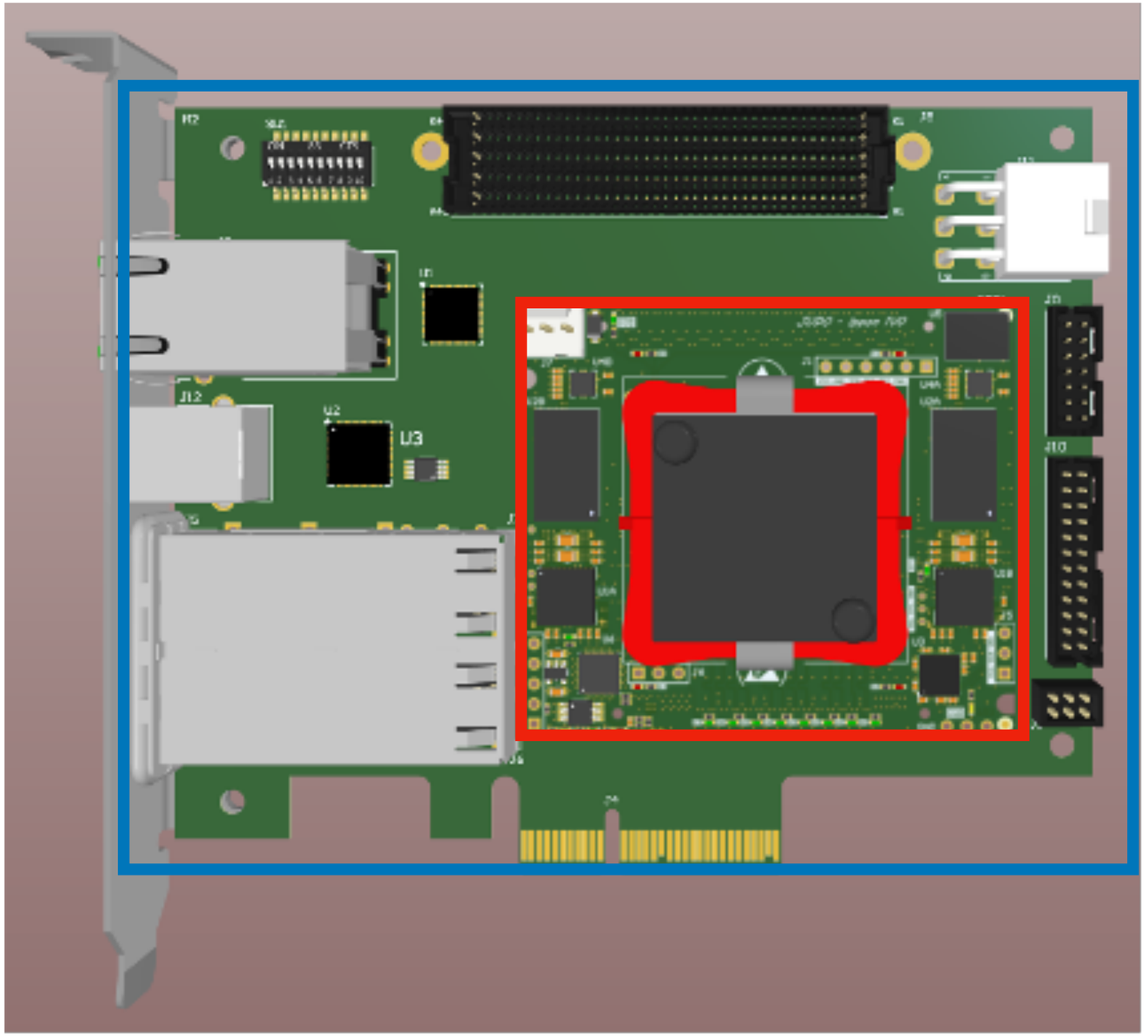
- Difference is in the number of logic cells
  - Depends on the application, e.g. CALOROC we plan the XCAU20P-2…
- DSP capabilities, buffering, clocking
- GTH/GTY = 16.3 Gbps/32.72 Gbps
- Availability:
  - Xilinx/AMD is trusted and long lasting. Typical availability is ~15 years (Ultrascale+ extended 2045)
- 100+ HP/HD pins enables interfacing many different FEB options
- High speed GTx pins would be for LpGBT communication (10Gbps)

Conclusion:

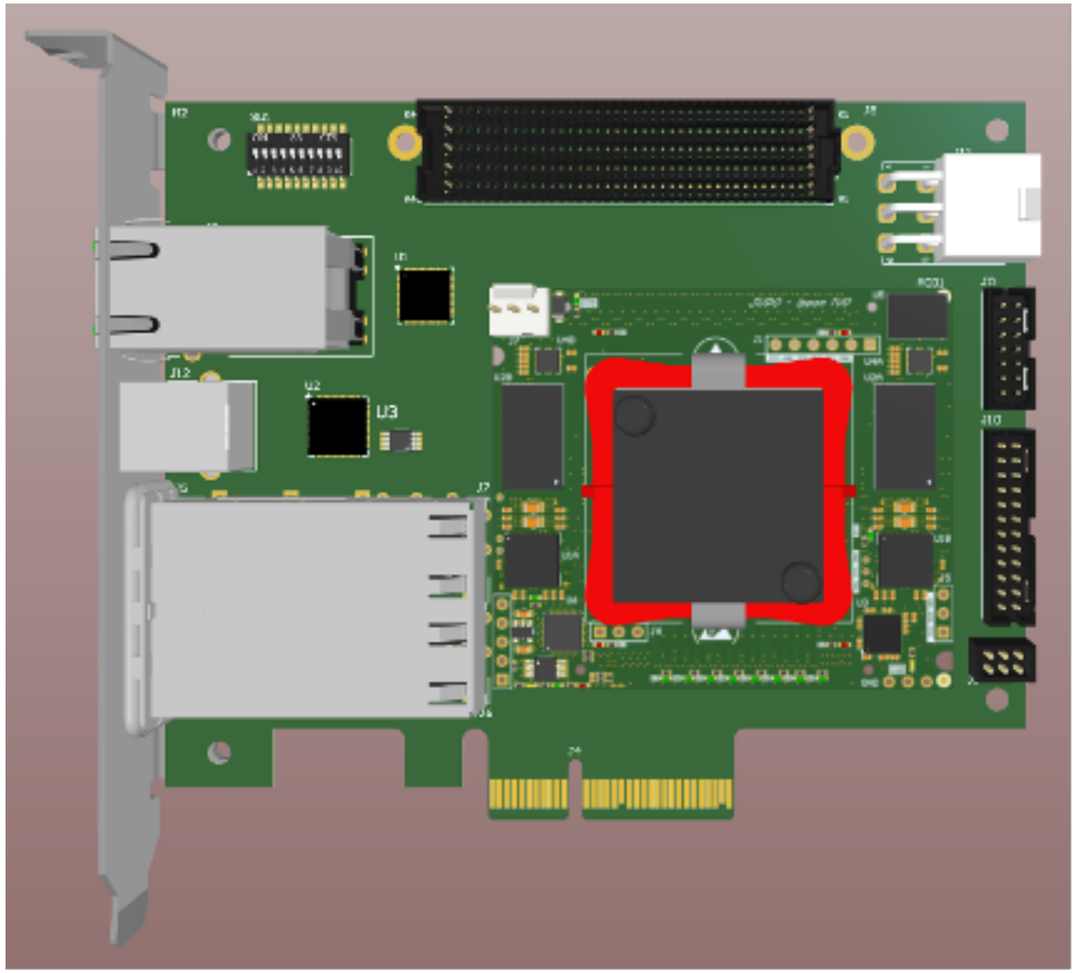
- B676 footprint would be the winner (unless space is a constraint), 1mm pitch helps with the PCB price also and easier production

- AMD UltraScale+ GTH (16.3Gb/s): Low power & high performance for the toughest backplanes
- AMD UltraScale+ GTY (32.75Gb/s): Maximum NRZ performance for the fastest optical and backplane applications;
33G transceivers for chip-to-chip, chip-to-optics, and 28G backplanes
- https://www.amd.com/en/products/adaptive-socs-and-fpgas/technologies/high-speed-serial.html

Basic idea – mother/daughter boards



Basic idea – mother/daughter boards



Mother board:

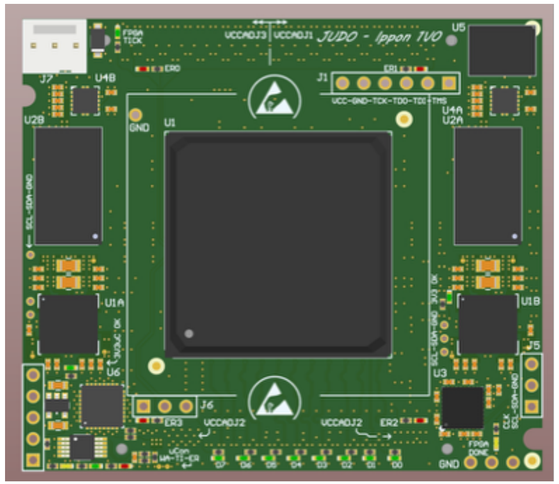
- User specific (or detector specific)
  - Depends highly on the need of a detector
- All connections to the FEB
- All connections to the DAM boards
  - SFP+, firefly or FMC with module
- Power distribution
- Low and high complexity on the clock distribution
- Compatible with the daughter cards

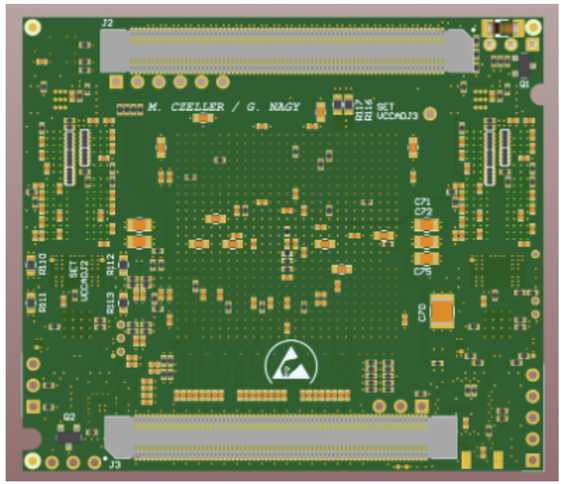
Daughter board:

- Same for every card, interchangeable with different FPGA
- 676 pin package
- 12-16 GTx
- 50+ differential pairs, HP
- 20+ single ended wire, HD
- On board memory (DDR4, optional)
- System controller on the board
- 12 V power input

Proposed daughter boards

Version A - two connector design 62x54mm

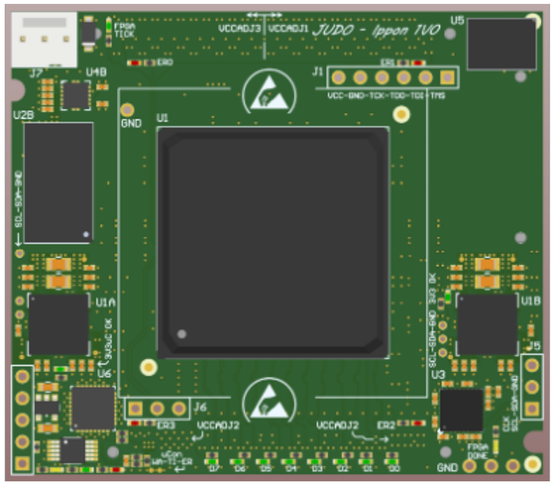


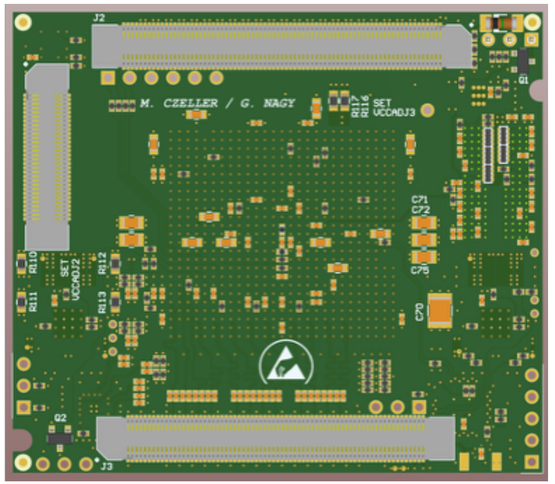


2 connector version, contains 2x independent DDR4 memory chips

46 HP differential pairs, 46x max 1250Mbps
12 MGT, 12x 16.3 Gbps
Ideal for aggregation tasks

Version B - three connector design 62x54mm

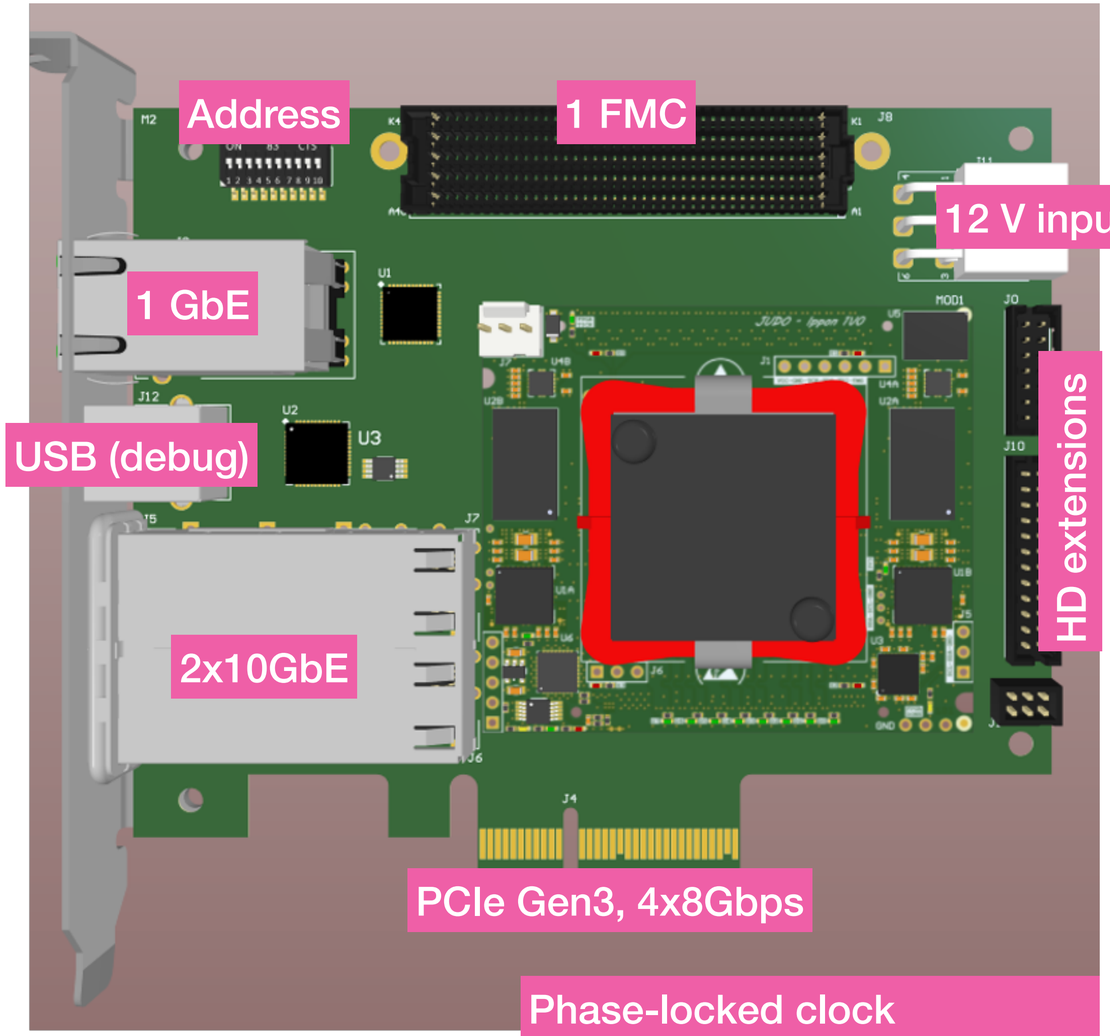




3 connector version, contains 1 independent DDR4 memory chips

46+24 HP differential pairs, 70x max 1250Mbps
12 MGT, 12x 16.3 Gbps
Ideal for interfacing with ASICs

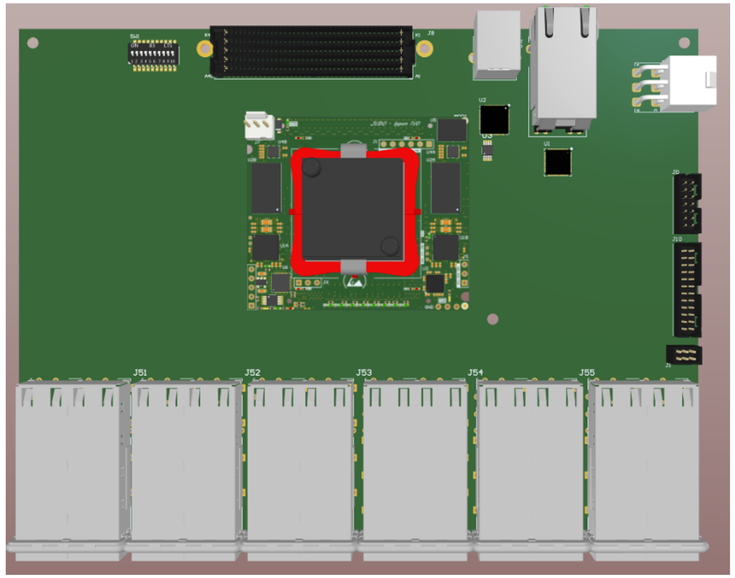
First version of the RDO

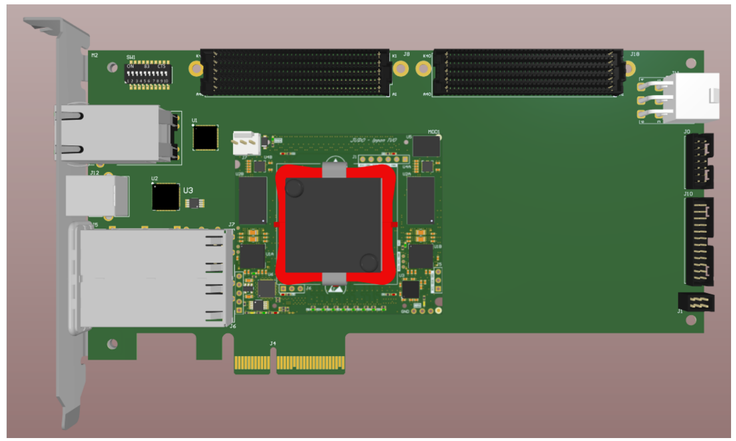


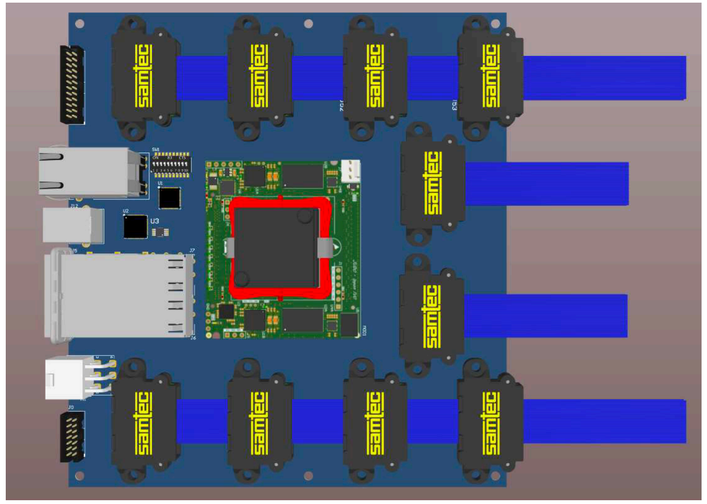
This version of the board is the first test article:

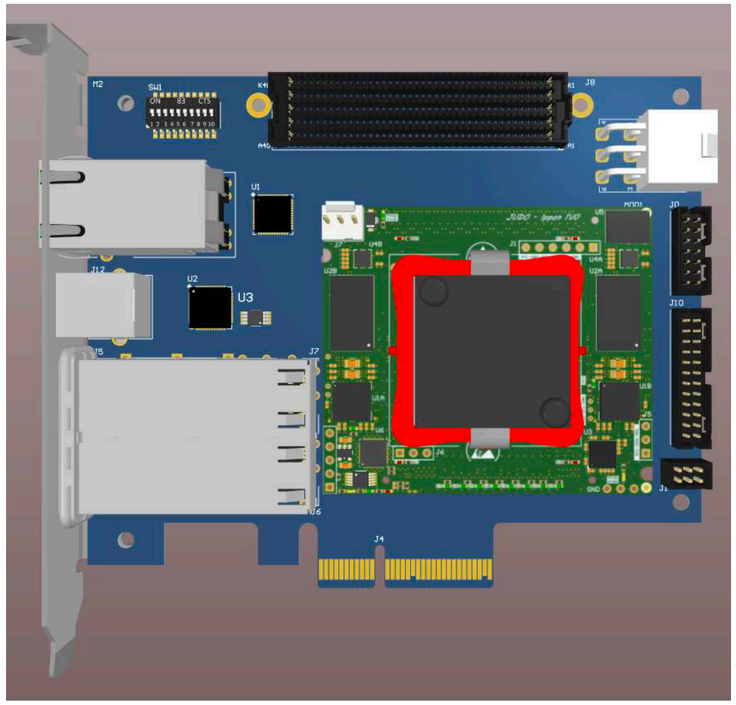
- Compatible with all the DB previously
- Develop the required DAM-RDO interface IP
- User IP can be developed by all the detector groups:
  - We could provide support
- Fast production (can be readily available soon)
- Cost effective board to start real detector applications

Different daughter board proposals





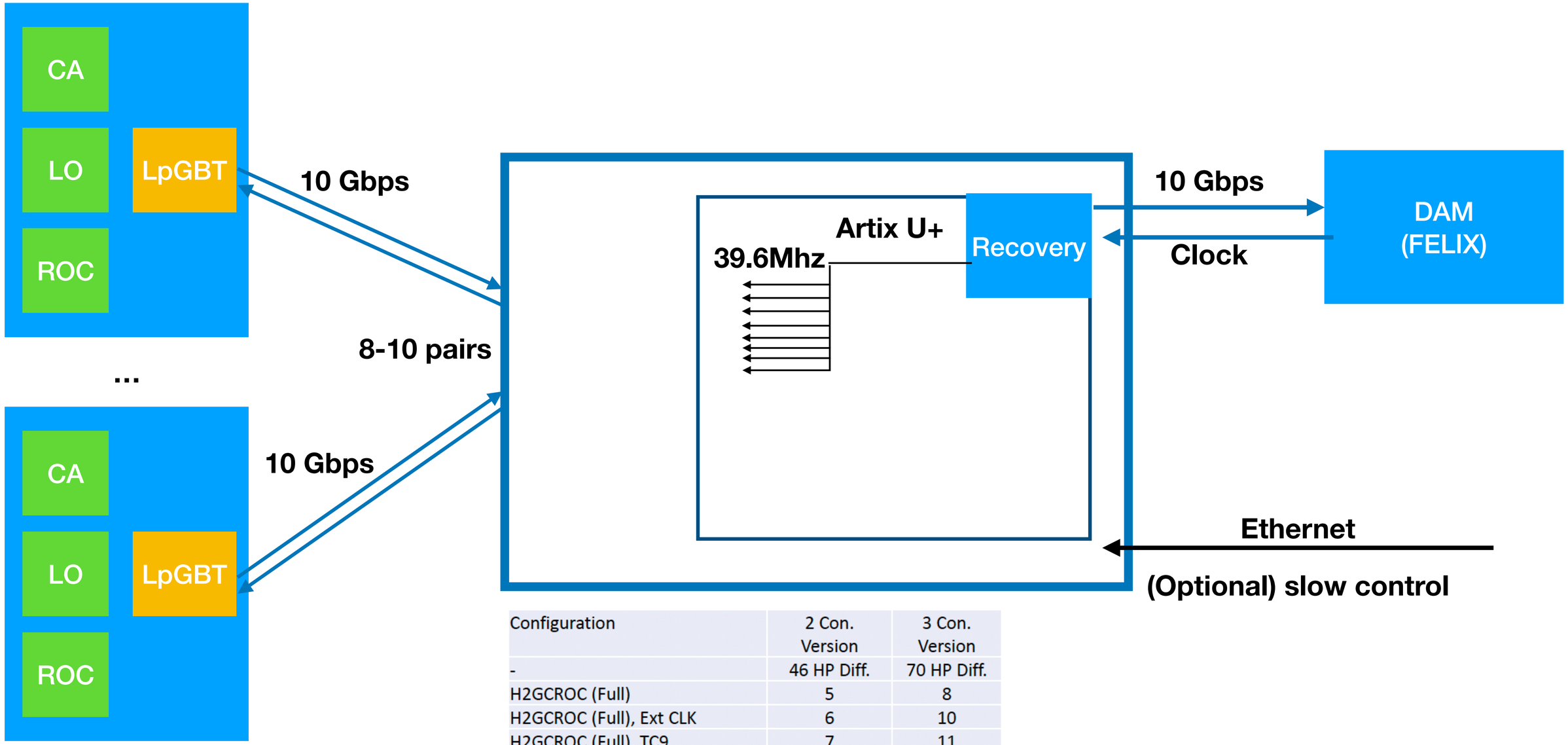




Some other ideas of the mother boards, these are just conceptual

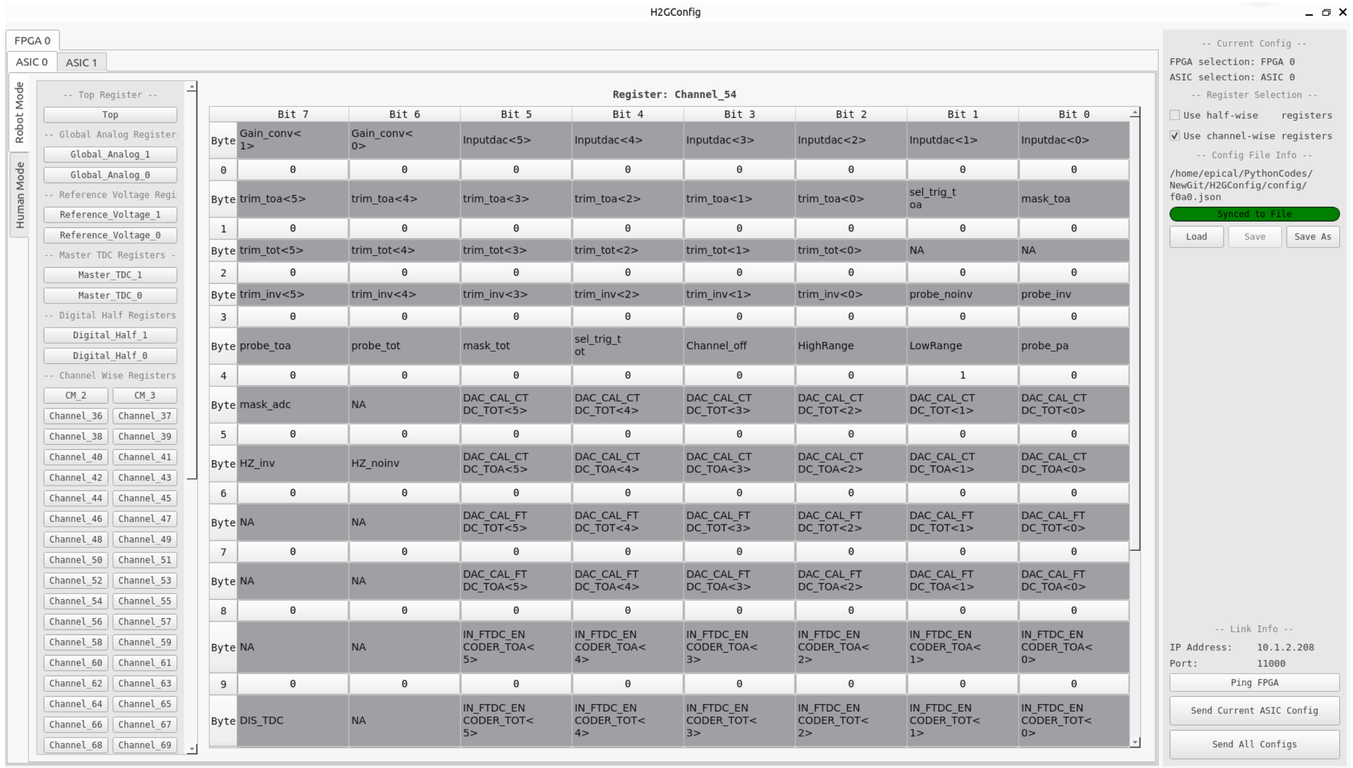
We would leave the mother board in the hand of the detector people, depending what FEB they are connecting to

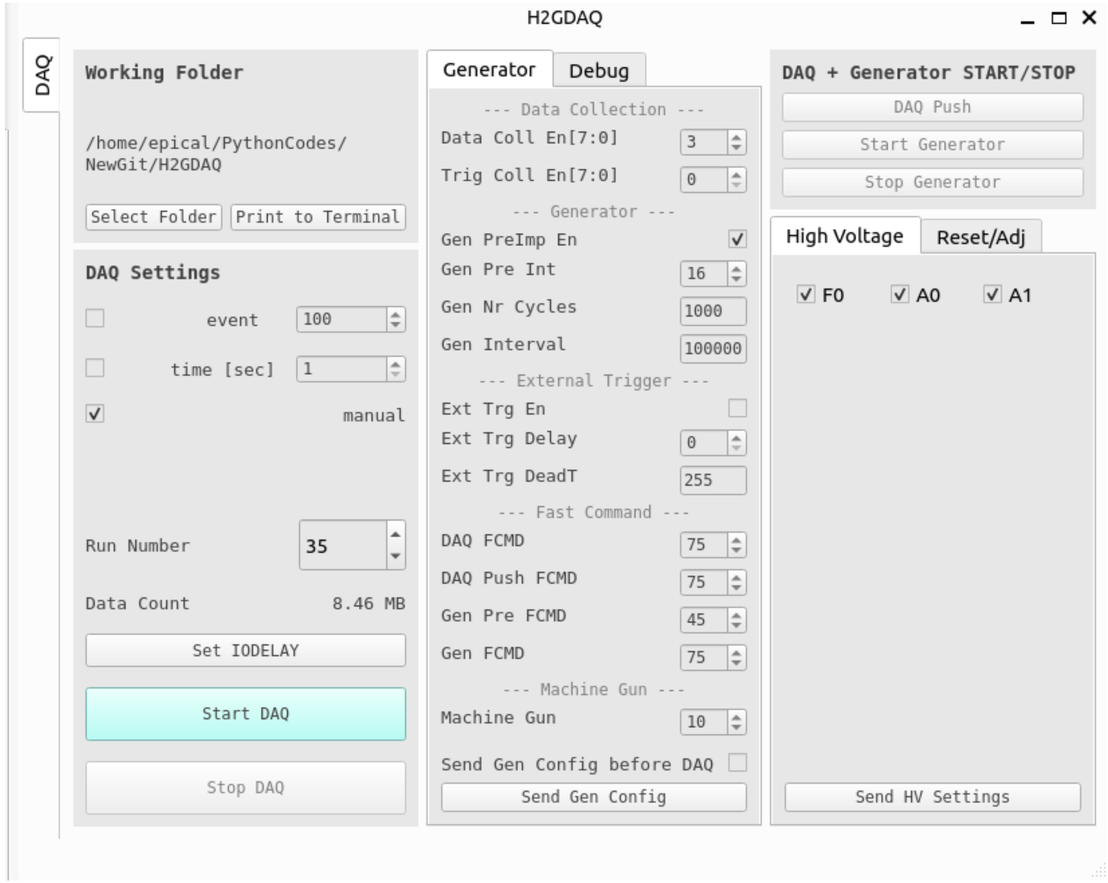
Specific proposal for Calorimetry (using the CALOROC)



Configuration	2 Con. Version	3 Con. Version
-	46 HP Diff.	70 HP Diff.
H2GCROC (Full)	5	8
H2GCROC (Full), Ext CLK	6	10
H2GCROC (Full), TC9	7	11
H2GCROC (Full), Ext CLK, TC9	9	14

Slow Control (Software)





We already have a H2GCROC/DAQ setting software working with the KCU (RDO+DAM) and H2GCROC protoboards

- We can also adopt this software (based on python3) on the new RDO (+DAM also) and other ASICs too.

Summary

The RDO would be based on Artix Ultrascale+, with possible upgrade to Kintex Ultrascale+ (lower end) if there are some specialized needs

- Mother/daughter card design
  - All designs will be kept within the ‘house’
- Mother card are detector specific:
  - In case of calorimeters (CALOROC LpGBT aggregator), it should be unified
  - Other detectors we could help with engineering
- Daughter card
  - Plan to have several of them, interchangeable depending on the scale of the detector and performance needed
  - Support for the RDO-DAM firmware communication
  - Help in RDO-FEB communication if needed

Time line:

- 80h of engineering time already went in to the daughter board, est. 80h more needed
- 80-100h for the first iteration of the daughter board
  - This can be an evaluation platform for many detectors (testbeam support)
  - Can help with more specialized daughterboard (e.g. two FMC for TOF)
- How many should we produce - PED request