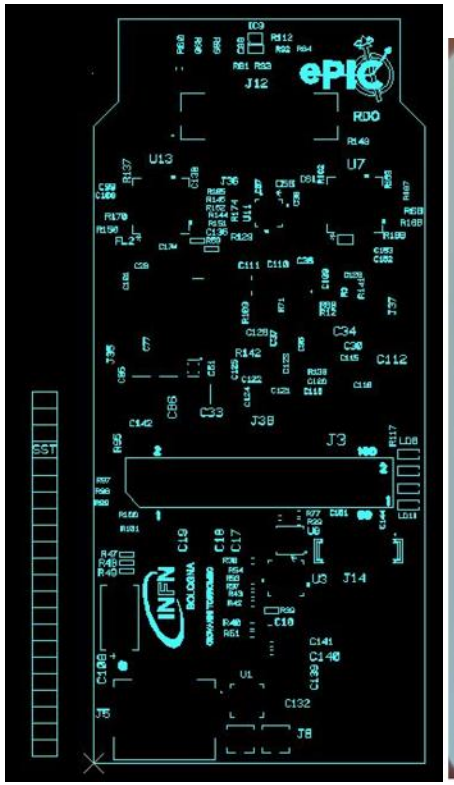
dRICH RDO

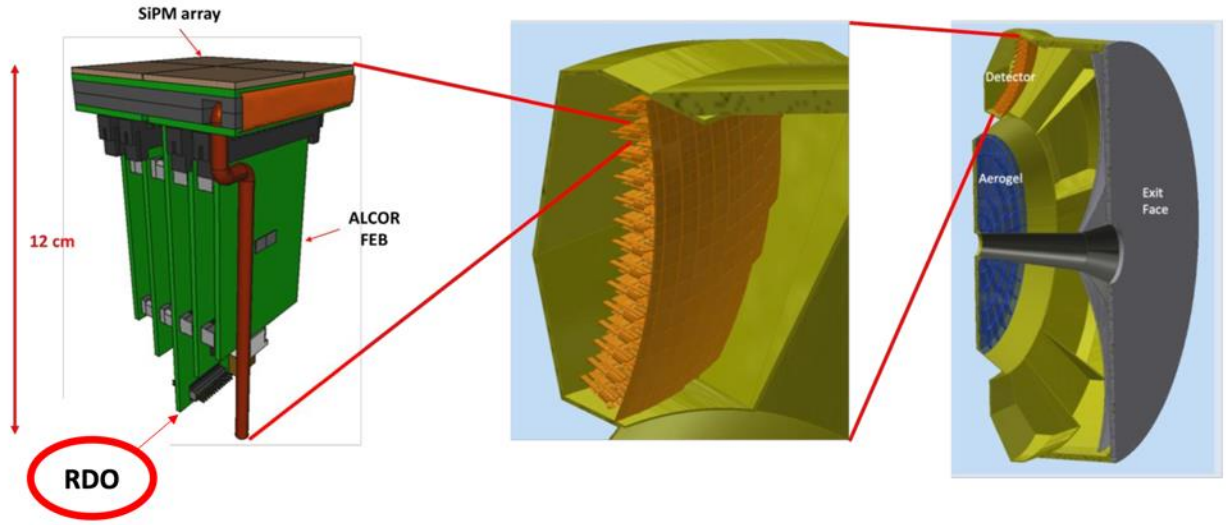


P. Antonioli , D. Falchieri, S. Geminiani,
L. Rignanese, G. Torromeo (INFN Bologna)

+ all the dRICH team (with a special reference to Rome1/2 colleagues)

EICUG/ePIC Meeting
JLab 14-18 July 2025

dRICH RDO

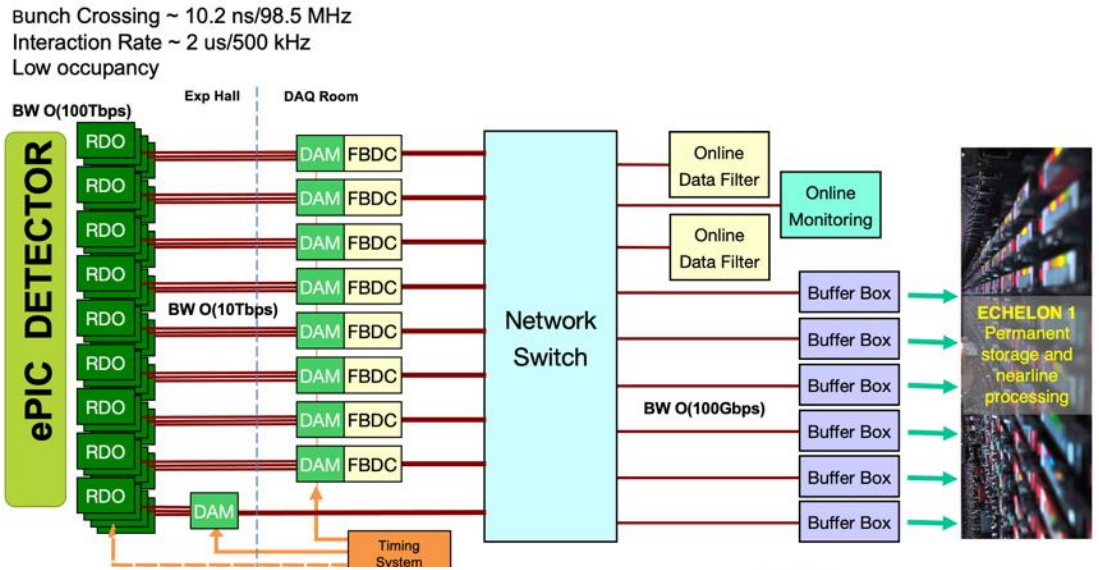


- R&D and design choices for dRICH RDO ePIC
- miscellanea progresses and points of attention:
  - firmware
  - radiation tests
  - power consumption

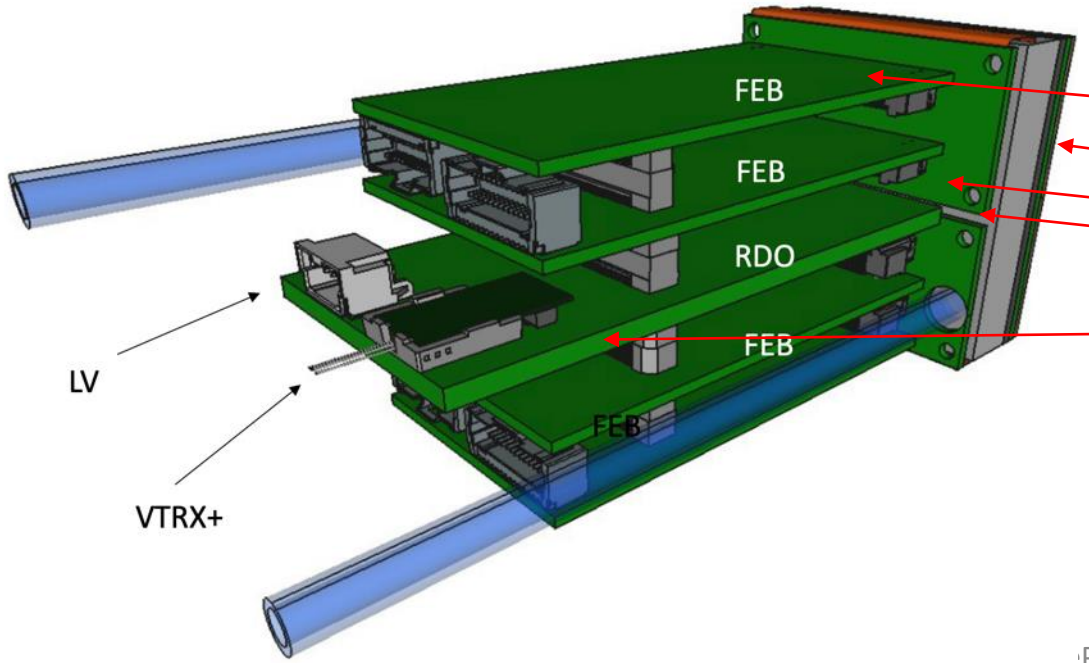
  } *updates already given @eRD109/ePIC DAQ meetings*
- plannning and validation tests (including 2026 activities) → match with “picoDAQ”
- which link DAM-RDO protocol for dRICH?

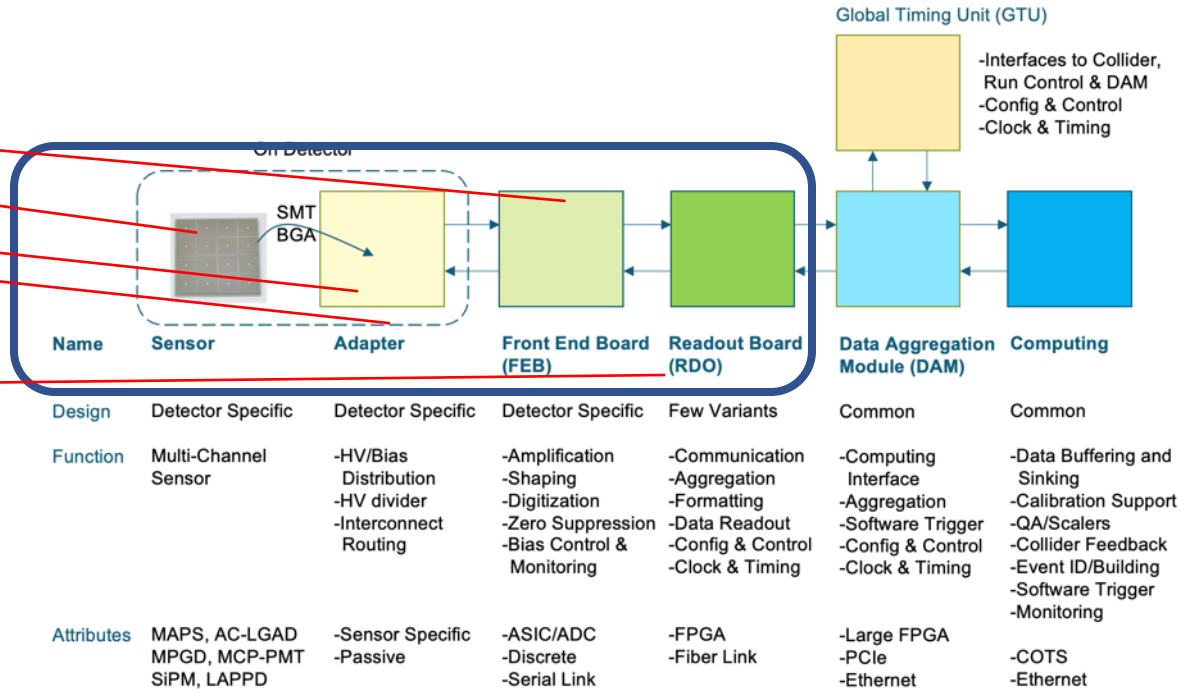
Emphasis: ”lessons learned planning picoDAQ→microDAQ → miniDAQ”

RDO role in ePIC and dRICH PDU

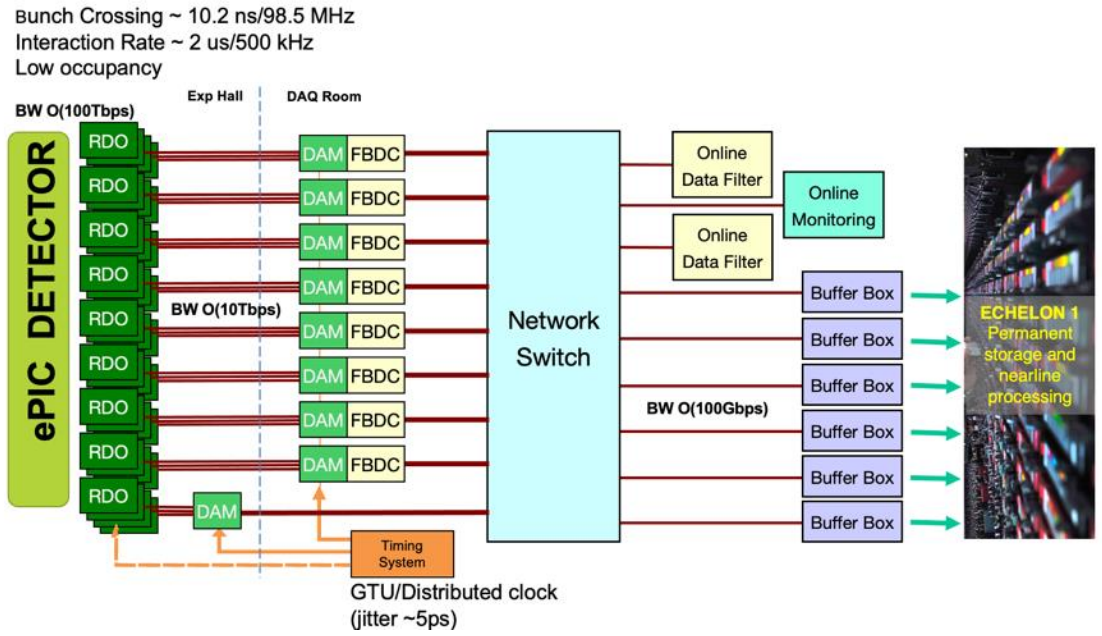


RDO as interface between detector specific ASIC and ePIC DAQ

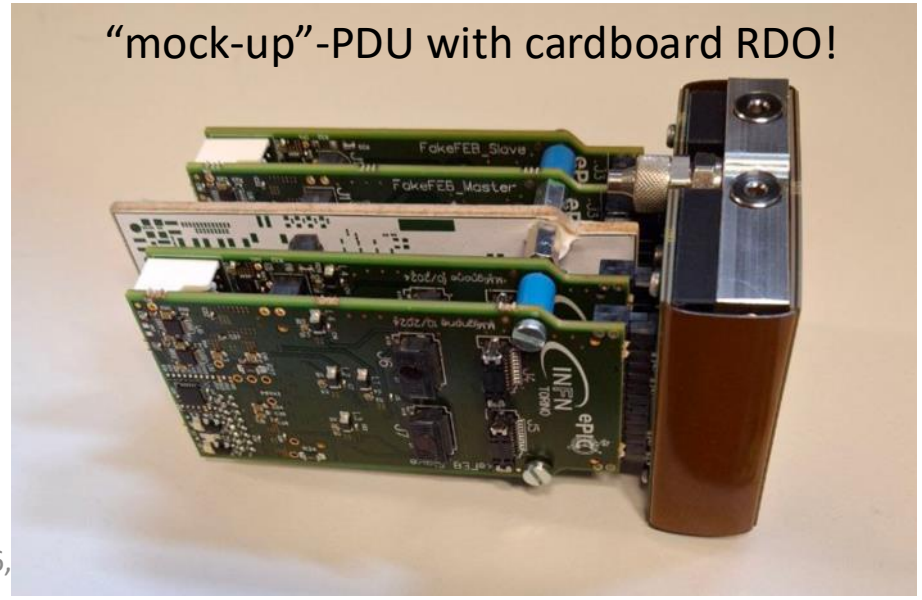


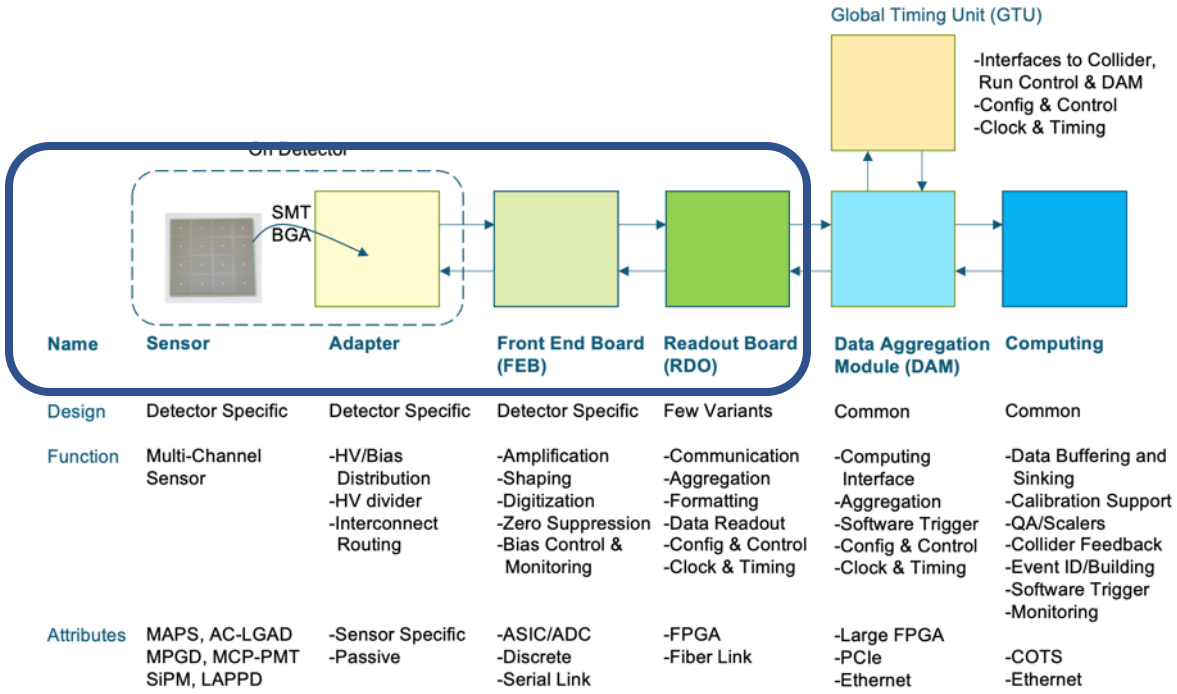


RDO role in ePIC and dRICH PDU



RDO as interface between detector specific ASIC and ePIC DAQ

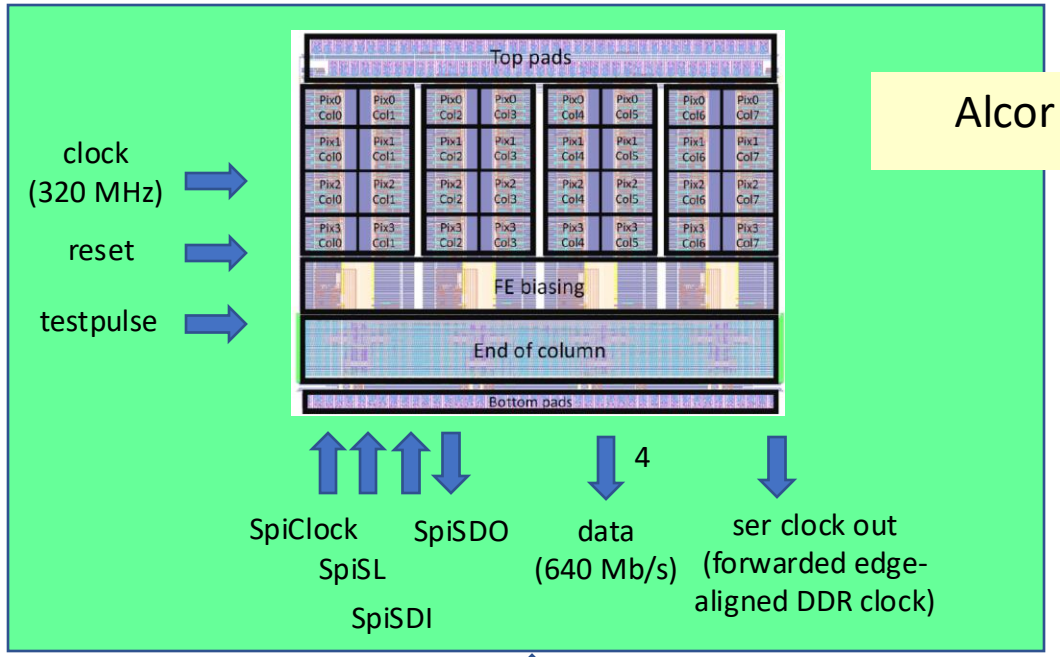




R&D toward RDO: reading the ASIC (I)

We started in 2021 reading out 1 Alcor chip, we needed to choose:

- FPGA board
- interface board
- interconnection cables



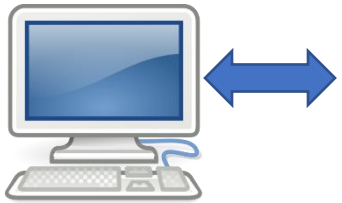
Alcor chip board

12 differential pairs (LVDS)

interface board

custom board

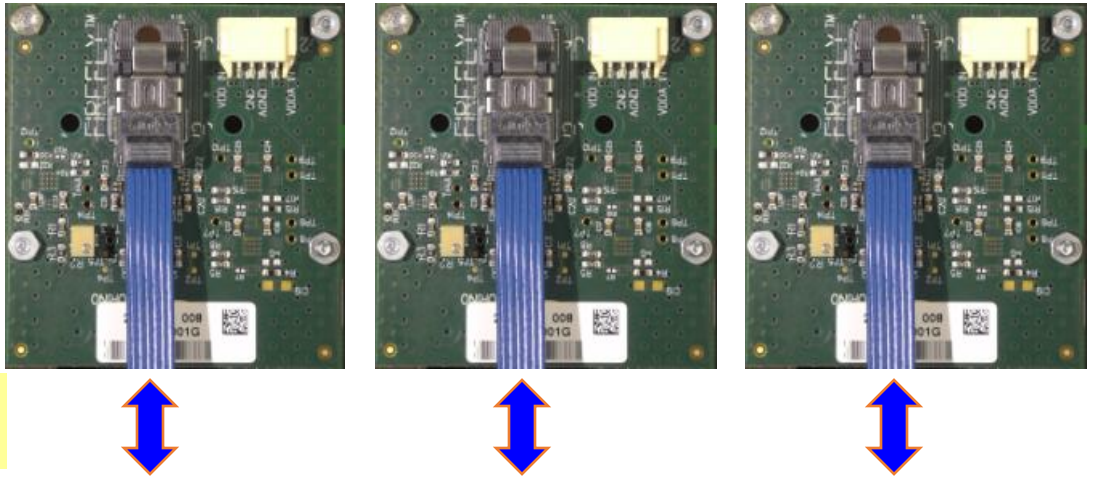
split the problem and be commercial as much as you can



FPGA board

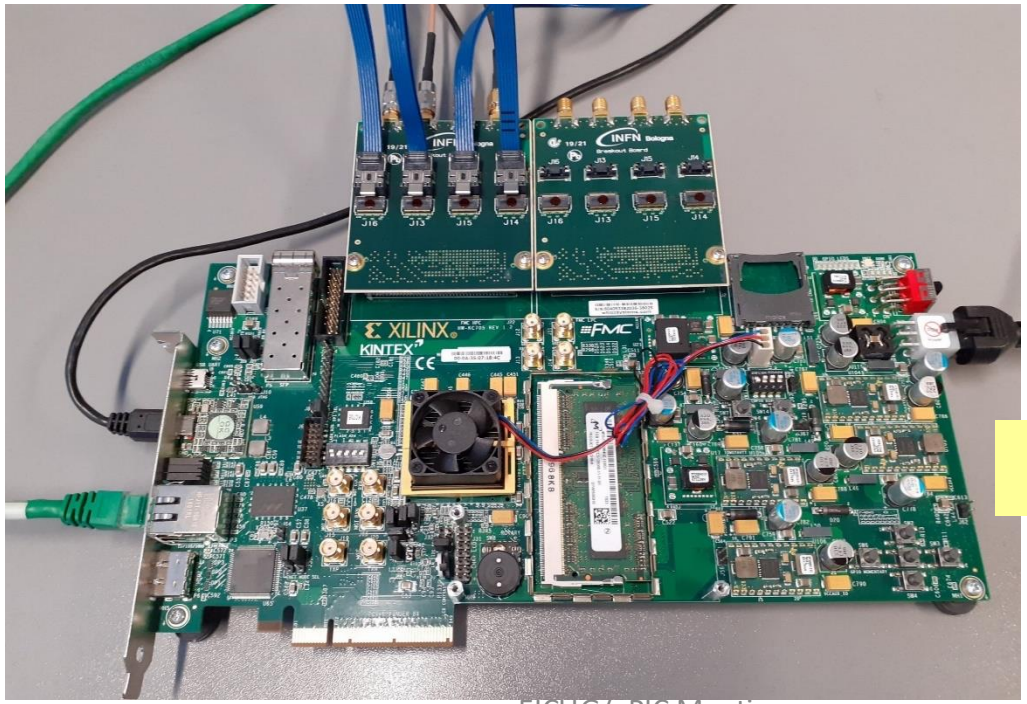
off-the-shelf

R&D toward RDO: reading the ASIC (II)



Alcor front end boards

Samtec Firefly cables



custom FMC→ Firefly breakout board

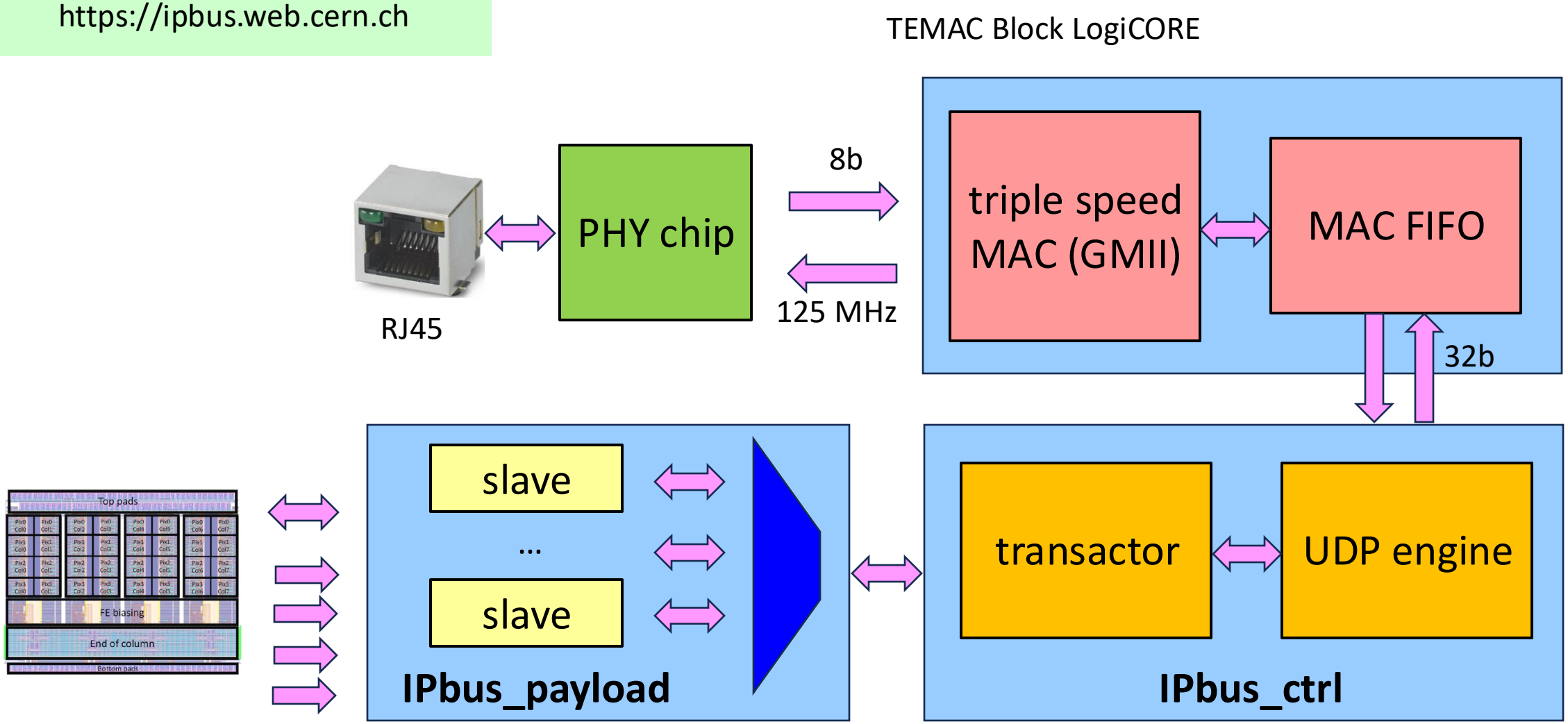
1 Gb ETH

CERN IPbus

FPGA board KC705

initial RDO R&D: link protocol

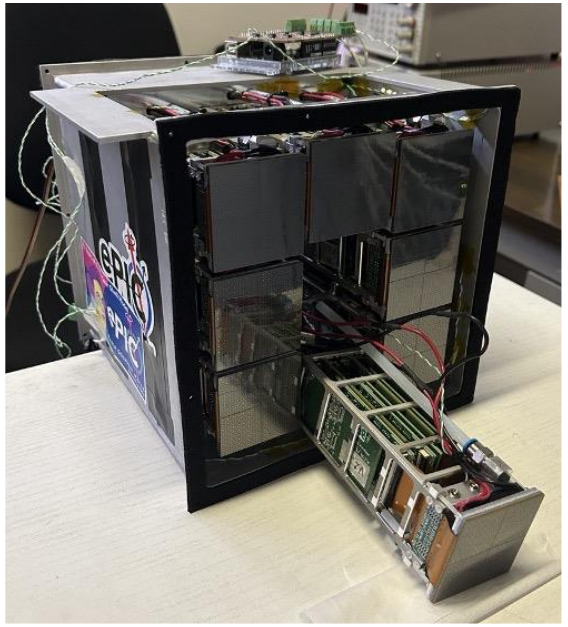
https://ipbus.web.cern.ch

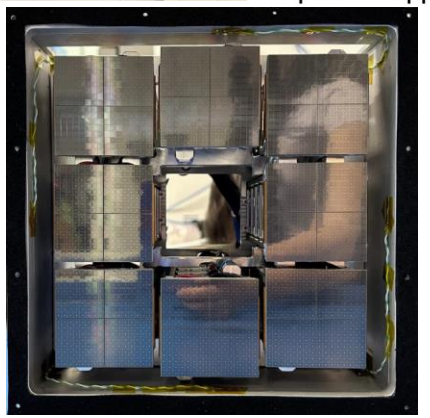


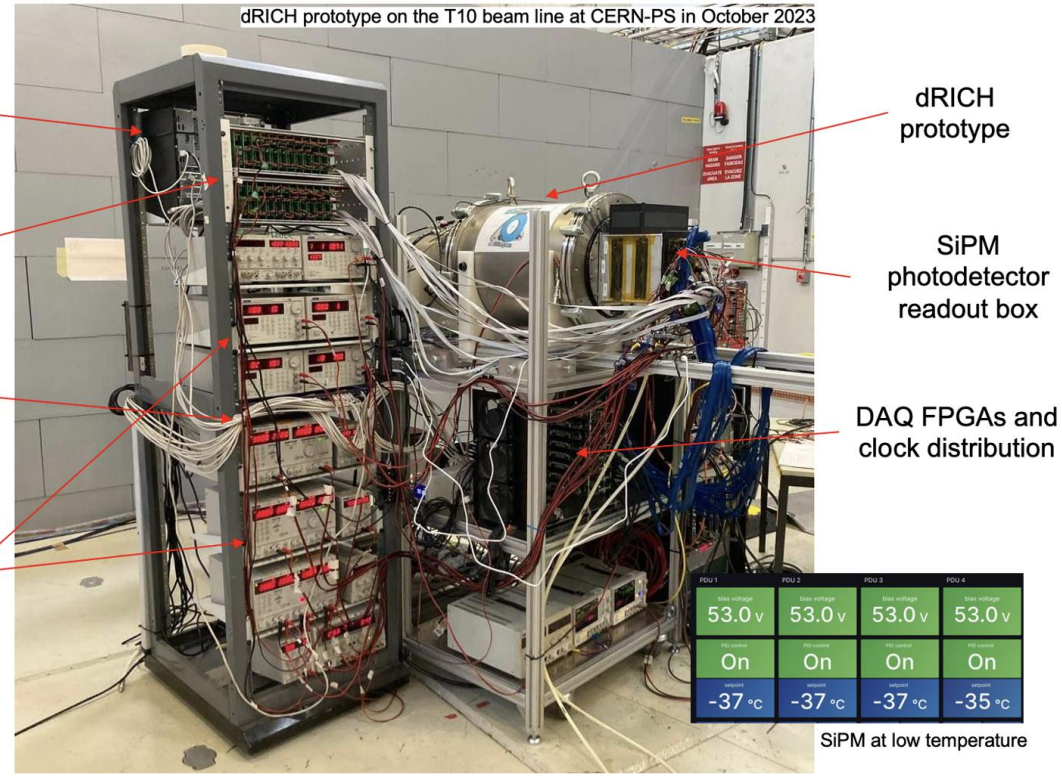
The firmware uses the CERN IPbus UDP-based core, which allows one to easily exploit the Ethernet port for receiving/transmitting data (and using easily cheap network infrastructure)

an easy ready-to-start protocol was key to start fast

scale up to a test beam up to 2 kchannels







11 KC705 FPGA boards in parallel ➔ 64 AlCOR chips ➔2048 SiPMs

next step is bringing readout inside the PDU (RDO comes after)

requirements & design choices for dRICH RDO

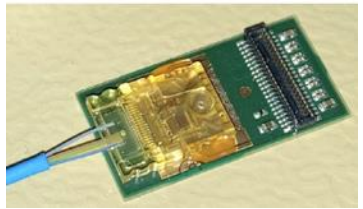
dRICH RDO requirements (from DAQ PDR review June 2024)

- **space**: 40 x 90 mm area
- RDO not accessible: **remote firmware upgrade** must be possible

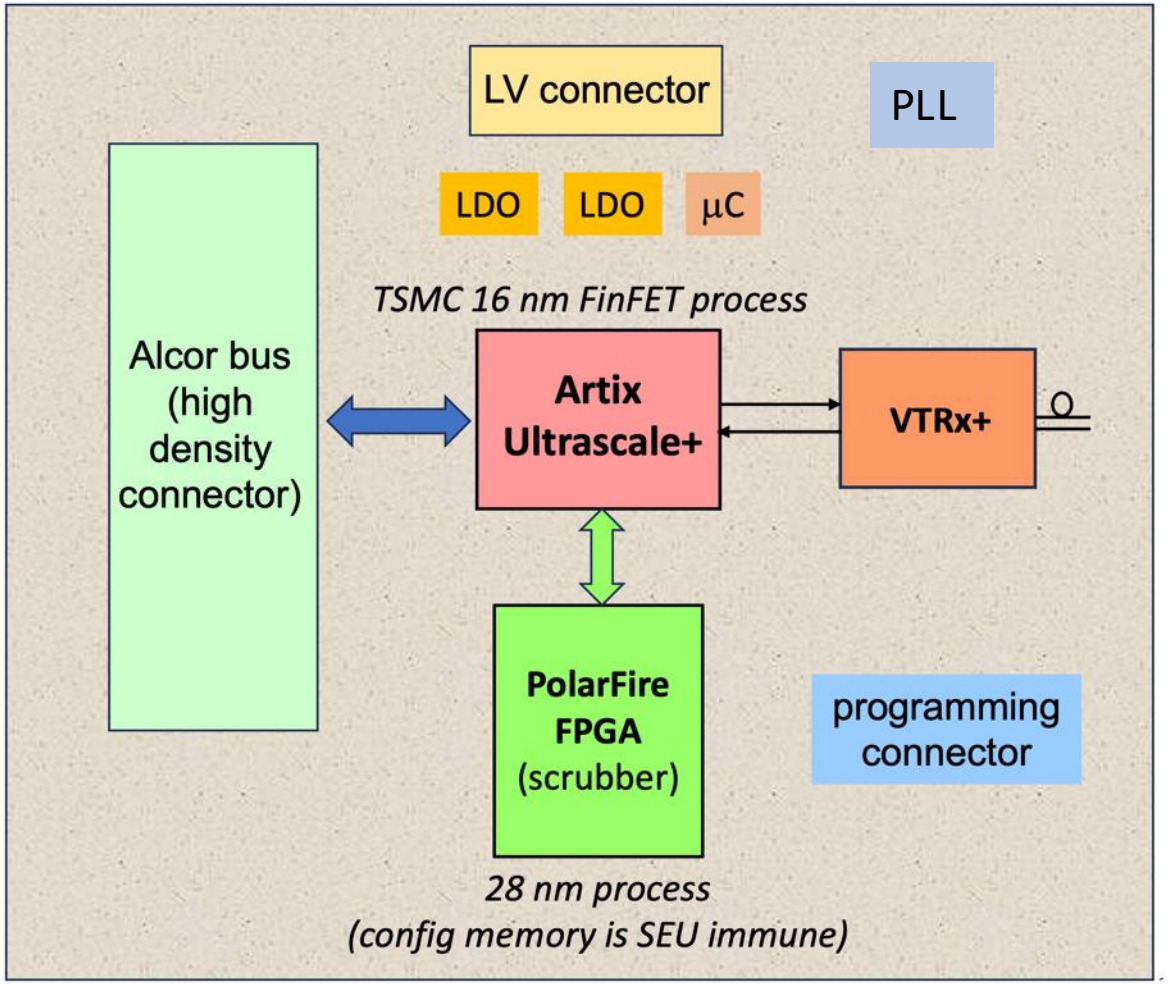
- RDO FPGA need **high speed** (“high performance”) 120 I/O pins to implement ALCOR bus (for TOP/BOTTOM FEB)
- RDO connector need high speed specs. and (minimum) 60 I/O pins each

- RDO must implement clean **clock** multiplication by factor 4 (ALCOR@394 MHz, EIC clock 98.5 MHz)
- RDO must reconstruct clock via optical link
- RDO must produce clean clock (minimize jitter)

- opt. tranceiver must minimize space/power consumption + “rad hard” and bandwitdh up to 10 Gbps (we have been the first pointing to VTRX+ in ePIC!)



requirements and design choices for dRICH RDO



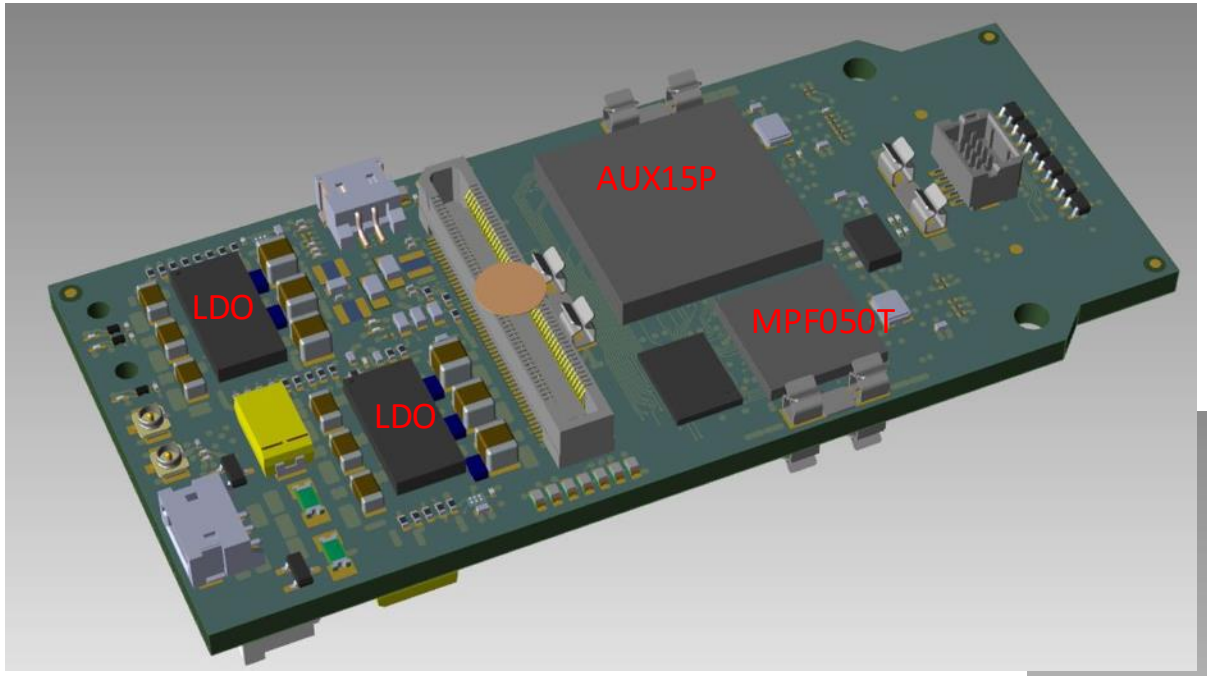
- a performing new generation FPGA (US+) + scrubbing
- devoted PLL to manage clock (SkyWorks 5319 / 5326)
- VTRX+ as optical tranceiver

Long and painful elaboration of exact RDO requirements + detailing project + components selection + layout time

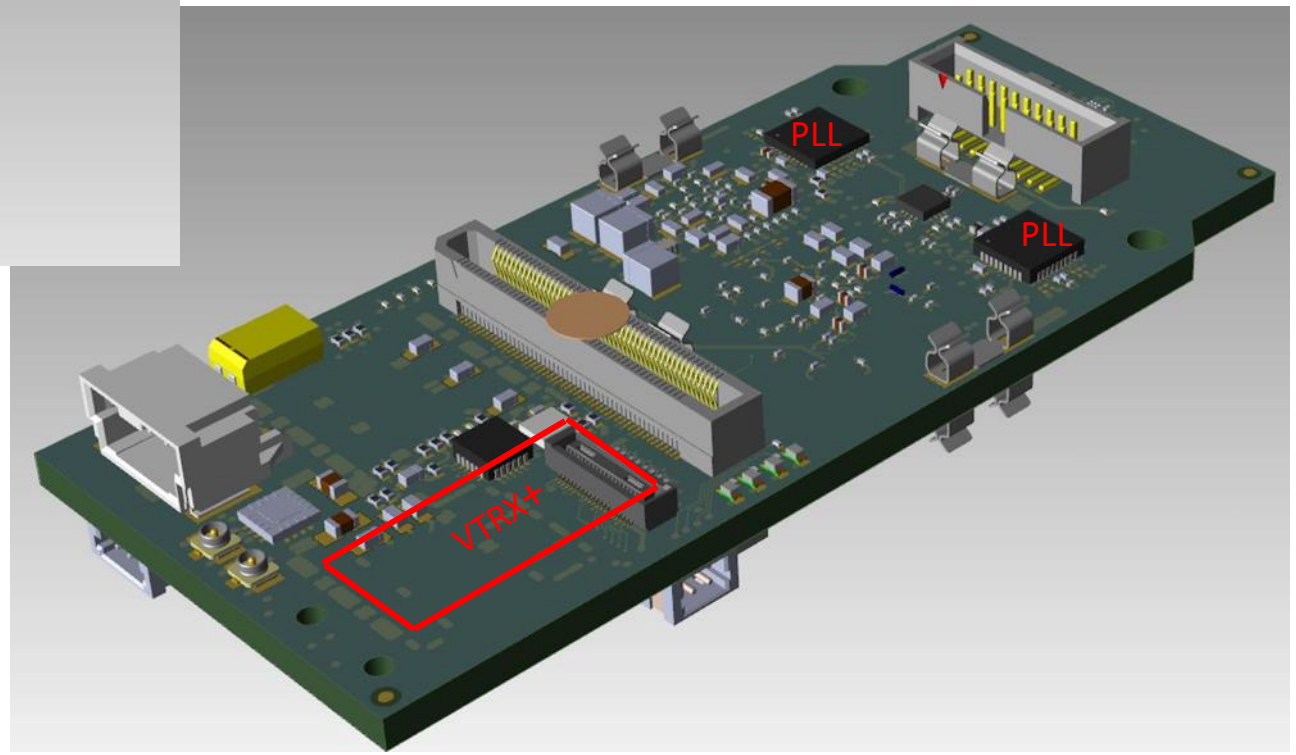
We should receive first 2 prototypes **this week!**
(1.5 year after starting the design)

Much more details on D. Falchieri's talk at Workshop on Electronics for Physics Experiment and Applications @INFN (March 2025)

dRICH RDO: layout



Complex and small card, 16 layers layout

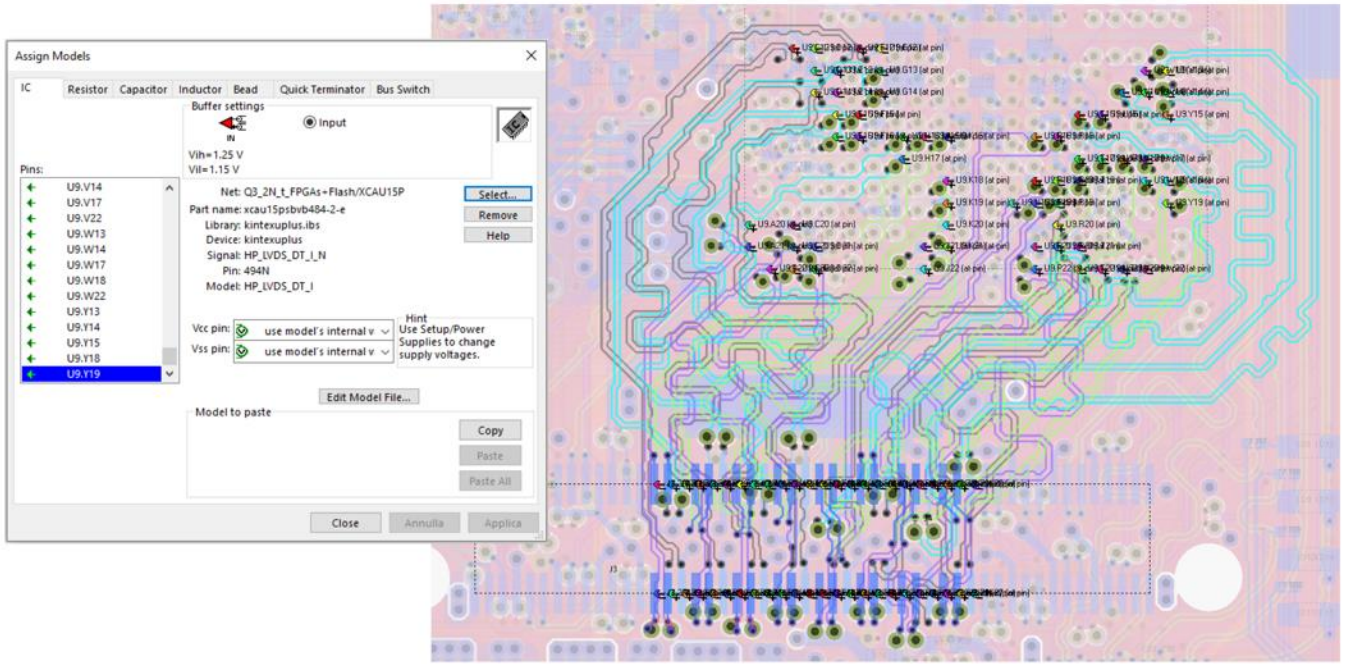


A small uC (ATTiny 417) acts as RDO power manager controlling LDOs

A lot of work on layout and cross-checks

optimization of FPGA pin assignment vs layout

Routing of 32 lanes ALCOR bus

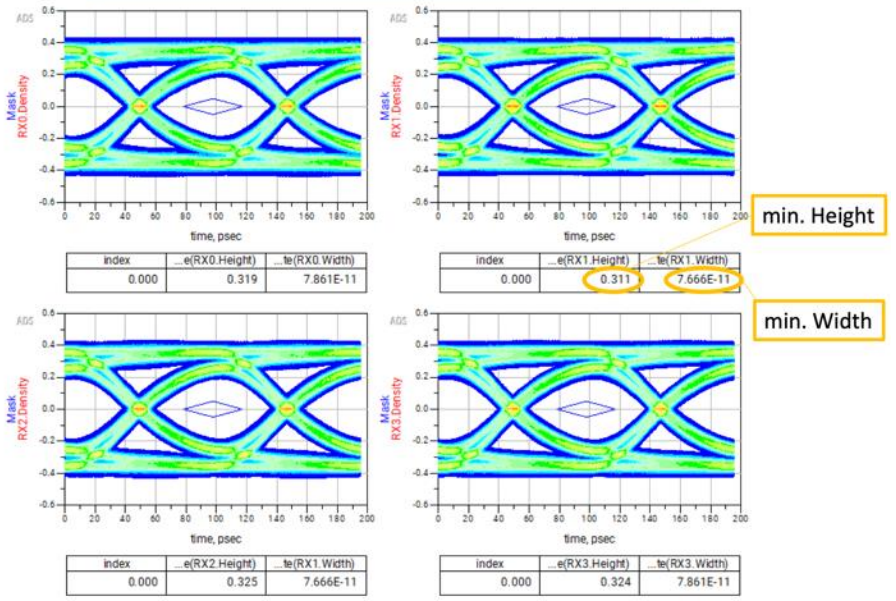


high-speed differential line modeling

ARTEL S.r.l. PCB ENGINEERING

4 Channels TX ARTIX Ultrascale+ GTH to VTRX+ receiver
AC coupling termination 100 Ω dielectric FR408HR

ADS Keysight

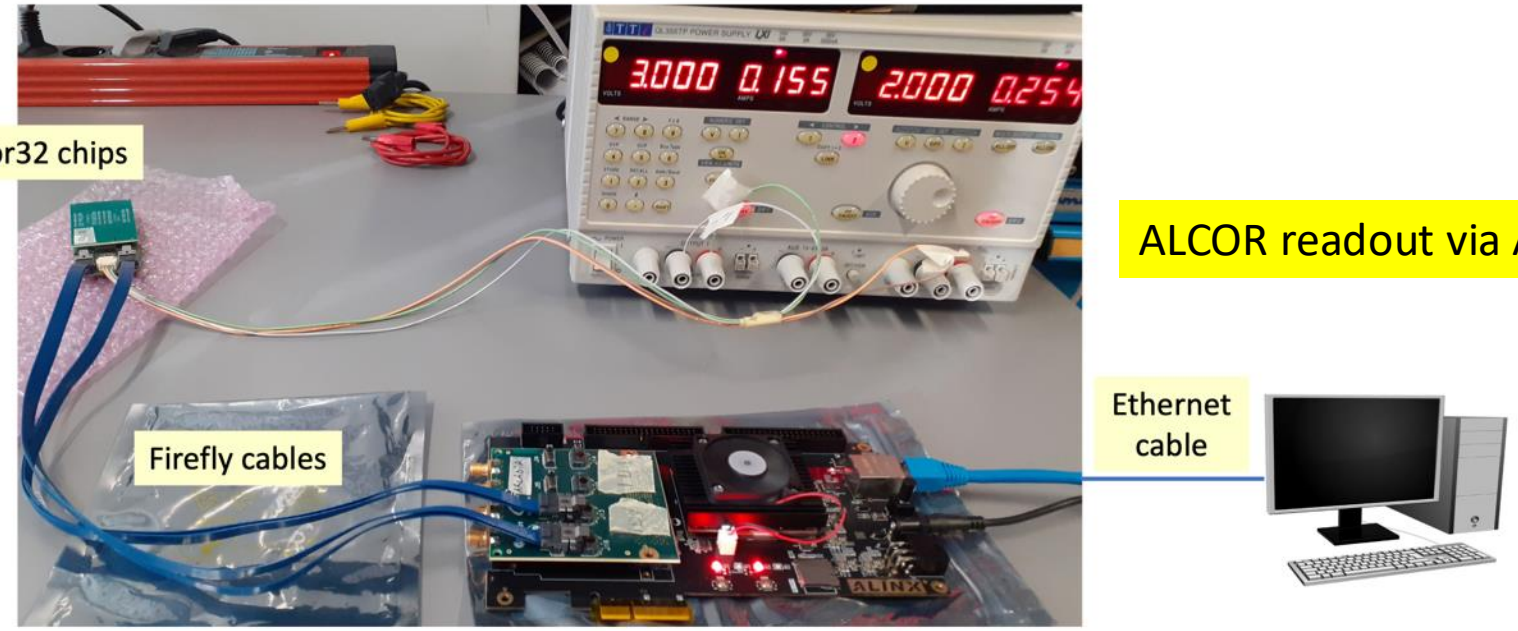


Much more details in D. Falchieri's presentation at WG Electronics and DAQ/eRD109 (April 2025)

D. Falchieri, G. Torromeo

RDO firmware progresses (I)

- pin placement for layout design
- intense use of [ALINX AUX15P evb card] (same FPGA) as RDO GYM (waiting for real cards!)



Ethernet cable

ALCOR readout via AUX15P

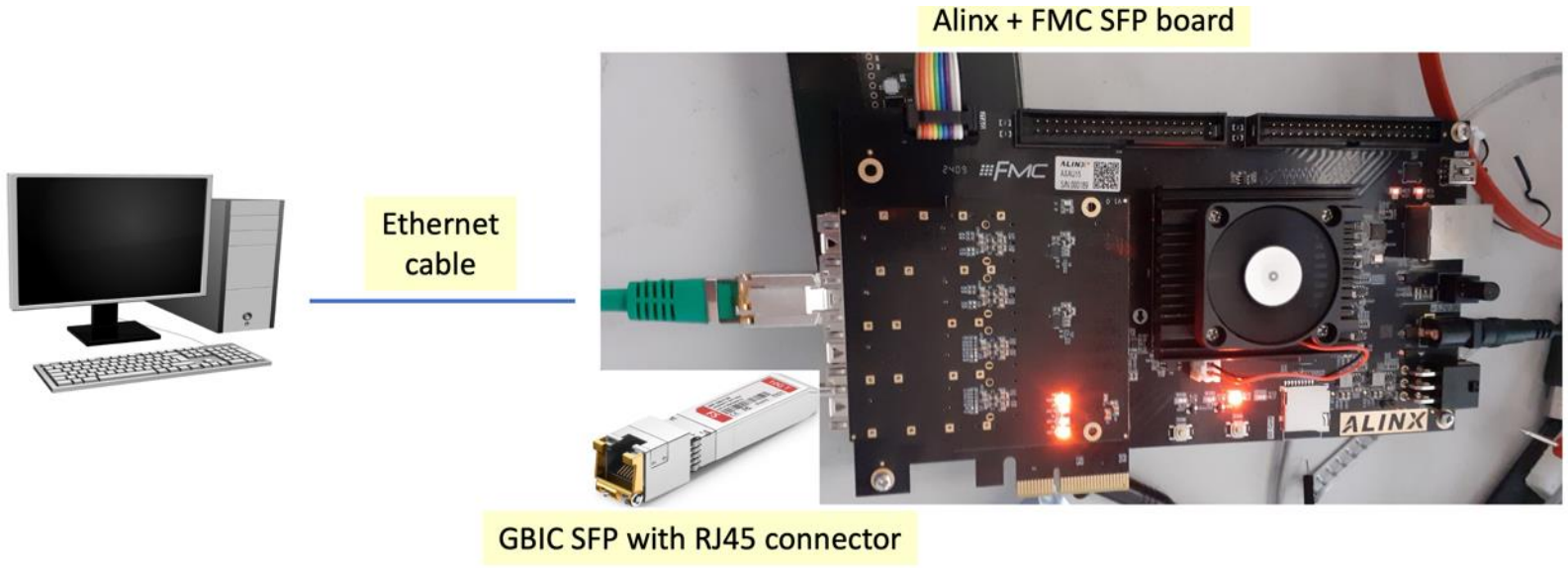
In order to test the Artix – Alcor interface, we implemented the IPbus firmware on the FPGA. Now we can program the Alcor registers via SPI and we can correctly receive the data

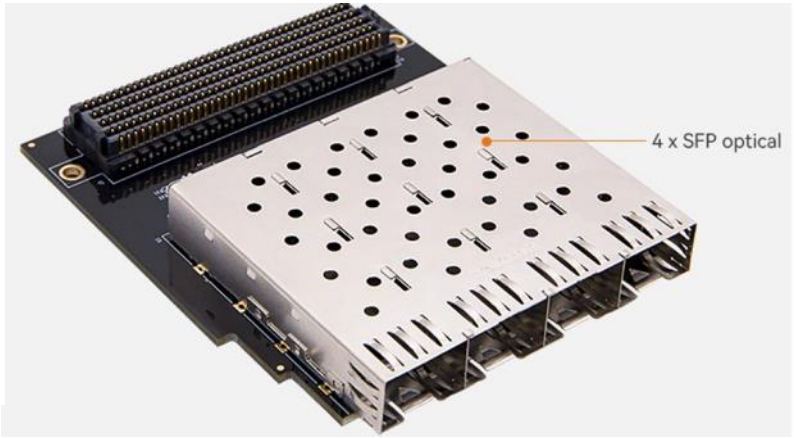
successfully ported KC705 FW (reading ALCOR) to AUX15P including SERDES
More details in D. Falchieri's talk at Electronics and DAQ WG/eRD109 (May 2025)

D. Falchieri, S. Geminiani

RDO firmware progresses (II)

- pin placement for layout design
- intense use of [ALINX AUX15P evb card] (same FPGA) as RDO GYM (waiting for real cards!)



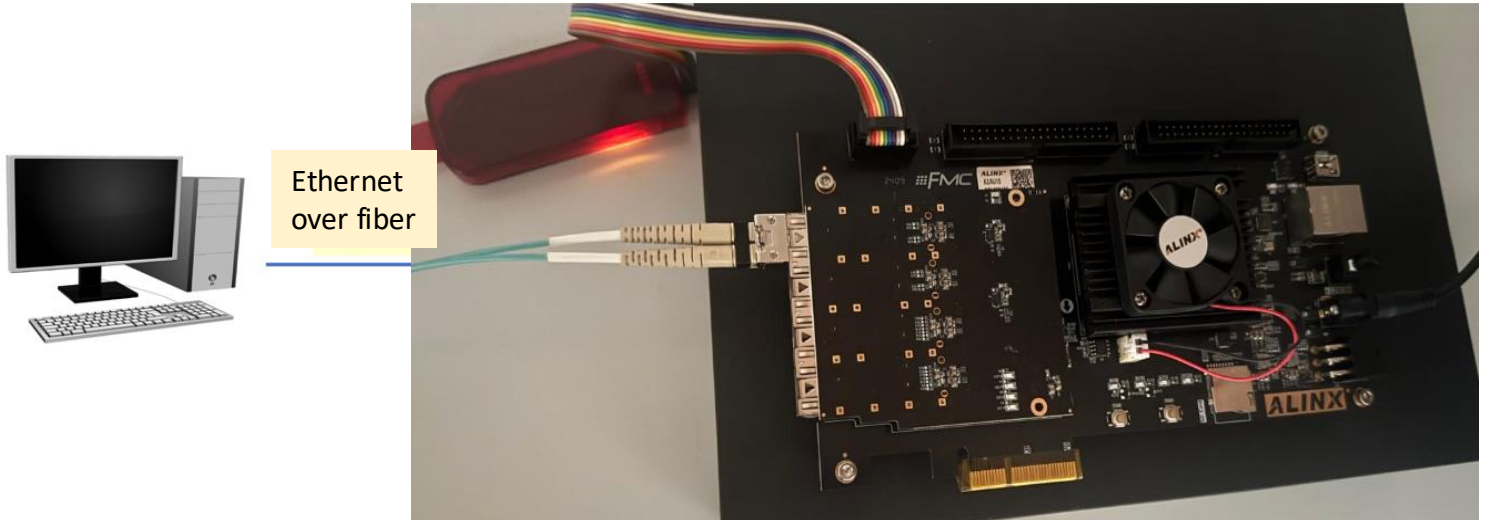


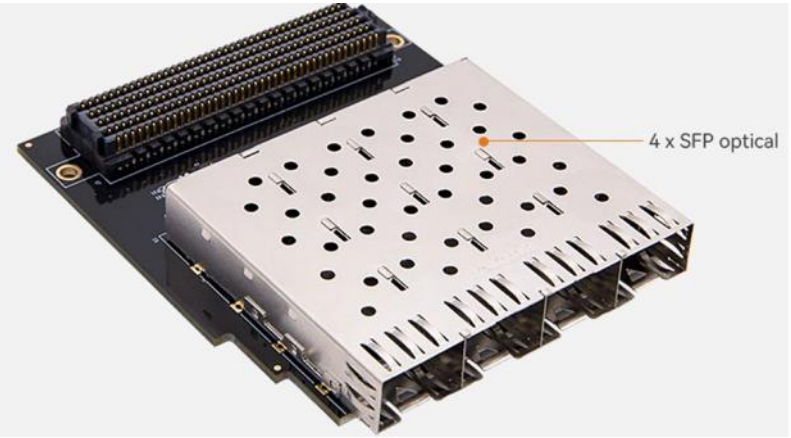
- successfully implemented IPBUS communication over optical link (commercial SFP), first with GBIC SFP then with fiber
- prototyped PLL programming at FPGA boot via I2C using a VC707

"collecting pieces of the firmware needed on RDO"

RDO firmware progresses (II)

- pin placement for layout design
- intense use of ALINX AUX15P evb card (same FPGA) as RDO GYM (waiting for real cards!)





successfully implemented IPBUS communication over optical link (commercial SFP), first with GBIC SFP then with fiber:
→ configuration foreseen for test beam

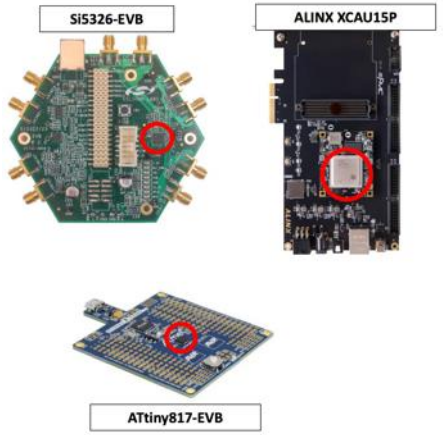
More details in D. Falchieri's talk at Electronics and DAQ WG/eRD109 (July 2025)

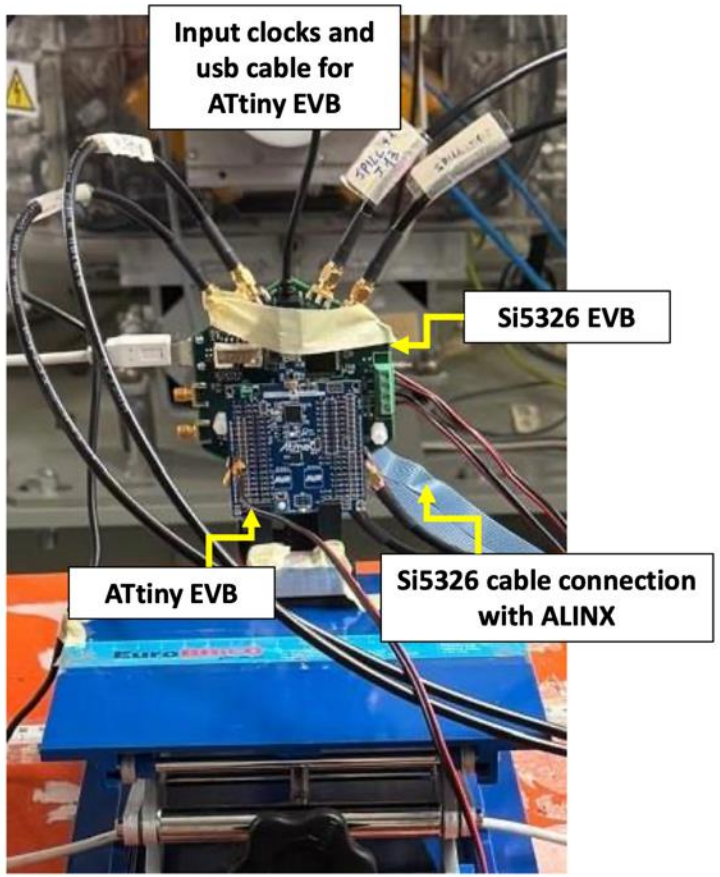
"collecting pieces of the firmware needed on RDO"

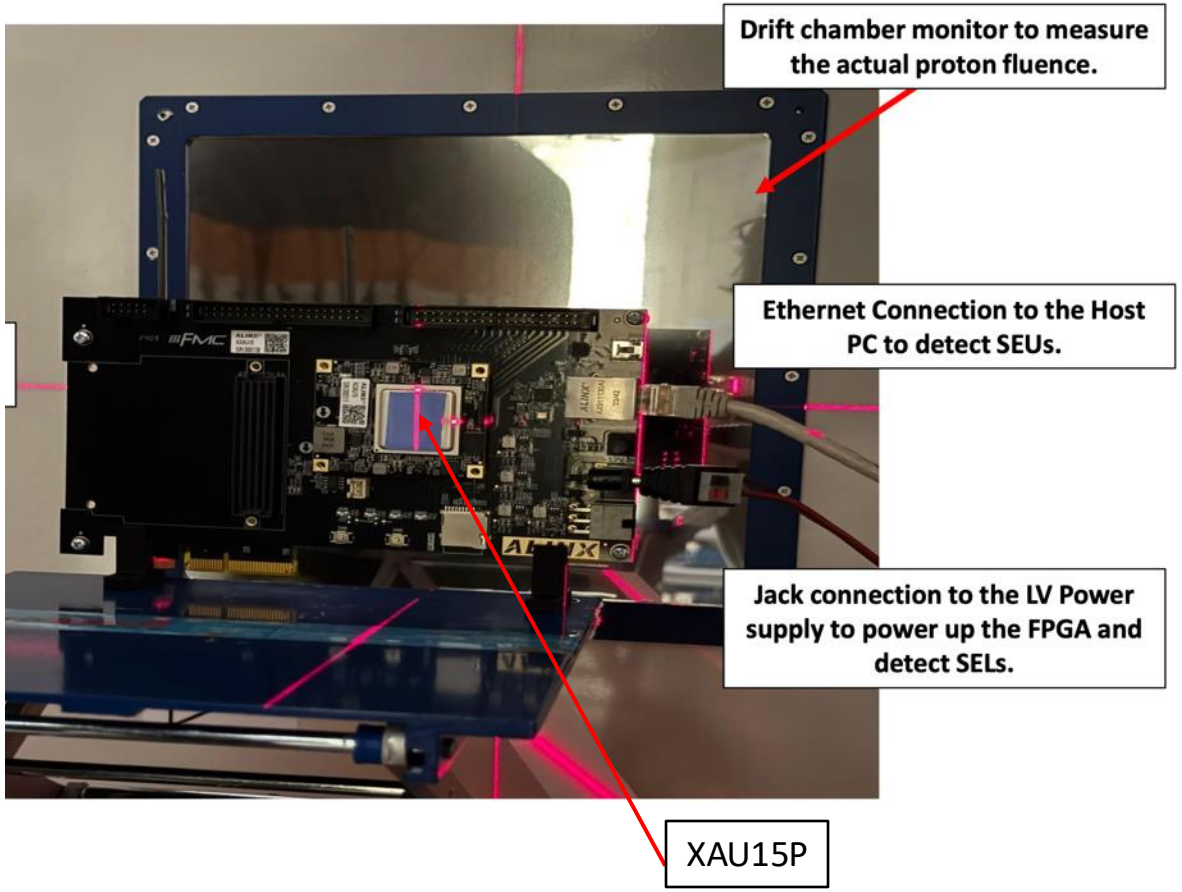
D. Falchieri, S. Geminiani

Irradiation tests

- Waiting for full RDO we tested several key components: PLL (Si5326), uC (ATtiny417) and AMD FPGA (AUX15P)
- irradiation with a proton beam at Centro di Protonterapia in Trento / December 2024
- TID ≅2.3 krad (1000 fb^{-1}) and Φ(h>20 MeV) ≅700 Hz/cm2 (including a safety factor 5)







See presentation by S.Geminiani @ePIC Collaboration meeting (Jan 2025) + results in backup

Comments: investigation addendum for ATtiny + first measurements of this kind in ePIC AFAIK

RDO power consumption estimates

LV Channel	Device	LDO	Vin (V)	Vout (V)	Iout (A)	Vdrop (V)	Ptotal (W)	Pdevice (W)	Ploss (W)
LVH 2.7 V	AUX15P	LTM4709-1H	2.7	1.20	0.1070	1.50	0.289	0.128	0.161
		LTM4709-2H	2.7	1.80	0.4820	0.90	1.301	0.868	0.434
		LTM4709-3H	2.7	2.50	0.0060	0.20	0.016	0.015	0.001
	MPF050T	LTM4709-2H	2.7	1.80	0.0025	0.90	0.007	0.005	0.002
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	VTRX+	LTM4709-1H	2.7	1.20	0.0150	1.50	0.041	0.018	0.023
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	MT25QU01	LTM4709-2H	2.7	1.80	0.0550	0.90	0.149	0.099	0.050
	Si5326	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	Si5319	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	TMP119	LTM4709-3H	2.7	2.50	0.0005	0.20	0.001	0.001	0.000
	ATtiny417	ADP1752	2.7	2.50	0.0030	0.20	0.008	0.008	0.001
	I2Cexp-4FEB	LTM4709-3H	2.7	2.50	0.0680	0.20	0.184	0.170	0.014
	LED		2.7	2.70	0.0000	0.00	0.000	0.000	0.000
	IBIAS-LDOH		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	IBIAS-LDOL		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	Total LV 2.7				**1.4290**		**3.86**	2.69	1.16
LVL 1.4 V	AUX15P	LTM4709-1L	1.4	0.85	1.6530	0.55	2.314	1.405	0.909
	AUX15P	LTM4709-2L	1.4	0.90	0.0430	0.50	0.060	0.039	0.022
	MPF050T	LTM4709-3L	1.4	1.00	0.2580	0.40	0.361	0.258	0.103
	Total LV 1.4				**1.9540**		**2.736**	1.702	1.034

Device	Total Power (W)	Area (mm2)	W/mm2
AUX15P	2.455	361	6.80
MPF050T	0.438	121	3.62
LDOH	1.155	72	16.04
LDOL	1.034	72	14.36
SI5326	0.457	36	12.70
SI5319	0.457	36	12.70
VTRX+	0.193	100	1.93

FPGA power consumption simulated **not completely** given FW is incomplete

Take home message:

1.5 A @ 2.7 V
2.0 A @ 1.4 V

→ **> ≈ 7 W/RDO**

RDO power consumption estimates

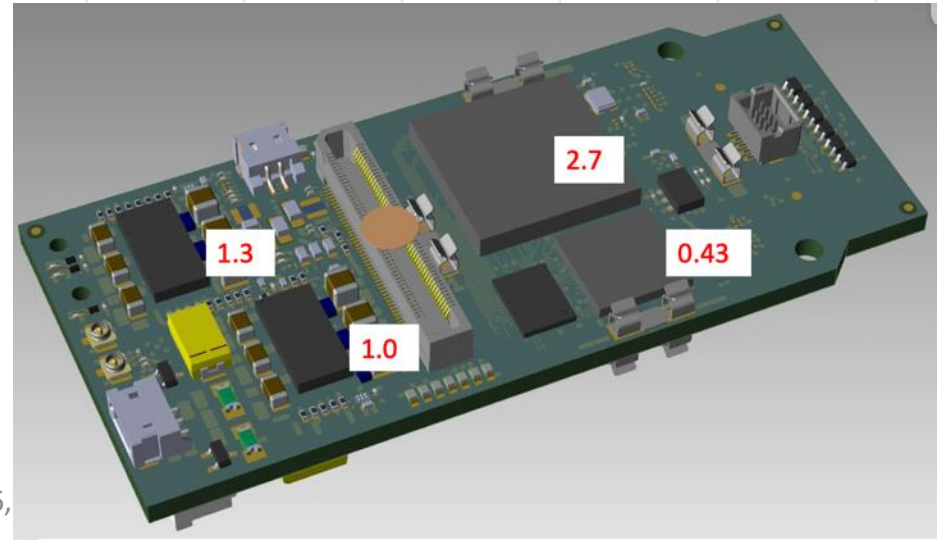
LV Channel	Device	LDO	Vin (V)	Vout (V)	Iout (A)	Vdrop (V)	Ptotal (W)	Pdevice (W)	Ploss (W)
LVH 2.7 V	AUX15P	LTM4709-1H	2.7	1.20	0.1070	1.50	0.289	0.128	0.161
		LTM4709-2H	2.7	1.80	0.4820	0.90	1.301	0.868	0.434
		LTM4709-3H	2.7	2.50	0.0060	0.20	0.016	0.015	0.001
	MPF050T	LTM4709-2H	2.7	1.80	0.0025	0.90	0.007	0.005	0.002
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	VTRX+	LTM4709-1H	2.7	1.20	0.0150	1.50	0.041	0.018	0.023
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	MT25QU01	LTM4709-2H	2.7	1.80	0.0550	0.90	0.149	0.099	0.050
	Si5326	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	Si5319	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	TMP119	LTM4709-3H	2.7	2.50	0.0005	0.20	0.001	0.001	0.000
	ATtiny417	ADP1752	2.7	2.50	0.0030	0.20	0.008	0.008	0.001
	I2Cexp-4FEB	LTM4709-3H	2.7	2.50	0.0680	0.20	0.184	0.170	0.014
	LED		2.7	2.70	0.0000	0.00	0.000	0.000	0.000
	IBIAS-LDOH		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	IBIAS-LDOL		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	Total LV 2.7				**1.4290**		**3.86**	2.69	1.16
LVL 1.4 V	AUX15P	LTM4709-1L	1.4	0.85	1.6530	0.55	2.314	1.405	0.909
	AUX15P	LTM4709-2L	1.4	0.90	0.0430	0.50	0.060	0.039	0.022
	MPF050T	LTM4709-3L	1.4	1.00	0.2580	0.40	0.361	0.258	0.103
	Total LV 1.4				**1.9540**		**2.736**	1.702	1.034

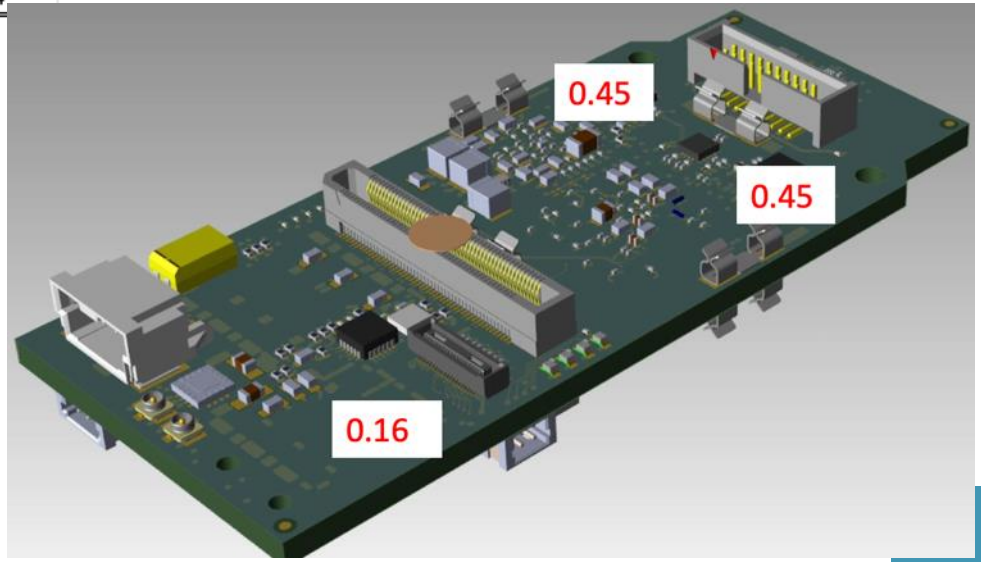
Actual FPGA power consumption simulated **not completely** given FW is incomplete

Take home message:

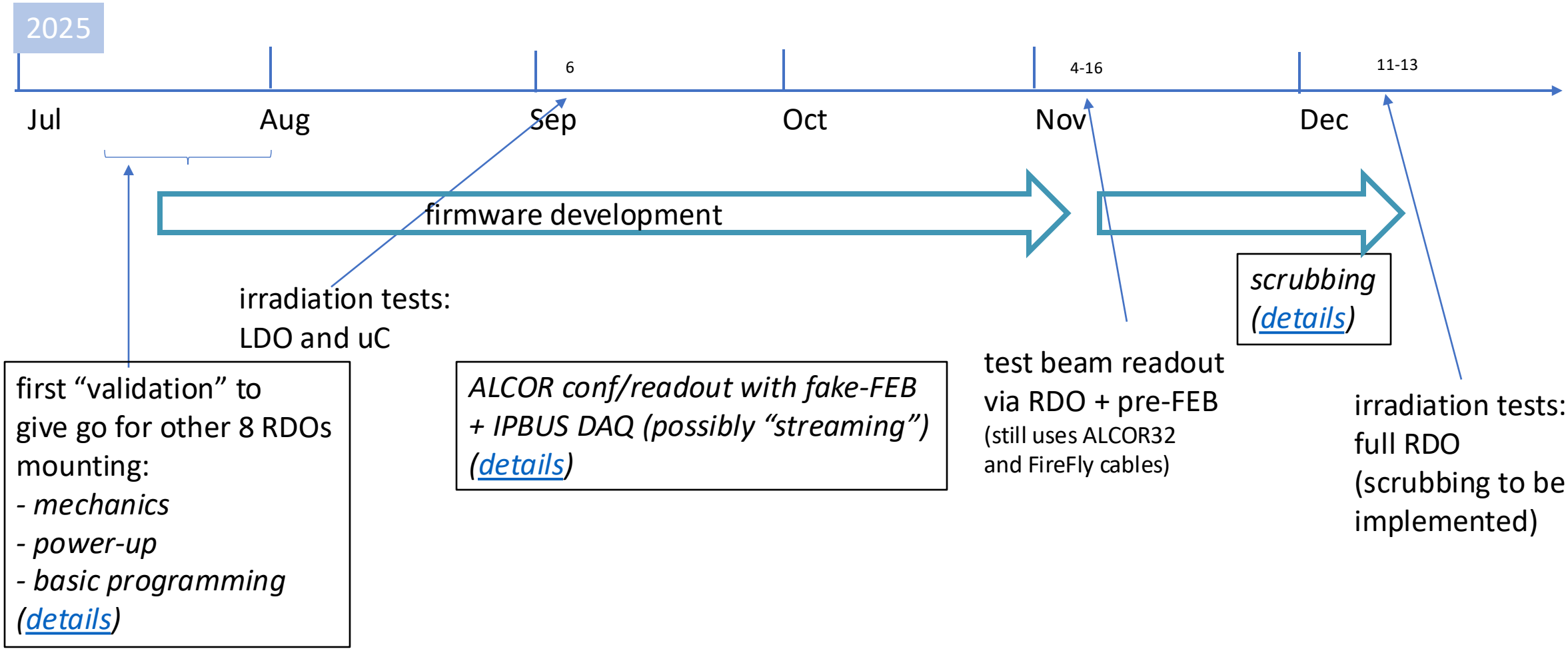
1.5 A @ 2.7 V
2.0 A @ 1.4 V

→ **> ≈ 7 W/RDO**





Plannning and validation tests



2026 *remote programming, **ePIC link implementation, test with FELIX**, QA production test card (details)*

match dRICH RDO with ePIC/DAQ timeline

PicoDAQ development --- Streaming DAQ Milestones

Detector Install: FY29Q2 - FY31Q2
Cosmics: FY31Q3
Early CD-4: FY32Q4

DAQ Releases:

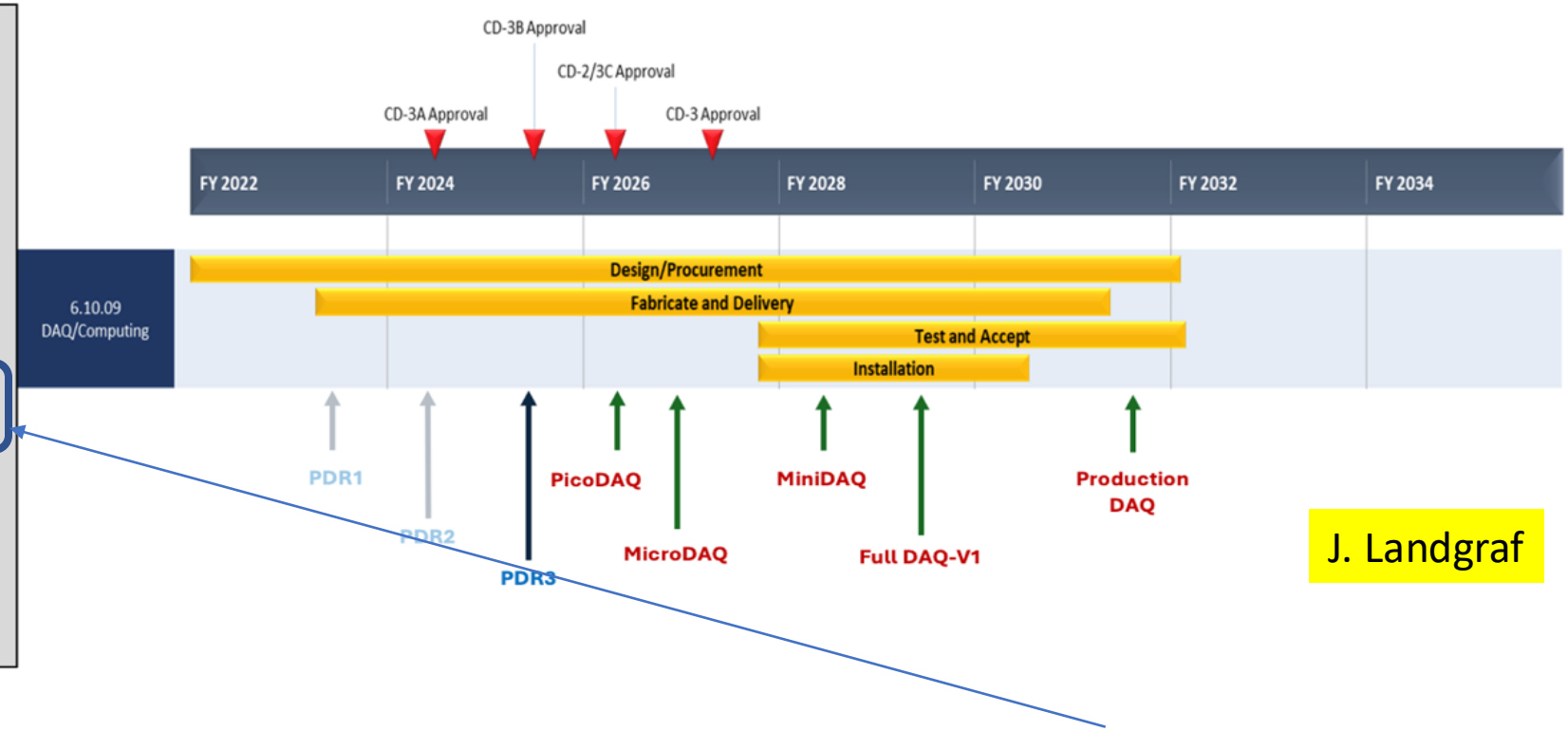
PicoDAQ FY26Q1
Readout test setups

MicroDAQ: FY26Q4
Readout detector data in test stand using engineering articles

MiniDAQ: FY28Q1
Readout detector data using full hardware and timing chain

Full DAQ-v1: FY29Q2
Full functionality DAQ ready for full system integration & testing

Production DAQ: FY31Q3
Ready for cosmics



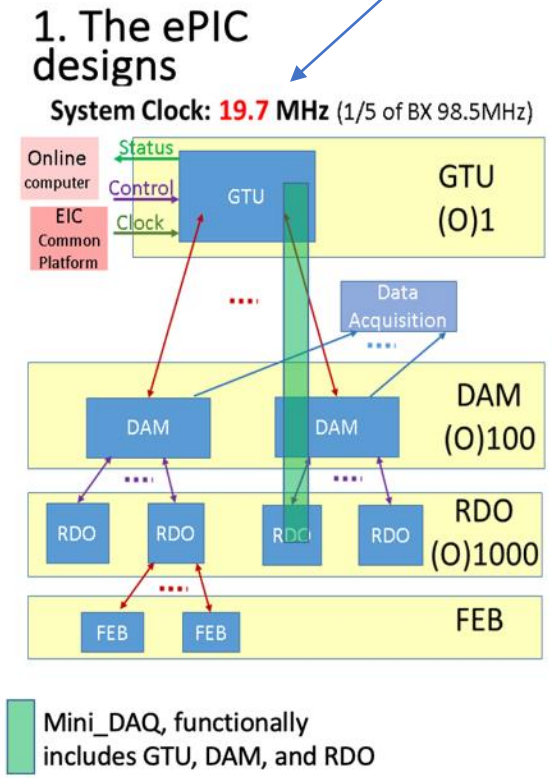
J. Landgraf

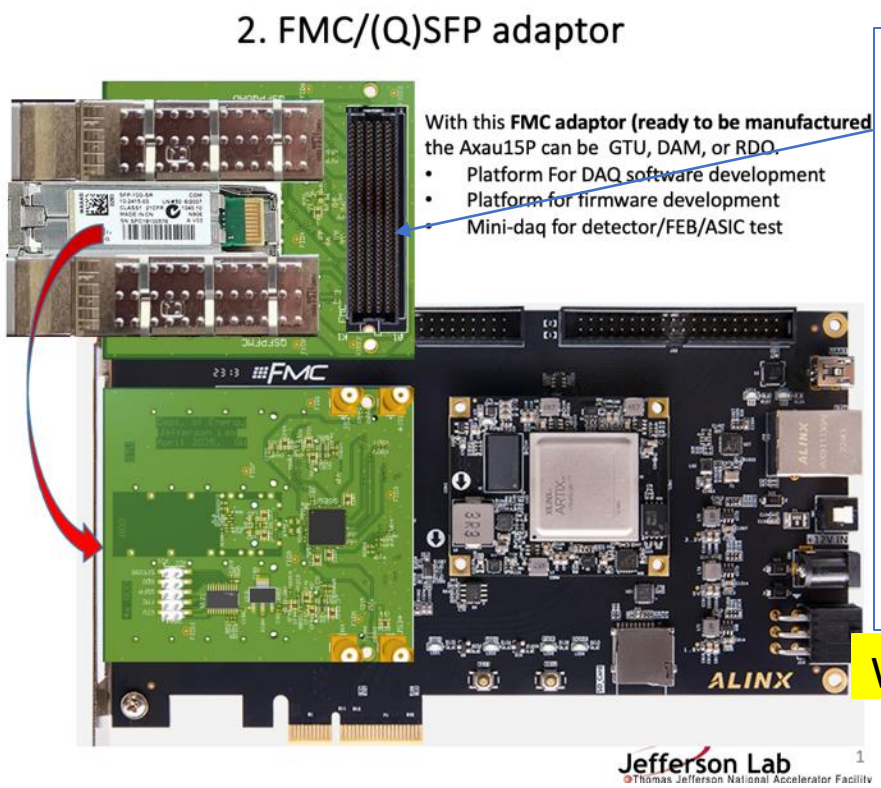
- The ”EIC” link protocol doesn’t seem yet there according to this schedule until MiniDAQ (too late for us!)
- but ALINX AUX15P is now populer and there are ideas to use it as “proto-RDO”, “proto-DAM” and “proto-GTU”
  → see next slide

which protocol as EIC link protocol for dRICH?

this is to support detectors with lpGBT, but per se we could consider to receive a 39.4 MHz clock - close to 40.08 MHz à la LHC. This would be instead of 98.5 MHz. We assume BC would be reconstructed correctly via RevTick.

This could make life easier with FELIX but… → see next slide





Once this piggy back card is produced (by JLab), this would allow us to use a pair of ALINX/AUX15P to mimic a "RDO" and a "FELIX" link

When could be available for groups?

Second step: FLX-182 (Rome1) ⟷ dRICH RDO

W. Gu

which firmware flavour in ePIC FELIX ?

Flavour	Link Wrapper	Decoders	Encoders	Remarks
0: GBT	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The GBT mode flavour is available in 8 and 24 channel versions, with a complete set of encoders / decoders, and a so called SemiStatic configuration where some decoders/encoders are left out. FELIX aims to provide a 24 channel fully configurable version for FLX712, it has been demonstrated to work but with high resource count (78% LUTs)
1: FULL	ToHost FULL, FromHost GBT or LTI	FULL 8.4.15 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14 LTI-tx 8.6	The FULL mode flavour is available in 24 channels for FLX712 and FLX128. The ToHost side/decoding is using 9.6Gb/s 8b10b data without logical links. FromHost/encoding is identical to GBT, with an option to transmit a copy of the LTI-TTC link data at 9.6Gb 8b10b with additional fields for XOFF
2: LTDB	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	LTDB mode is a 48 channel version of GBT mode, but with reduced e-link configurability. This flavour only includes the EC and IC e-links, as well as an AUX e-link (Egroup 4, link 7) with HDLC/8b10b/Direct configuration. Additionally TTC distribution is available on all FromHost/ToFrontend e-links.
4: PIXEL	lpGBT	HDLC (EC/IC) 8.4.14 Aurora 8.4.11 TTCToHost 8.4.17 BusyToHost 8.4.18	RD53A/B 8.5.8 TTC 8.5.14 HDLC (IC/EC) 8.5.12	The Pixel flavour was designed to read out the ITk Pixel detector over lpGBT with Aurora e-links. The encoder uses a custom protocol for RD53 and includes a trigger and command state machine.
5: STRIP	lpGBT	HDLC (IC) 8.4.14 Endeavour (EC) 8.4.10 8b10b 8.4.13, 8.4.9 TTCToHost 8.4.17 BusyToHost 8.4.18	HDLC (EC) 8.5.12 Endeavour (EC) 8.5.7 LCB 8.5.9 R3L1 8.5.10	The Strip flavour was designed to read out the ITk Strip detector over lpGBT with 8b10b e-links. The encoder uses a strip custom protocol with so called trickle merge.
9: LPGBT	lpGBT	HDLC (EC/IC) 8.4.14 8b10b 8.4.13 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The lpGBT Flavour is the lpGBT equivalent of the GBT flavour. It involves 8b10b, HDLC and TTC protocols and the aim is to have a fully configurable 24 channel build available. The LPGBT flavour will include encoding and decoding schemes for the HGTD
10: INTERLAKEN	64b67b	ToHost Interlaken, FromHost LTI 8.4.19	LTI-tx 8.6	The Interlaken Flavour has 24x 25.78125 Gb/s Interlaken links in ToHost direction. Note that no more than 12 links can be fully occupied as otherwise the PCIe Gen4 bandwidth will be saturated. As encoders, the Interlaken flavour implements the TTC-LTI encoder, a copy of the received LTI frame but with additional XOFF bits.

Table of available link “flavours” in FELIX cards and FPGA resources usage (courtesy by A. Lonardo)

FELIX FPGA resource usage

		KU115	VM1802	VP1552
GBT 24 channel	LUT	80.65%	69.60%	35.71%
	FF	77.03%	50.94%	26.13%
	BRAM	70.00%	89.45%	34.04%
	URAM		62.20%	22.14%
FULL 24 channel	LUT	52.59%	44.35%	22.75%
	FF	38.40%	33.21%	17.03%
	BRAM	40.46%	20.99%	7.99%
	URAM		62.20%	22.14%
LPGBT 24 channel	LUT	112.51%	82.94%	42.55%
	FF	52.39%	38.62%	19.81%
	BRAM	68.94%	79.52%	30.26%
	URAM		62.20%	22.14%
PIXEL 24 channel	LUT	82.40%	60.75%	31.17%
	FF	62.04%	45.74%	23.46%
	BRAM	61.20%	62.25%	23.69%
	URAM		62.20%	22.14%
STRIP 24 channel	LUT	67.04%	49.42%	25.35%
	FF	49.94%	36.81%	18.88%
	BRAM	121.43%	104.45%	39.75%
	URAM		145.14%	51.65%
INTERLAKEN 8 channel	LUT		9.15%	4.69%
	FF		7.89%	4.05%
	BRAM		40.43%	15.39%
	URAM		0.00%	0.00%

Table 5.2: Resource utilization for all firmware flavours estimated for the

Note dRICH aims to use FLX-155 resources too for data reduction!

See A. Lonardo talk at ePIC Jan 2025 meeting

Update:
Rome1/2 has now the FLX-182 sent by BNL up and running!

- scale up to 48 lpGBT links might be a problem for FLX-155?
- as dRICH we use just the VTRX+ tranceiver not the lpGBT ASIC so lpGBT protocol not strictly needed but we would recommend to use anyway one of the existing flavour (perhaps FULL?)

Summary

- some lessons learned in these 4 years “prototyping” ASIC readout
- eager to test real RDO prototypes (exp. this week)
- many pieces of work validating / to validate step by step design choices
- a lot of work ahead of us!
- we need to be sure by 2026 we are production-ready for RDO

- validating “EIC/ePIC link”
- overall PDU integration

} two main next challenges in 2026

- as soon as we define which protocol to use we can start testing critical RDO features (still untested: clock reconstruction): we need a “quasi-final” FW to be reasonably sure we can go for production in 2027
- a choice of the protocol among the FELIX-supported flavours would be beneficial for us to advance in 2026 and build up joint work Bologna/Rome1/Rome2 but likely woud be beneficial for ePIC as well

Backup

Irradiation tests

MTBF= Mean Time Between Failure
SEU = Single Event Upset
SEL = Single Event Latchup

from conclusions presented in January:

1. We integrated $\mathbf{TID \sim 2.8 \cdot TID_5}$ for the AU15P, $\mathbf{TID \sim 10 \cdot TID_5}$ for the ATtiny and $\mathbf{TID \sim 18 \cdot TID_5}$ for the Si5326.

   No significative cumulative effect or SEL for Si5326 and AU15P, while the **ATtiny stopped working at TID = 23 krad**.

   → **Devices tested up to a TID largely exceeding expected TID @dRICH: no destructive effects seen for $\mathbf{TID \leq TID_5}$**

2. **Si5326: MTBF = 3.8 h (for 1248 RDOs)** and the jitter analysis showed the **output clock is very stable.**

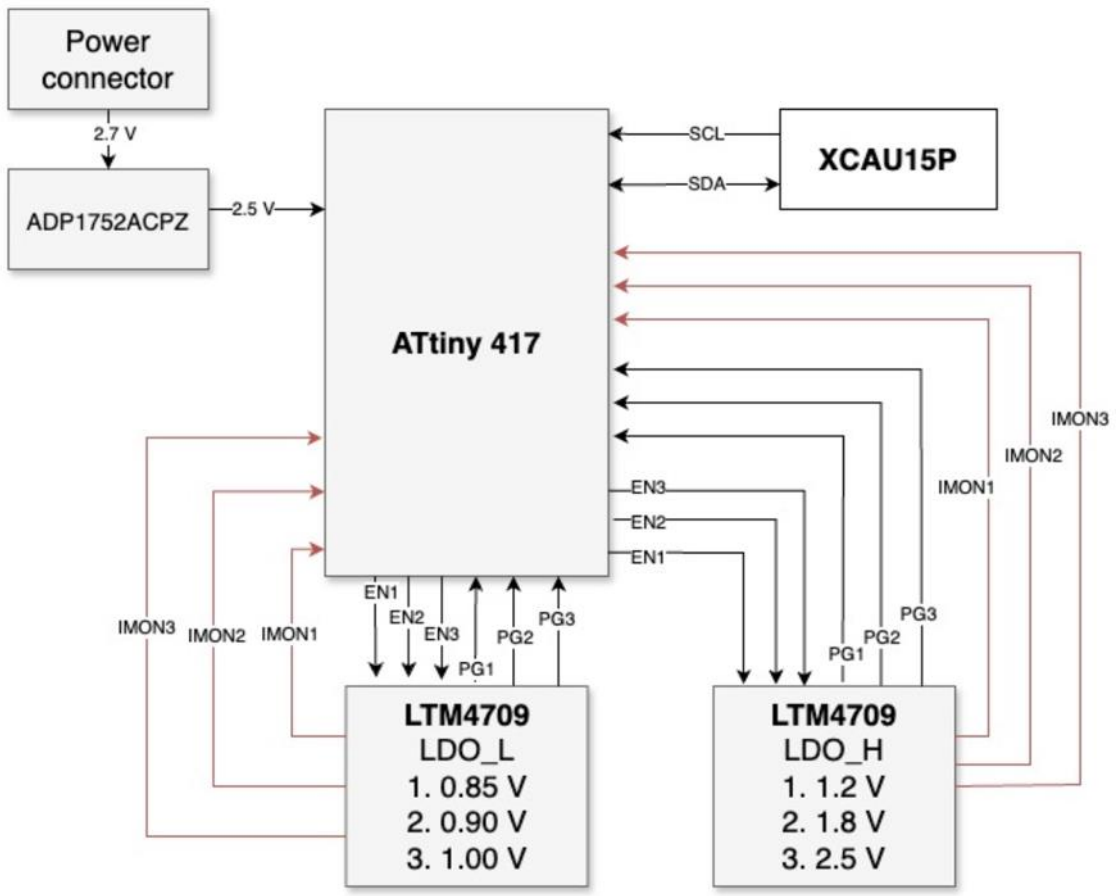
   → **The RDO AU15P will control the chip configuration every t ≪ 3.8 h.**

3. **ATtiny: SRAM MTBF = 4 h** and **FLASH MTBF > 43 h (for 1248 RDOs)** .

   → **The FLASH MTBF is a safety limit and key RAM registers will be implemented with TMR checks.**

Comments: investigation addendum for ATtiny + first measurements of this kind in ePIC AFAIK

RDO power management



ATtiny417: Datasheet

ATtiny417 provides monitoring of “power good” signals and current monitoring

I^2C interface with AUX15P to report current values

L. Rignanese

RDO next steps for go for production (8 RDOs)

1. Mechanical pairing with fake-FEB
2. Power-up : 2.5 / 1.4 jumper to avoid power to other sections
3. Prg uC via external connector
4. Power-up with uC (post-programming uC): check Vout LDO
5. Prg Artix via external connector
6. Prg Polarfire via external connector
7. Prg Artix → SkyWorks (programming 125 MHz of Si5319)
8. Check consumptions
9. Check UFL I/Os
10. Link IPBUS via VTRX+ [MT-MPO adapter + "polipo"]
11. Prg ALCOR via fake-FEB (via IPBUS → VTRX+)
12. ALCOR readout (via IPBUS → VTRX+)

Note: we can't test everything before give the "go" for next 8 RDOs...

RDO next steps for test beam

1. External clock processed by SI5326 (note: we need 16 SMA-UFL cables)
2. Readout of all I2C sensors
3. I2C programming of regulators on fake-FEB
4. Manage different IP (without jumpers)
5. Cooling ?!
6. A mini rack: 8 RDO + fake-feb on both sides etc...

Optional (bonus):

1. IPBUS + UDP streaming

RDO next steps per test @TIFPA

1. Writing QSPI Flash via SPI (writing via JTAG)
2. Scrubbing
3. Comunication between PolarFire and Artix
4. Current monitor via uC
5. Communication between uC and ARTIX

Optional (bonus):

1. Polarfire program ARTIX at boot
2. QSPI Flash writing via IPBUS (Remote Programming!)
3. During the test: one fake-feb connected and we read 2 ALCOR32? (note: ALCOR not exposed to radiation)

RDO next steps towards full ePIC DAQ

- Check noise from charged pump
- Check noise (light) from VTRX+ / engineer “shield”
- Link EIC → clock reconstruction (need project input)
- Clock at 394 MHz/ ALCOR@394 MHz
- Polarfire program Artix at boot
- Remote programming (writing PolarFire via VTRX+)
- Remote programming (writing Flash memory via VTRX+)
- IPBUS —> EIC link over VC709/707
- Data format // buffering // “frame”
- Test with ALCOR64 + FEB
- Test with FELIX
- test in magnetic field (PDU)
- PDU in detector box etc…

TB2026: dismount leds!!

- **pre-production** during 2026 (if we don't need it before) “RDO26”
- test card for testing RDO