Thursday, January 16, 2025

Streaming Readout PET

LDRD Q1 Report – January 21, 2025

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U.S. DEPARTMENT OF ENERGY | Office of Science

JSA

Q1 Accomplished Goals

A) Detector prototype development

- Debug TCP firmware, switch to 10 Gig stack
- Implement off-ASIC ADC firmware
- Design concept for v2.0 front end layout

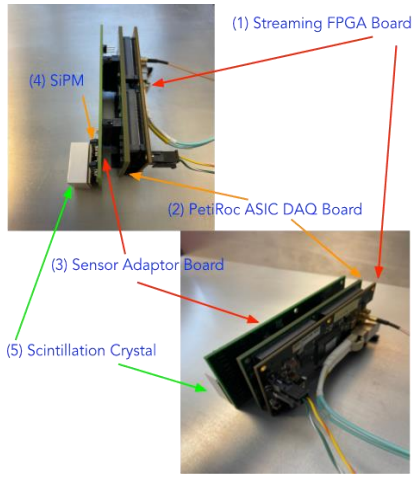
B) SRO data processing system development

- Explore SRO analysis architecture options
- Begin ERSAP-based software development

C) Broader scope project work

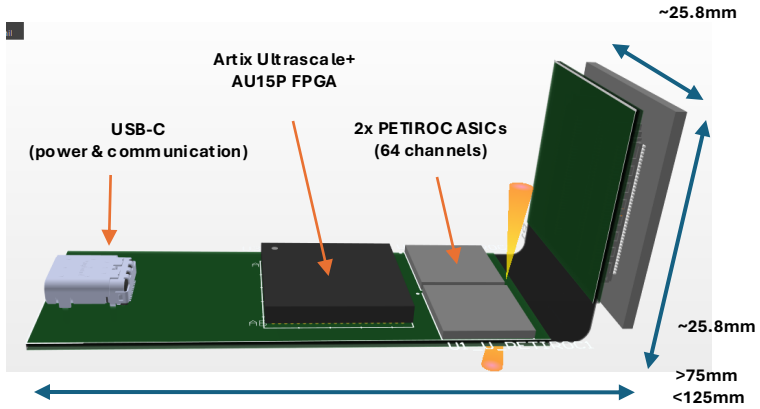
- Invention disclosure, APS abstract
- Networking at IEEE meeting
- Planning FY26 UMAB site visit
- Parts ordering – ASICs and Network Switch

Starting Points

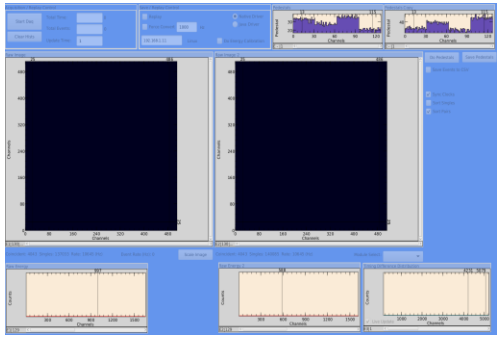


Existing Detector Front-end Electronics v1.0

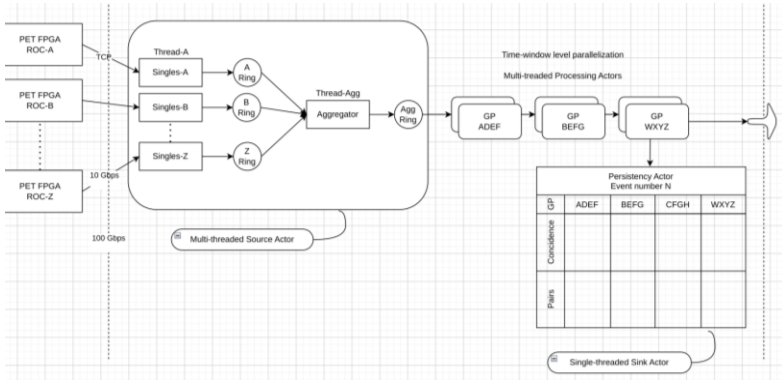
Q1 Design Progress



Potential Detector Front-end Electronics v2.0



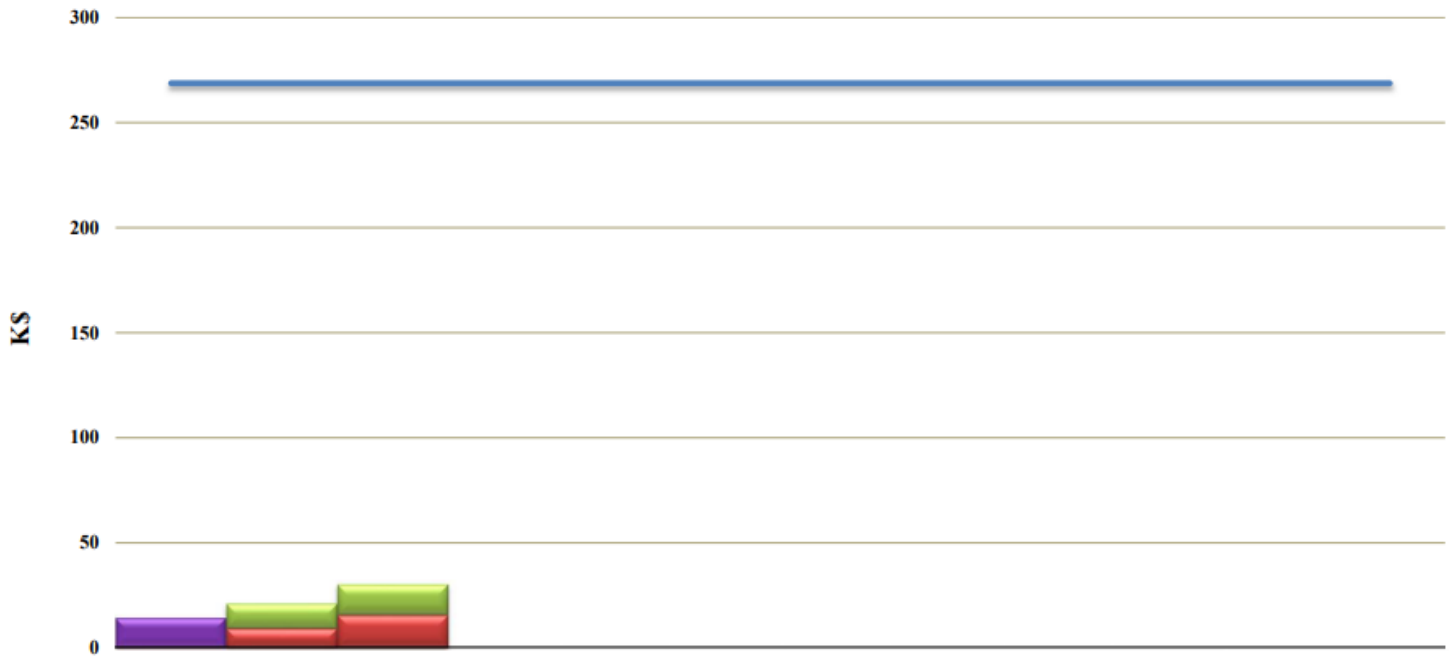
Existing KMax GUI running SRO data processing



Potential Time-window interleaving ERSAP Architecture

SPENDING

- **Spending is generally on target** – slower start-up than scheduled due to delayed start and holidays
  1) Labor: Spent ~$10k on labor direct, $16k loaded
  2) Equipment: Spent ~$12k on ASICs for detector front end, ~$11k pending for network switch
  3) Travel: Pending ~$4k for APS meeting travel in March



	Oct-24	Nov-24	Dec-24	Jan-25	Feb-25	Mar-25	Apr-25	May-25	Jun-25	Jul-25	Aug-25	Sep-25
YTD Spending	0	23	44	0	0	0	0	0	0	0	0	0
Pending	14	0	0	0	0	0	0	0	0	0		
Open Obligations	0	0	0	0	0	0	0	0	0	0	0	0
Expenses	0	12	14	0	0	0	0	0	0	0	0	0
Labor	0	9	16	0	0	0	0	0	0	0	0	0
Funding	269	269	269	269	269	269	269	269	269	269	269	269
3-Mo Avg Projection												

BACKUPS

DELIVERABLES

Deliverables – milestones and timeline:

- Three primary aims
  1) Implement ERSAP to existing SRO PET detectors, DAQ, and analysis system in FY 25
  2) Design and build improved version of modular PETIROC ASIC PET detectors in FY 25
  3) Deploy detector array, perform imaging and parallelized scaling tests with distributed computing in FY 26

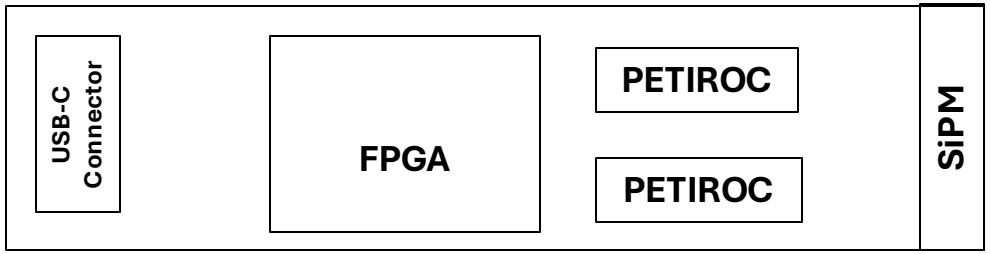
Year 1			Year 2		
1)	**Implement ERSAP in FY 25:** ☐ (✓) Implement FPGA based PETIROC signal digitization ☐ Factorize analysis components into ERSAP microservices ☐ Reproduce old system performance with ERSAP-based system ☐ Develop vertical multi-threaded, horizontal multi-node scaling	**FY 2025:** • Month 3 • Month 6 • Month 9 • Month 12	3)	**Deploy detector array, imaging and parallelized scaling tests in FY 26:** ☐ Procure and test new detector front-ends ☐ Integrate modular 8-detector array with new SRO system ☐ Verify detector and imaging performance for new system ☐ Deploy the system and perform phantom imaging tests at UMAB ☐ Finalize reports on local and farm streaming scalability tests	**FY 2026:** • Month 3 • Month 3 • Month 6 • Month 6 • Month 12
2)	**Design and build modular PETIROC ASIC PET detectors in FY 25:** ☐ (✓) Optimize FPGA multi-detector readout firmware ☐ (✓) Optimize detector power supply and readout cabling ☐ Design and order new PETIROC modular detector PCBs ☐ Get electronics parts, build, and test 8 new detector front-ends	**FY 2025:** • Month 3 • Month 3 • Month 6 • Month 12			

Detector Prototype Development

- Debugged existing prototype FPGA firmware
  - Issue with missing TCP packets/bad ethernet cable – removed bad cable
  - Implemented 10-Gig firmware wrapping around existing 1-Gig hardware

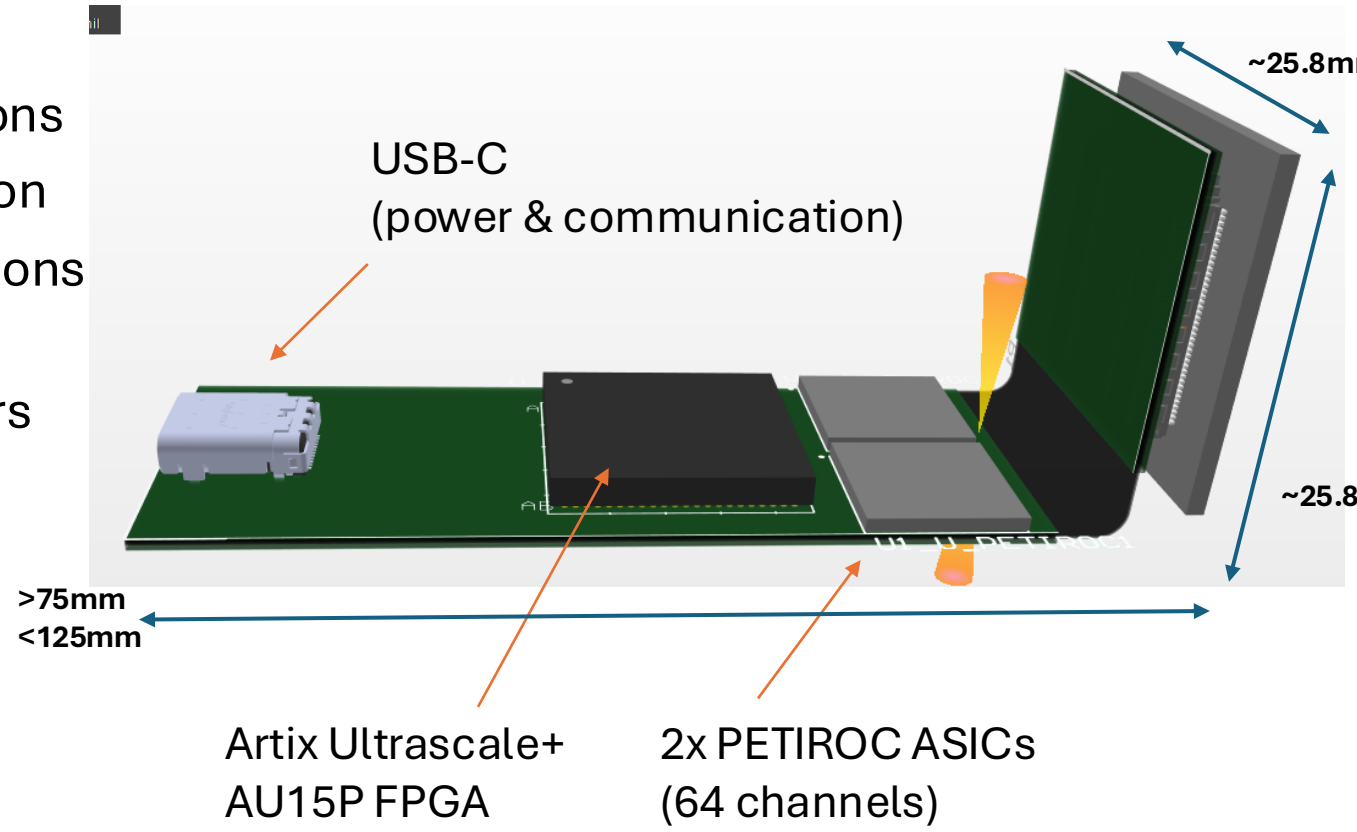
- Implemented off-ASIC ADC firmware
  - Implemented FPGA firmware to bypass PETIROC digitization, using faster on-board ADC now

- Designed concept for v2.0 front end layout
  - Modular detector design – locks in design choices for v2.0



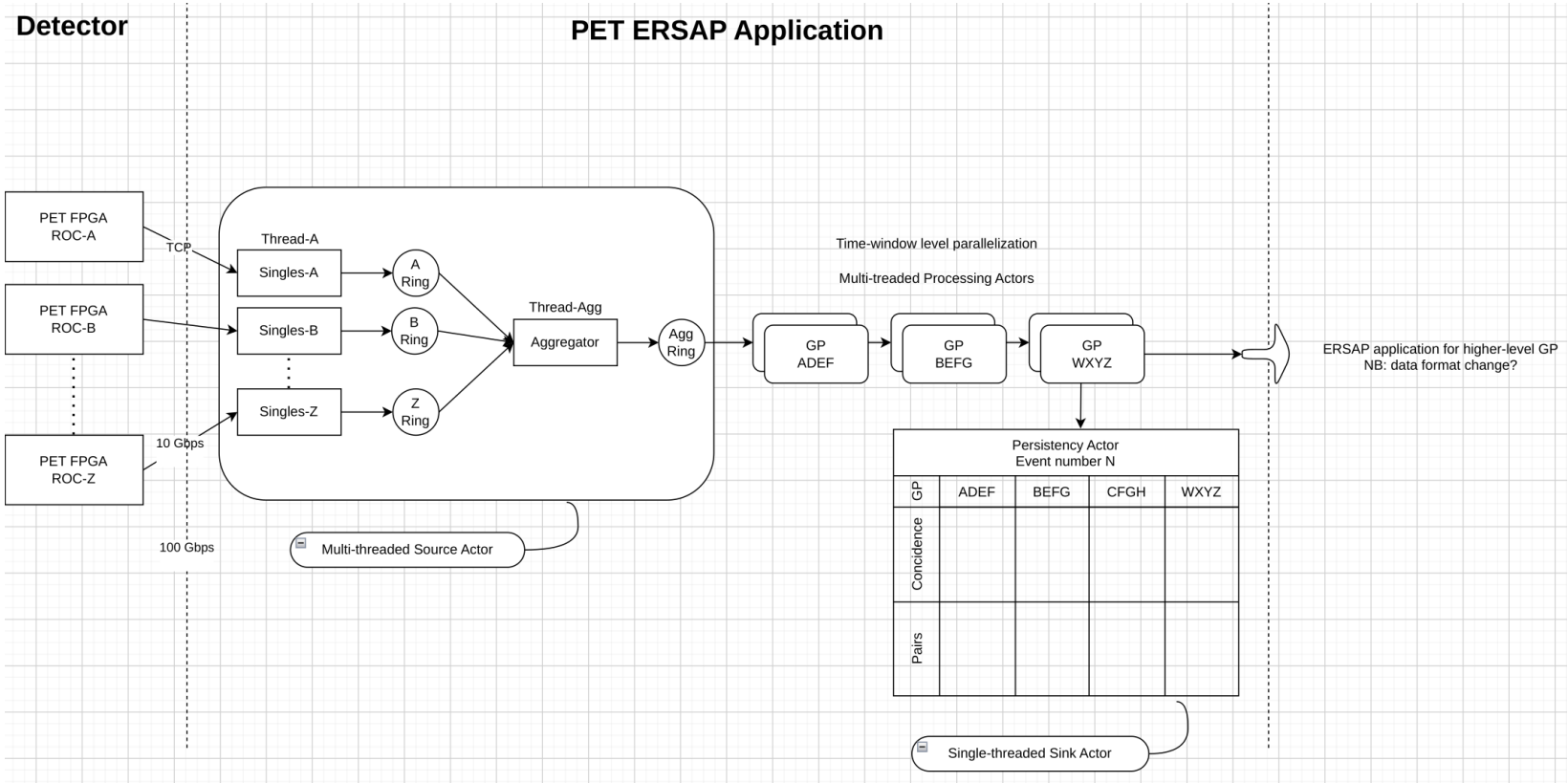
Detector Prototype Development

- Designed concept for v2.0 front end layout
  - Modular detector design
  - Aiming for 4-side buttable
  - SiPM and scintillator separated
  - Flex cable permits multiple orientations
  - & permits thermal and optical isolation
  - USB-C connector simplifies connections
  - Communication board (not shown) synchronizes and powers all detectors



SRO Platform Development

- Explored SRO analysis architecture options
  - Event-based processing from FPGA
  - Time-windowing at singles or geometry processor
  - Potential for time-windowing in the FPGA
  - Updated diagram for one potential architecture
    - All time-interleaving in a single actor option



- Began ERSAP-based software development
  - John is working on GitLab CD/CI implementation
  - John is converting KMax singles and geometry processors into ERSAP actors

Broader Project Goals

- Submitted Invention Disclosure, APS Abstract
  - Submitted invention disclosure to RTPO
  - Poster session abstract at 2025 APS Global Summit
- Networked at IEEE meeting
  - Met Simon Cherry at UC Davis
  - Met LBNL PET detector researchers
  - Attended Edge Computing workshop and contributed to workshop report
- Planned FY26 UMAB site visit
  - Discussed planning for trip to UMAB School of Medicine with Mark Smith and Guang Li
- Parts ordered
  - Purchased ASICs for 8+1 detectors
  - Purchased network switch

SUMMARY

- We are on track to meeting deliverable goals
  - SRO platform development is underway
  - Detector front-end design work is underway
  - Sub-contracted imaging studies are on track for FY26