



# FRIBDAQ Experience and Requirements

Giordano Cerizza  
[cerizza@frib.msu.edu](mailto:cerizza@frib.msu.edu)

12 February 2025

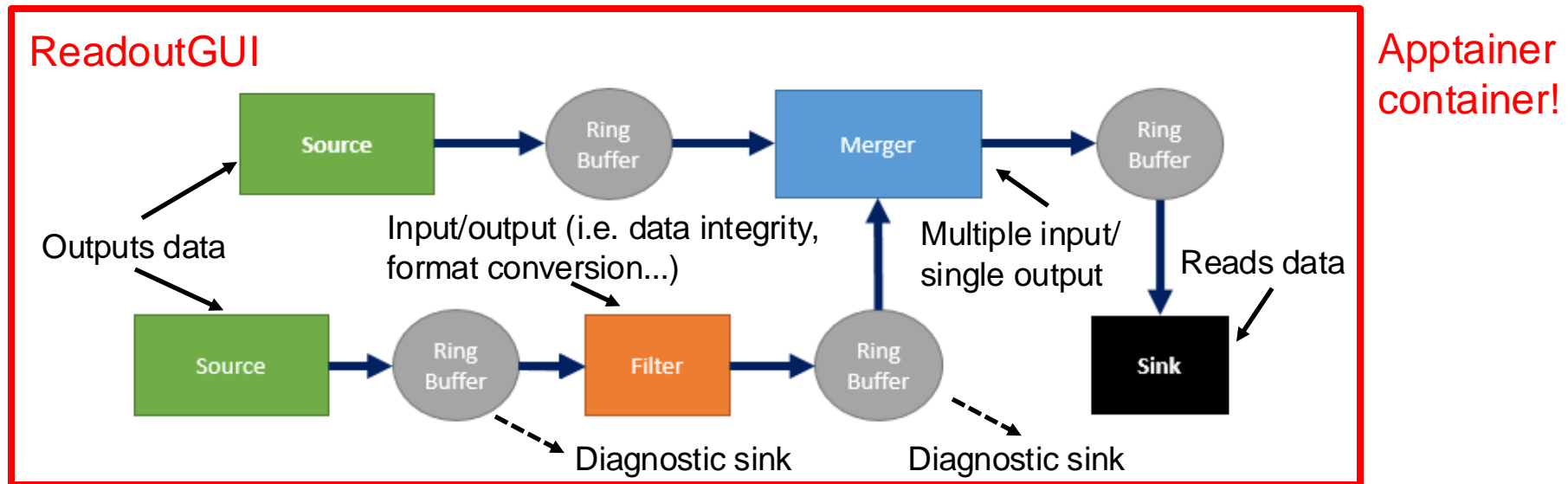


Office of  
Science

This material is based upon work supported by the U.S. Department of Energy, Office of Science, Office of Nuclear Physics and used resources of the Facility for Rare Isotope Beams (FRIB) Operations, which is a DOE Office of Science User Facility under Award Number DE-SC0023633.

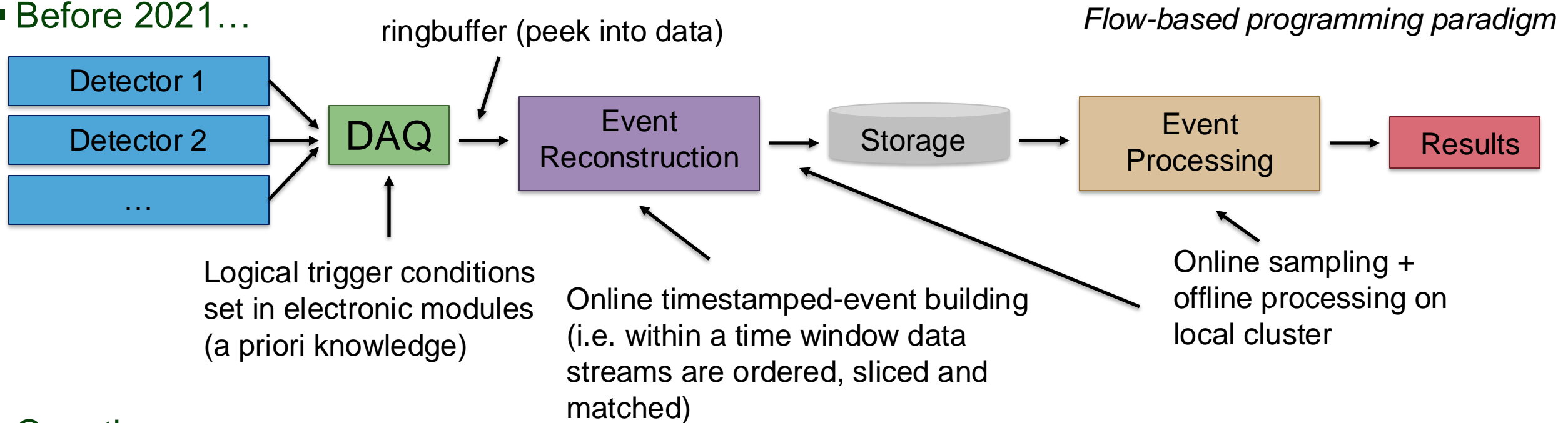
# FRIBDAQ Readout Architecture

- Software suite (C++, Tcl – being replaced by PyQT5, Python) that provides a flexible and extensible framework for handling the data flow produced by nuclear physics experiments
- Support for a wide variety of electronics: VME, CAMAC, CAEN and XIA digitizers, GET, SRS
- Manage the data stream by breaking it into smaller pieces
- ReadoutGUI is the “conductor” of the system
  - Pipeline management, data recording, consolidation of data to output, ...



# FRIB Approach to SRO

## ■ Before 2021...

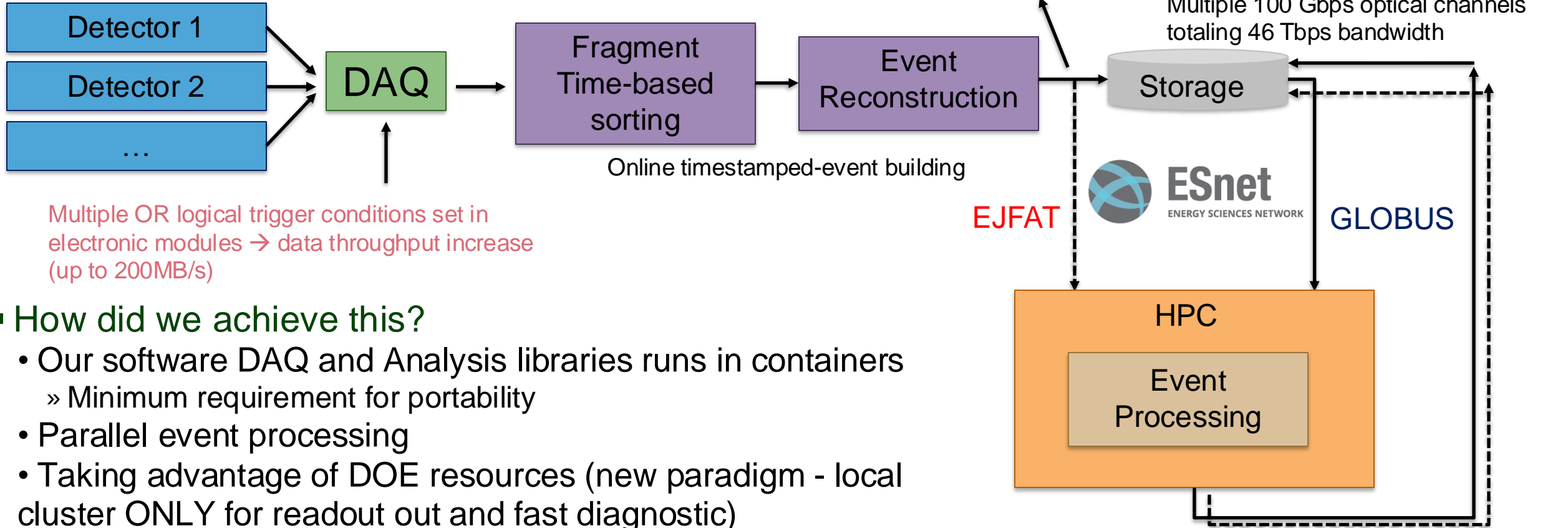


## ■ Questions:

- Can SRO electronics and global timing synchronization improve data taking and data analysis efficiencies with very rare isotope beams? (FYI 1h beam is ~20k\$)
- Where should we put efforts considering the limited resources in hardware R&D?
- How do we manage the continuous increase in data rates?

# FRIB Approach to SRO

## After 2021 ...



## How did we achieve this?

- Our software DAQ and Analysis libraries runs in containers
  - » Minimum requirement for portability
- Parallel event processing
- Taking advantage of DOE resources (new paradigm - local cluster ONLY for readout out and fast diagnostic)

## Did it work? Spoiler: yes 😊



# Shopping List

- **New VME controller**
  - Wiener VMUSB obsolete and out of production
  - MVLC possible candidate but we need to access the API to control it – closed software...
  - We would prefer list mode readout but block mode is fine, ethernet data throughput
- **Global timing distribution system (resolution needed ~10-30ps at 200m)**
  - MIKUMARI (SPADI-Alliance) – HRTDC (Triggered/SRO)
    - » Good cost/channel, 64 channel, good resolution ~20ps, open source → actively collaborating with API software
  - WhiteRabbit
    - » DOE SBIR digitizer with WR timing (ongoing evaluation)
      - High cost/channel, limited number of channel per board, limited sampling frequency
  - CTS (Clock timing station): clock translator board for VME (WR, MIKUMARI, ...) → actively collaborating with RIKEN/SPADI-A in firmware development
- **General SRO electronics**
  - TDC, ASICs chips for TPC, QDC/ADC/waveform digitizer
    - » Some solutions have been developed by the SPADI-A and seem to fit our needs

