

SoLID DAQ preRD and plans



Data
Acquisition

SoLID collaboration meeting
January 9th 2025



Alexandre Camsonne

- Outline

- Capital
- Testing
- GEM chip
- Streaming DAQ

- Conclusion

Capital equipment DAQ

Requested

Item	cost/item	number	total
FADC 250	6000	104	624000
Gigabit serial connectors			40000
Cables	100	1664	166400
VETROC	4000	30	120000
TD	3000	16	48000
VTP	10000	31	310000
SSP	5000	4	20000
VTP	8000	1	13000
TS	4000	1	4000
TID	3000	31	93000
SD	2500	32	80000
VXS crate	15000	32	480000
VME CPU	7000	32	224000
		Total	2217400

Updated

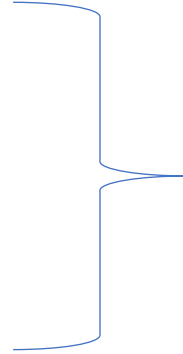
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Testing

- SBS GEn
 - VTP readout
 - APV25
 - High data rate : 2.1 GB/s
- NPS
 - Calorimeter trigger
- SBS GEp
 - Calorimeter trigger
- Moller
 - Compton
 - Counting DAQ
- HKS
 - Trigger with Cerenkov
 - High resolution TOF with MRPC
- Hall C experiments in HMS and SHMS : measure physics asymmetries ?
- Future parasitic beam tests
 - FADC + VTP + VETROC + VMM in on crate for testing : PVDIS one crate setup available with calorimeter and Cerenkov trigger
 - Acquired SAMPIC 64 channels sampler for MRPC
 - APV25 available after GEp5



Calorimeter trigger

Future SoLID preRD

- Highest priority : GEM chip
 - Evaluate SALSA chip in high background environment
 - Continue testing VMM board signal to noise
 - Develop dedicated ASIC chip for GEM
 - Test with uRWell
- Calorimeter and Cerenkov readout
 - FADC ASIC to be placed on detector : only LV and optical fibers going out instead of BNC cables
- High resolution timing
 - AARDVARC test in beam
 - High resolution FADC timing ASICS
 - Timing distribution with CODA
- Measure physics asymmetries (Hall C?)

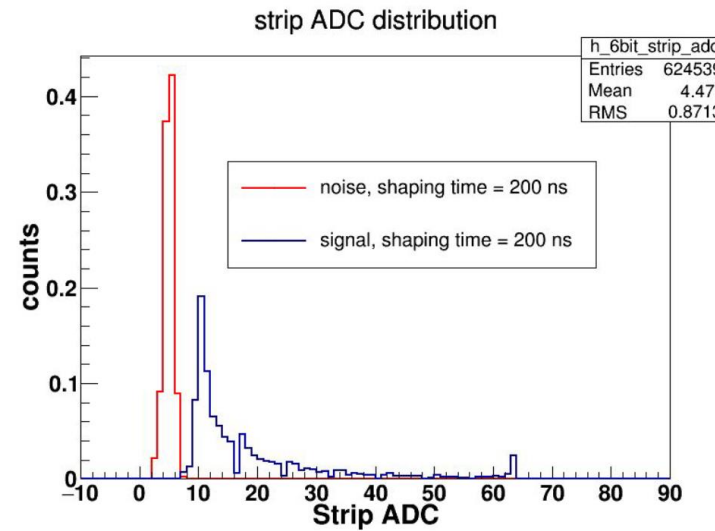
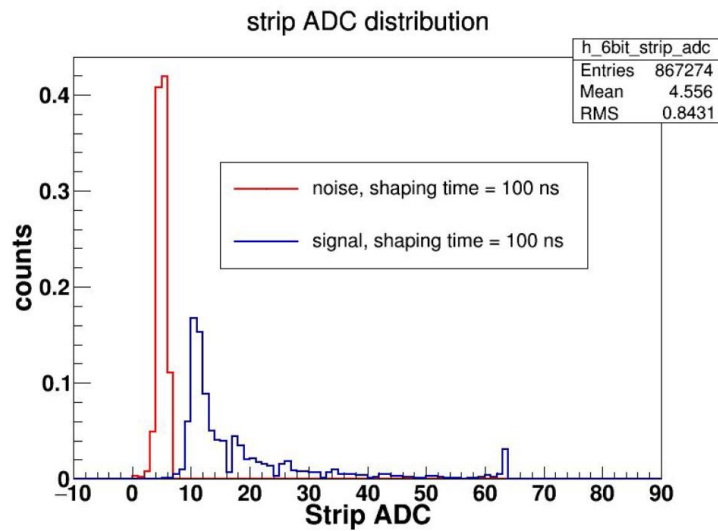
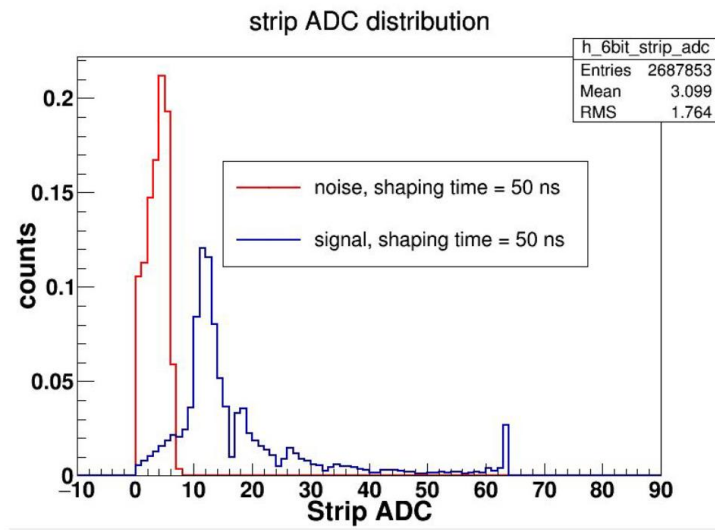
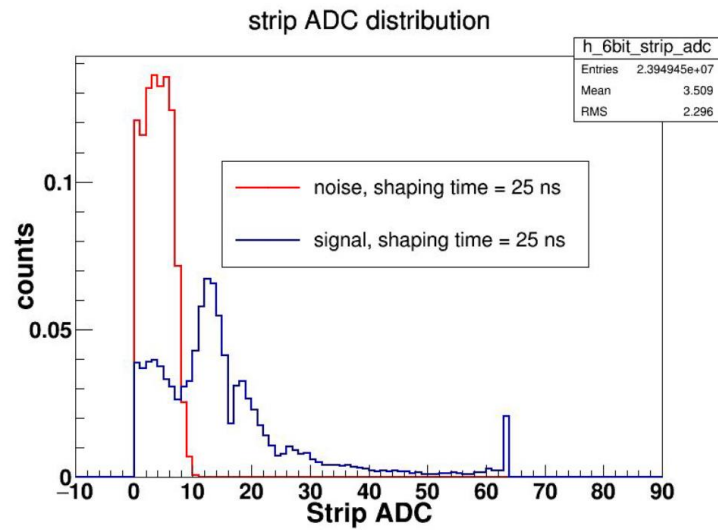
Test stands

- ESB
 - Racks and space starts to be available
 - Still need to clean up
- Detector group GEM/ uRWell
 - Plan to setup VMM prototype

VMM test

- Ordered two test board 1500 \$ x 2
- Build 6 SoLID prototype boards
- Evaluation board : can look at data with detector small subset of channels
 - Issue with external trigger but waiting for new firmware
 - Can check pedestal width
 - Signal to noise with detector with source and cosmics
 - Look at direct readout signals for 12 channels of detector
- Prototype development for data performance, test direct output with detector and X-ray source

Noise 6 bit 16mV/fC Sr90



- Amplitude for MIP not change much
- Pedestal width dependent on peaking time

Conclusion VMM testing so far

- 90 ns dead time in 6 bit mode
- Some noise seen in prototype
- Noise larger with decreasing integration time
- MIP a bit low in dynamic range of 6 bit prototype
- Implementing 10 bit to cross compare with evaluation board
- 250 ns for 10 bit mode
- Implement higher gain : Compton preAMP maybe ? Or higher gain chip
- Would like to explore SALSA option : same performance as APV25 with no dead time

Salsa

- Collaboration of Irfu CEA Saclay and U. of Sao Paulo.
- SALSA

- 64-Ch, updated design from SAMPA V5, migrating to 65 nm CMOS.
- Peaking time: 50 – 500 ns
- Inputs: Cin optimized for 200 pF; Rates: 25 kHz/Ch; Dual polarity.
- ADC: 12 bits, 10 – 50 MSPS.
- Extensive data processing capabilities.
- Triggerless and triggered operation.
- Power: 15 mW/Ch
- Gbps links.
- I2C configuration.

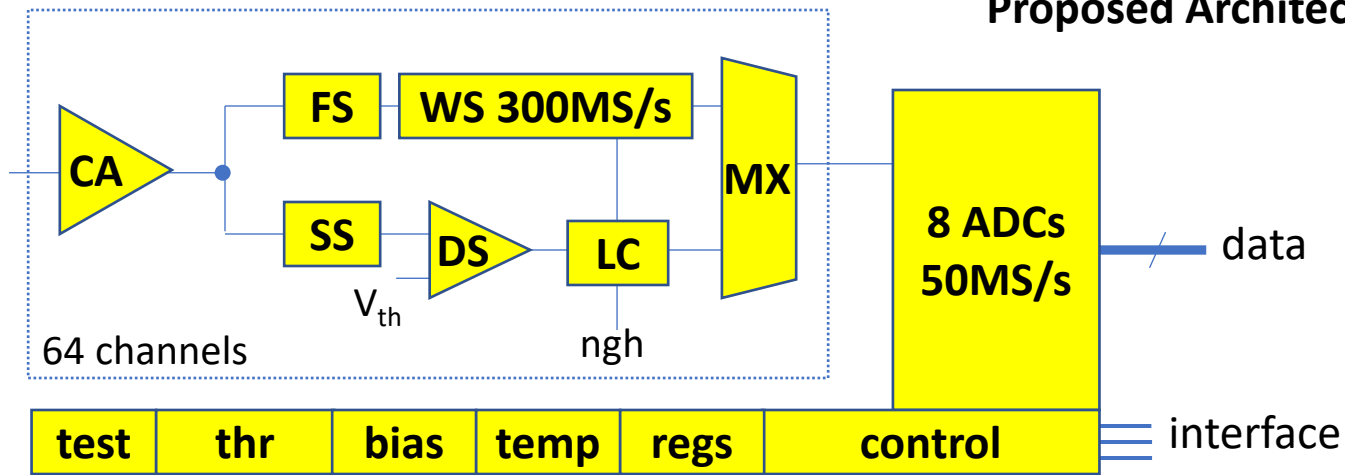
- Evaluation board available this year - Might want a dedicated SoLID version to match tracker low gain operation and handle high rates at input
- Can bypass analog part but need to develop analog front end
- Data links somewhat limited

- Might want a dedicated version of SALSA

New potential dedicated ASIC

- High luminosity running need to run
- Pile-up and deadtime can be significant
- Dedicated chip
 - Optimized gain and dynamic range
 - Optimize shaping time for high rate operation : from 50 ns to 25 ns or better
 - Zero dead time
 - High speed links to allow streaming

Proposed Architecture



CA: charge amplifier

- optimized for 50-200pF
- programmable gain 25fC to 250fC

FS: fast shaper

- programmable 5-20ns

SS: slow shaper

- for discrimination (zero suppression)
- programmable 20-100ns

DS: discriminator

- trimmable per channel
- external trigger option

WS: waveform sampler

- 128 sampling cells (127 effective)
- continuous sampling until trigger
- 300MS/s \rightarrow \sim 400ns waveform
- programmable pre-post trigger samples

LC: local control logic

- internal or external trigger
- neighbor (sub-threshold) logic

ADCs

- 8 operating at 10-bit 100MS/s
- waveform conversion time \sim 2.5 μ s

Data

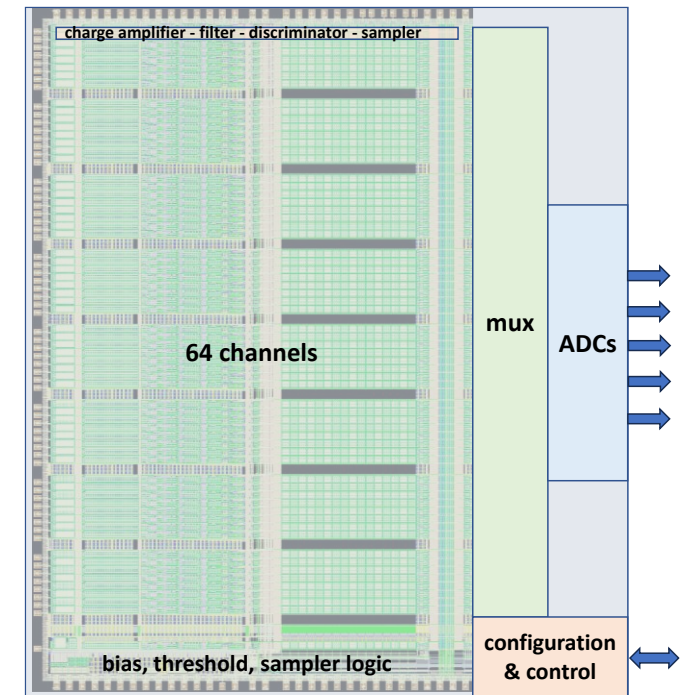
- channel, trigger, 127 samples = 1,280 bits per waveform
- up to 8 waveforms with sub-threshold neighbors = 10,240 bits
- up to 8 SLVS outputs operating in DDR at \sim 500MS/s
- conversion/readout time (dead time) \sim 2.5 μ s per event
- maximum event rate \sim 330kHz
- maximum data rate \sim 4Gb/s

Architecture

- event-driven analog/digital with acquisition/readout
- SEU tolerant register and logic
- DSP-ready

Power, Size, Technology, Schedule

- power consumption below 3mW/channel
- anticipated die size \sim 6x8 mm²
- technology TSMC 65nm 1.2V
- development time \sim 24 months (1st proto in 12 months)



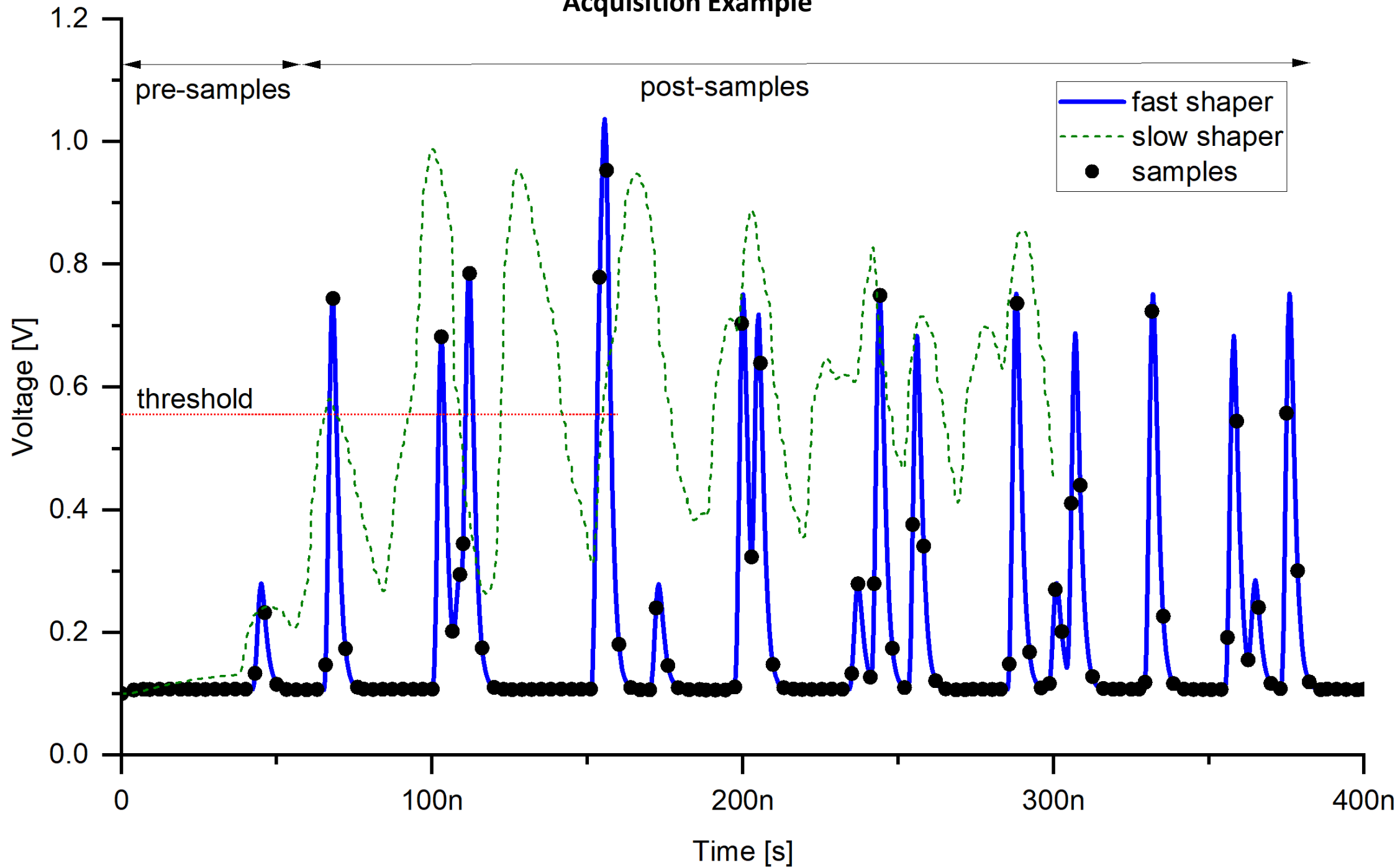
Design

- charge amplifier, shapers and samplers based on verified architectures
- ADCs from collaborative effort
- first prototype design time
 - \sim 12-13 months plus ADCs
 - ADC can be parallel effort
- second prototype design time
 - \sim 4-5 months

Key Features

- power-efficient analog zero-suppression
- efficient data generation and transfer
- highly flexible, highly programmable

Acquisition Example



ADC Collaborator Selection

Collaborator	Potential	US	Delivery [months]	Silicon Verified	Deliverables	Cadence	Architecture	Area [mm²]	Conversion Rate [MS/s]	Resolution [bit]	ENOB [bit]	Power [mW]	Calibration	Clock [MHz]	Input [ppV]	Output	Notes
Alphacore 1	?	*	?	no	?		?	?	100	12	?	?	?	?	?		
Alphacore 2	no	*		no			time interleave		500	12							
Pacific Microchip	low	*	?	no	?		?	< 1 to 2	50	12	>9	10	yes	500	1		migrates from 28nm
UM/Flynn	high	*	9	yes	sch, lay, support	*	SAR-assisted pipeline	0.16	100	14	~12	few	no	sampling	1		state-of-the-art
LBL/Grace	moderate	*	6-8	partial	sch, lay, support	*	pipeline	starts at 20	50?	12	>9	< 12	required, synthesized		1?		starts from 2.5V design
Cadence/Leuciuc	low	*															not offered, TBC
Grenoble/Dzahini	moderate		6-8	no	sch, lay, support	*	SAR		50	10	>9	1	no or trim	600	diff, 2?, 1.4pF		needs refs, high Z
AGH/Idzik	high			yes	sch, lay, support?	*	SAR	0.02	90	10	>9	1	no	sampling	1.1		Cadence fee pending
D&R/Agile	?	(*)	?	?	?	?	SAR	?	64	12	11.3	?	?	?	?		signed NDA, awaiting details
D&R/GUC 1	no																no response
D&R/GUC 2	no																no response
D&R/GUC 3	no																no response
D&R/NTLab 1	low			yes				1.03	100	12		60			1	serial	
D&R/NTLab 2	low						SAR		40	12	10.2	12			1	serial	

- UM/Flynn: works at state-of-the-art, provides higher resolution, may help with fast interface, may support future higher-performance versions, can provide DSP capability
- AGH/Idzik: has collaboration with IpGBT, has 8-ADC prototypes available for testing

Streaming readout overview

Streaming readout

- Send all data from each detector continuously (or self triggered)
- Pro
 - No trigger
 - If can be recorded : record all physics available
 - If cannot be recorded : full reconstruction and record event of interest with advanced triggering or loose trigger
 - AIML algorithm very efficient with unbiased data samples
- Con
 - Need deadtime less electronics : ideally all FADCs (but high power consumption)
 - Large amount of data to transfer to computer farm : cost in network
 - Large amount of data to be processed
 - Large amount of data to be recorded

Streaming readout option numbers

Detector	Area m2	SIDIS	Singles rate MHz	Event size bytes	Data rate GB	PVDIS	Singles rate MHz	Event size bytes	Data rate GB	JPSi	Singles rate MHz	Event size bytes	Data rate GB
LGC	0.7	16	112	16	1.792	80	560	88	49.28	40	280	16	4.48
HGC	1.2	160	1920	16	30.72		0	88	0		0	16	0
SPD_FA	15.2	0.02	3.04	16	0.04864		0	88	0	0.06	9.12	16	0.14592
SPD_LA	3.7	0.12	4.44	16	0.07104		0	88	0	0.25	9.25	16	0.148
EC_preshower_FA	19	33	6270	16	100.32	90	17100	88	1504.8	77	14630	16	234.08
EC_shower_FA	19	10	1900	16	30.4	9	1710	88	150.48	14	2660	16	42.56
EC_preshower_LA	4.1	45	1845	16	29.52		0	88	0	80	3280	16	52.48
EC_preshower_LA	4.1	5	205	16	3.28		0	88	0	19	779	16	12.464
GEM	37	800	296000	16	4736	500	185000	16	2960	1600	592000	16	9472
	Rate in GB/s				4932				4664				9818

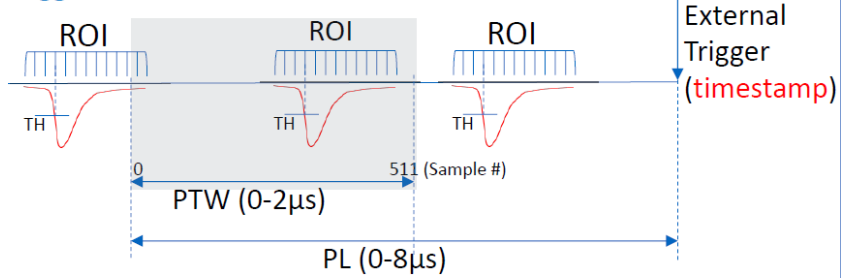
Around 10 to 5 TB/s, about 1000 more data than triggered

Updates from latest streaming workshop

- <https://indico.bnl.gov/event/24286/timetable/#20241202>
- Relevant talks for SoLID
 - CODA in streaming mode
 - Background reduction
 - TPC real time tracking
 - Event selection of streaming data with AIML
 - ...

FADCs - Triggered vs Streaming

Triggered Mode

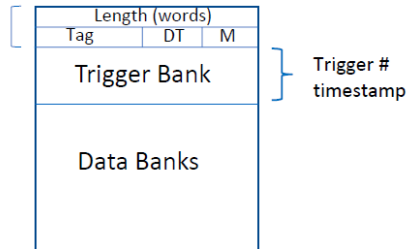


PL: Programmed Lookback
PTW: Time window

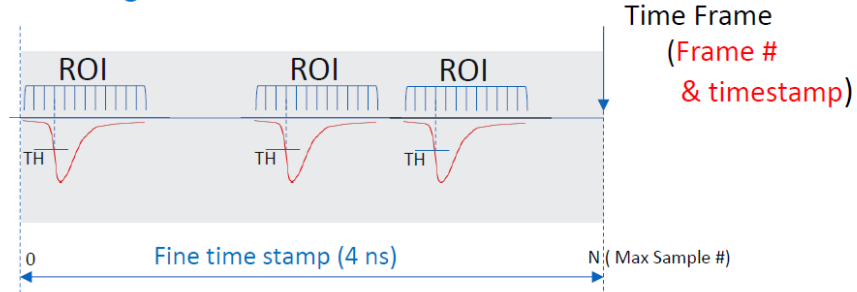
Data we get on a trigger:

- FADC waveform values for the ROI
- Threshold Sample # (hit time)
- Trigger absolute timestamp (48 bits)

ROC Data Format



Streaming Mode

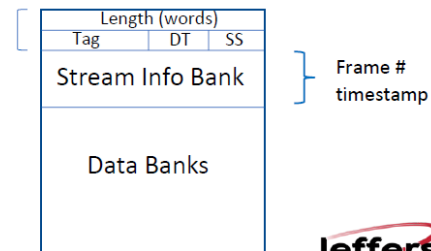


1 Frame = N Clocks (up to 16bits, currently 65536 ns)

Data we get for a Frame:

- Pedestal subtracted sums over an ROI for every hit over threshold
- Threshold sample # fine time stamp for each hit
- Frame # and absolute time stamp for the frame

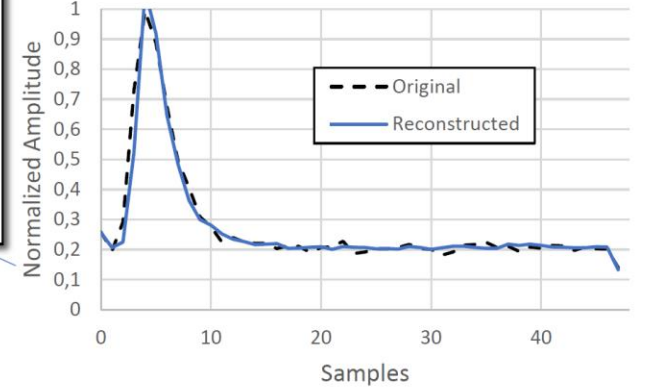
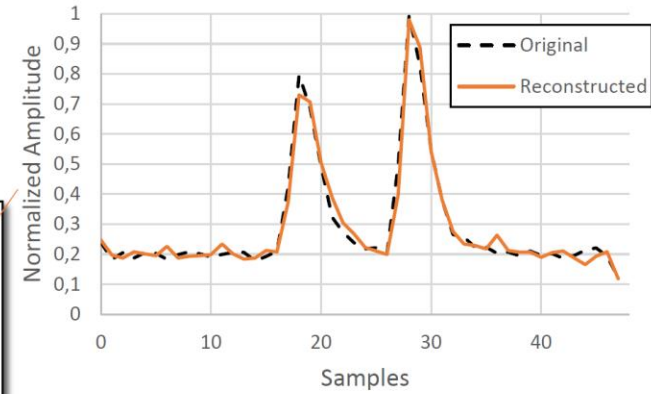
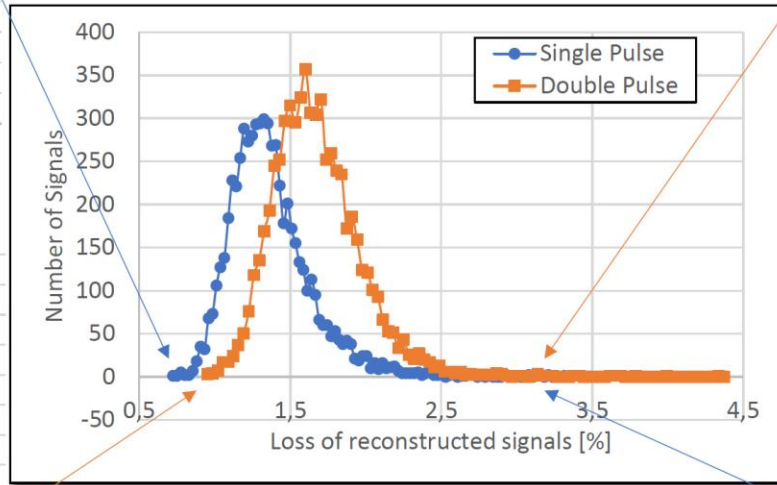
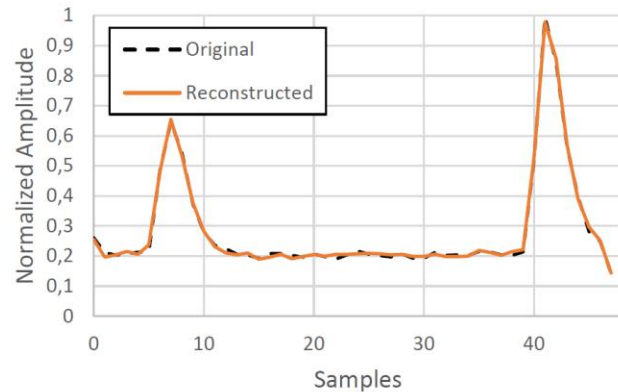
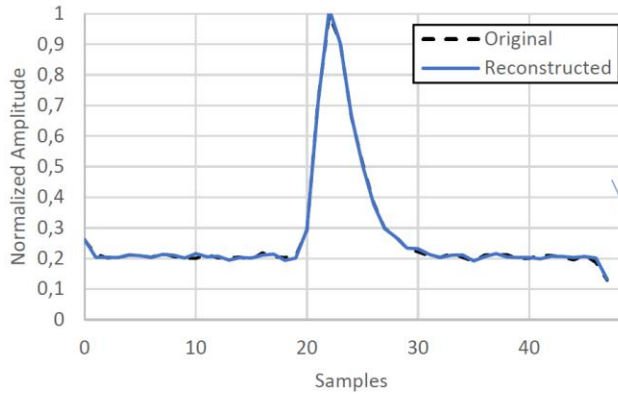
ROC Data Format



Jefferson Lab



Signals Compression



Fabio Rossi

The proposal

Intelligent experiments through real-time AI: Fast Data Processing and Autonomous Detector Control for sPHENIX and future EIC detectors

A proposal submitted to the DOE Office of Science
April 30, 2021

- Embed ML algorithms on FPGAs
- Stream MVTX and INTT to FPGAs and determine if HF event is present through topology
- Send tag downstream to readout TPC
- Allows us to sample remaining 70% of collisions
- Successfully renewed in 2023
- Successful LOI in Nov. 2024, DOE requested full proposal in Jan. 2025 with outlook to EIC

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Constructing ML algorithms

- Developed algorithms as Graph Neural Networks (GNN)
- Advantageous over Convolutional Neural Networks (CNN) by adding edge information
- Detector and physics knowledge will improve predictions
- Algorithms deployed at several points on FPGAs:
 1. Data decoding – conventional logic
 2. Hit clustering – conventional logic
 3. Local to global conversion – conventional logic
 4. Fast tracking – machine learning
 5. Topological separation of HF signal from background – machine learning

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• Conclusion

- Capital equipment
 - All elements received for SoLID DAQ besides CPU : test stands available for next beam test
- Test stands behind set up
- Developments of SoLID trigger and readout in previous and upcoming experiments
- GEM chip solution to be finalized
 - VMM can work but not ideal
 - SALSA promising but need R&D
 - Looking into possibility of dedicated ASIC
- Streaming option
 - About 5 to 10 TB/s about 1000 more than triggered
 - Might be able to handle with AIML progress, network progress and CPU
 - Streaming readout is an option with upgrade of data links and HPDF
 - Development of AIML data reduction method, might want to join existing effort
- SoLID in streaming mode, could be the ultimate JLab detector – Just run detector at full luminosity all the time and extract all possible physics after the run but data rates are challenging major R&D on how to handle background and data