Status of SVT for a 2025 Run

Tim Nelson

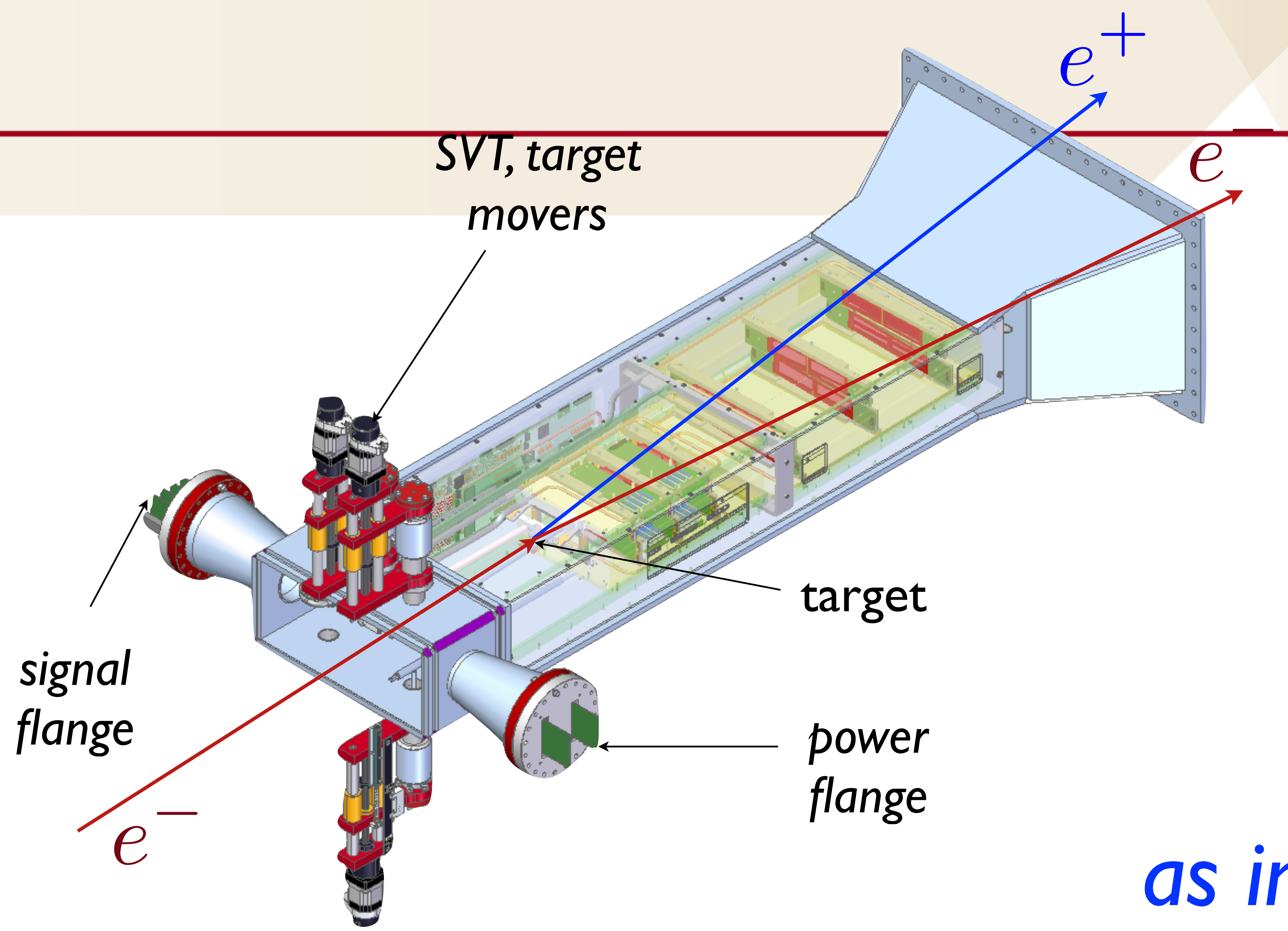
June 5, 2024

The HPS SVT

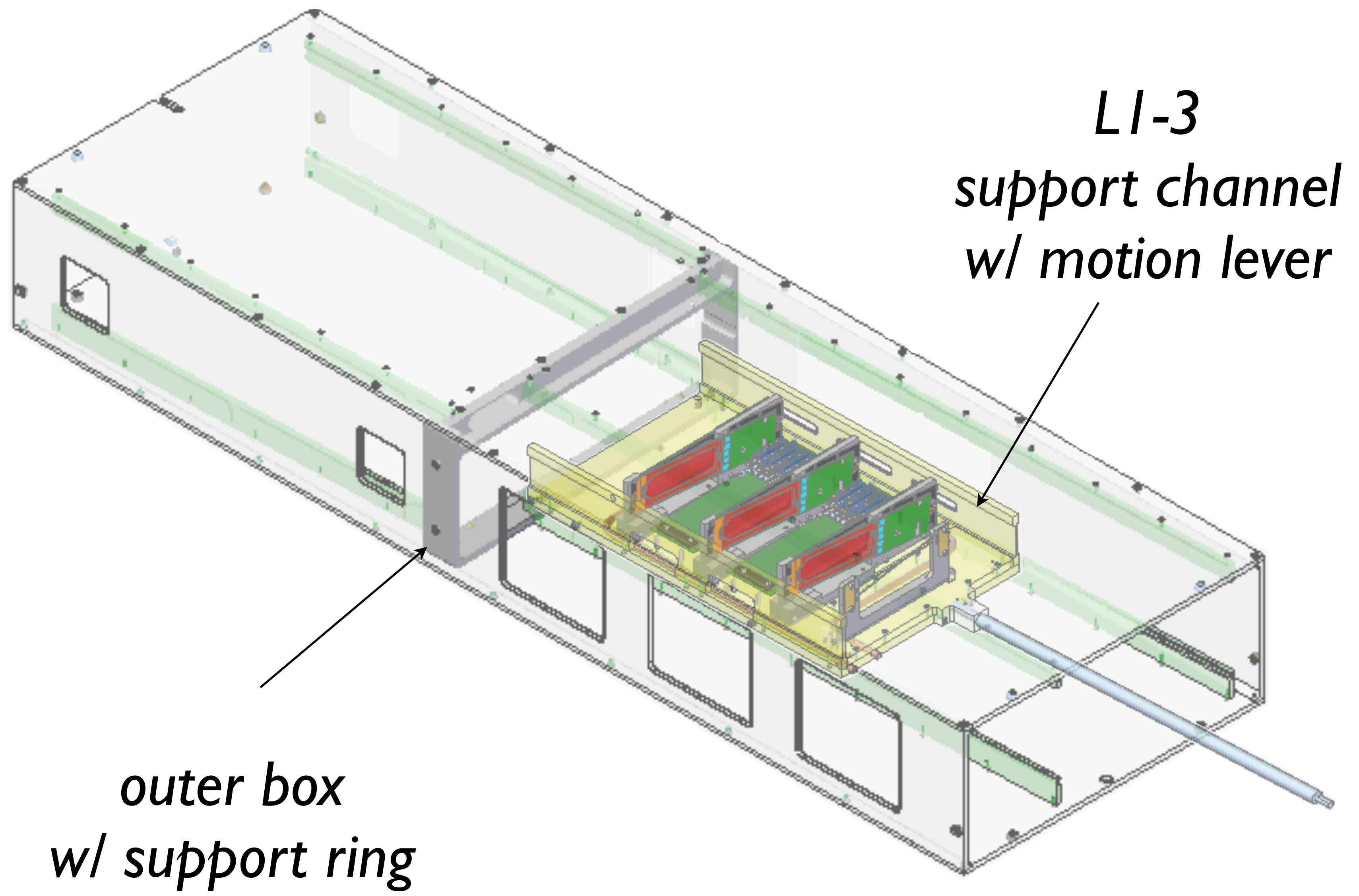
7 double-layers of silicon strips, each plane measures position (~6-10 μm) and time (~2 ns) with ~0.2% – 0.35% X_0/hit.

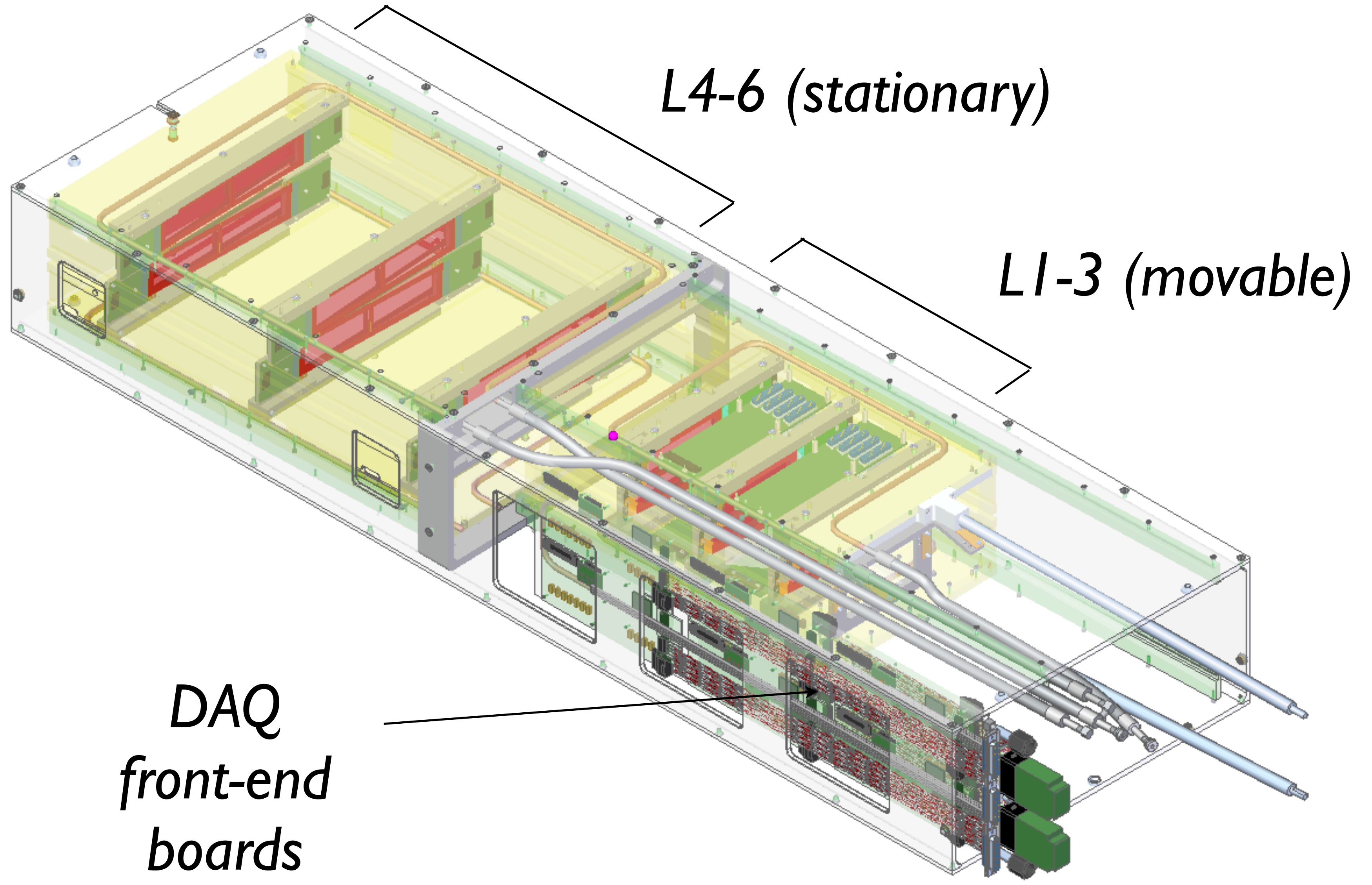
Operates in an extreme environment:

- beam vacuum and 1.5 Tesla magnetic field
  ⇒ constrains materials and techniques
- sensor edges 0.5 mm from electron beam in L1
  ⇒ must be movable, serviceable
- sensors see large dose of scattered electrons
  ⇒ must be actively cooled to -20 °C
- 24528 channels can output >100 gb/sec
  ⇒ requires fast electronics to process data



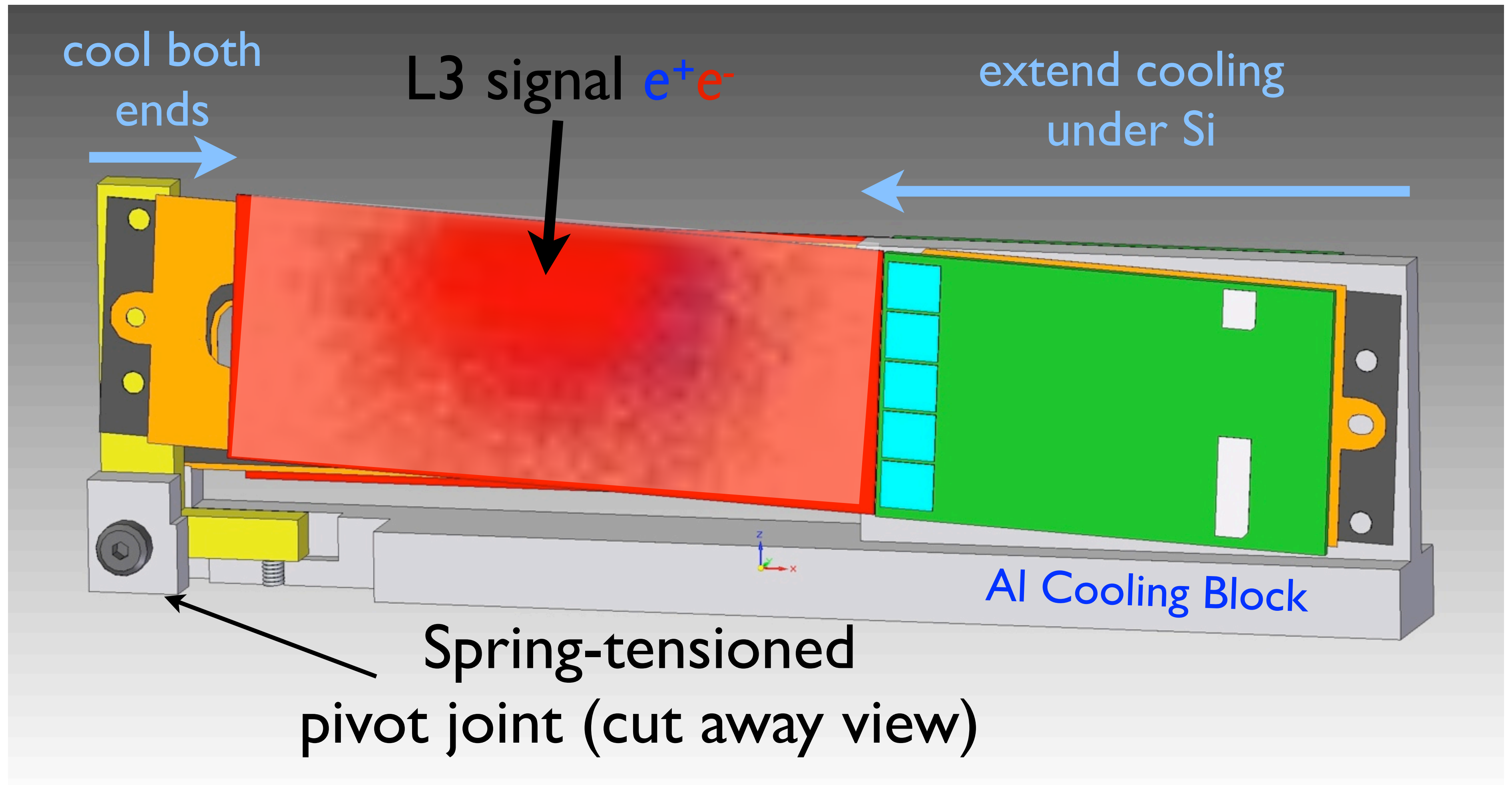
as installed in 2015





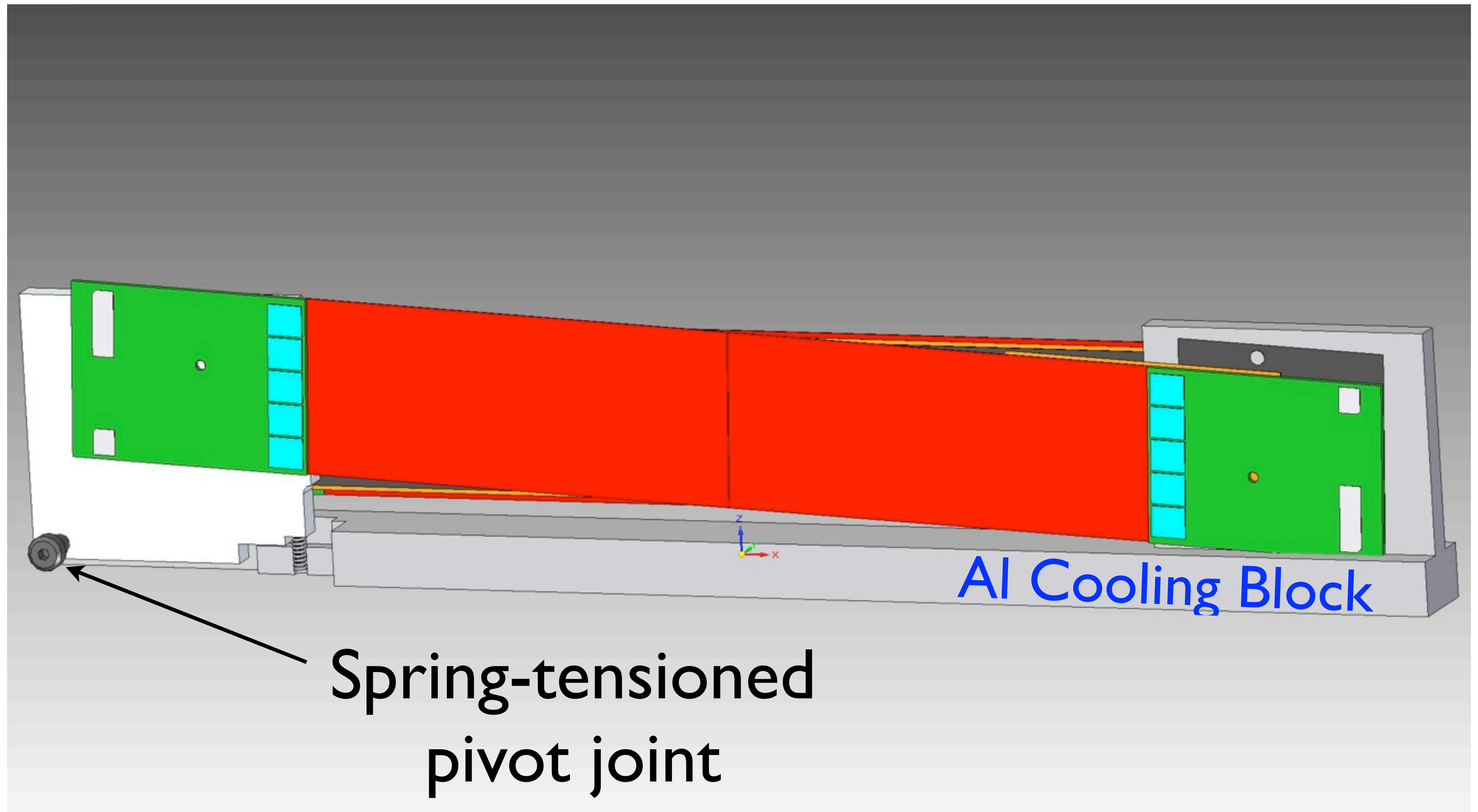
HPS SVT Modules

L3-4 reuses half-modules from HPS Test, but with improved module supports: tension CF between cooled uprights.



L5-L7 extends concept to allow same material budget for longer modules.

Eliminated pigtails in favor of cleaner solution, low-profile Samtec connectors



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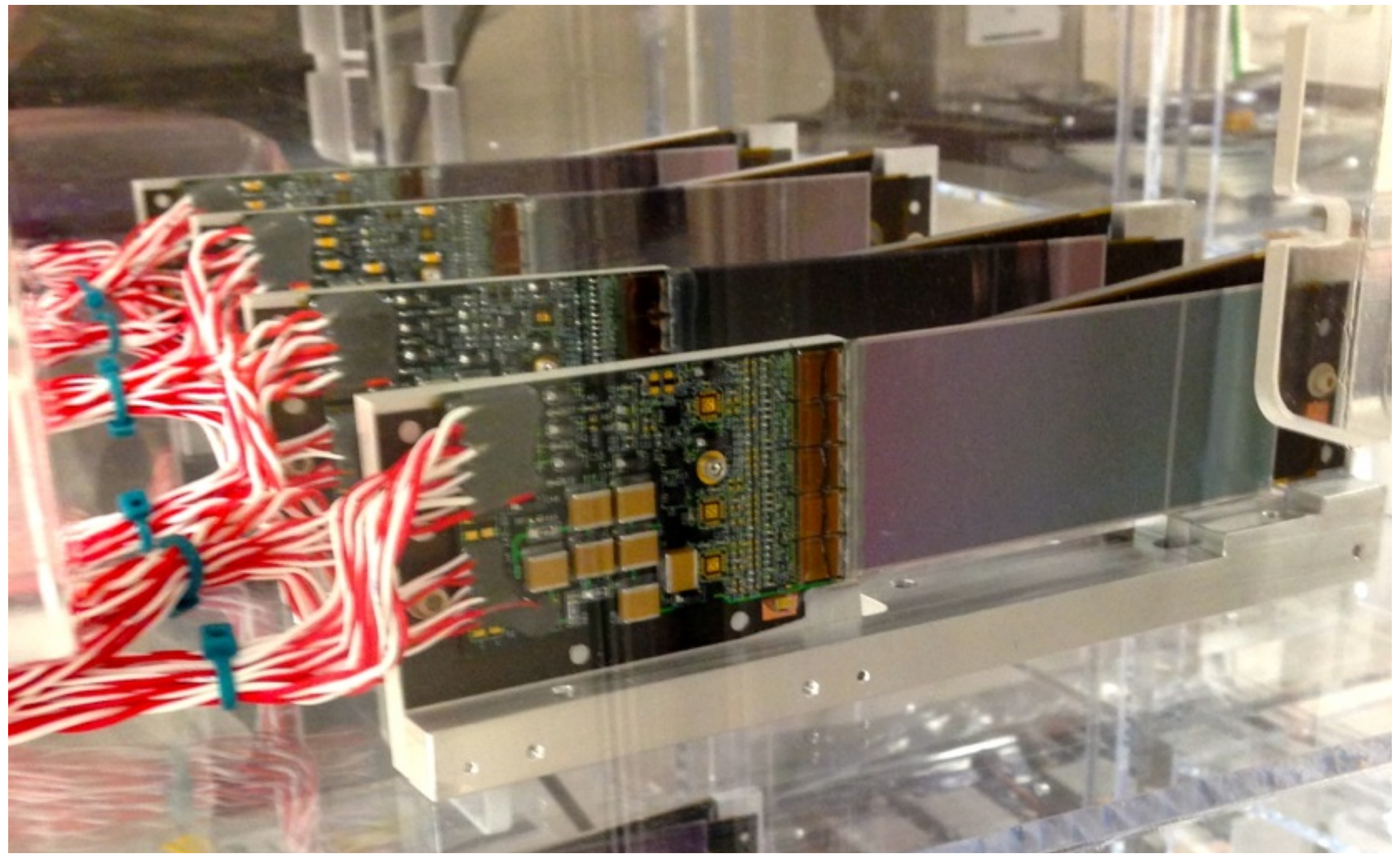

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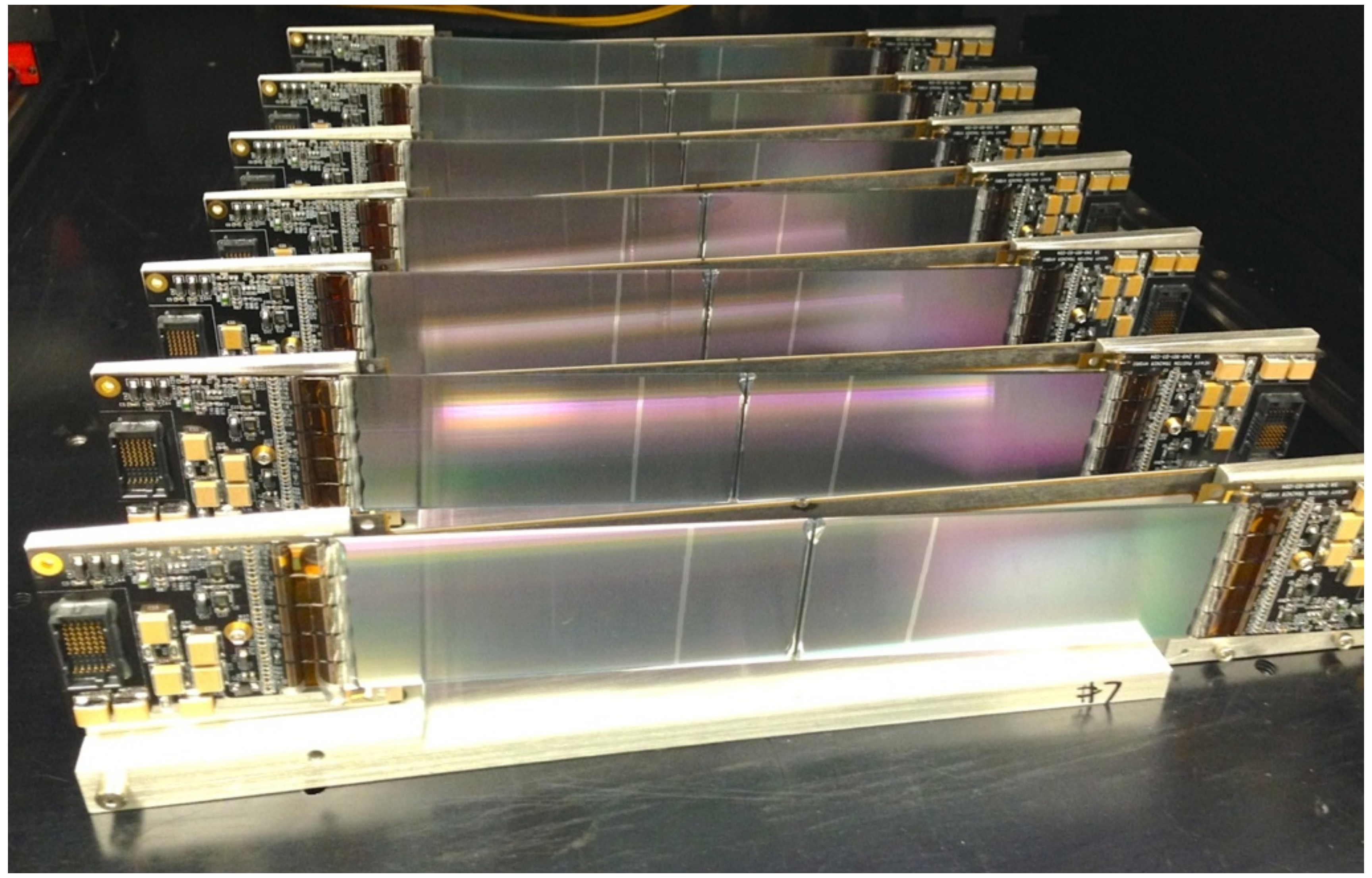
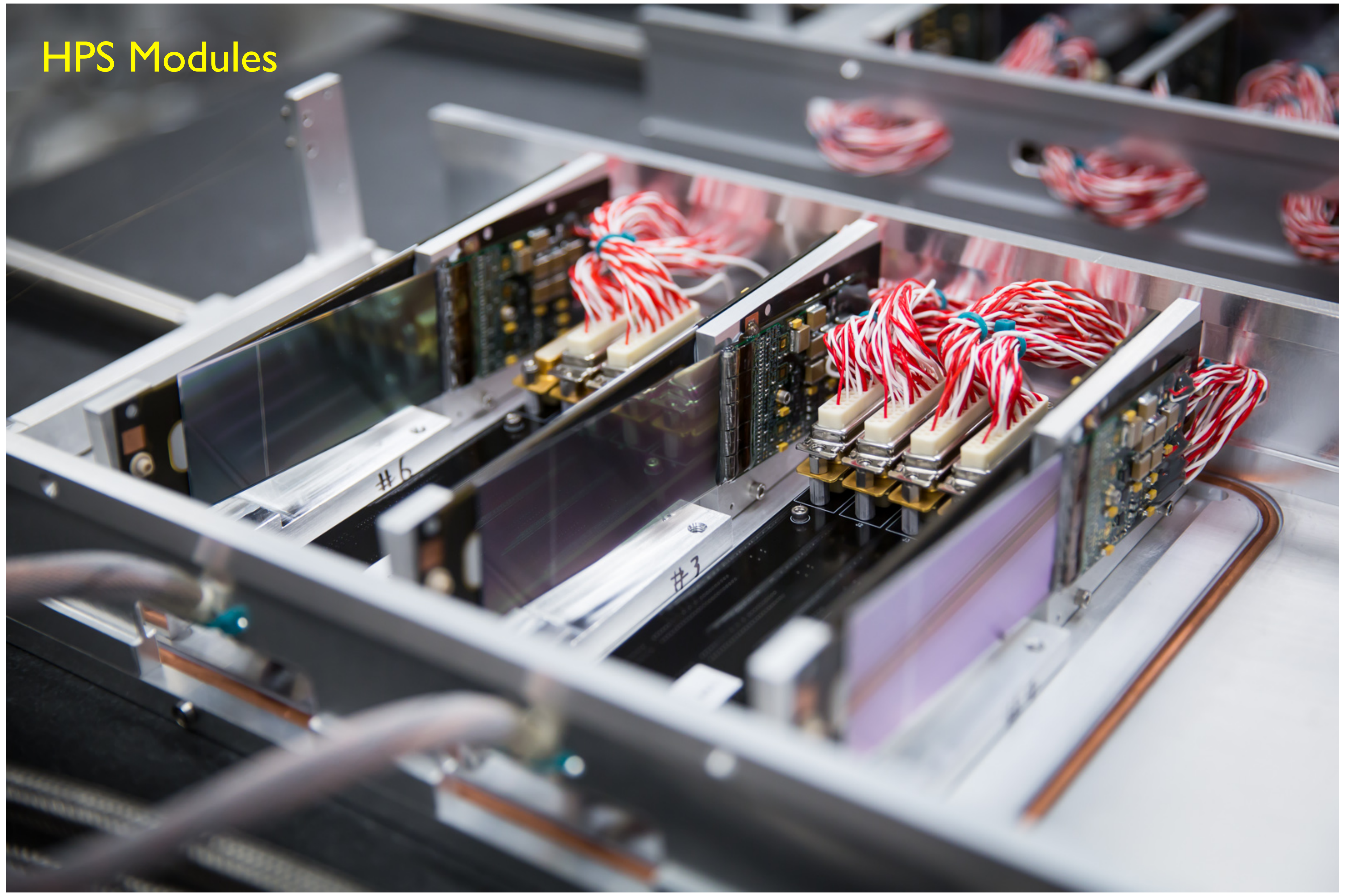
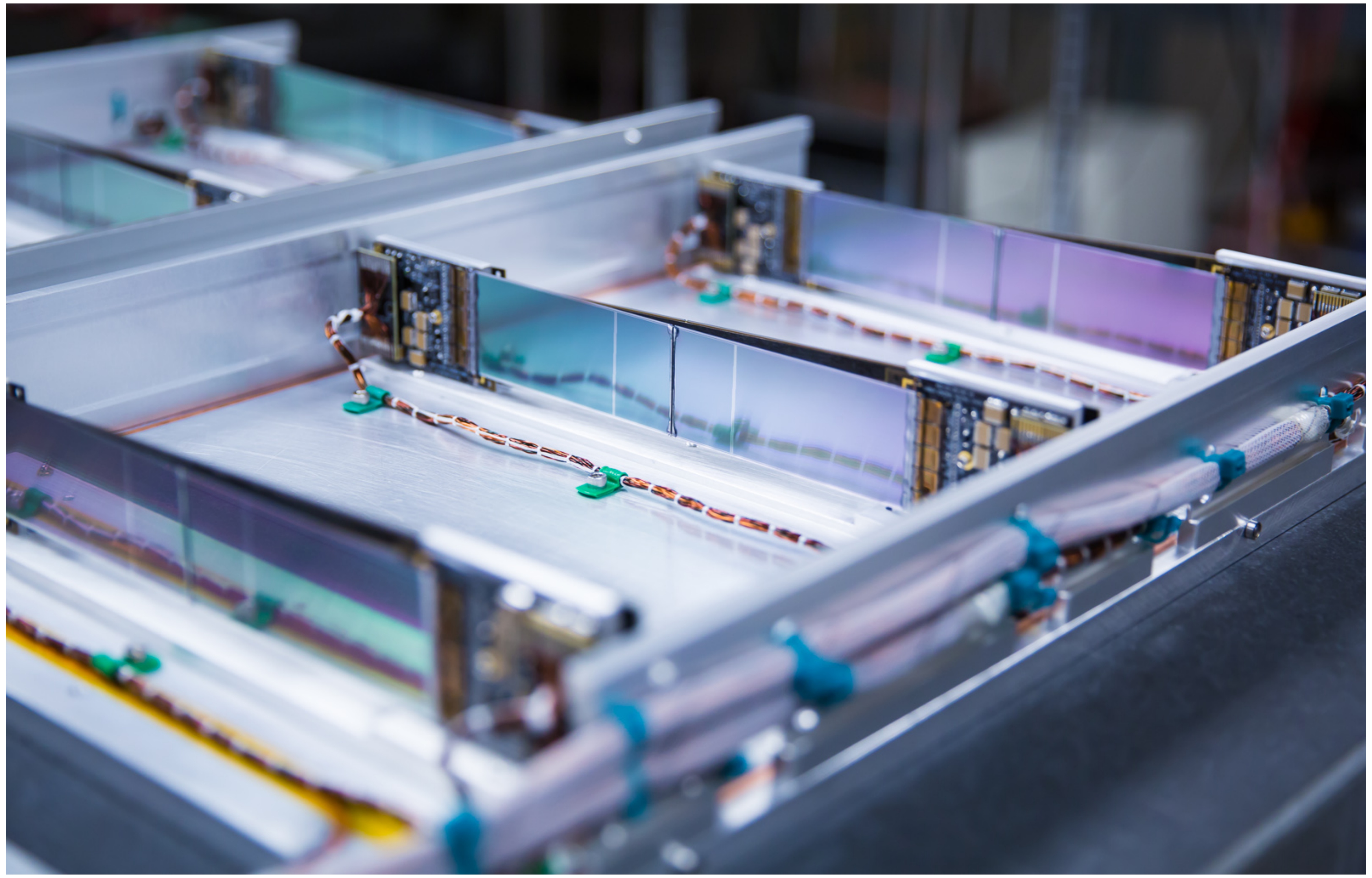


The HPS SVT (2015 baseline configuration)





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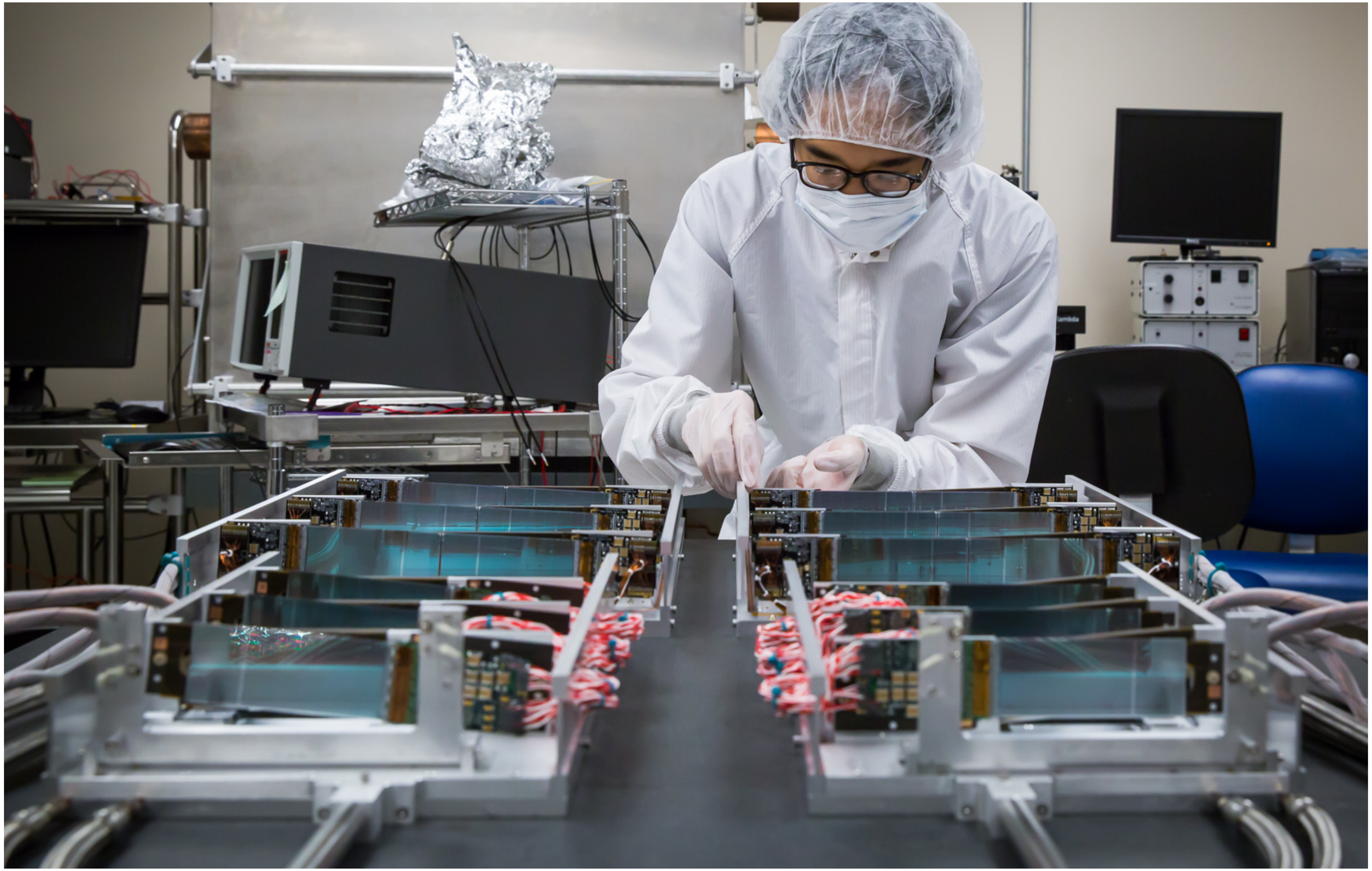

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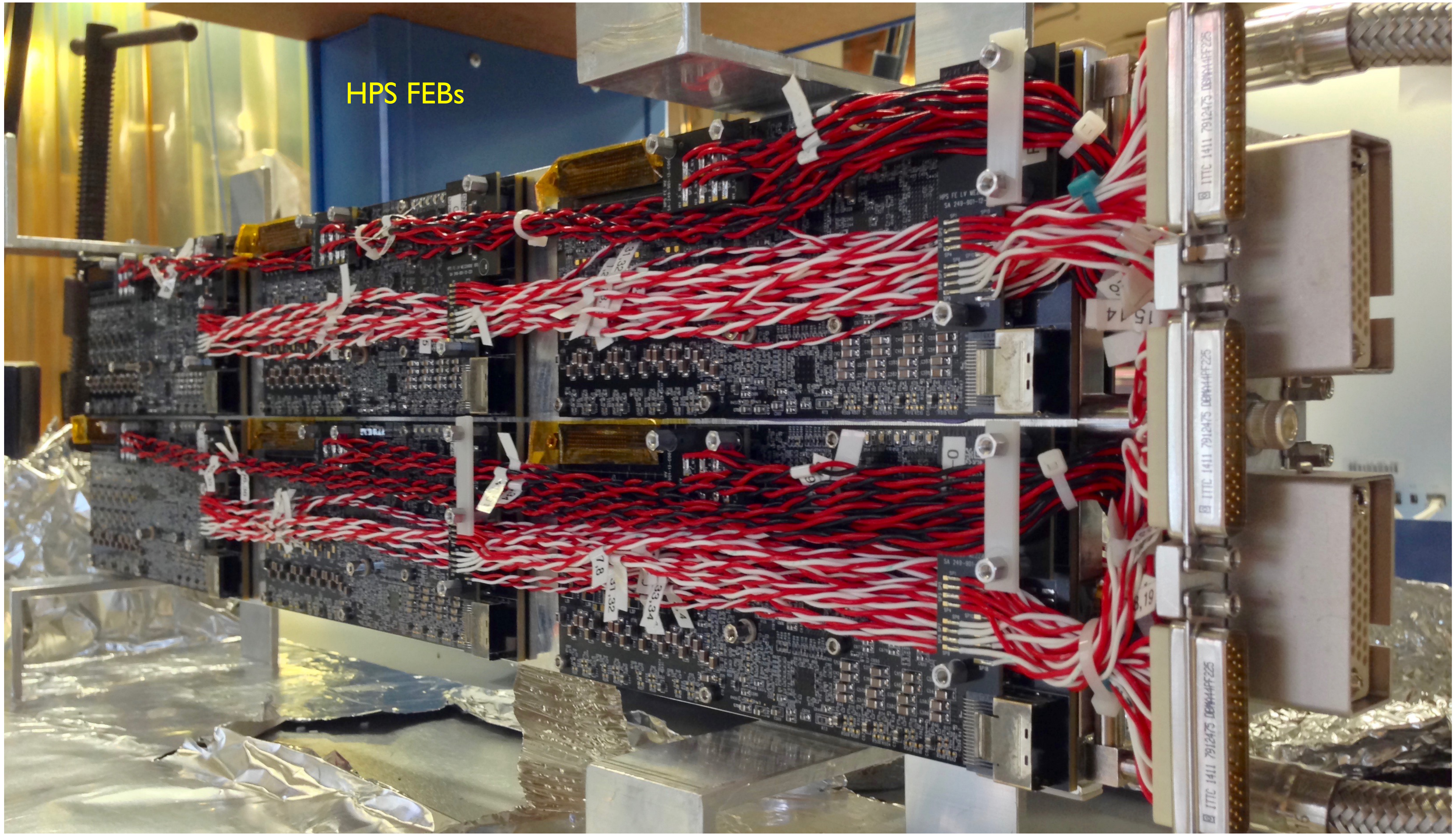

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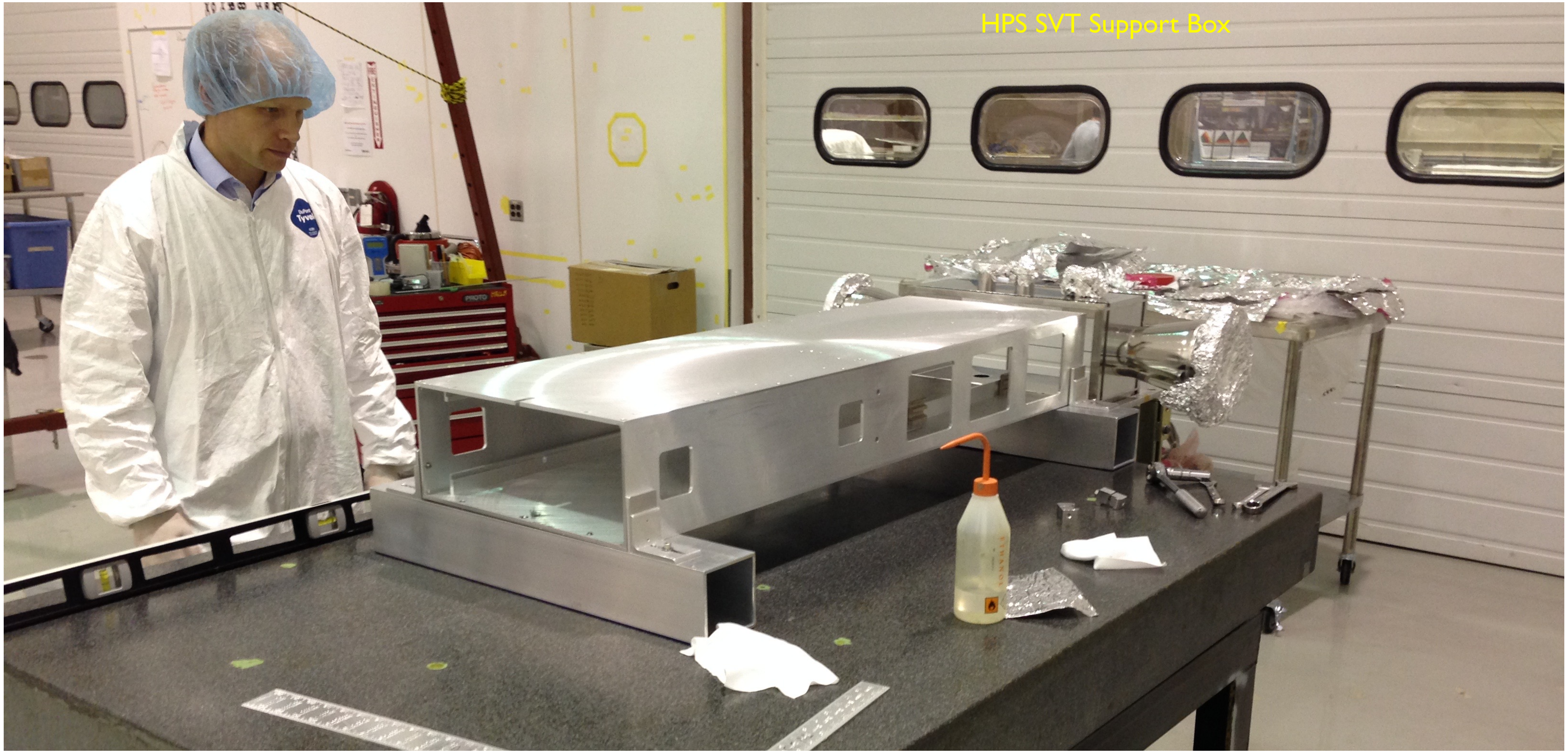

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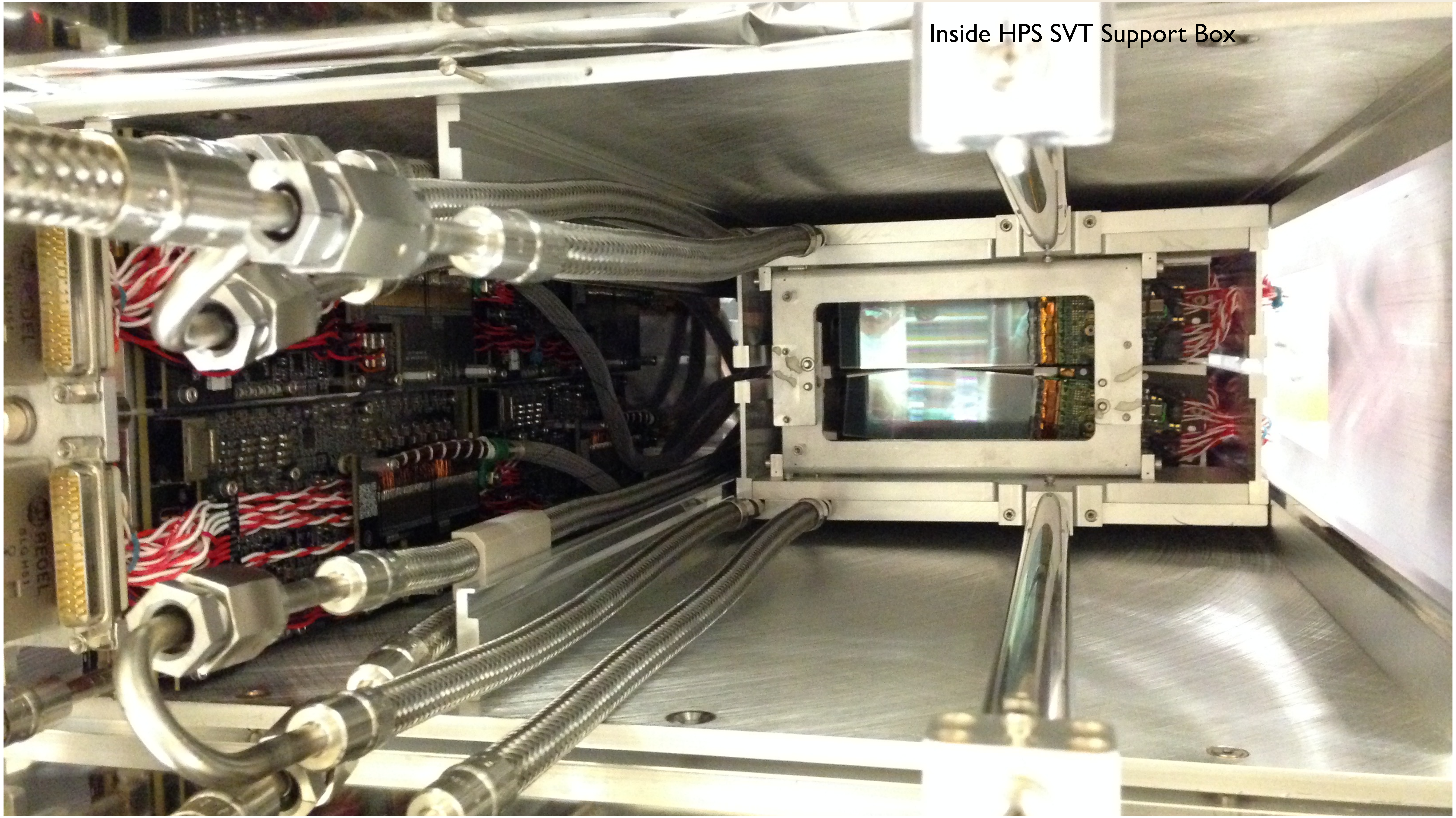

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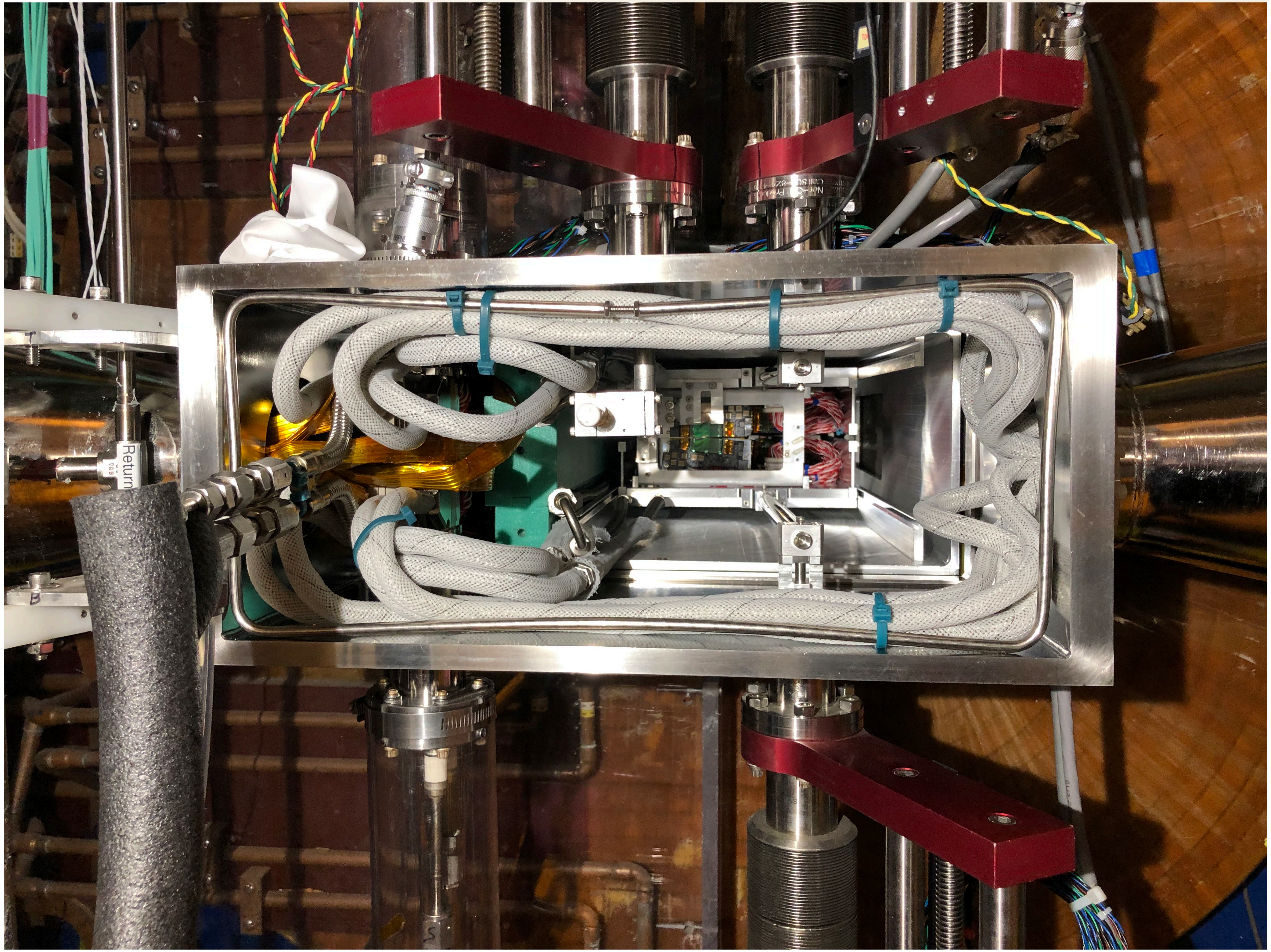
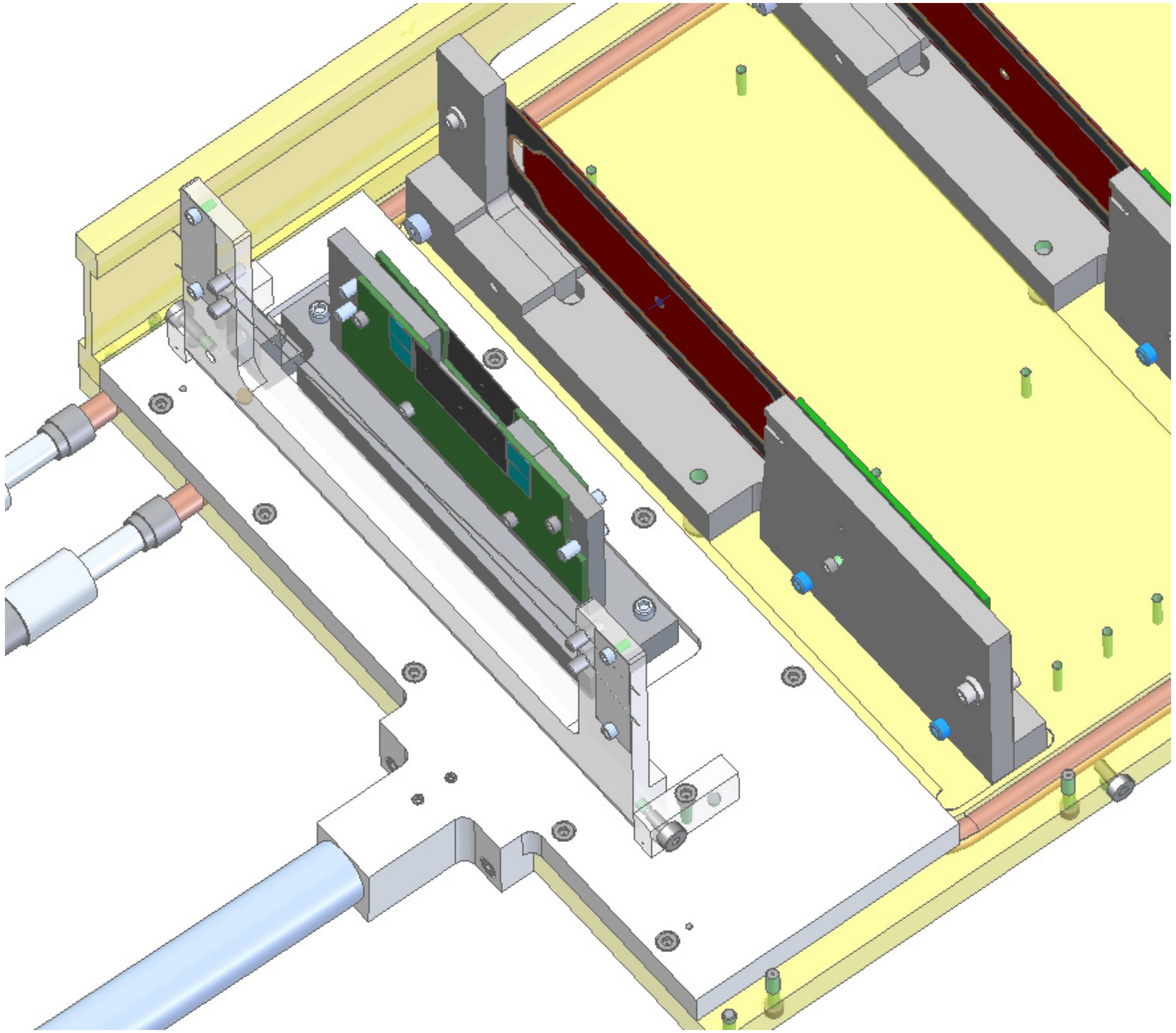


Changes for 2019: addition of new L1, and L2 replacement



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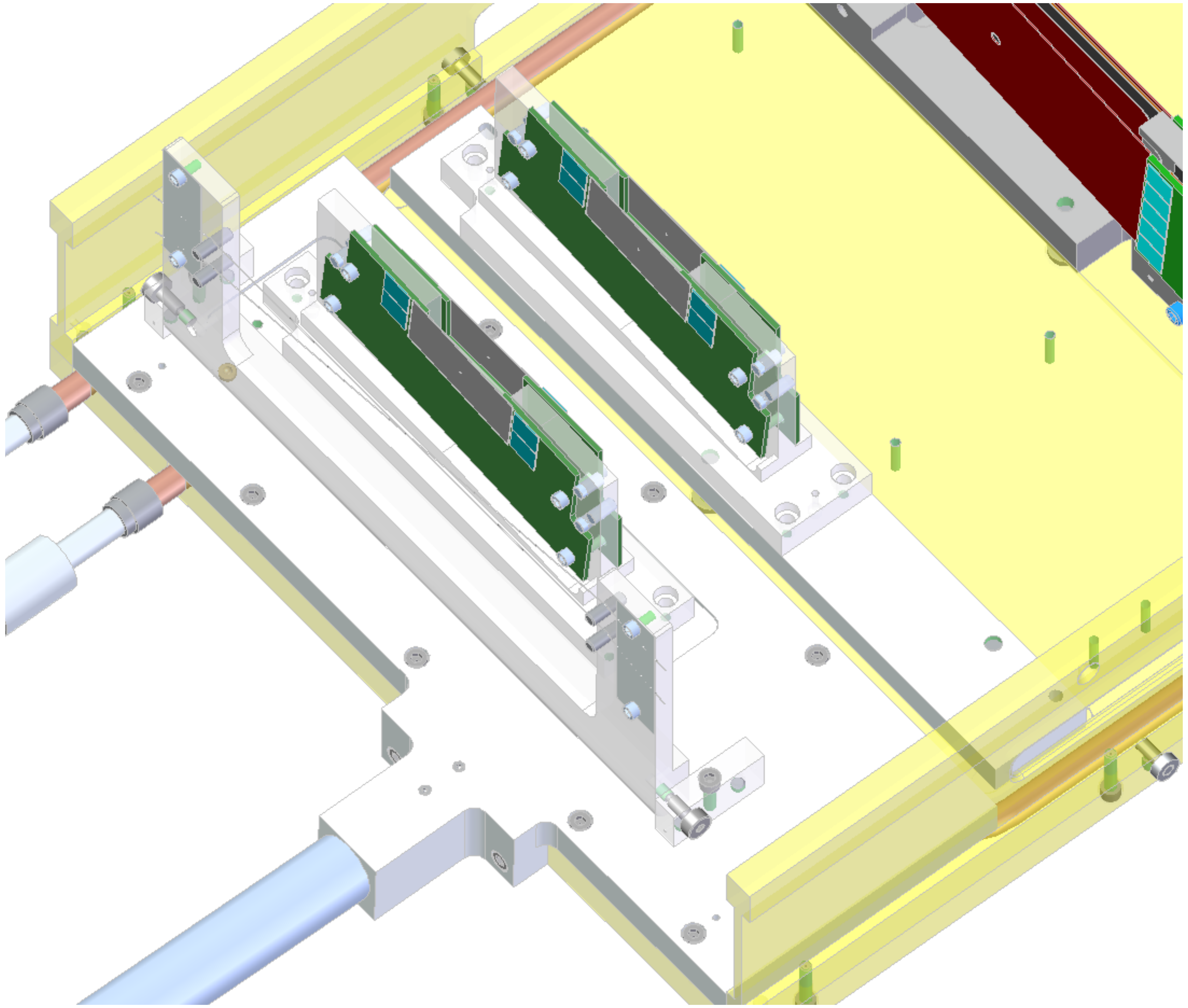

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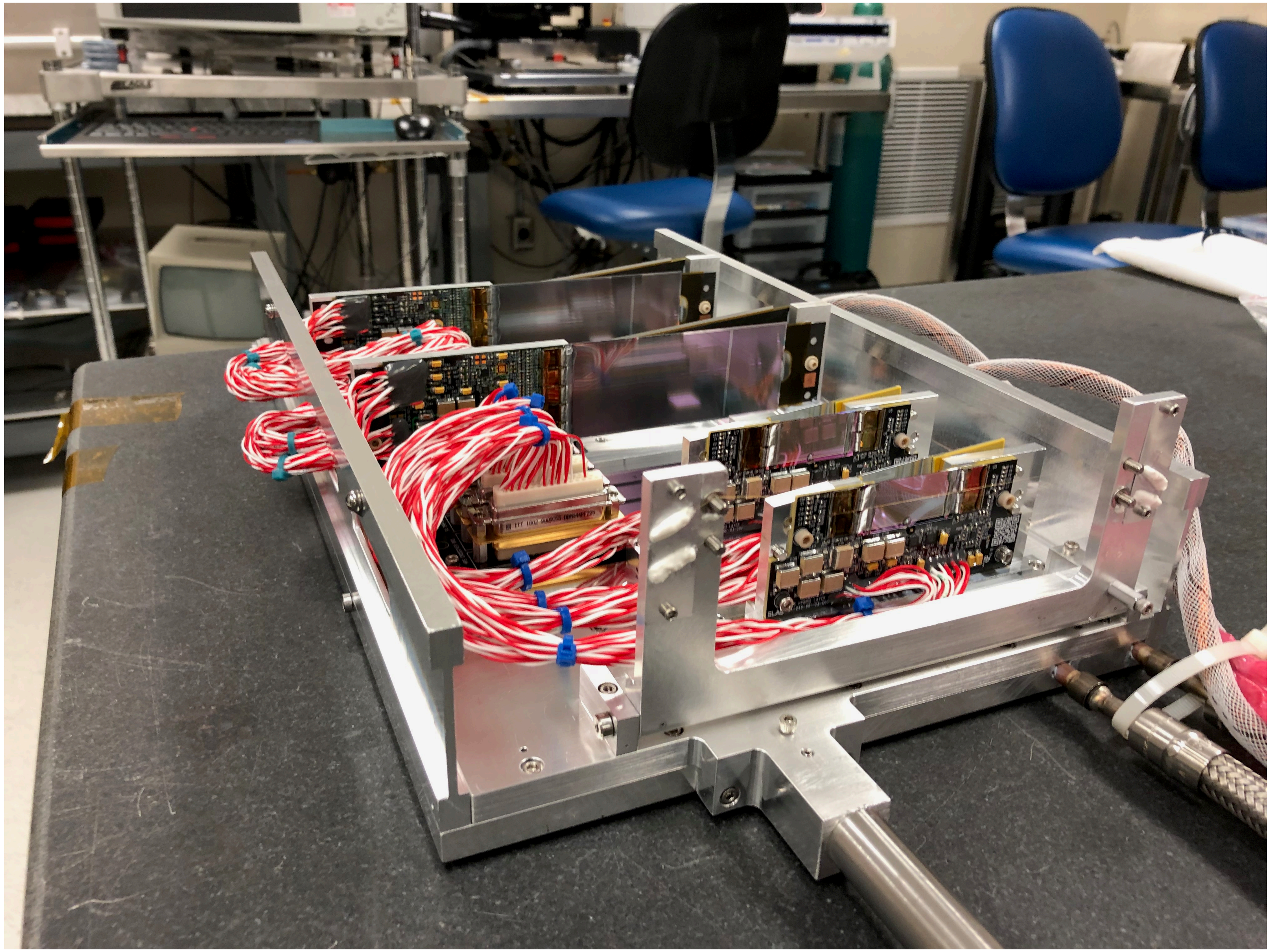
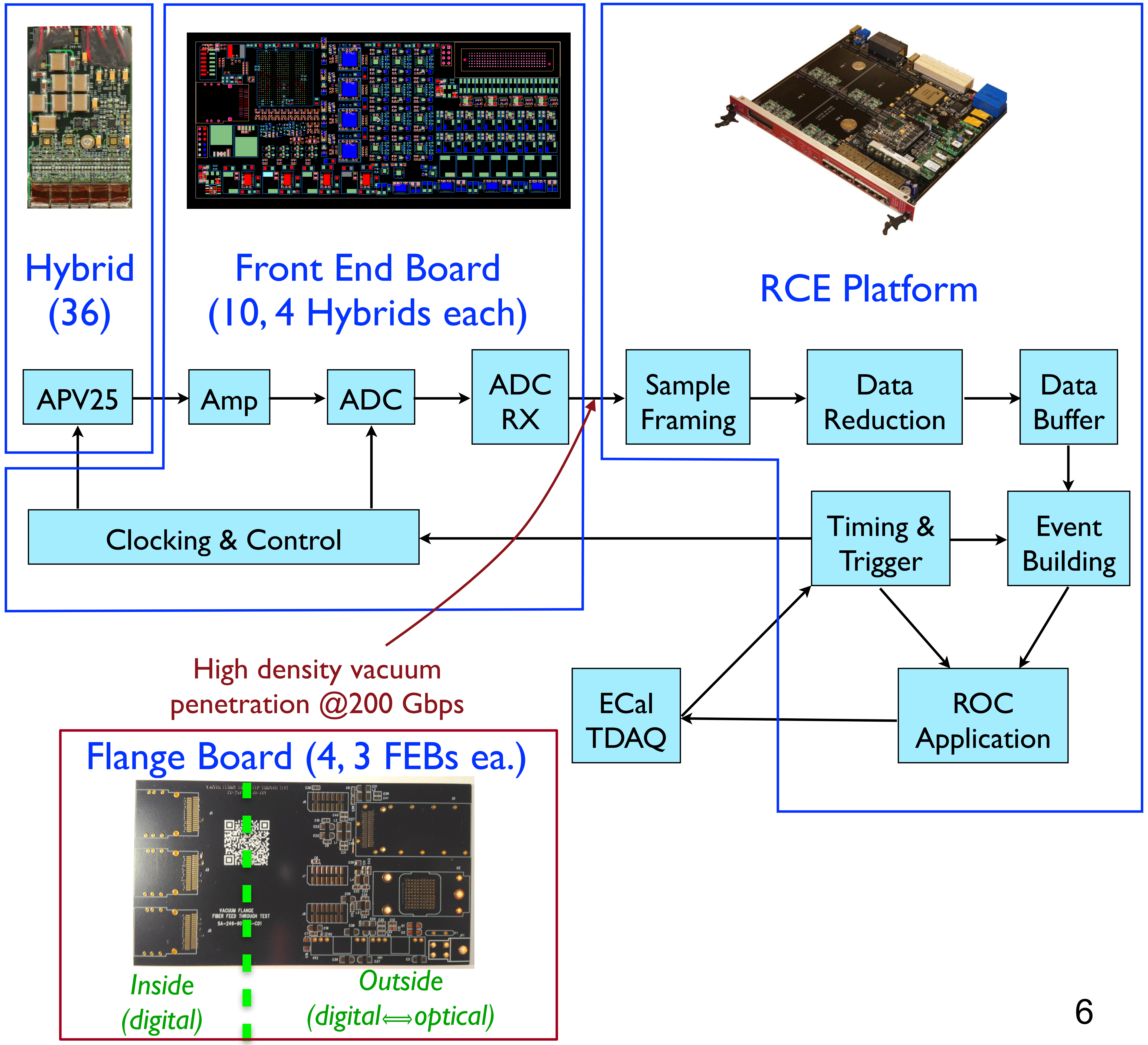


HPS SVT DAQ

- Hybrids hosting, 4-5 CMS APV25 each
- In-vacuum ADC, voltage generation and power distribution/control on Front End Boards
- Penetration for digital signals via high-density PCB through flange. Optical conversion on outside of flange.
- Firmware support for APV25 burst trigger mode (50 kHz trigger rate for 6 samples)
- Wiener MPOD power supplies



Overview of Work after 2021 Run

SVT

- L1-2 Modules: silicon won't withstand another run, only one spare (replace)
- L5-7 Modules: hole in L5, no spares (build more)

DAQ - details from Ben Reese

- FEBs: only two perfect spares. Design error could create failure mode. (replace)
- Data Flange: used spare in 2021, original no longer 100% (build another)
- TI PCIe Card: development work for version needs to be completed. (finish work)

We have funds in hand to do all of these things

We have time before another run to undertake them at a reasonable pace

Slim-edge Cleaving

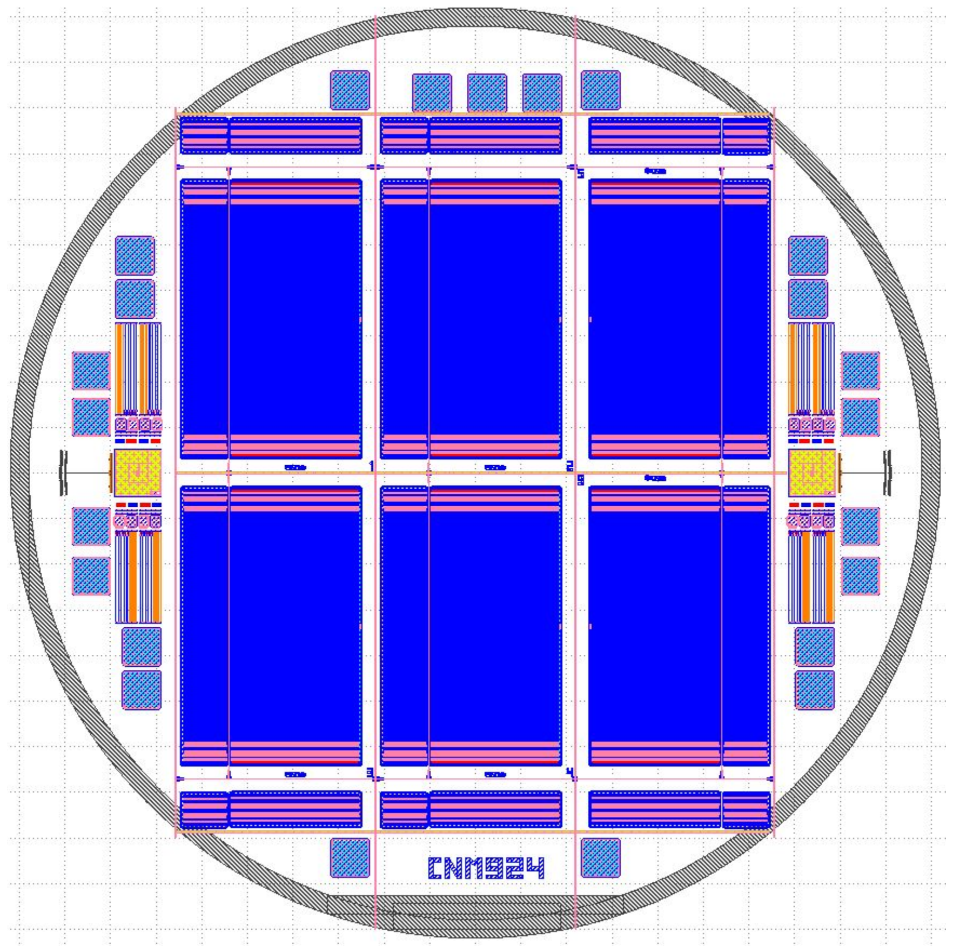
Process developed by Vitaliy at UCSC with collaborators ~10 years ago

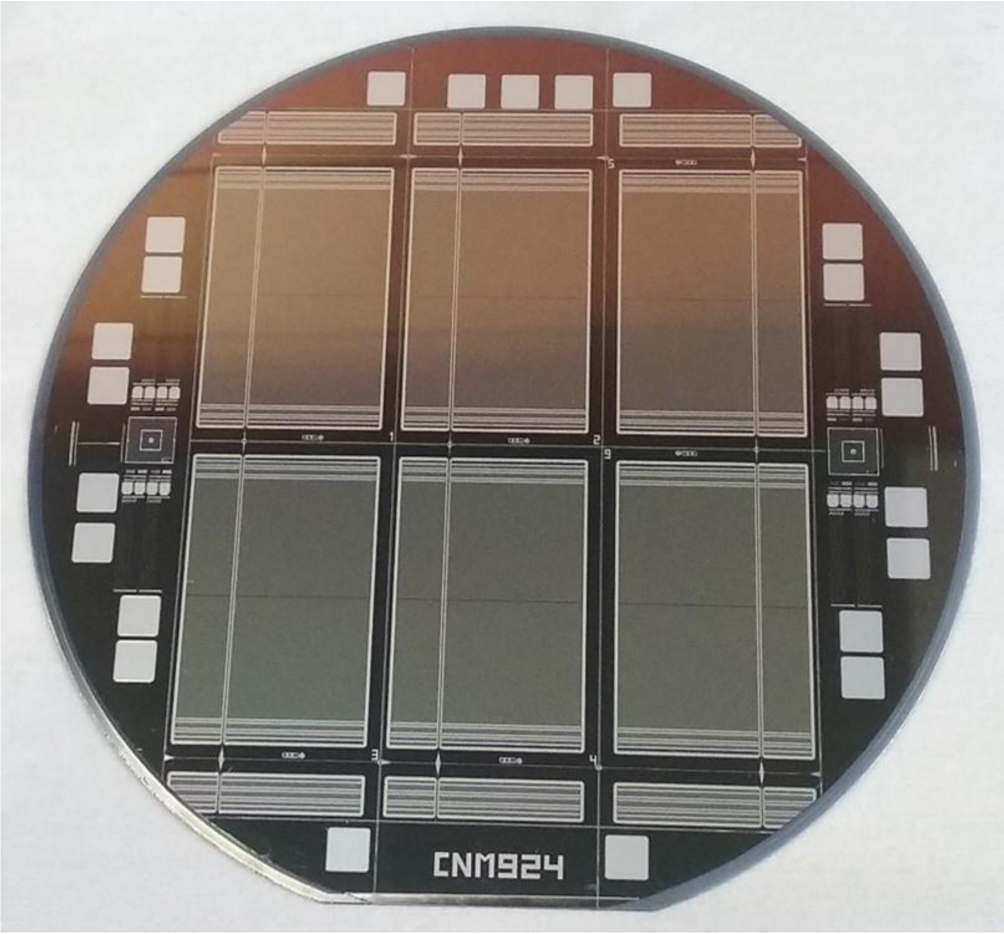
- Scribe a line with diamond tip or laser
- Put bending stress across scribe line
- Stress concentration along line creates clean "cleave"

New twist with CNM is to make the "scribe" part of the wafer processing

- 2019: Aligned cleaving path with crystal lattice
  - ➡ poor results: cleave initiated at one end doesn't follow lattice
- 2021: Removed top oxide layer from cleaving path
  - ➡ perfect cleaving w/ side effect - lack of oxide left line of Al metallization in path, compromising HV breakdown and reducing radiation tolerance
- 2023: Mask cleaving line to eliminate metallization in cleaving path
  - ➡ First wafers cleaved appear similar to 2019 sensors!

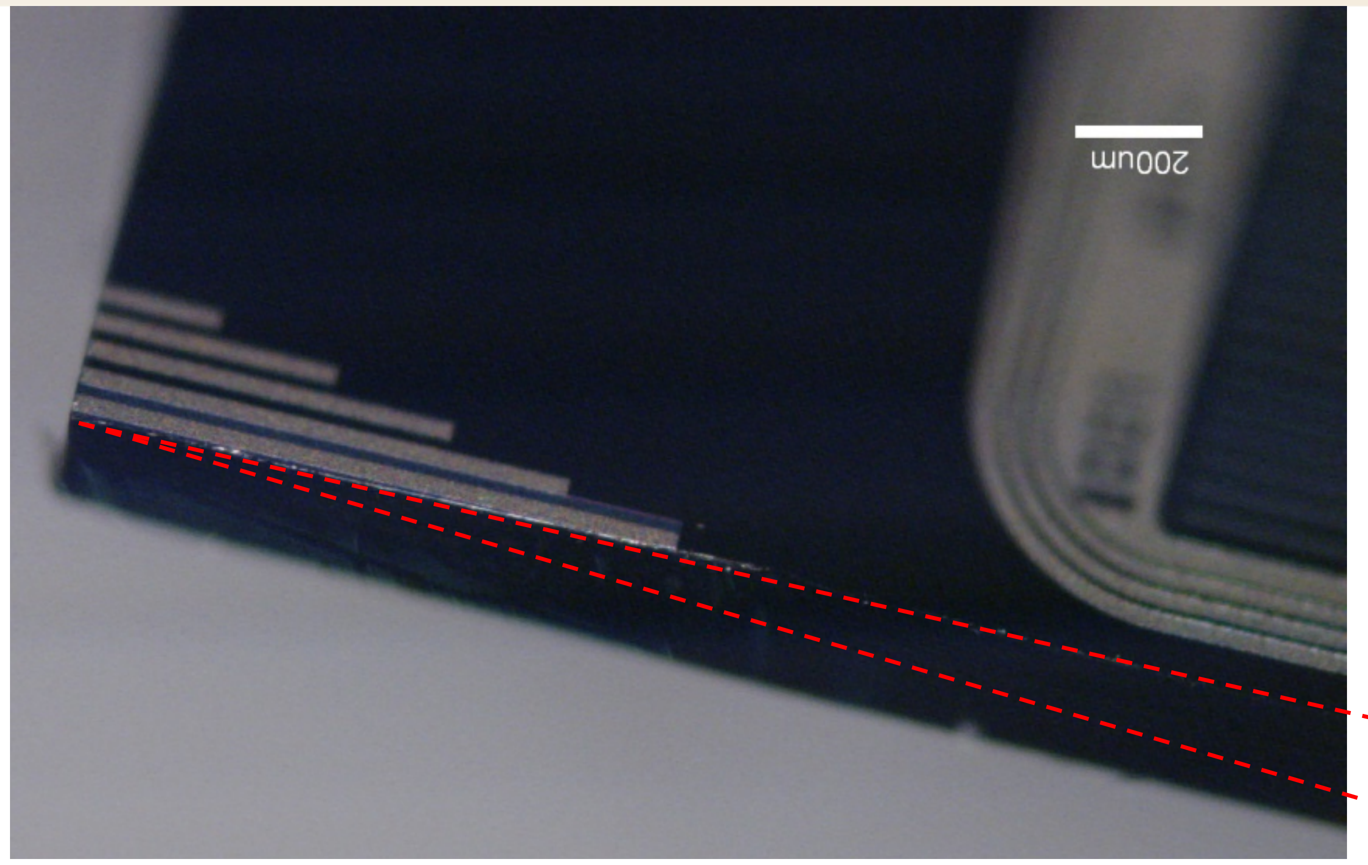
Have taken time to go slowly and figure this out.



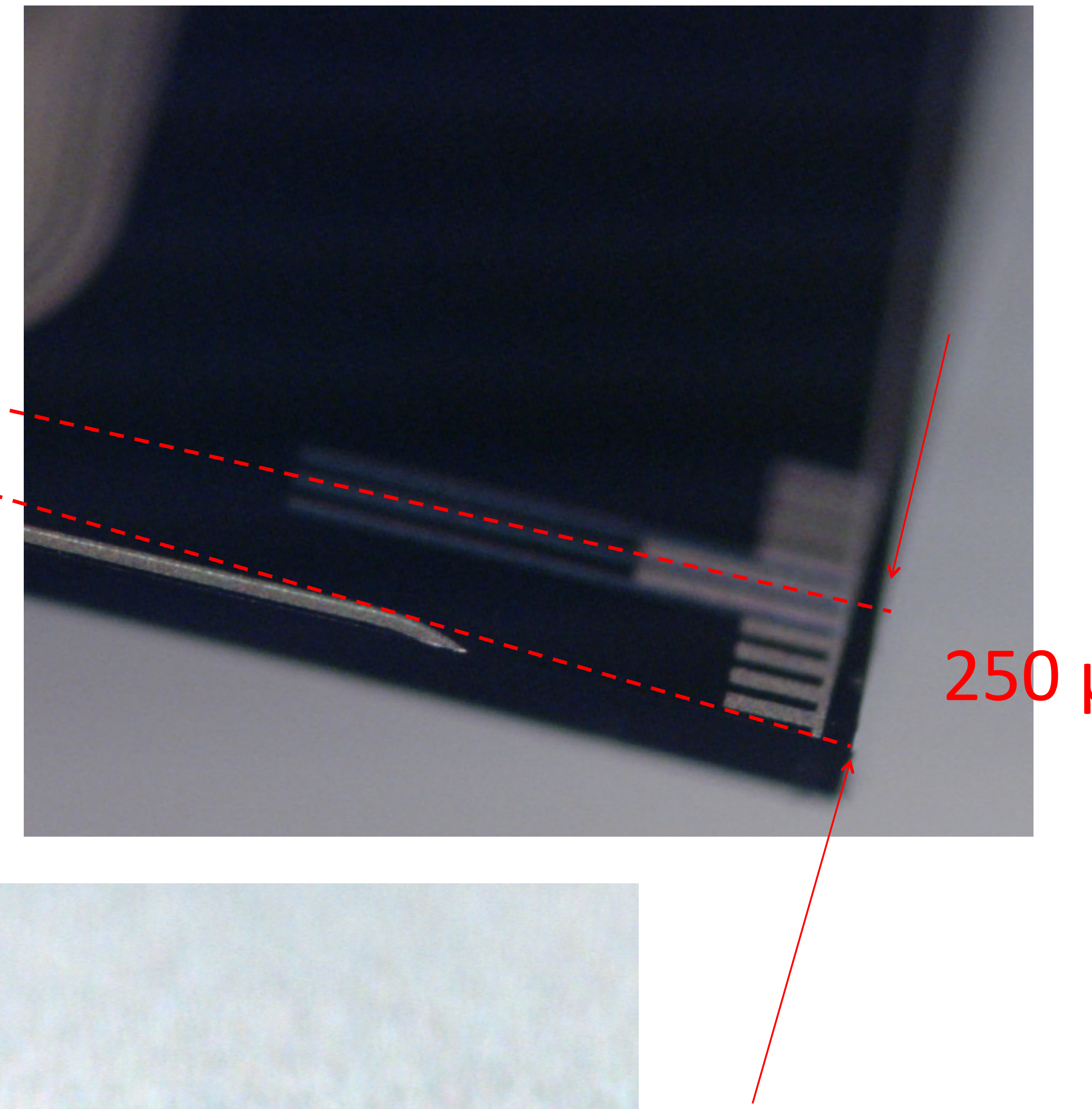


2019 Slim-edge Sensors

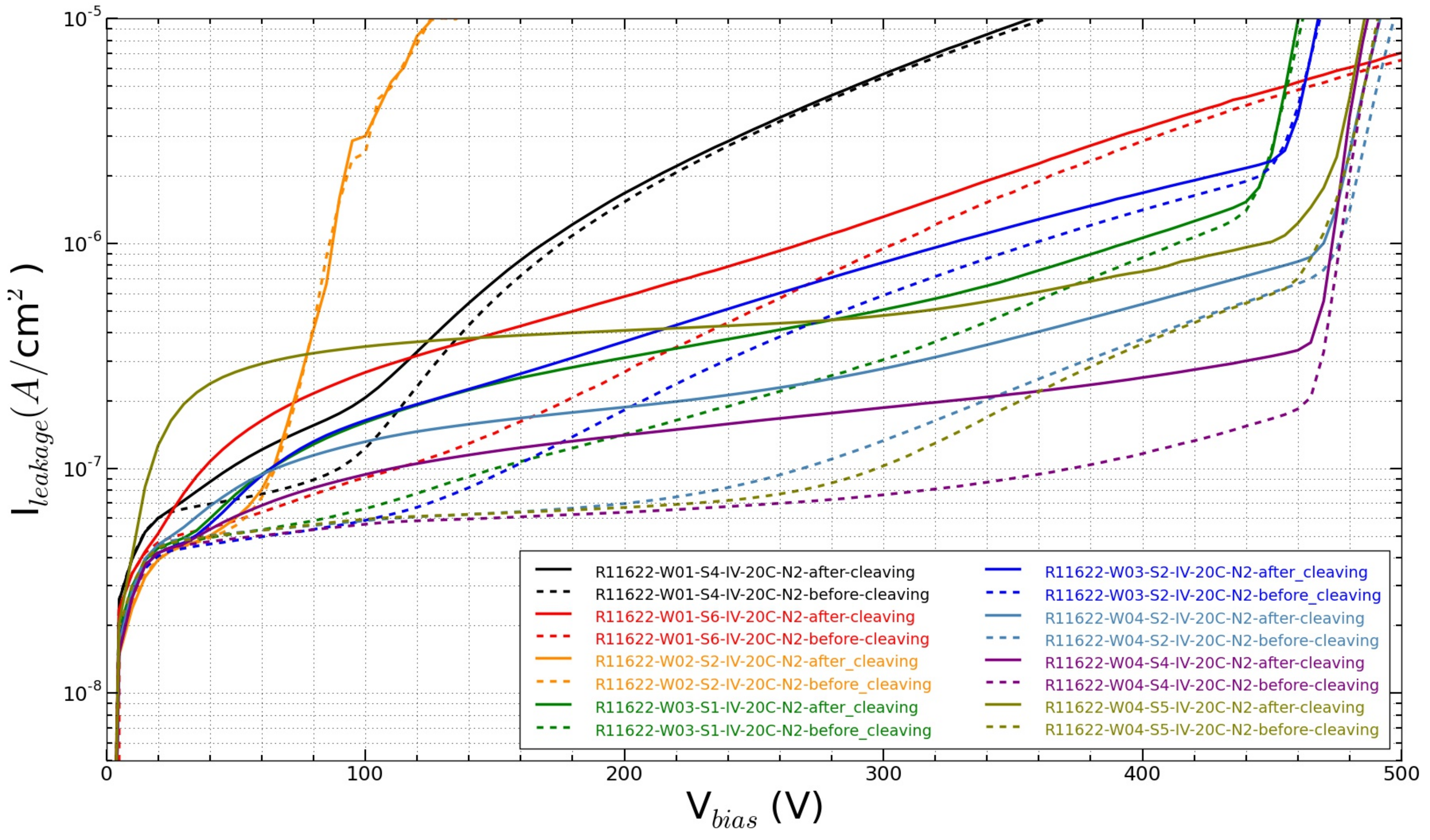
- Inconsistent cleaving
- Good breakdown characteristics

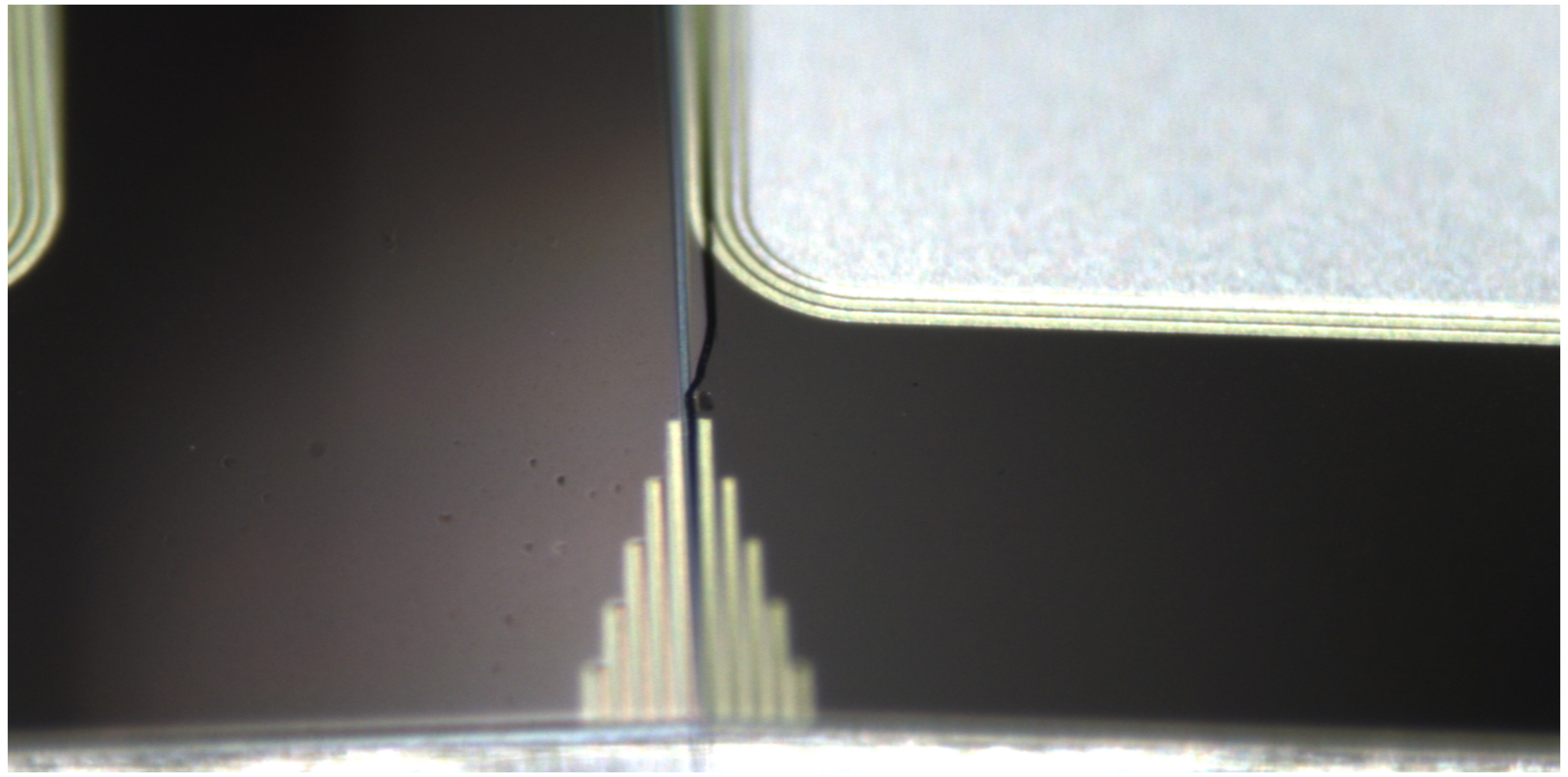


SECOND CLEAVING
Deviation of -250 µm over 33500 µm: -0,43 degrees



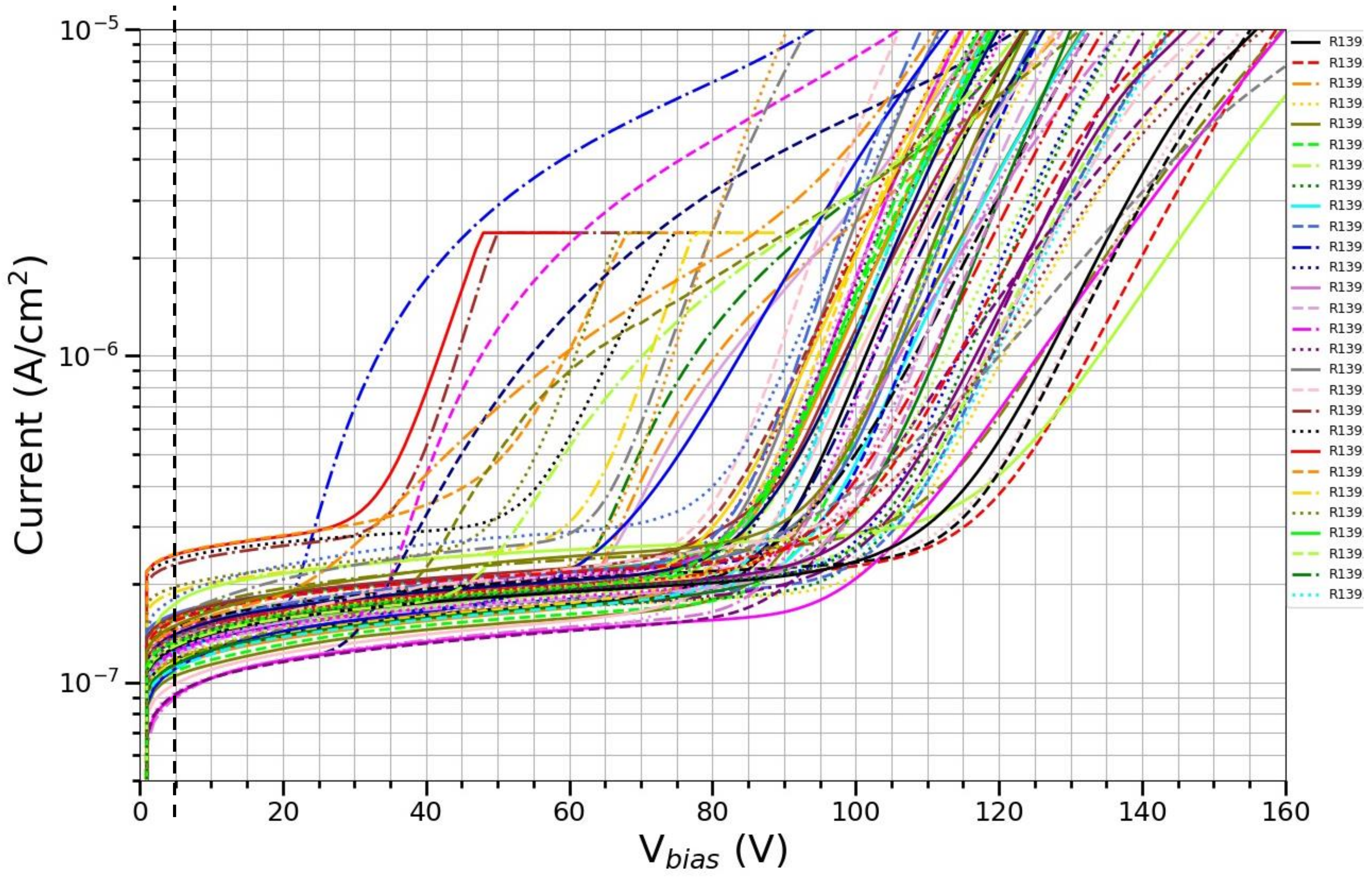
IV- characteristic before and after cleaving

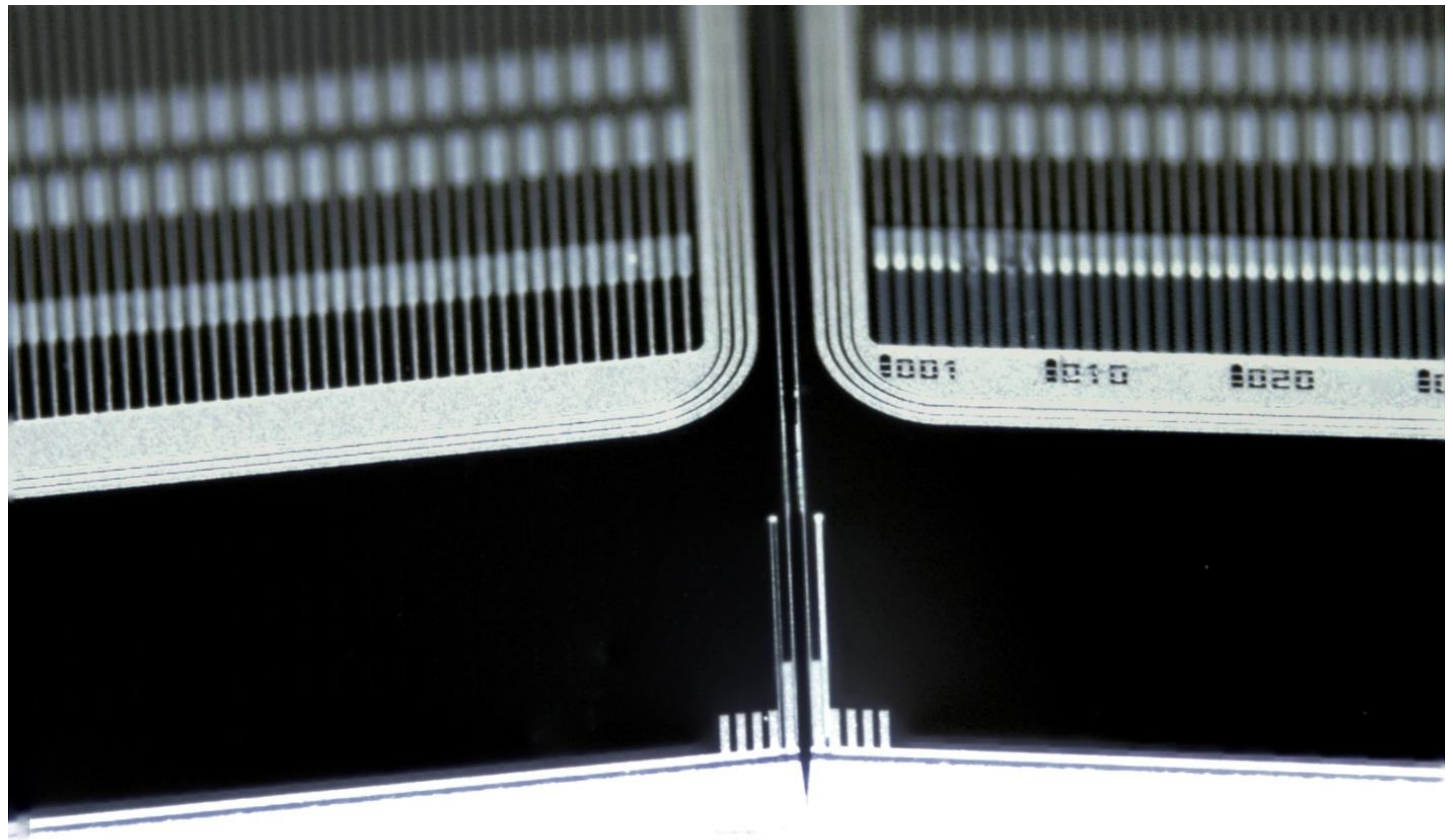


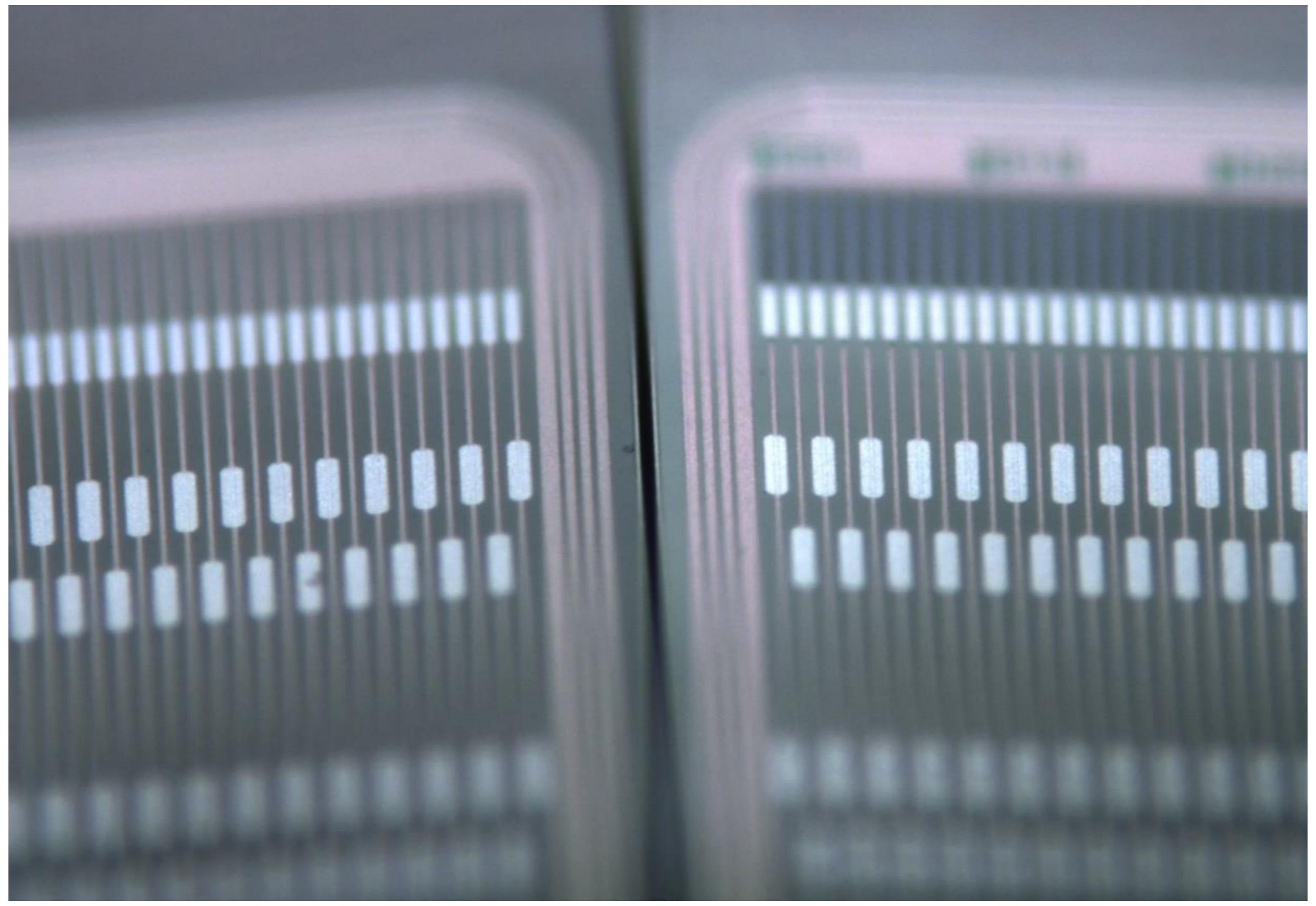


2021 Slim Edge Sensors

- Good cleaving
- Poor breakdown characteristics due to metal contact at edge



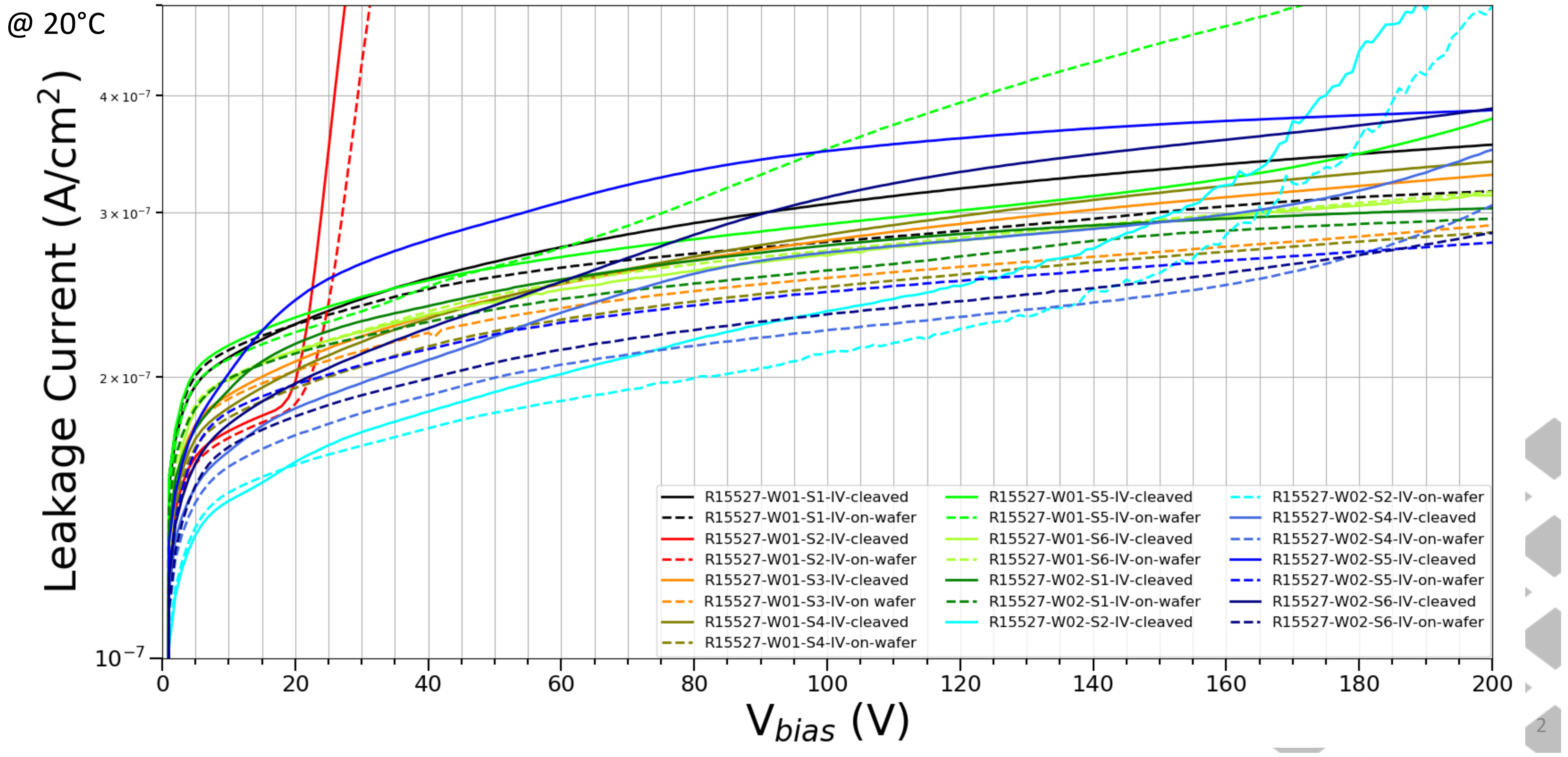


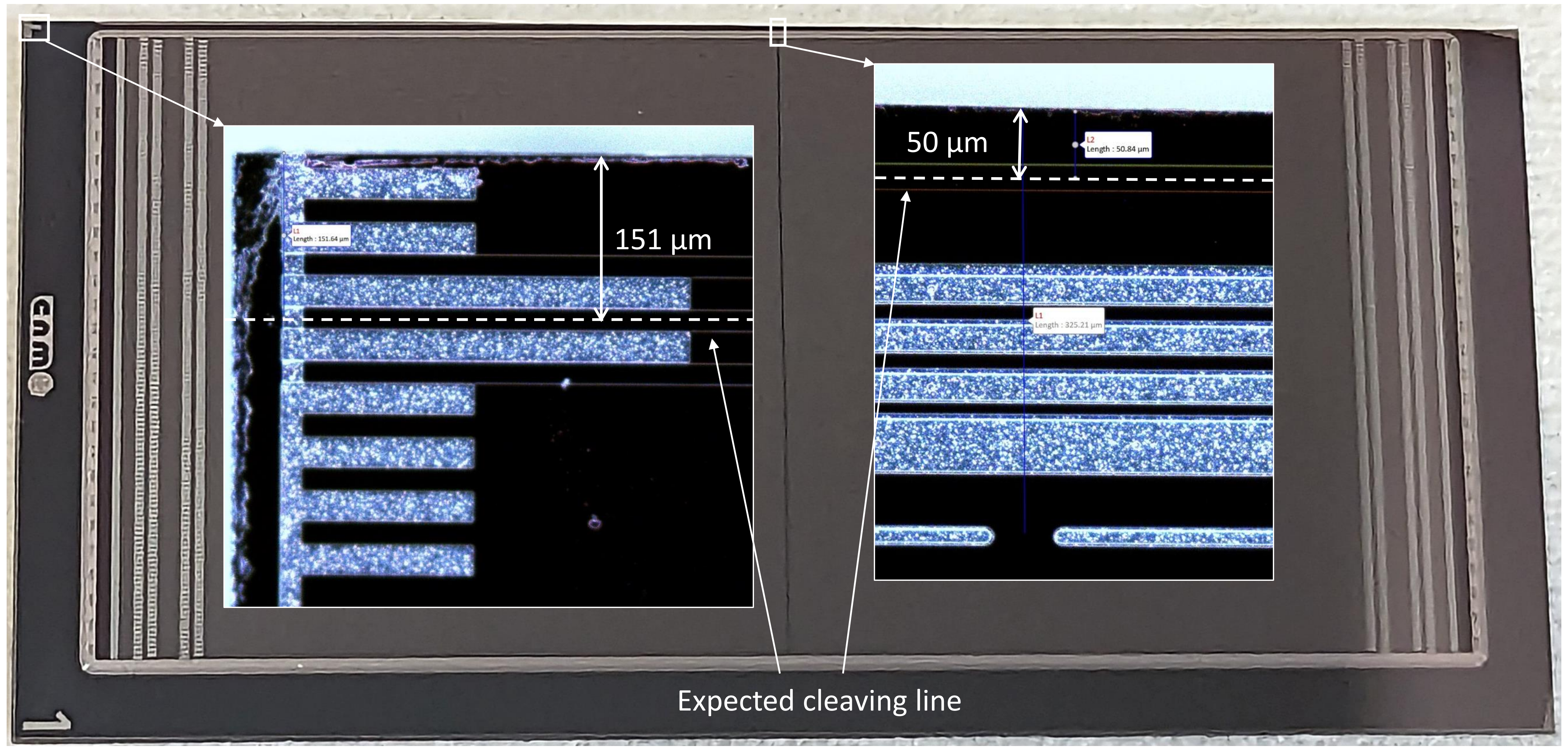


2023 Slim Edge Sensors

- Inconsistent cleaving
- Good breakdown characteristics

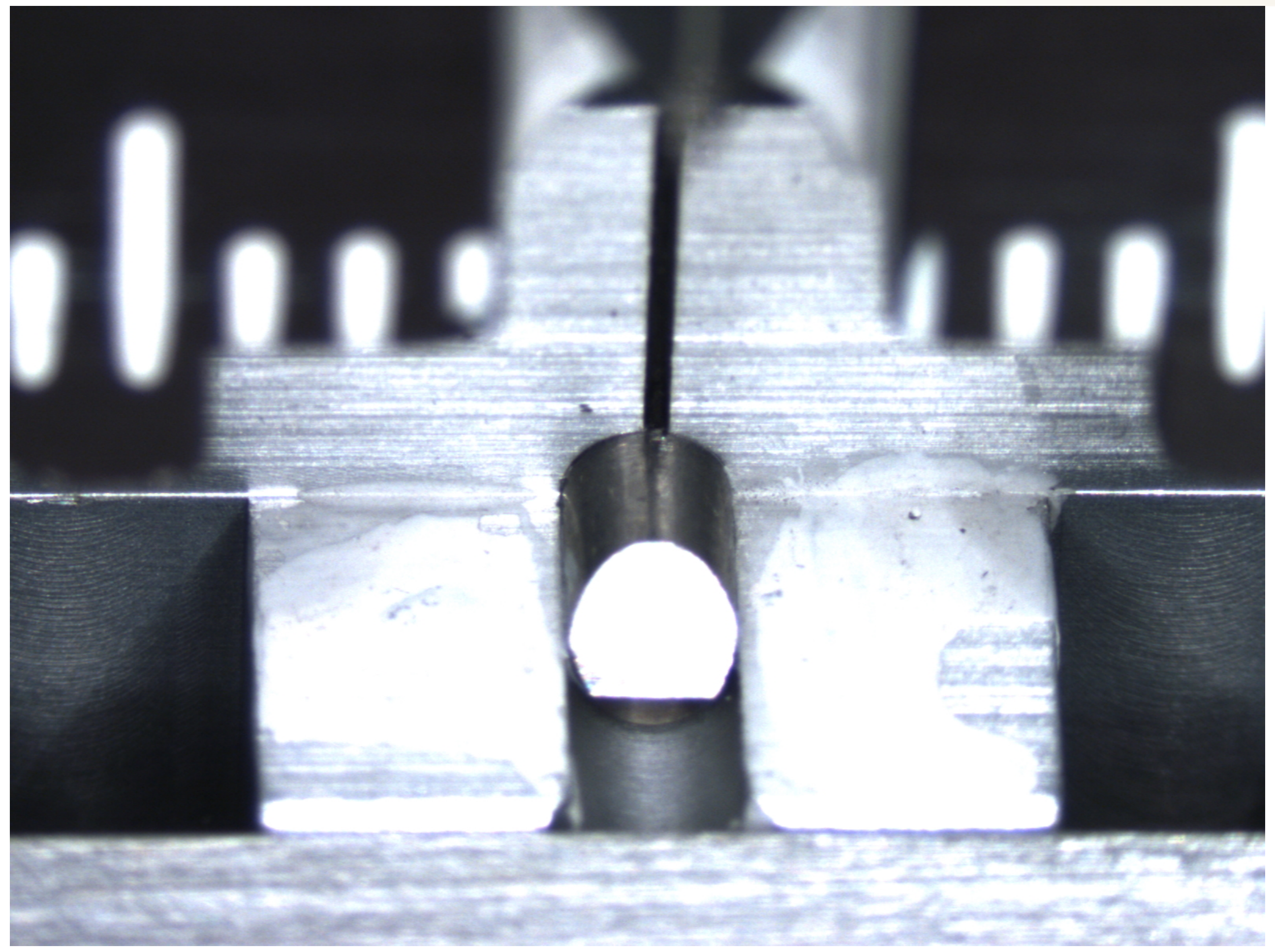
The leakage current measured after dicing and cleaving matches the leakage current measured on wafer: the cleaved edge is clean and smooth.

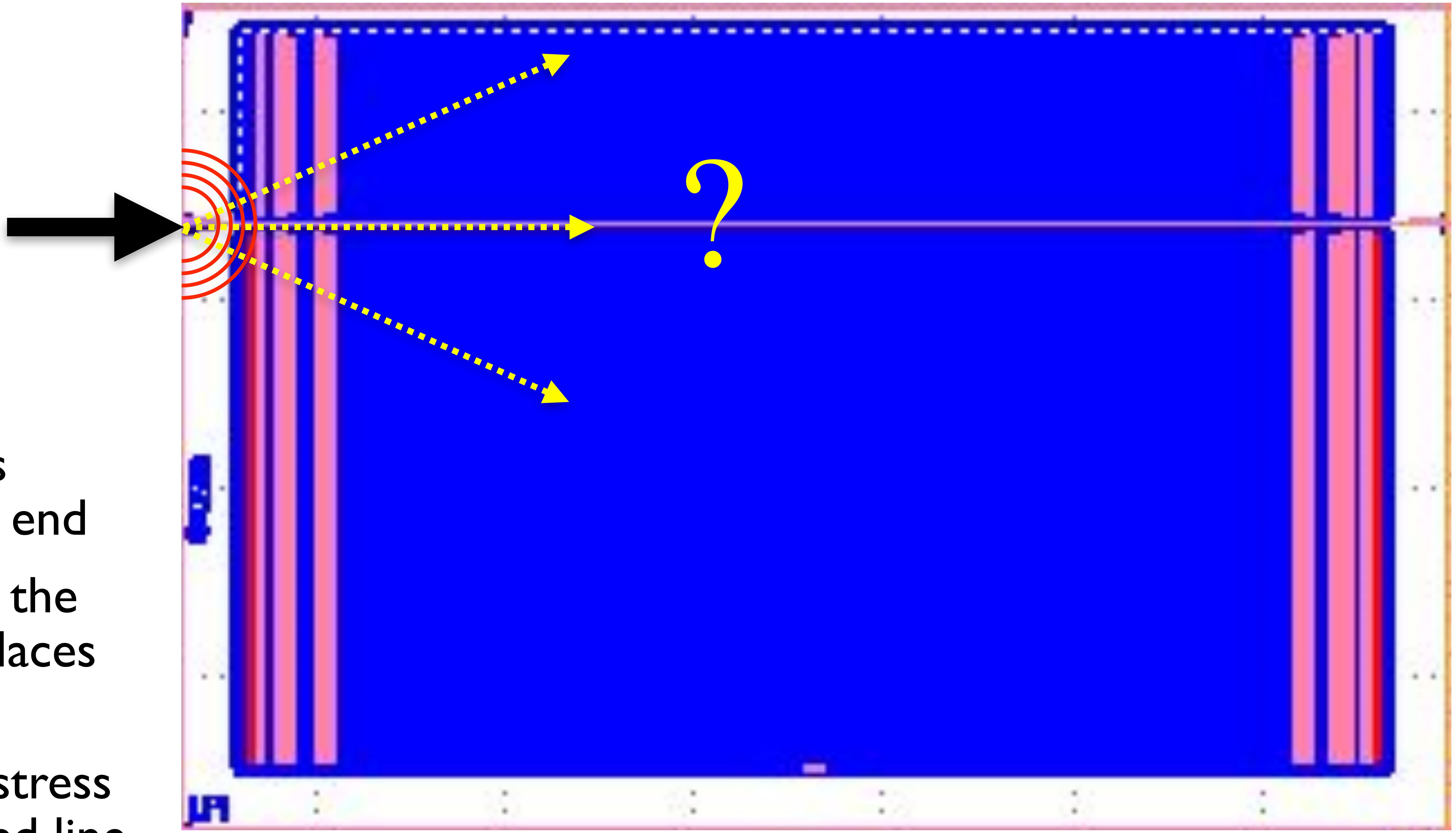




Sensor	Distance between the cleaved edge and the expected path (middle) (µm)	Deviation (degree)	Distance between the cleaved edge and the expected path (end) (µm)	Deviation (degree)
W01-S1	50	0,17	151	0,26
W01-S2	163	0,56	227	0,39
W01-S3	57	0,19	155	0,26
W01-S4	59	0,20	151	0,26
W01-S5	138	0,47	229	0,39
W01-S6	170	0,58	237	0,40
W02-S1	80	0,27	186	0,32
W02-S2	163	0,56	235	0,40
W02-S4	171	0,58	226	0,39
W02-S5	52	0,18	149	0,25
W02-S6	169	0,58	236	0,40

What are we missing?





The "cleave" of the silicon sensor is initiated with bending stress at one end

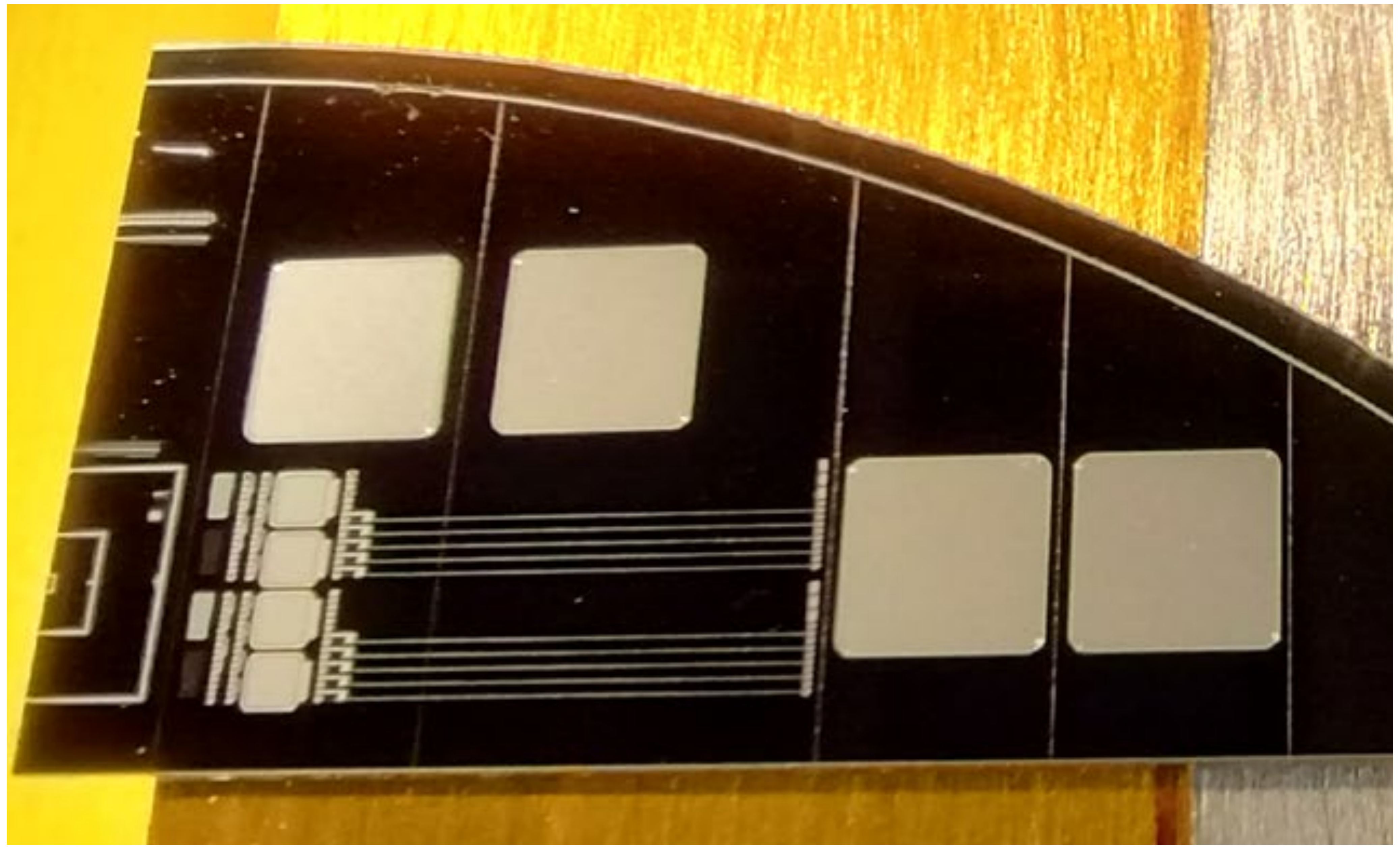
When snapping material like this in the shop – a common practice – one places stress along the entire scoring line.

Perhaps we need to place bending stress along the entire length of the scribed line

A (small scale) commercial process we have identified works this way. It's not clear we have a way to access equipment used in this process.

Recent Progress

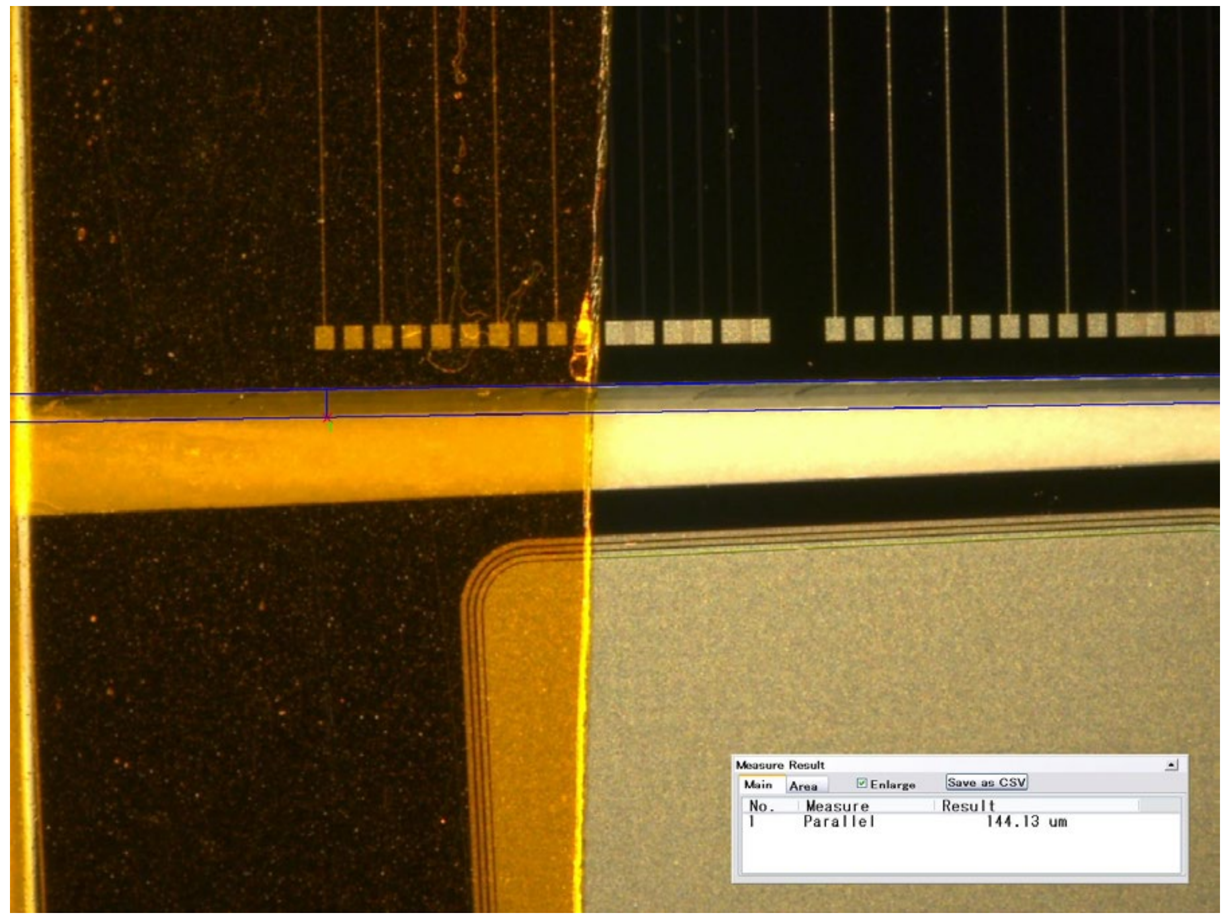
Scribed samples sent to UCSC for trials



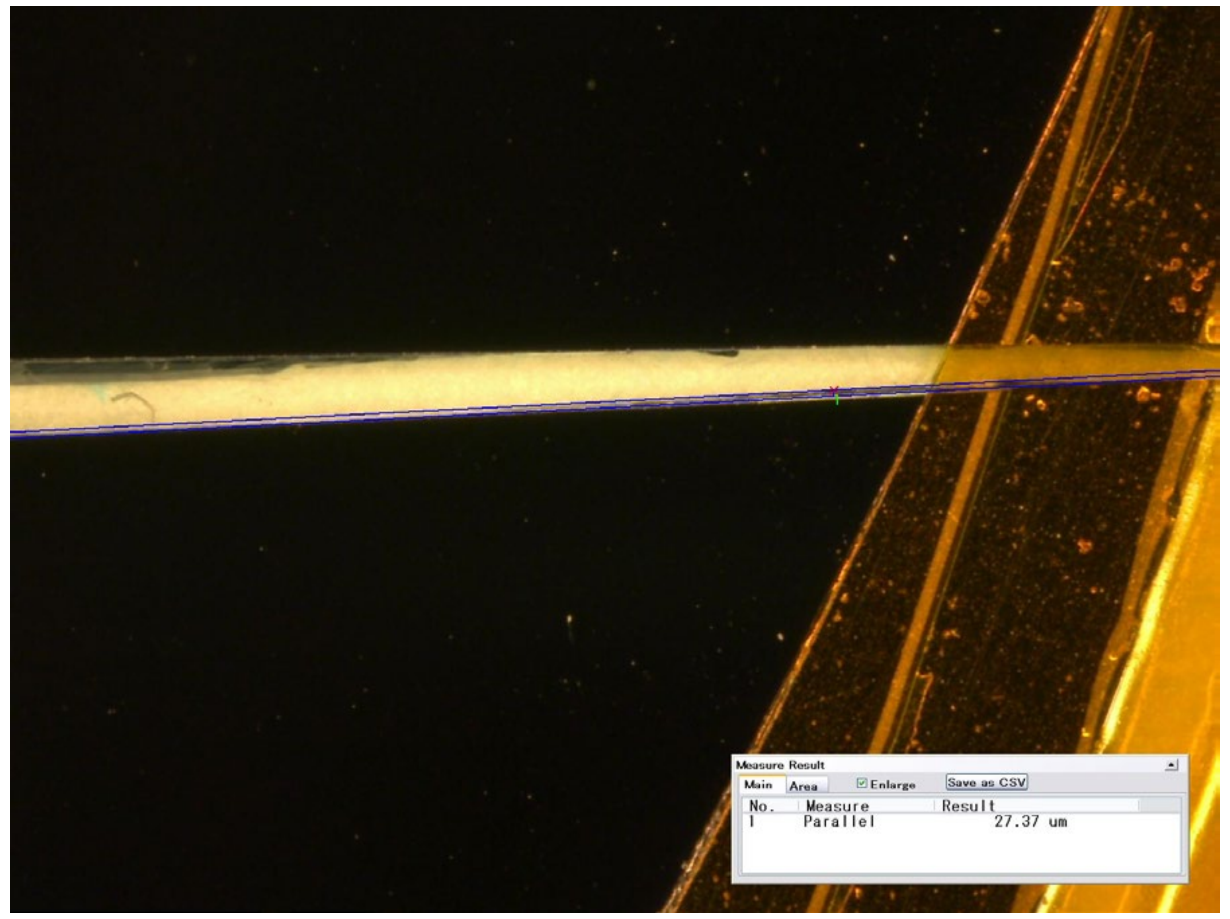
Better: deviations from cleaving path are small but side wall is often not perpendicular to sensor surface.

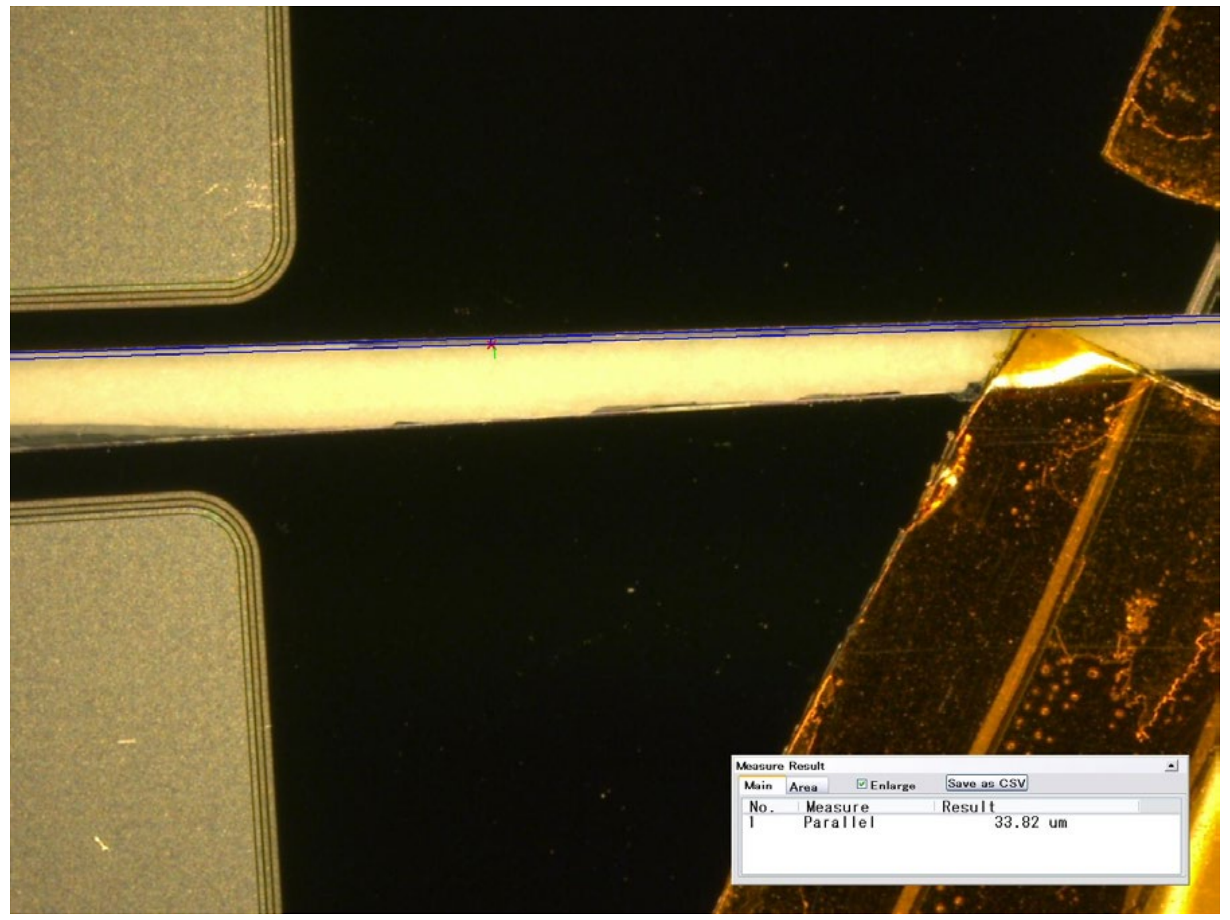
Second quality sensors being sent to Vitaliy for more realistic tests.

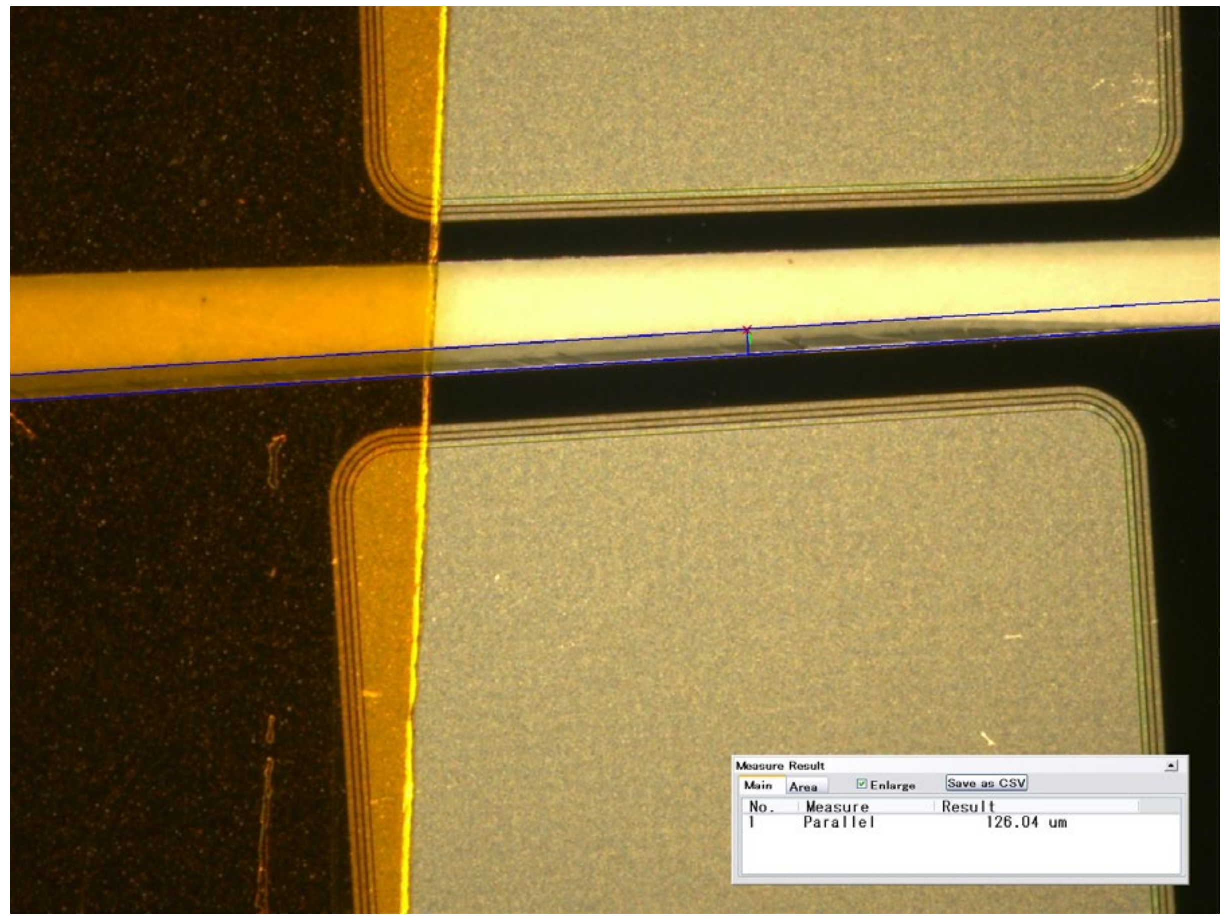
Bottom excess



Bottom deficit







Recent Progress

Scribed samples sent to UCSC for trials

Sample	Top line deviation	Bottom excess	Bottom deficit	Comment 1	Comment 2
	[um]	[um]	[um]		
1a	56	113	137	top deviation is **2 wiggles** of 500 um long	A crack line, 1090 um long, 194 um inward
1b	34	50	N/A	top devi is **1 wiggle**, of 300 um long	bot excess is small
2a	43	163	137	top deviation is **small angle**, likely due to wafer edge	
2b	~5	50	135		
3a	~0	128	32		
3b	120	-	138	top deviation is "offset" for a portion	
3c	~0	144	27		
3d	~0	34	126		
3e	~0	50	124		

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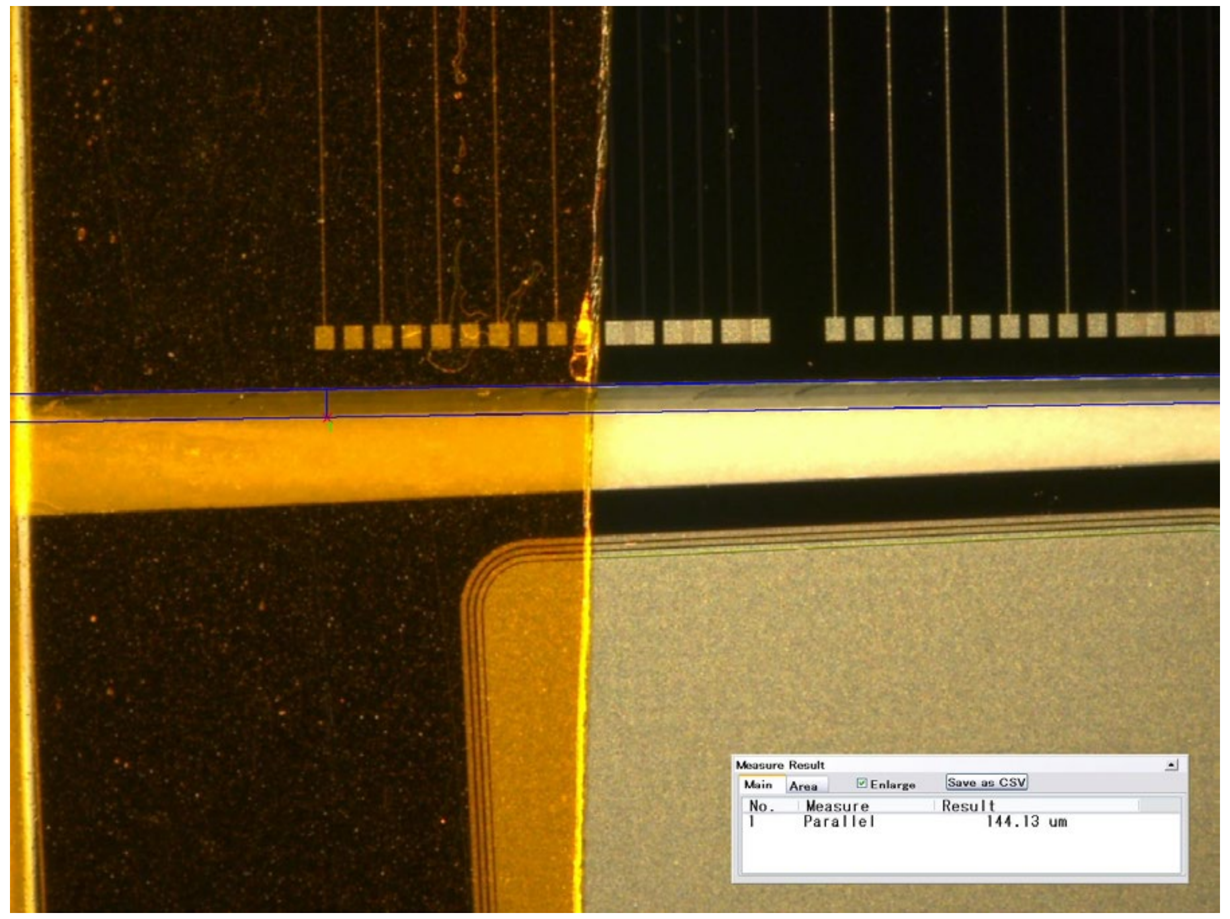
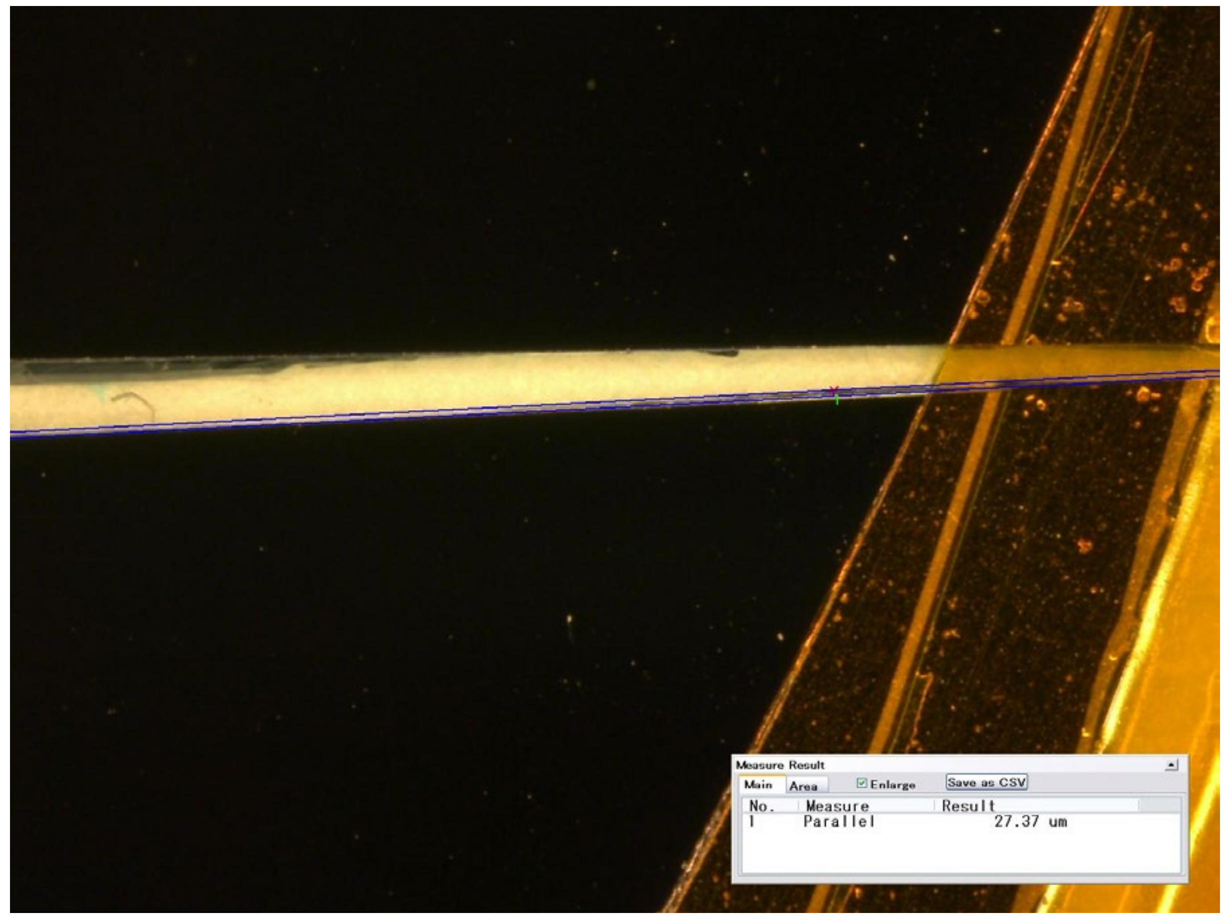
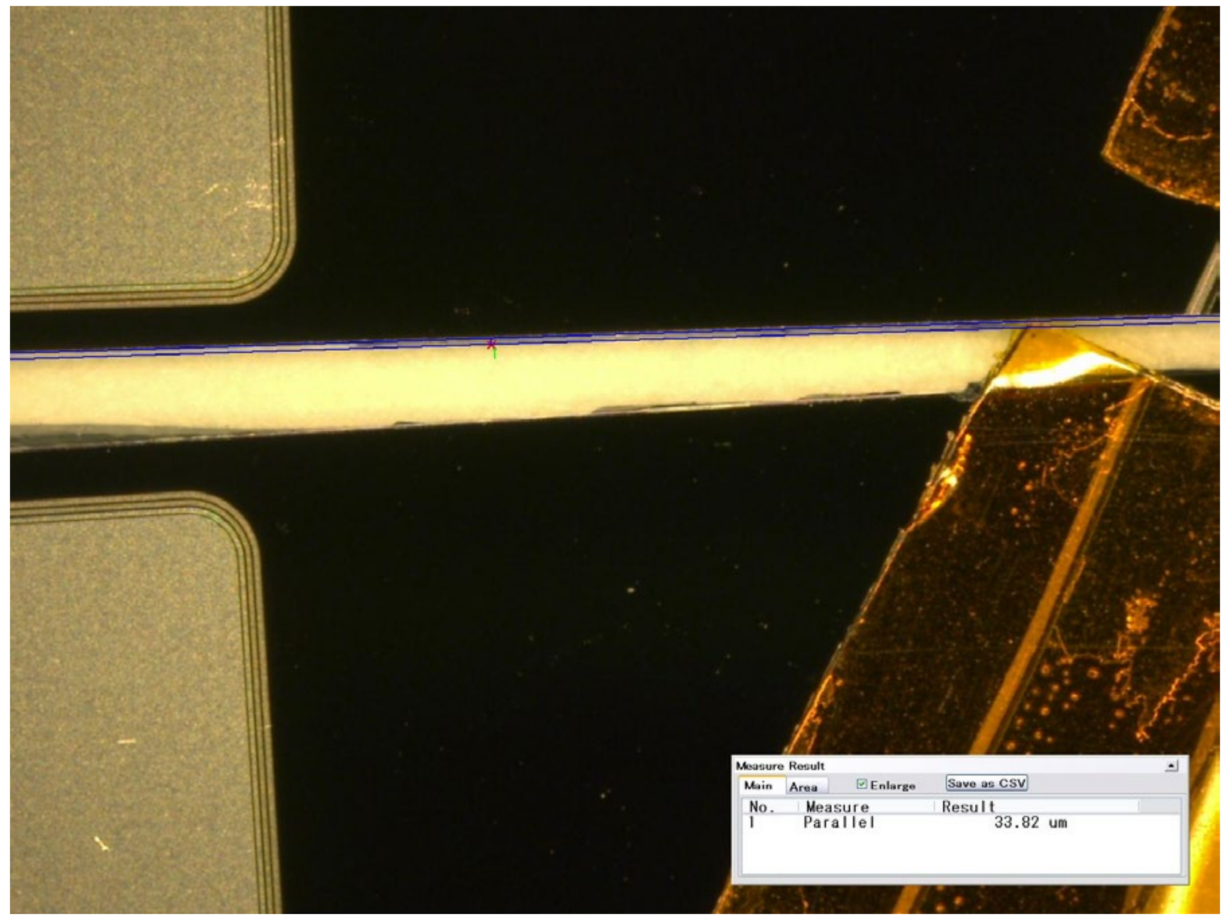
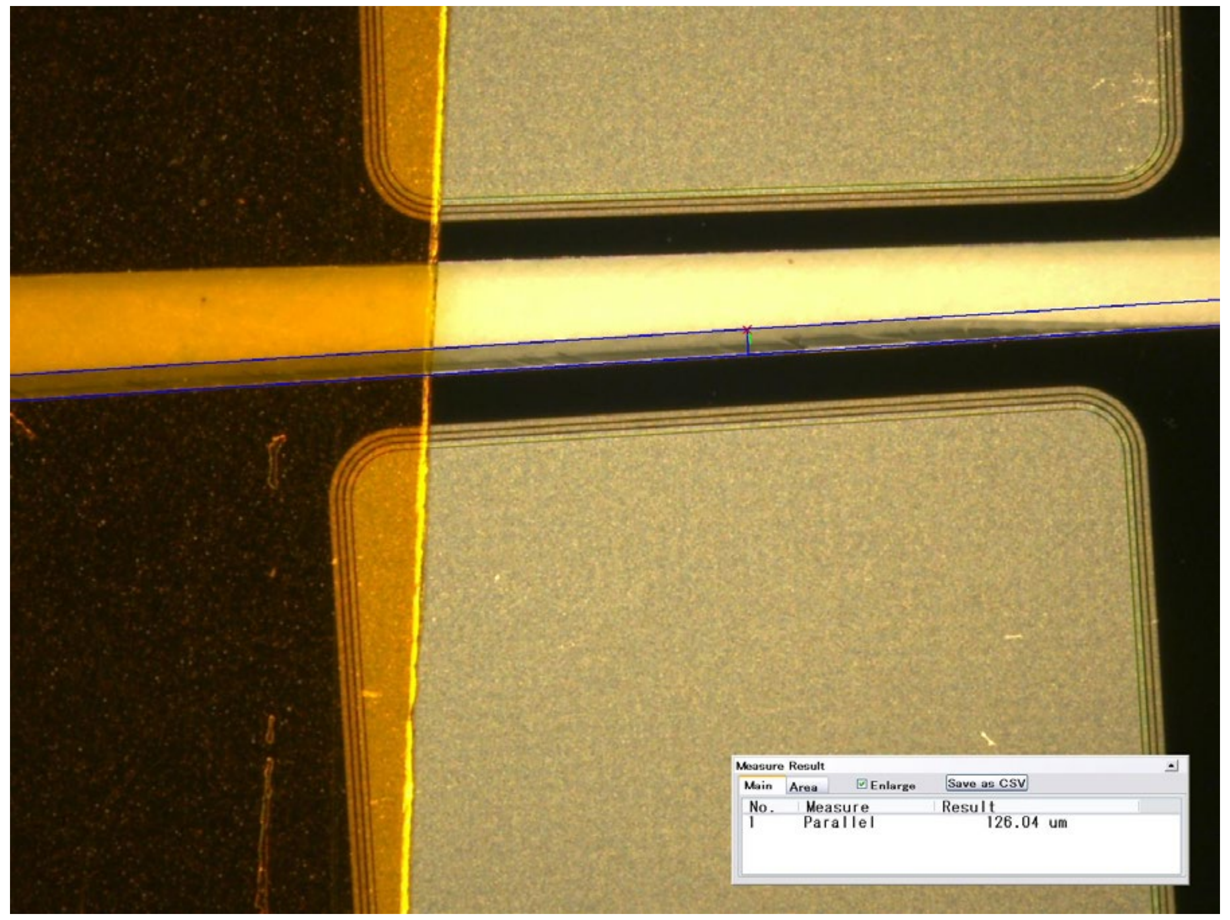
Bottom deficit









SVT L5-7 Modules

Long modules used in L5-7 were anticipated to be a low-risk item

- Built with knowledge and experience from test-run modules
- Far from target and beam plane, low radiation and risk of beam accidents
- 20 half-modules built (18 good), 12 needed for the detector

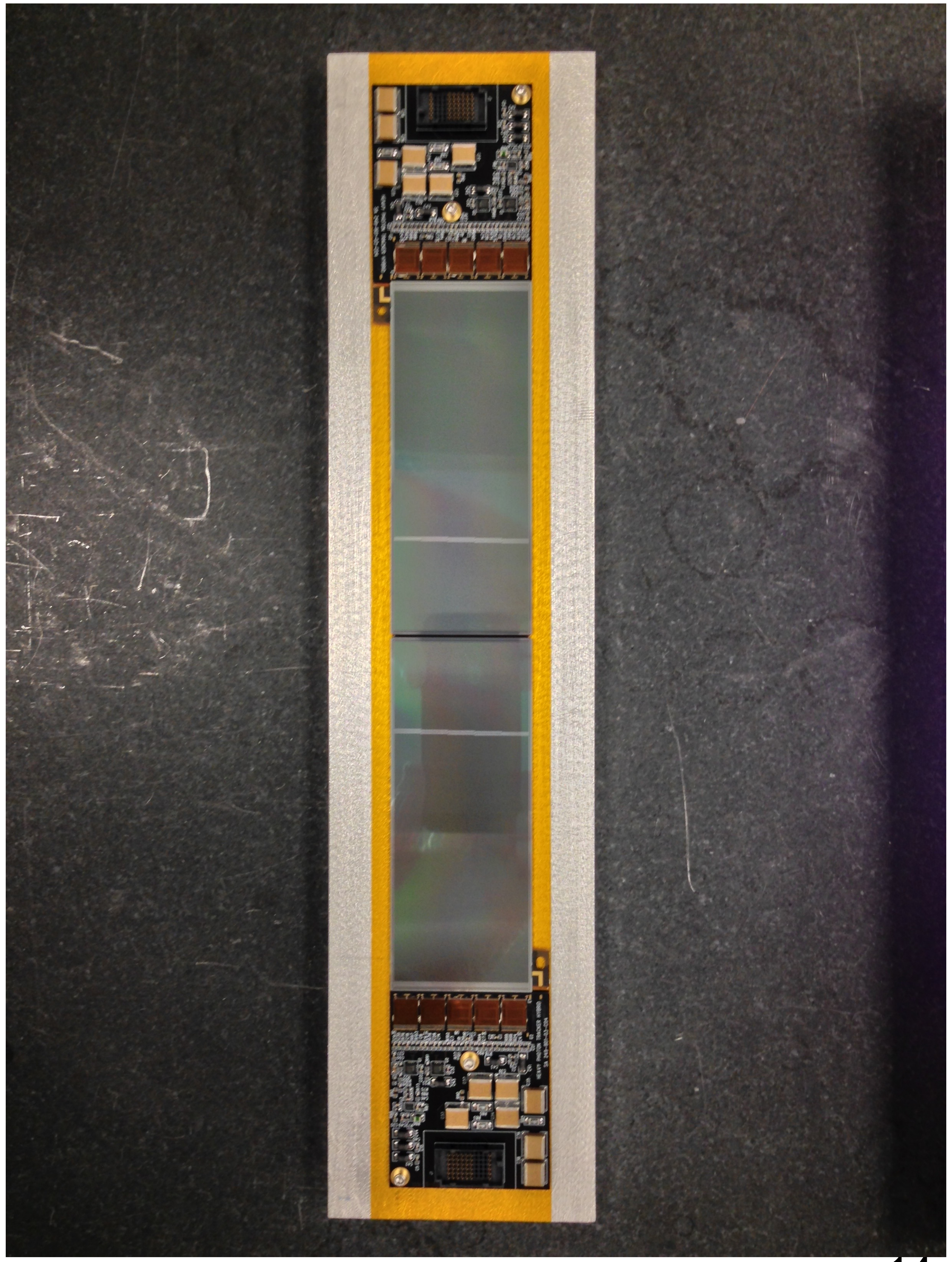
Instead, these modules have suffered mysterious problems during non-operational periods

- over time, wirebond damage to half-modules facing downstream (now also seen in short modules in L2-3)
- in 2021 partial shorts between some power rails and ground: investigation by Sarah/Cam ⇒ likely ESD damage

There are no more spares

Plan: build as many additional half-modules as we can

Would like to synchronize assembly and wirebonding work at UCSC with L1-2 modules.



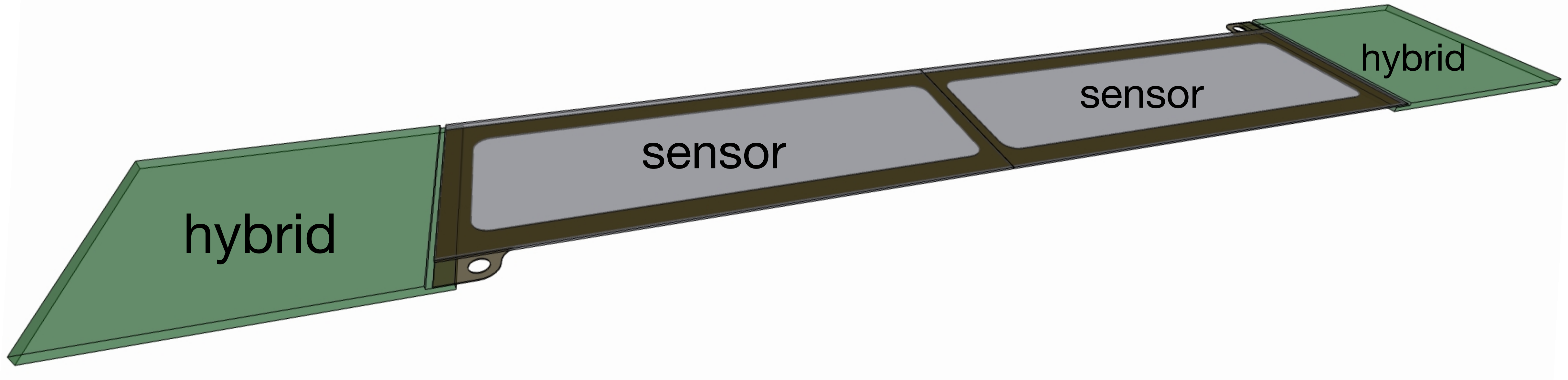
SVT: L5-7 Module Replacement

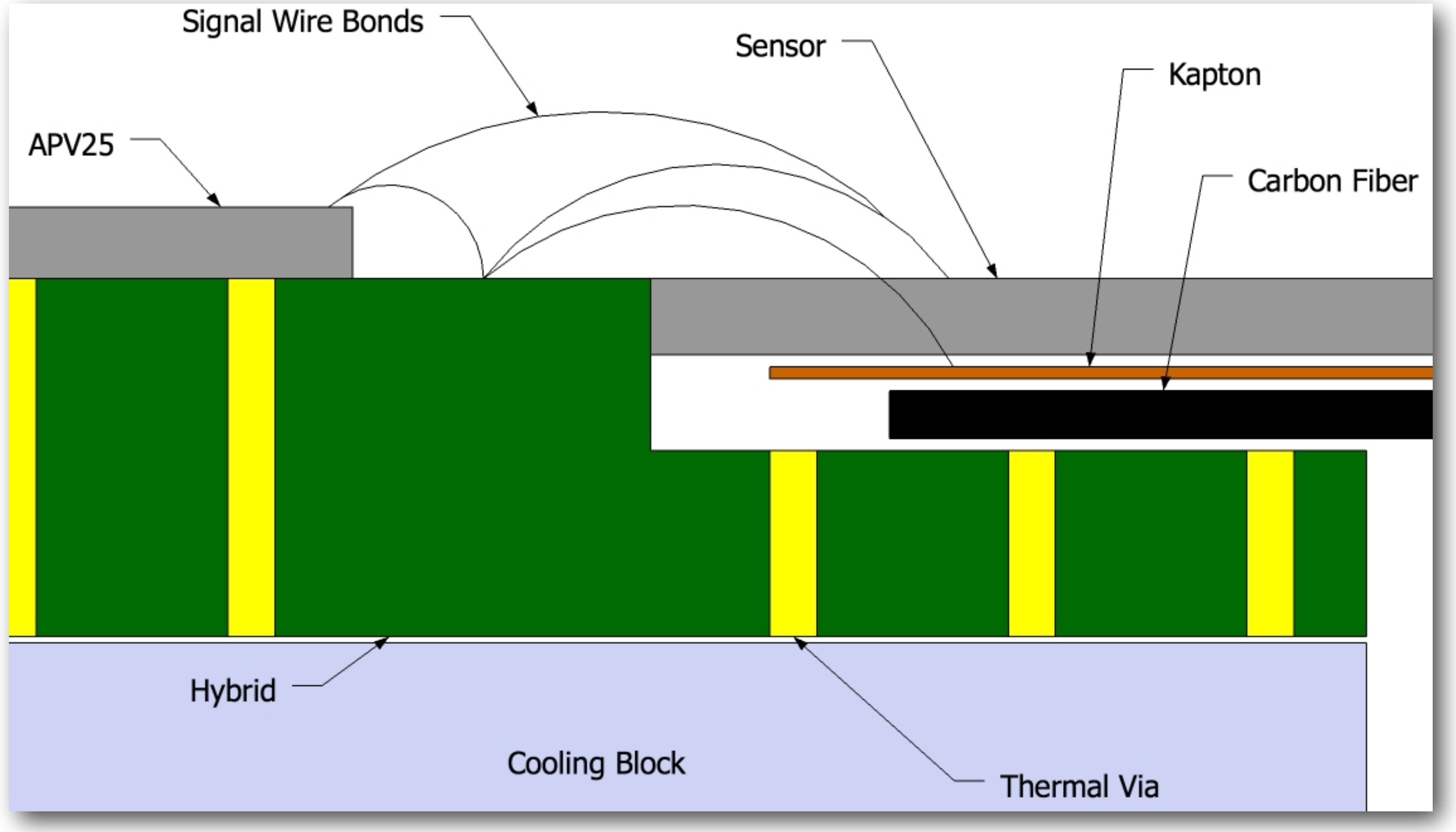
Status:

- APV25: chips in hand at UCSC. Will require use of some second-quality chips (most are ~100% functional, only mechanically imperfect)
- Hybrids: Delivered to SLAC, ready to assemble
- Sensors: Have some at SLAC. FNAL still has large quantity - pending delivery.
- Kapton: no design changes: 15 day lead.
- Carbon Fiber: Have 8 on hand. This may limit how many units we can make.

Considering alternatives if we cannot get more carbon fiber.

Also considering options for more Layer 3/4 modules in case testing shows new issues.





SVT FEBs

SLAC

After radiation damage to FEB5V regulator during 2019 run, we undertook a redesign for 2021

- 20 new FEBs were built (10 needed) with more radiation tolerant regulator and better board material
- Components discontinued since first run of boards required significant changes to the design
- One of these changes exposed a latent error in the original design in the specification of a *different* regulator
- This error caused damage to the new boards when first powered: several boards were lost to this. 12 good.
- We had no choice but to (slightly) overdrive these regulators on the remaining boards, but no failures.

Plan: Correct design error and order more FEBs

Status:

- New design uses same regulator as replacement for 5V regulator, changes to improve power-up reliability.
- 20 boards ordered and delivered.
- 2 loaded and ready for testing: on Ben's desk since late April waiting for testing effort

SVT Data Flange

SVT data flange converts FEB control+data on copper to optical connected to RCE back end.

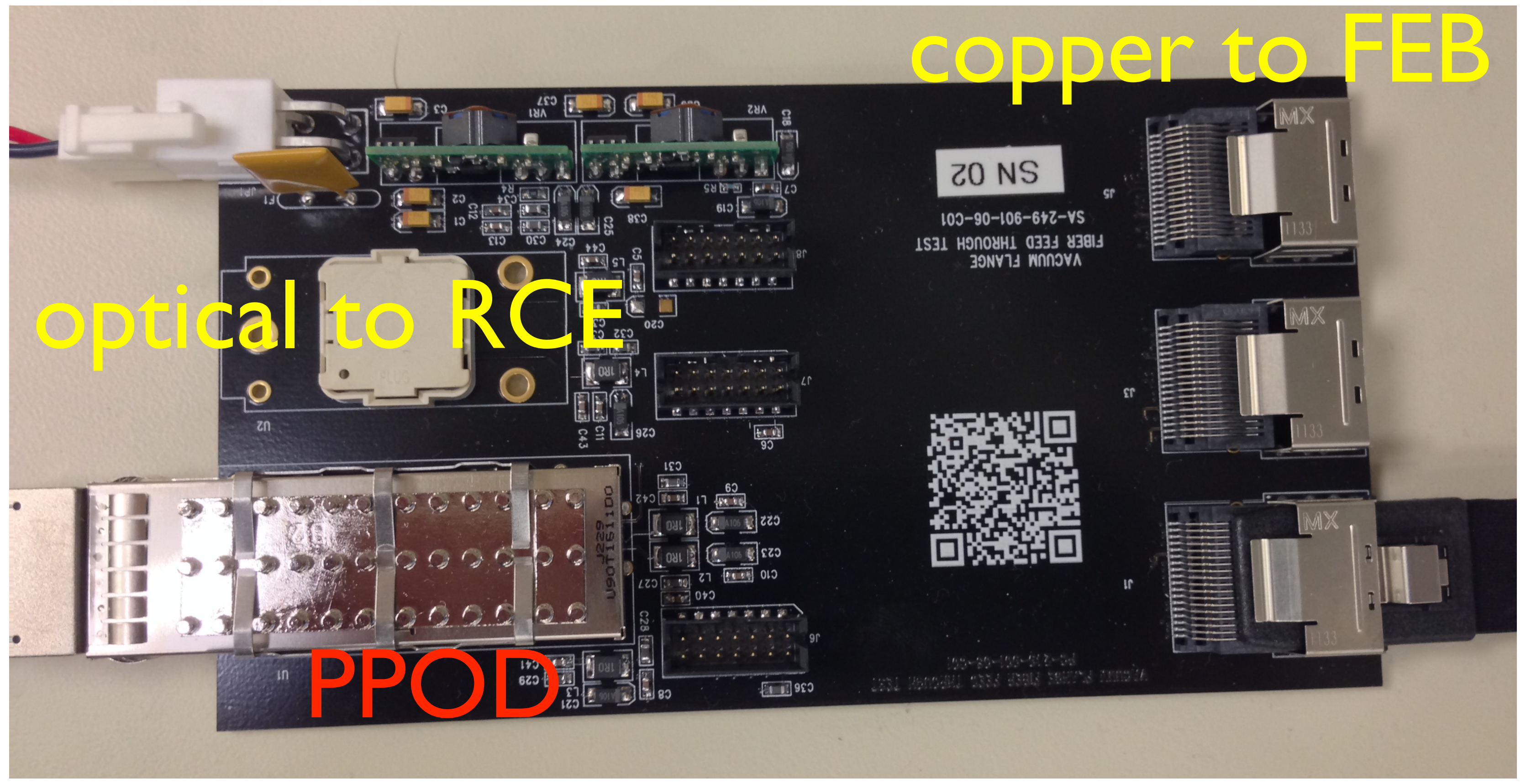
- Four boards with 3 channels each (12 links total)
- Boards are potted through 6" vacuum flange on positron side of upstream vacuum box.
- Two flanges were built: the first no longer has 10 reliably working channels. Spare was used in 2021.

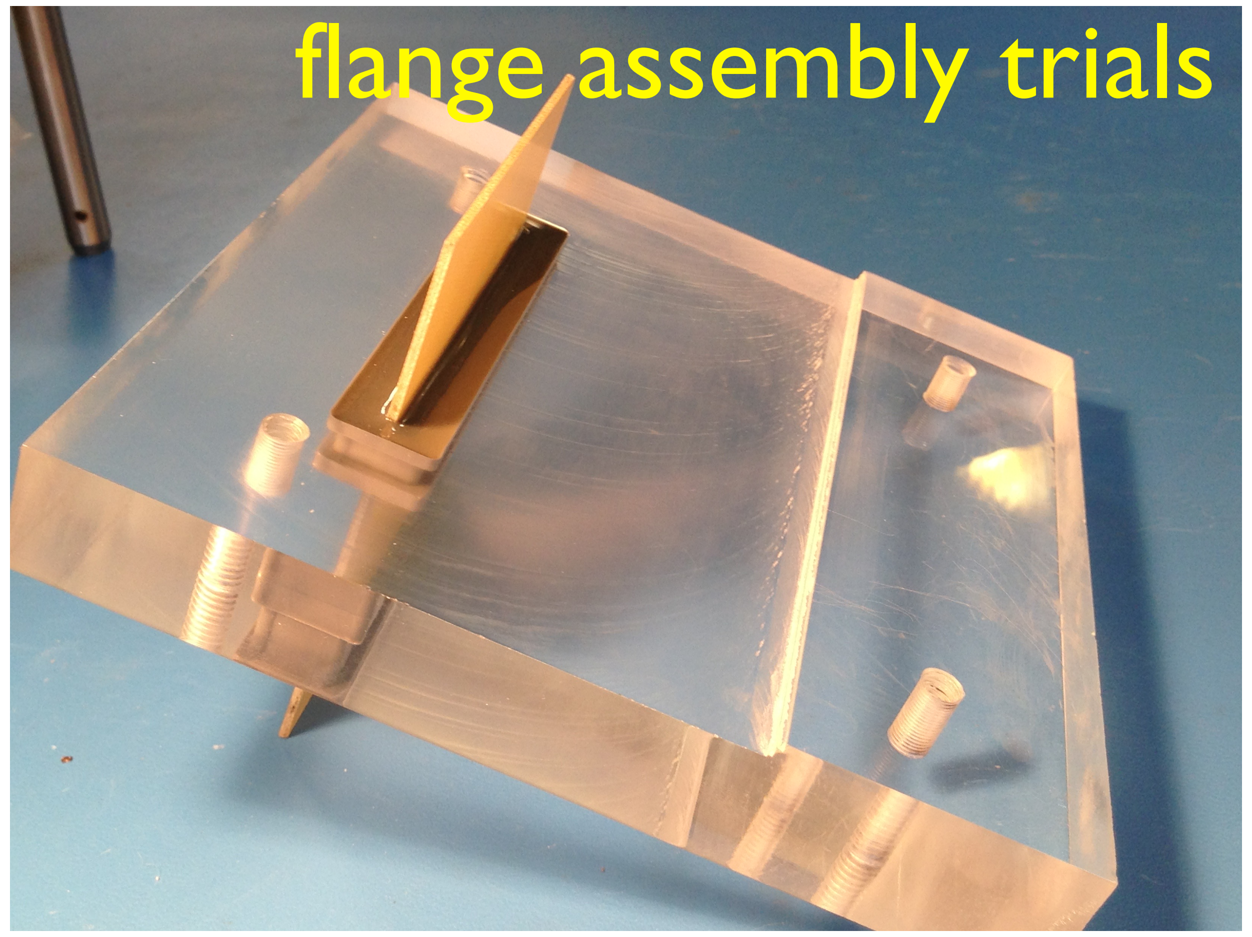
Plan: build another data flange

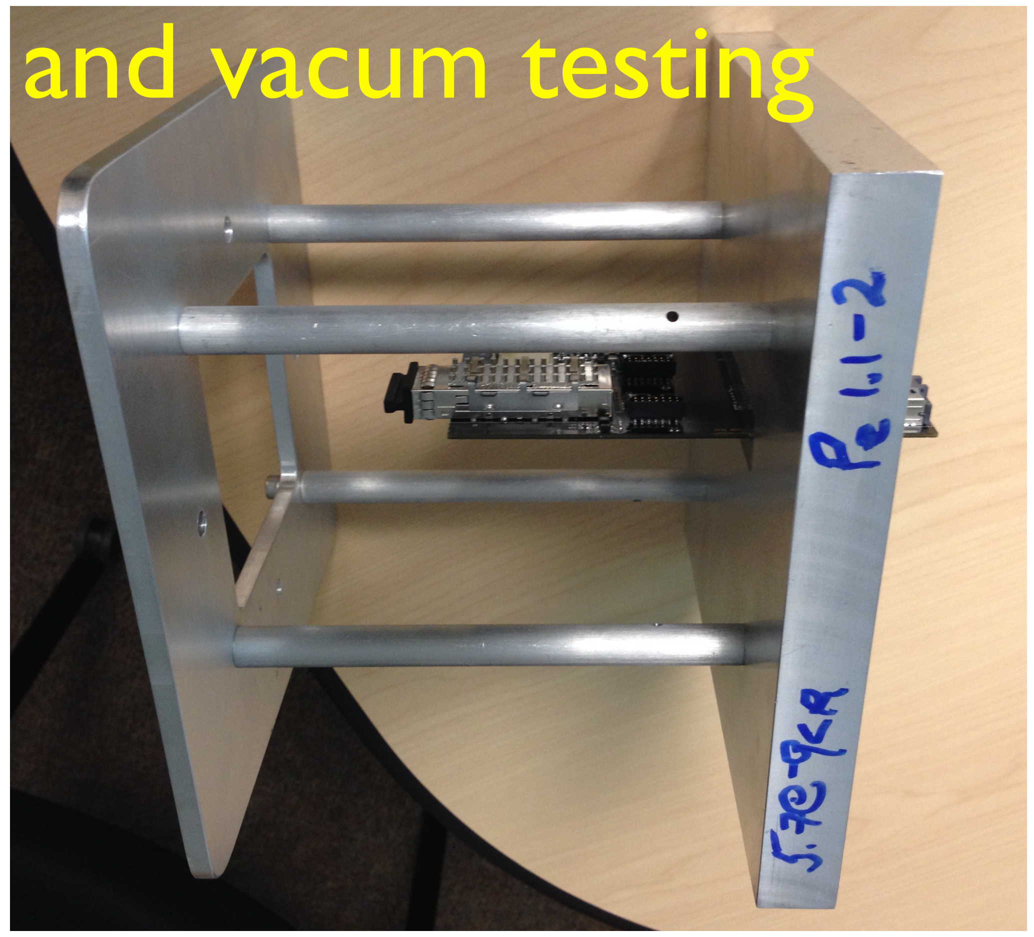
Status:

- Key component discontinued: PPOD transmitters
- Test to determine whether these can be reused
- If so, boards are easily obtained, otherwise some significant design work required.
- Matt McCulloch on board: estimates 60 hours/flange.

Will test alongside new FEBs







Work Plan for Coming Week

- Finish getting DAQ on network/working again
- Move power supplies and cables from Hall B to EEL
- Warm up SVT and set up on table
- Test full system; flanges, FEBs, modules
- Inventory and establish status of modules and shipping containers at JLab
- Return to SLAC any equipment or components that we will want to work with at SLAC