UNIVERSITY OF BIRMINGHAM | SCHOOL OF PHYSICS AND ASTRONOMY

ePIC SVT sensor development

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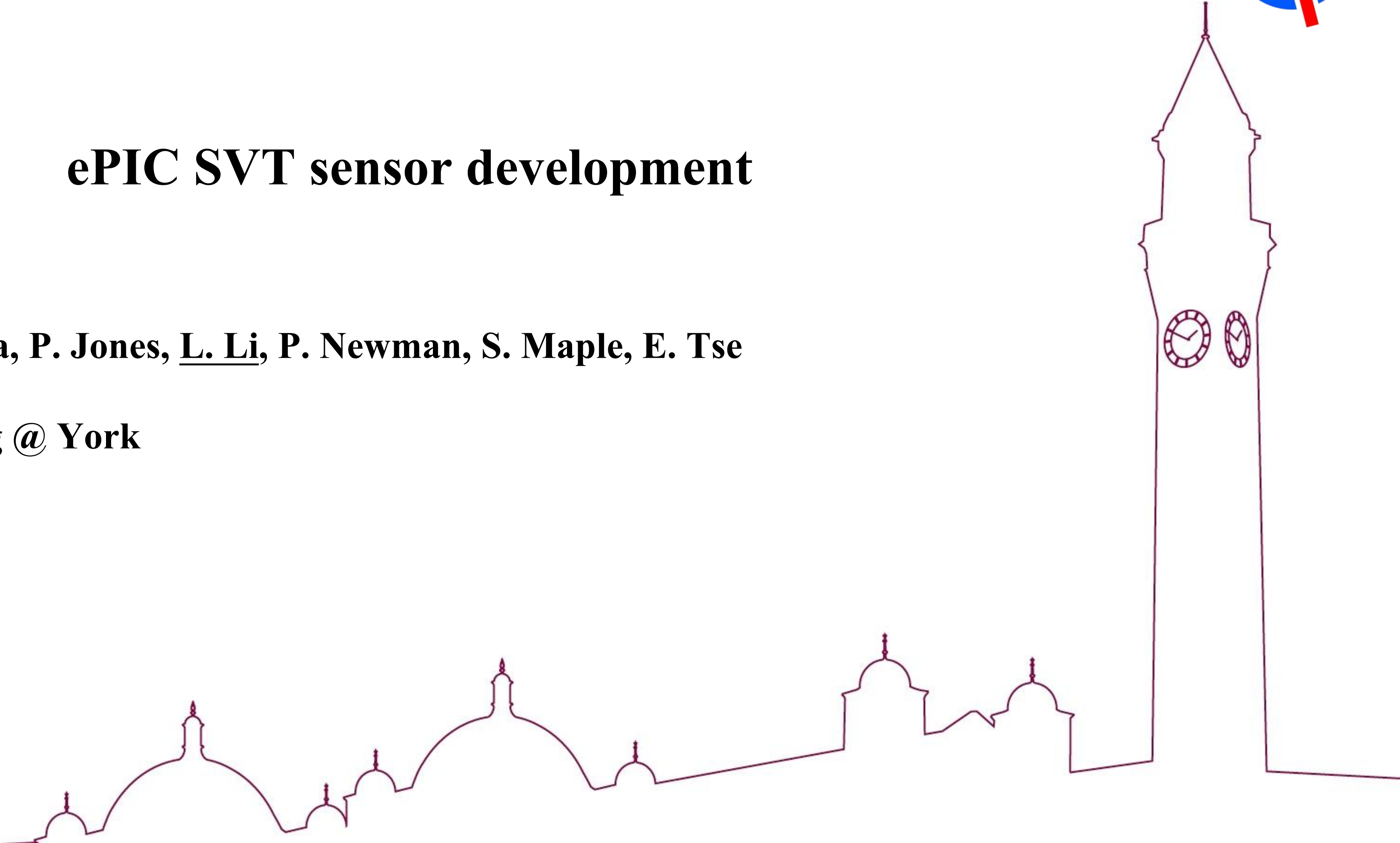
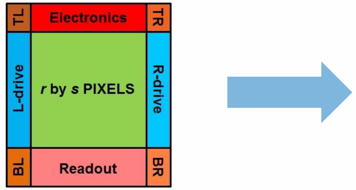
EIC-UG UK meeting @ York

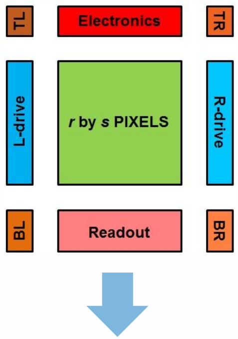
01/03/2024

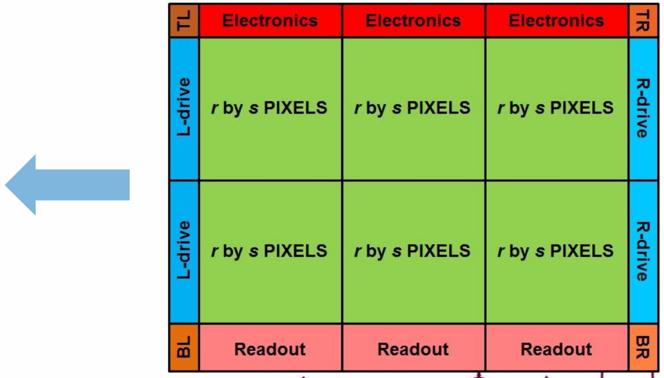


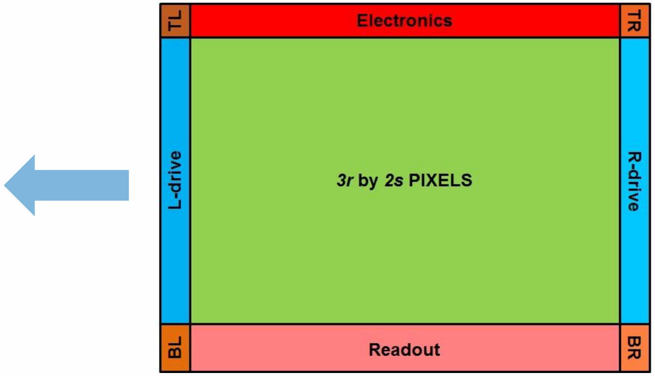
MAPS with stitching techology

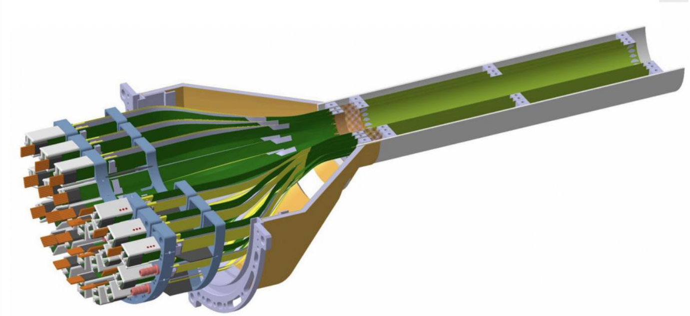
- Traditional Monolithic Active Pixel Sensor (MAPS) was constrained in the size of a single reticle($\sim \mathrm{cm}^2$).
- Stitched MAPS sensor could achieve larger active area
  - Lithography elements can be applied separately
  - To stitch these element up to a wafer scale
  - The thinned, curved and stitched MAPS could serve as the tracker on HEP experiments to increase the coverage and reduce the material budget
  - Not applied on HEP yet, but a 65 nm CMOS imaging sensor process is being developed with a partnership between ALICE-ITS3 and ePIC-SVT groups.



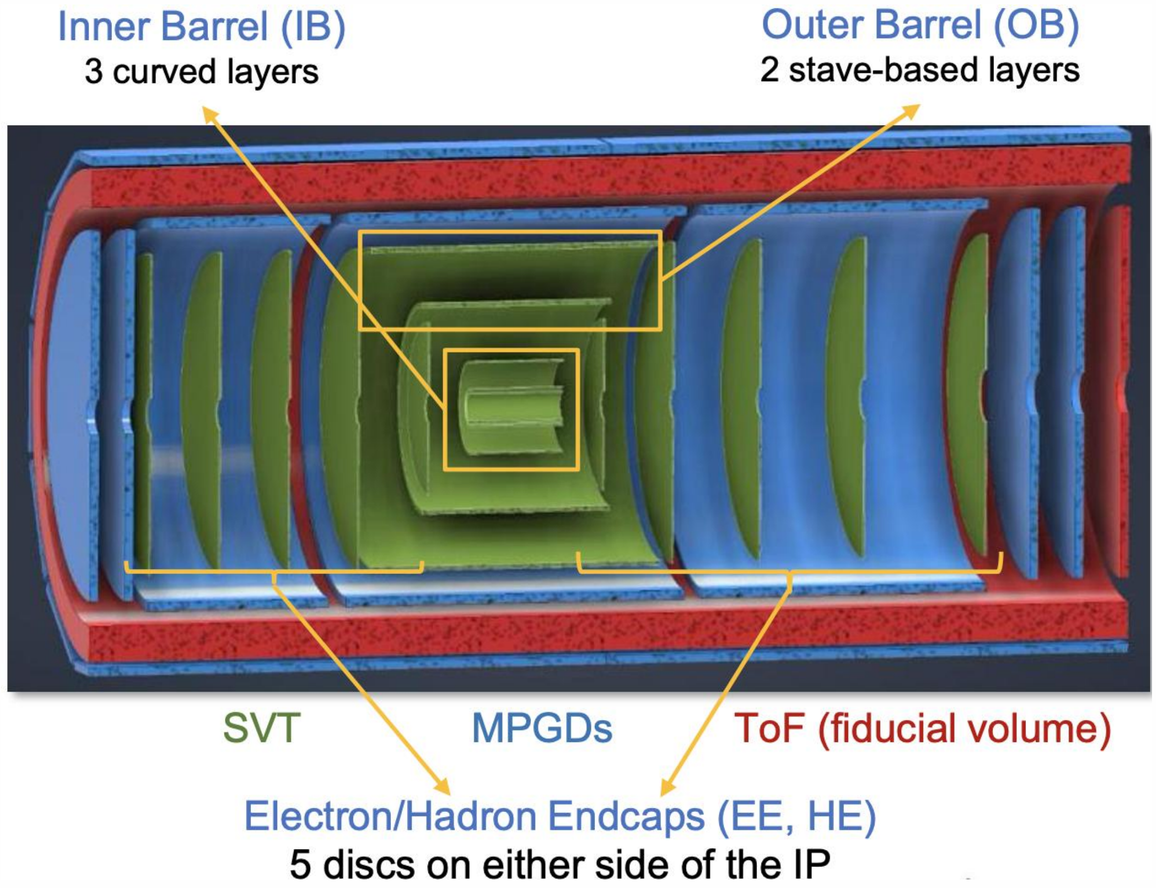








ePIC Silicon Vertex Tracker

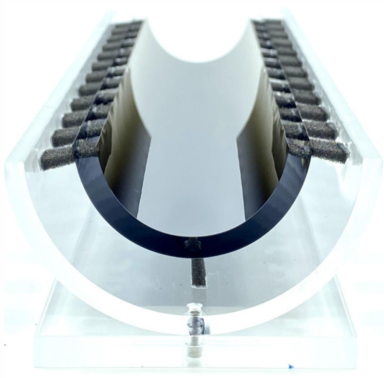


Total active area ~8.5 m^2
Radius ~0.45 m
Length ~2.5 m

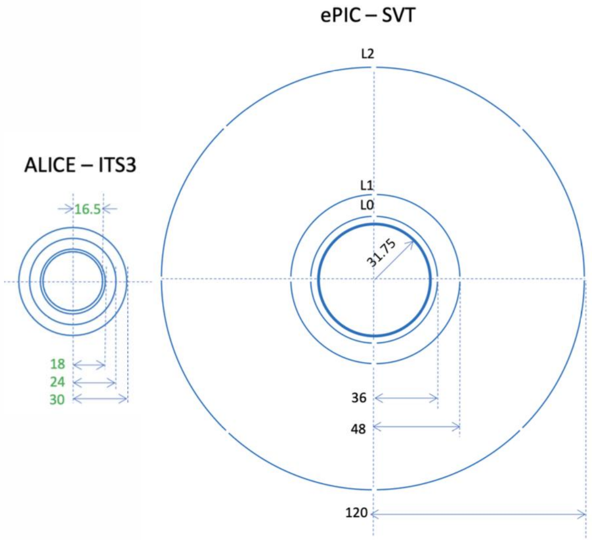
ePIC SVT target specifications	
Spatial resolution	~ 5 μm
Power	< 40 mW/cm^2
Frame rate	≤ 2 μs
Material budget(per layer)	IB: 0.05% X/X_0
	OB: 0.25%, 0.55% X/X_0
	EE/HE: 0.25% X/X_0

ePIC SVT Inner Barrel layers

- ☐ Inner barrel layers will utilise the full wafer scale sensor and ultra-thin detector concept.
  - Three layers of stitched, wafer scale, thin and bent sensors
  - Minimal mechanical support, air-cooling, no services in the active area



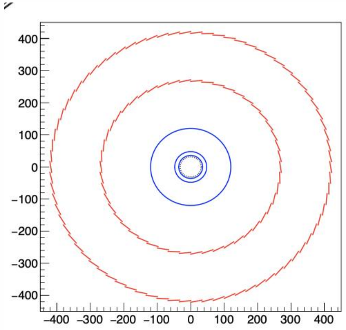
ALICE ITS3, arXiv.2105.13000
ALICE ITS3, arXiv.2212.08621

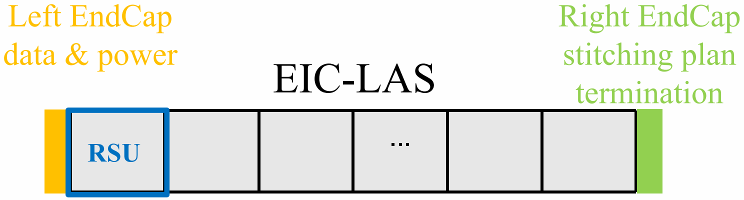


IB	r [mm]	l [mm]	X/X_0 %
L0	36	270	0.05
L1	48	270	0.05
L2	120	270	0.05

ePIC SVT Outer Barrel layers & Disks

- ❑ SVT outer barrels (Foucs of EIC-UK WP1)
  - Two layers of EIC Large Area Sensor (EIC-LAS) staves.
  - EIC-LAS is modification of the ITS3 sensor for high yield, low cost and large area coverage:
    - stitched but not wafer scale
    - possible modification in the periphery (LEC) to reduce number of readout links




Left EndCap data & power

EIC-LAS

Right EndCap stitching plan termination

BARREL	r [mm]	l [mm]	X/X0 %
Layer 3	270	540	0.25
Layer 4	420	840	0.55

- ❑ SVT EE/HE Endcaps
  - 5 disks of EIC-LAS sensors (same optimized sensor as OB) on either side of IP.
  - Disk inner openning defined by the beam pipe bake-out constains and off-centered where beam pipe diverges, details in Peter’s slides

DISKS	+z [mm]	-z [mm]	r_out [mm]	X/X0 %
Disk 0	250	-250	240	0.25
Disk 1	450	-450	420	0.25
Disk 2	700	-650	420	0.25
Disk 3	1000	-850	420	0.25
Disk 4	1350	-1050	420	0.25

R&D of ALICE-ITS3 & EIC-LAS

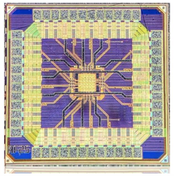
MLR1: qualification of CMOS 65 nm technology, prototype for circuit blocks

ER1: Stitching technology demonstrator (MOSS & MOST), yield studies

ER2: Fully functional sensor that satify ITS3 requirement

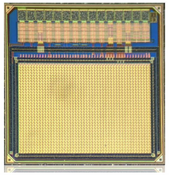
ER3: Final production and bug fix from ER2

APTS



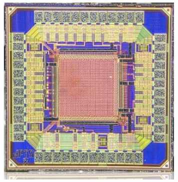
Charge collection study

CE65

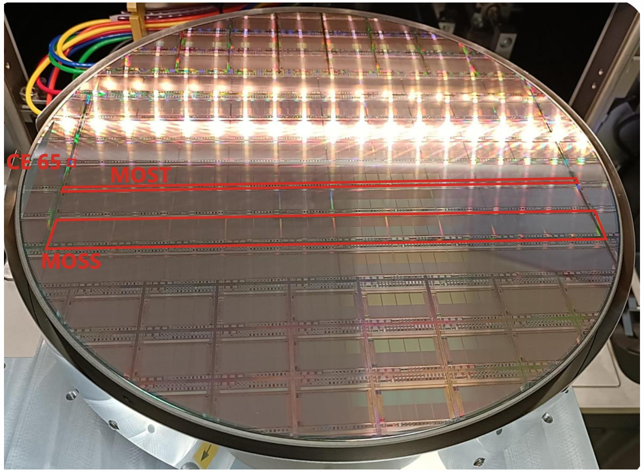


Mismatches
defect densities

DPTS



Digital readouts
Time-over-Threshold
information



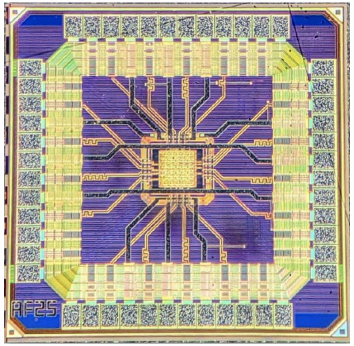
- Monolithic stitched sensor (MOSS)

- feasibility and yield factors study of wafer-scale sensors

- Monolithic sitiched sensor with Timing (MOST)

EIC-LAS will also be designed and qualified simultaneously.

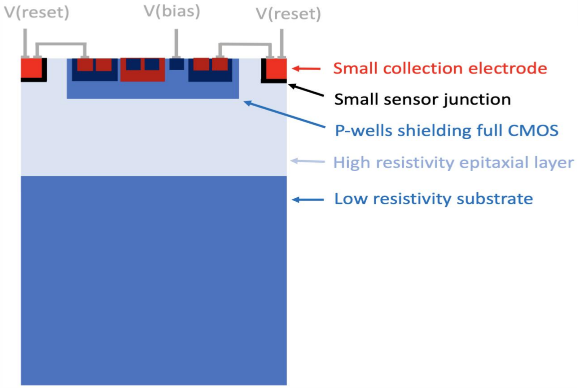
Development of MLR1 APTS sensor in UK



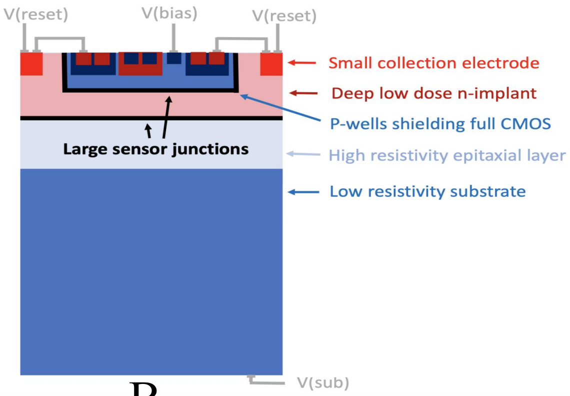
Analog Pixel Test Structure

- 65 nm CMOS technology
- 4 × 4 pixel readout
- Charge collection properties study

Flavor	Pitches	splits
Standard	10, 15, 20, 25	1, 2, 3, 4
B	10, 15, 25	1, 2, 3, 4
P	10, 15, 20, 25	1, 2, 3, 4

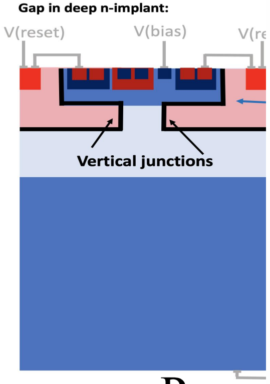


Standard



B

Deep low dose n-implant introduced to provide full depletion

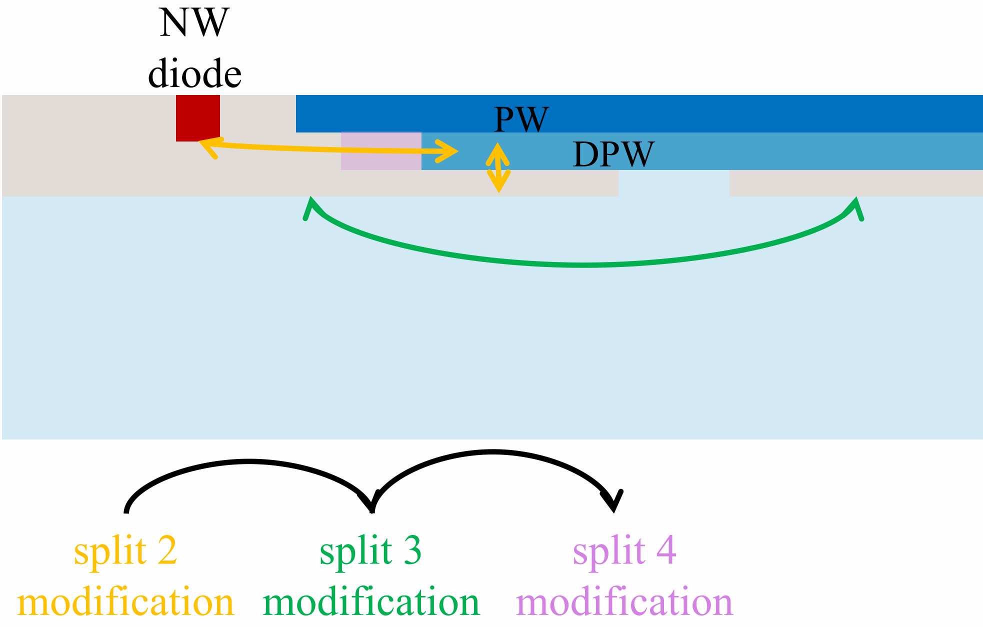


P

Based on B type sensor, gap in deep n-implant to optimise the electric field at the pixel edge to have fast charge collection

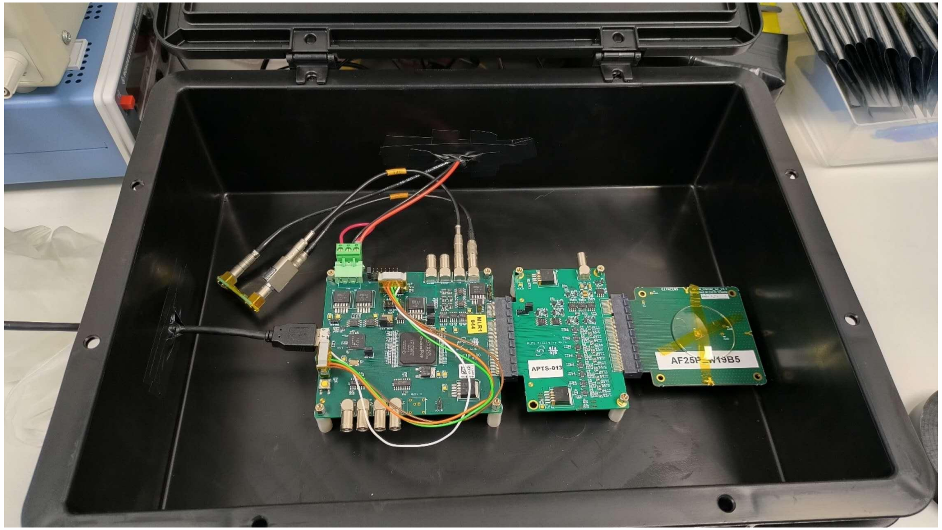
Process modifications for better charge collection

split 1: No extra modifications
split 2: Modification of deep P-well to impove isolation between circuit and sensor and prevent punch-through between deep N-well and circuits
split3: Modification of the doping level of deep N-well to achieve full depletion on basis of split2.
split4: Modification of deep P-well to form better lateral e-field to impove charge collection based on split 3.



Optimization of a 65 nm CMOS imaging process for monolithic CMOS sensors

Test setup & sensors bonded at Bham



- FPGA: MLR1-044
- Proximity: APTS-013(re-calibrated)
- Power supply: R&S HMP2030
- Sensors:
  - 22 sensors bonded at bham from splits 2 and 3.
  - 1 chip at least for each configuration (flavour, pitch, split).
  - All sensors passed the visual inspection and resistance test.
  - Sensors characterised using Fe-55 source @ Liverpool

flavour	pitch	Wafer 16 (split 2)	Wafer 19(split 3)
B	10	AF10B_W16B1	AF10B_W19B6
		AF10B_W16B4	
	15	AF15B_W16B2	AF15B_W19B1
		AF15B_W16B6	AF15B_W19B2
	25	AF25B_W16B3	AF25B_W19B4
		AF25B_W16B5	
P	10	AF10P_W16B1	AF10P_W19B8
		AF10P_W16B2	
	15	AF15P_W16B3	AF15P_W19B1
		AF15P_W16B4	
	20	AF20P_W16B8	AF20P_W19B3
			AF20P_W19B9
			AF20P_W19B10
	25	AF25P_W16B7	AF25P_W19B5

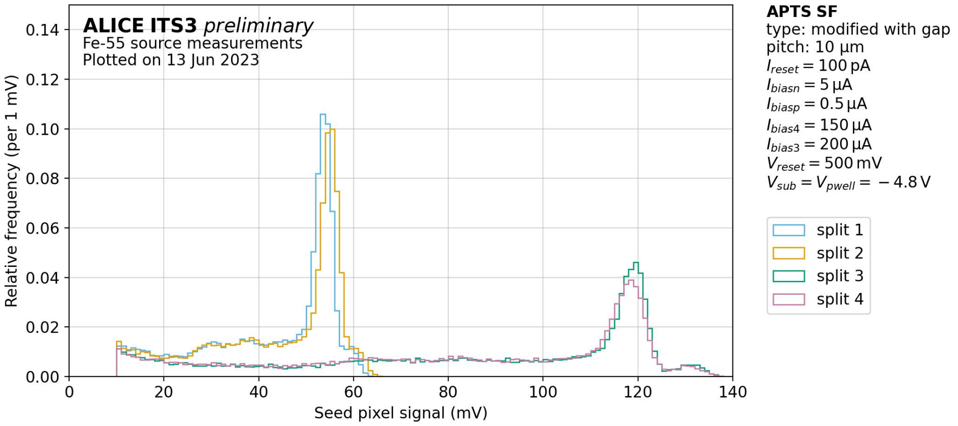
+ AF15P_W22B3

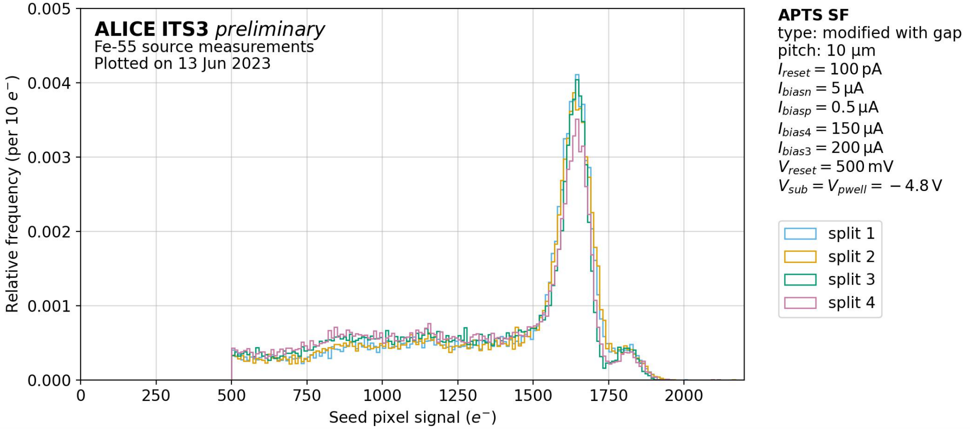
Chips highlighted in yellow selected for this presentation. More results in the backup slides.

Split comparison of Fe-55 measurements (P-types)

Seed pixel signal of pitch 10 µm

Plots approved June 2023

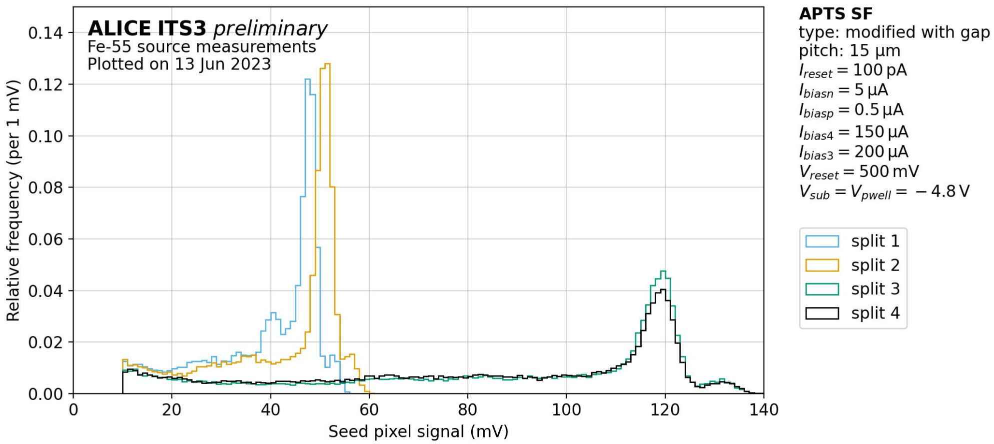


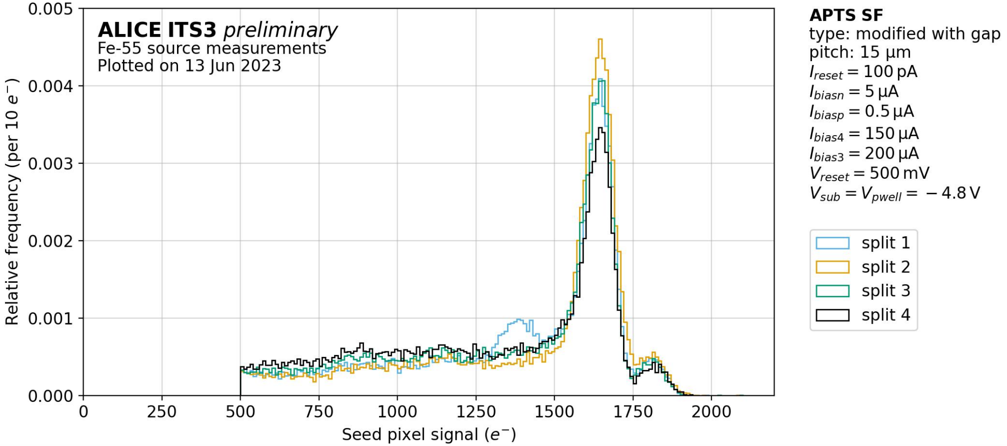


- 150K events were recorded for the spectra reconstruction in mV unit.
- Different signal amplitudes were observed between split 1&2 and split 3&4.
- Spectra converted to electron unit, after the sensor calibration using Fe-55 k-α peak.
- Similar charge collection was observed among all splits in electron unit.

Seed pixel signal of pitch 15 µm

Plots approved June 2023





Seed pixel signal of pitch 20 µm

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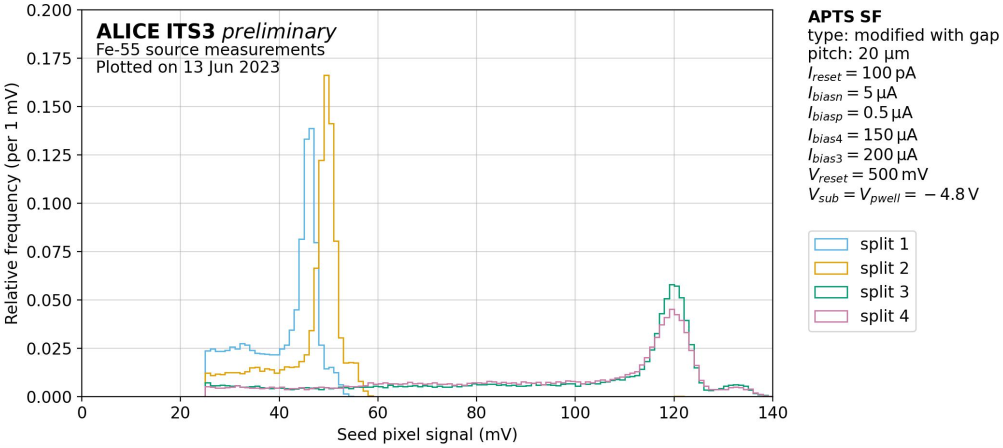

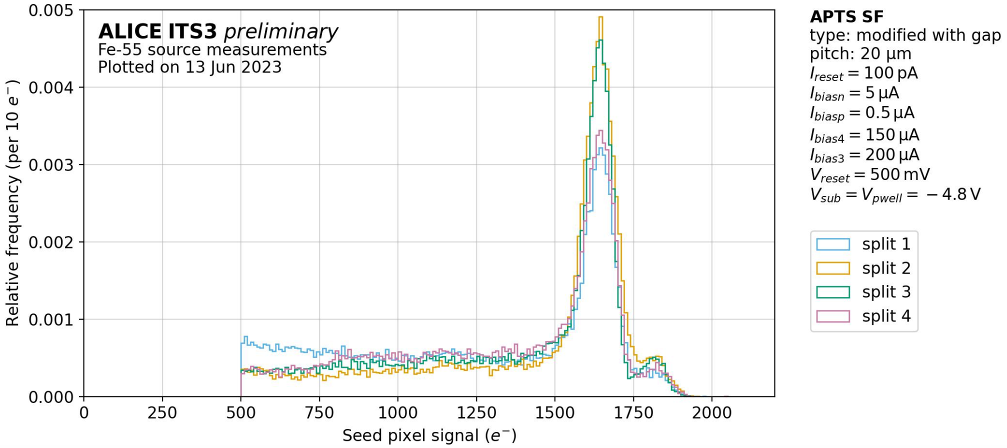

- For pixel pitches >= 20 µm, a tail of smaller charges appears in split 1, indicating worse charge collection properties.
- The electric field weakens at the edges of the pixel, leading to smaller charge collected.

Seed pixel signal of pitch 25 µm

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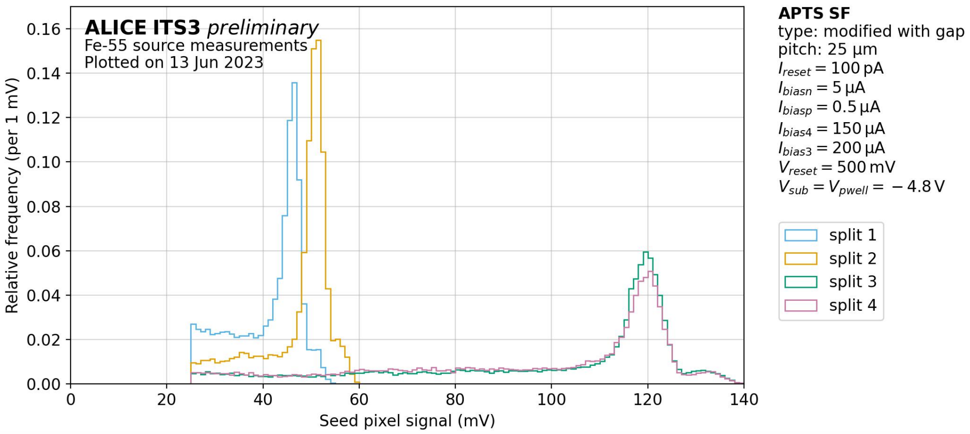
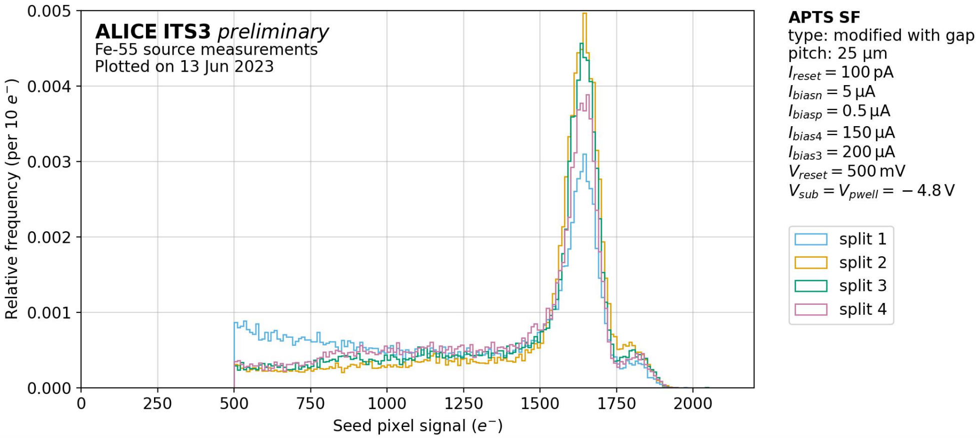
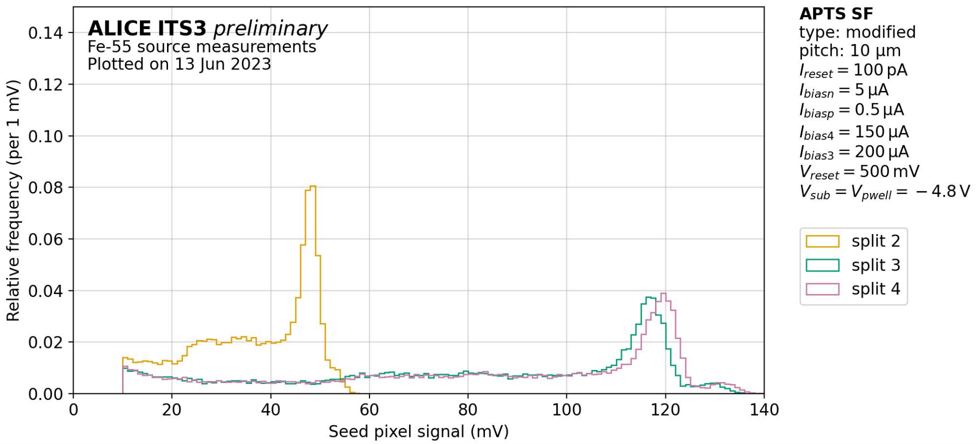


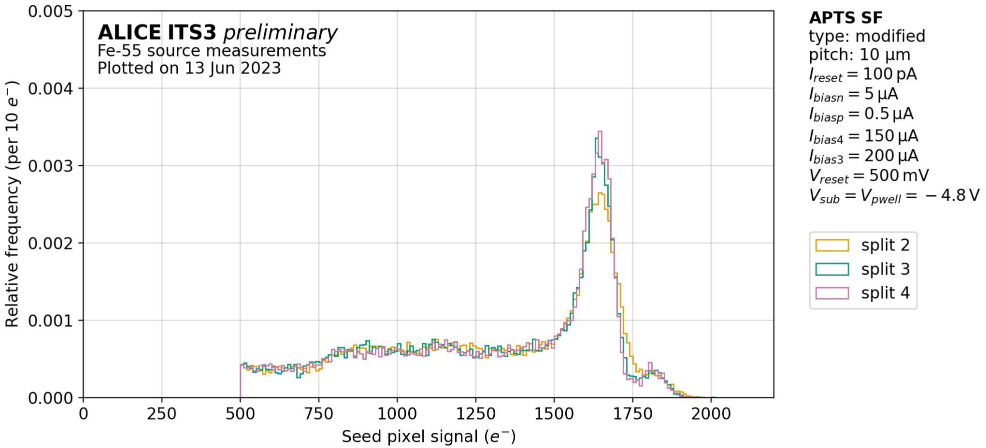


Split comparison of Fe-55 measurements (B-types)

Seed pixel signal of pitch 10 µm

Plots approved June 2023

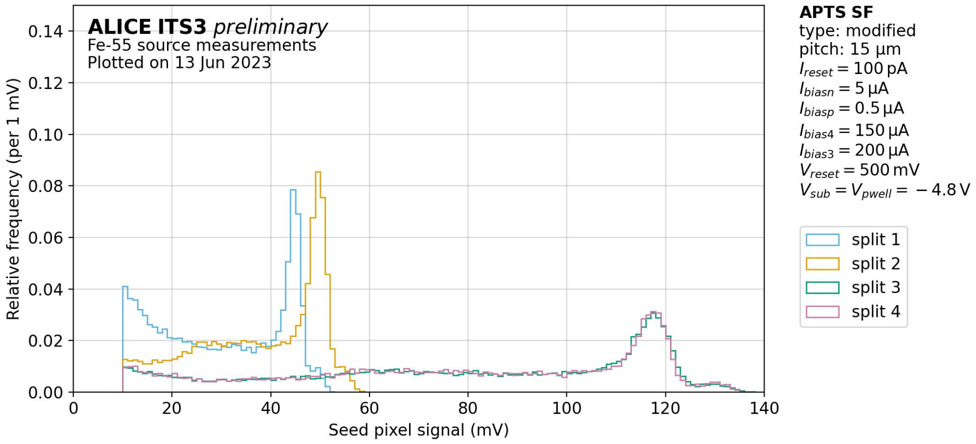


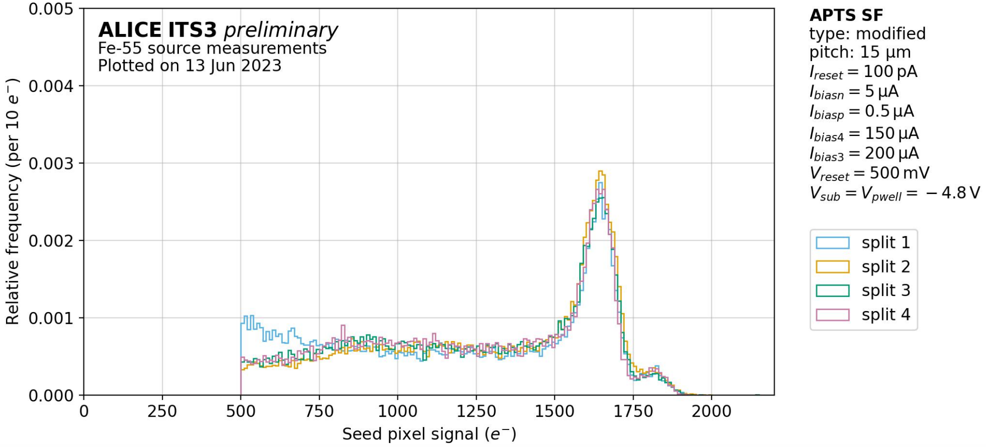


- No measurements from split 1
- Different signal amplitude were observed between split 2 and split 3&4 in mV unit.
- Similar charge collection was observed among all splits in electron unit.

Seed pixel signal of pitch 15 µm

Plots approved June 2023





For pixel pitch of 15 um, a tail of smaller charges appears in splits 1 which is also the result of weak e-field at the pixel edge.

Seed pixel signal of pitch 25 µm

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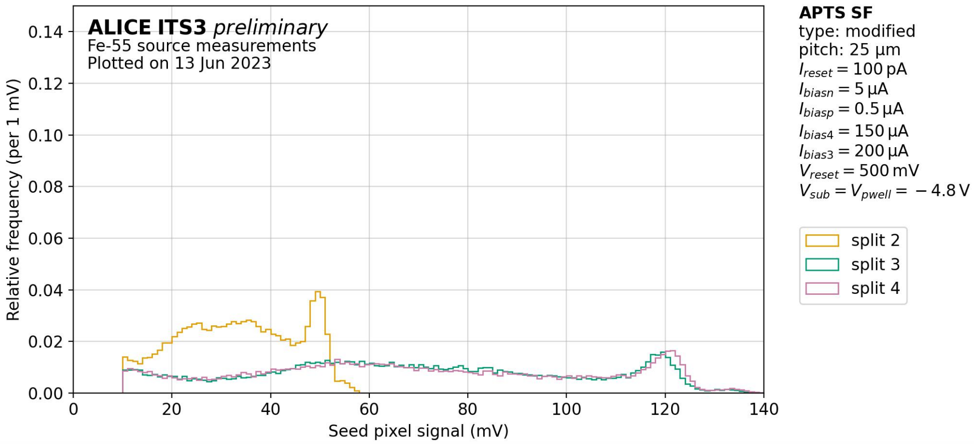
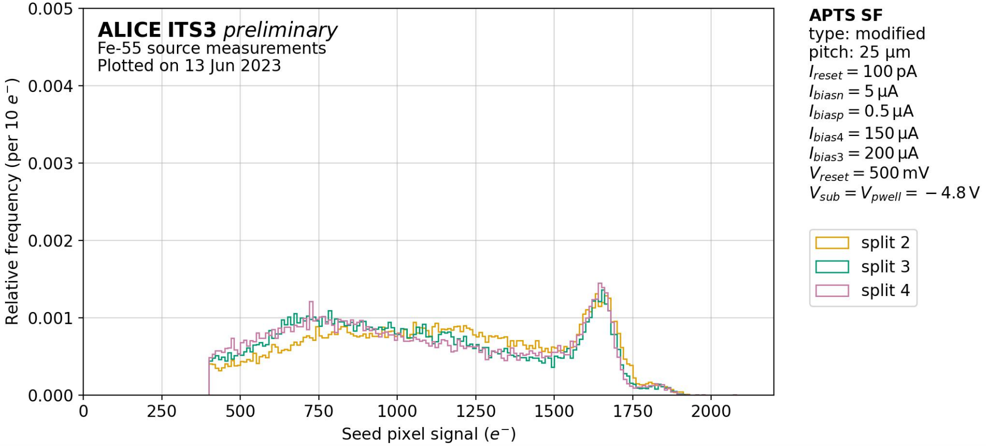


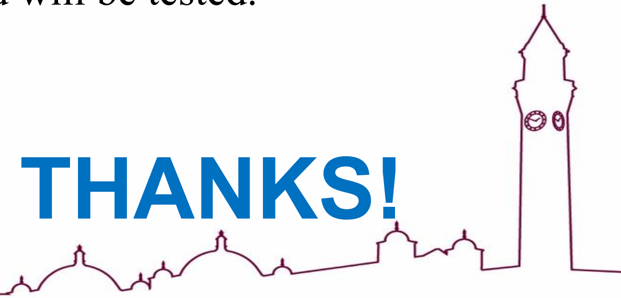


Bumps at the lower ends of the spectra were observed in all splits which are the result of charge sharing with adjacent pixels.

Summary & outlook

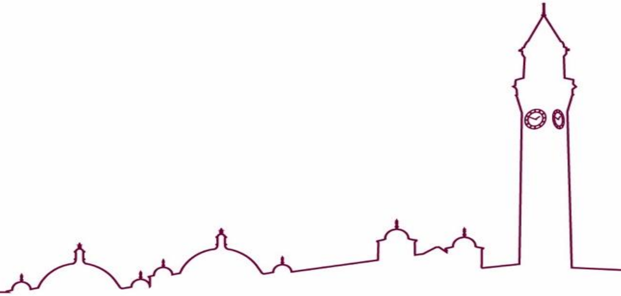
- ❖ **Summary**
  - ☐ The ePIC-SVT detector will be realised with stitched MAPS
    - ▪ Implemented in a 65 nm CIS process which is also used in ITS3 sensor.
    - ▪ Wafer scale sensors as ITS3 for SVT IB.
    - ▪ EIC-LAS, the modification of ITS3 sensor, will be designed and produced for OB/endcaps, considering OB geometry, material budget and readout requirements.
  - ☐ Fe-55 measurements of MLR1-APTS sensor:
    - ▪ Worse charge collection is observed in split 1 with larger pixel pitches, this indicates the charge loss due to the weak e-field at the edge of the pixel.
    - ▪ Optimised charge collection in split 3&4 was varfied through the comparison among splits

- ❖ **Outlook**
  - ☐ Measurement of ER1 senors(MOSS, MOST, baby MOSS & baby MOST) collaborating with ALICE ITS3 group is in plan.
  - ☐ Stitching technology, uniformity of sensor performance and sensor yield will be tested.

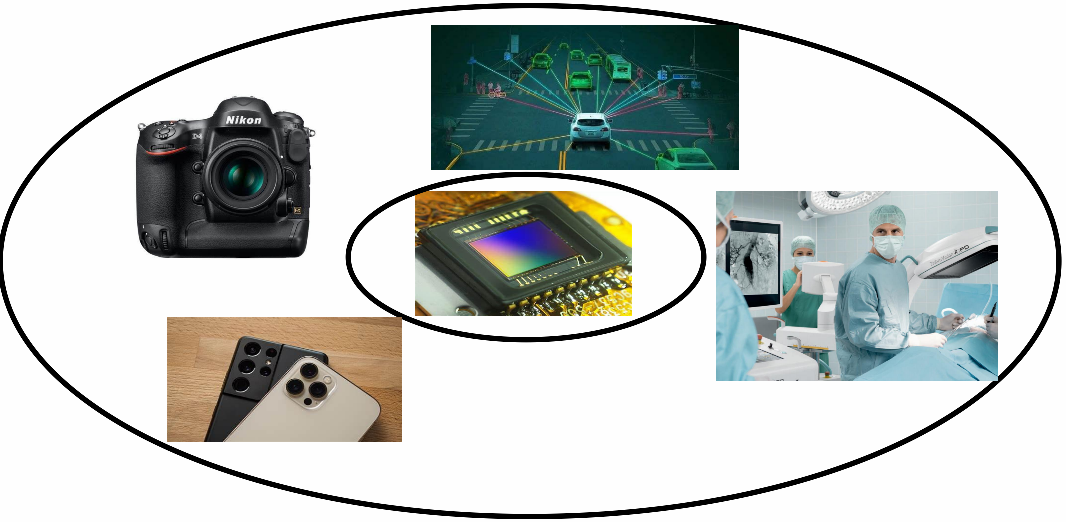


THANKS!

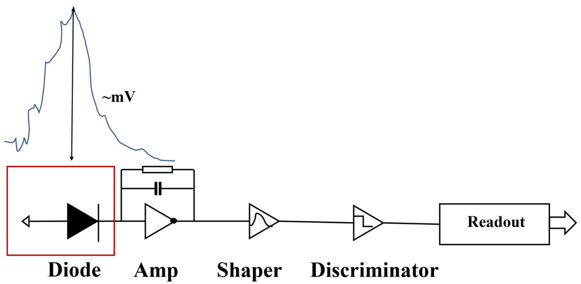
Back up



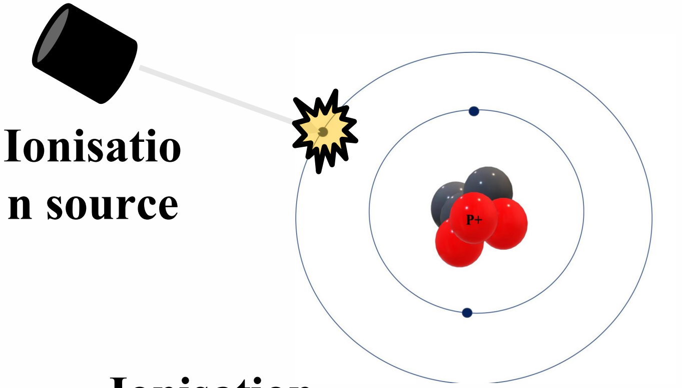
Working principle of MAPS



Signal processing & reconstruction

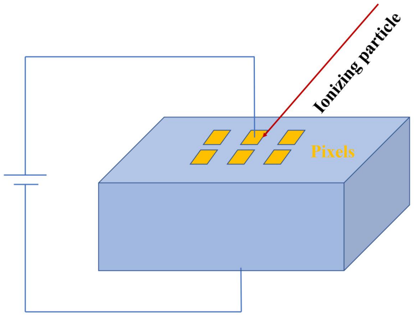


Ionisation source

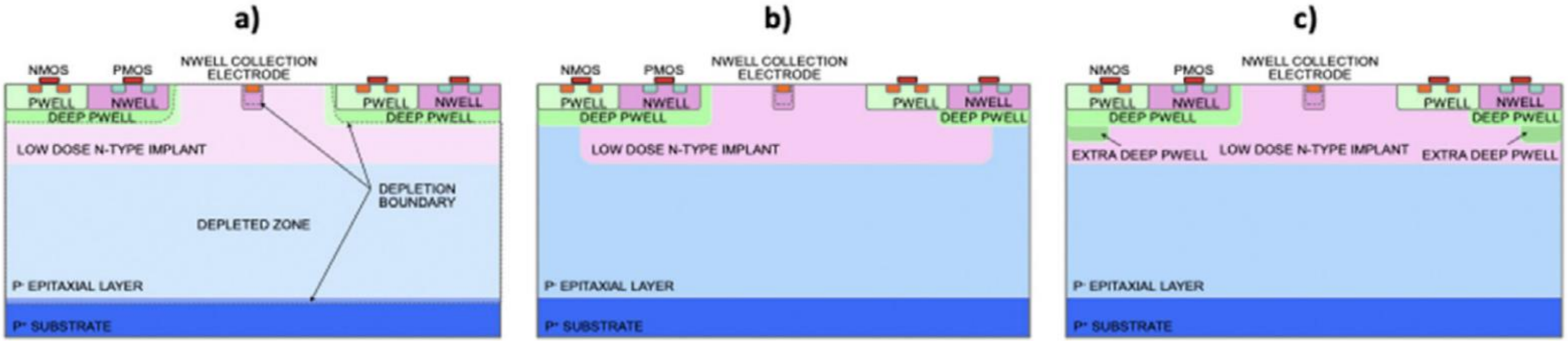


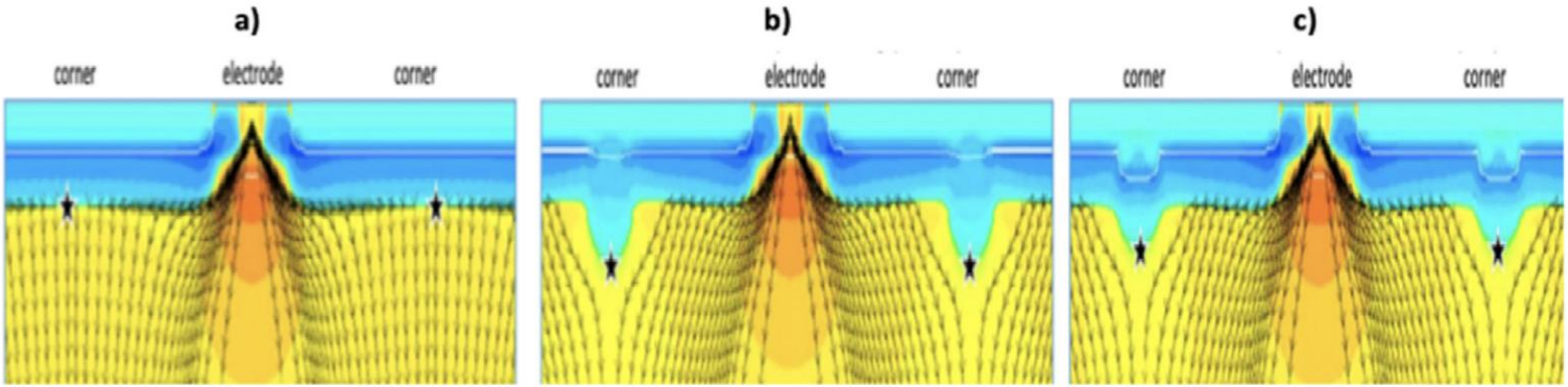
Ionisation

Charge generation & collection



TCAD simulation of the lateral e-field in various modified process





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