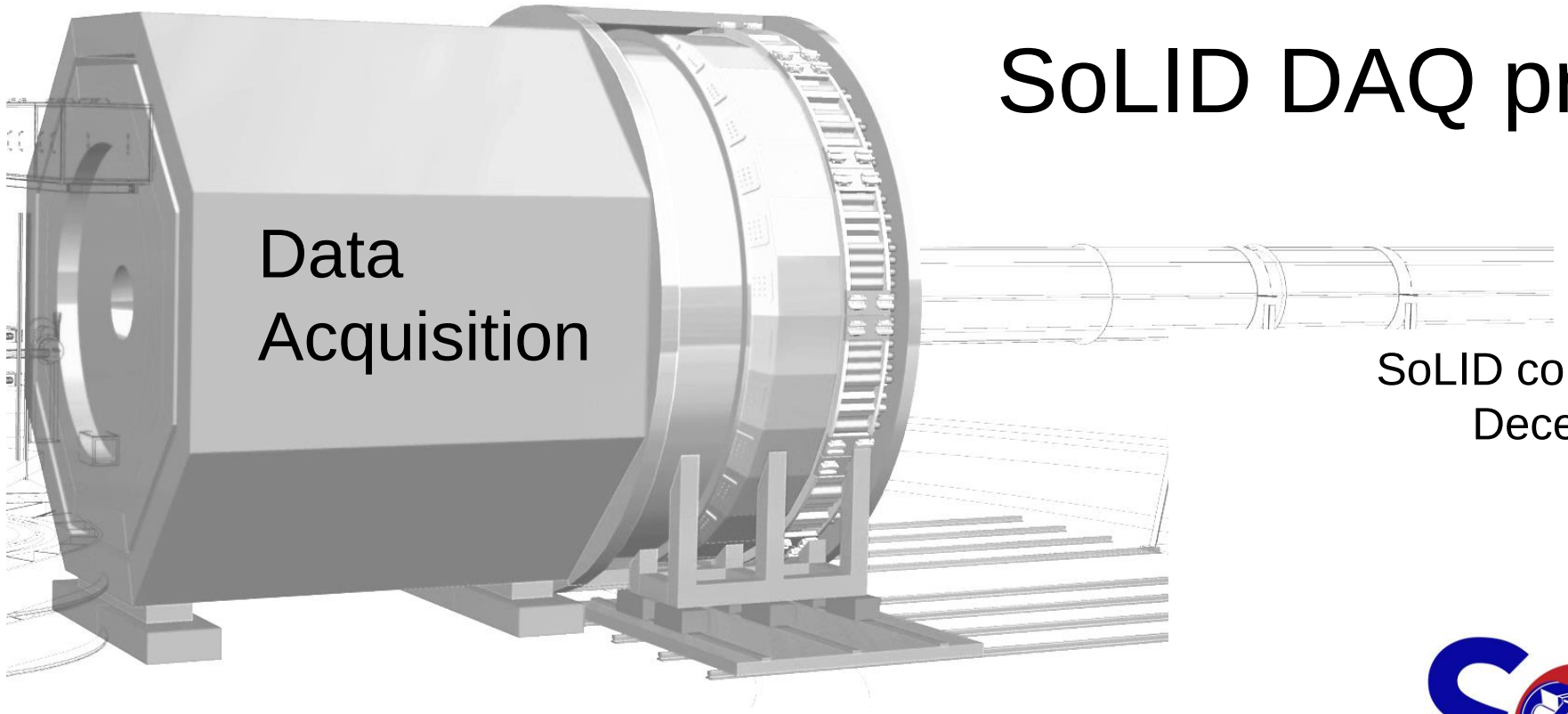


SoLID DAQ preRD and plans

SoLID collaboration meeting
December 8th 2023

Alexandre Camsonne

- Outline

- Reminder preRD
- Capital project
- VMM tests
- GEM chip
  - VMM
  - SALSA
- SBS, Moller testing
- Conclusion

SoLID preRD tasks reminder

- A : VMM high rate test (need beam test)
  - A1 : procure evaluation board and test direct readout
  - A3 : develop prototype determine maximum trigger rate
  - A2 : study behavior in high background
- B : APV rate capability (complete)
  - B1 : develop Fast Readout
  - B2 : demonstrate 100 KHz rate with 1 sample 30% occupancy
    - Max rate with exisiting electronics 5 KHz with 6 samples
    - If replaced upgrade MPDs 10 KHz with 6 samples
    - SBS could record up to 1.6 GB/s, expect to be able to record 2.1 GB/s with 3 event recorder
- C : FADC development (complete)
  - C1 : Fast VXS readout (used in HCAL)
  - C2 : Calorimeter trigger (used in NPS, and GEp)
  - C3 : PVDIS trigger and test (tested during Cerenkov test)
  - C4 : PVDIS trigger and test 2 sectors (tested on bench)
  - C5 : SIDIS trigger and test (tested on bench)
    - Opportunity to test during GEp5

Tasks and milestones

- D : Gas Cerenkov Test support
  - D1 : readout for Cerenkov test (complete)
  - D2 : Cerenkov data with high background (complete)
  - D3 : MAROC data with high background (complete)
  - D4 : evaluation improvement with MAROC pixel readout (to test in beam)
- E : NALU ASOC Time of flight chip
  - E1 : install evaluation board (complete)
  - E2 : sample high background data (to test in beam)
  - E3 : timing resolution (to test in beam)

Capital equipement

Item	cost/item	number	total	Ordered	Can order 2023	Order 2024/2025
FADC 250	6000	104	624000			624000
Gigabit serial connectors			40000	40000		
Cables	100	1664	166400			
VETROC	4000	30	120000		120000	
TD	3000	16	48000		48000	
VTP	10000	31	310000	400000		
SSP	5000	4	20000			
VTP	8000	1	13000			
TS	4000	1	4000			
TID	3000	31	93000			
SD	2500	32	80000			
VXS crate	15000	32	480000	438000		8x18=128
VME CPU	7000	32	224000			224000
		Total	2217400			
	FTE/year cost	months				
Syracuse	80000	12	80000.00			
FEDAQ	120000	2	20000			
Hall C	120000	2	20000			
			2337400			

Give capability to deploy FADC, VTP for other experiments to continue testing the SoLID trigger in beam

About 900 K$ 2023

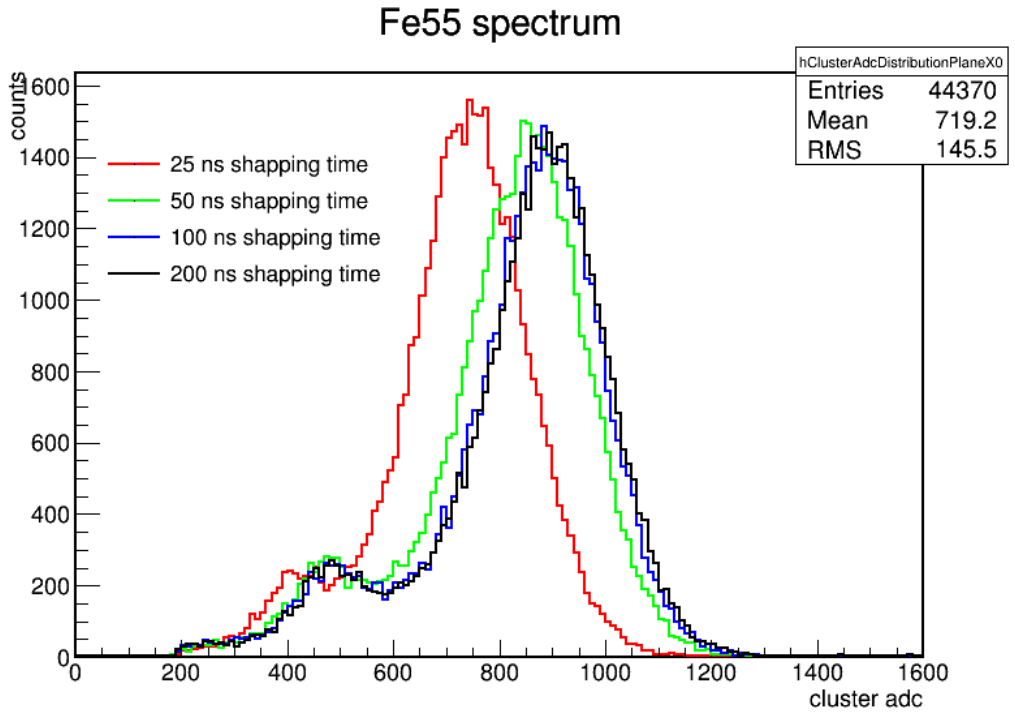
Plan to use VTP trigger for GEp, NPS and HKS

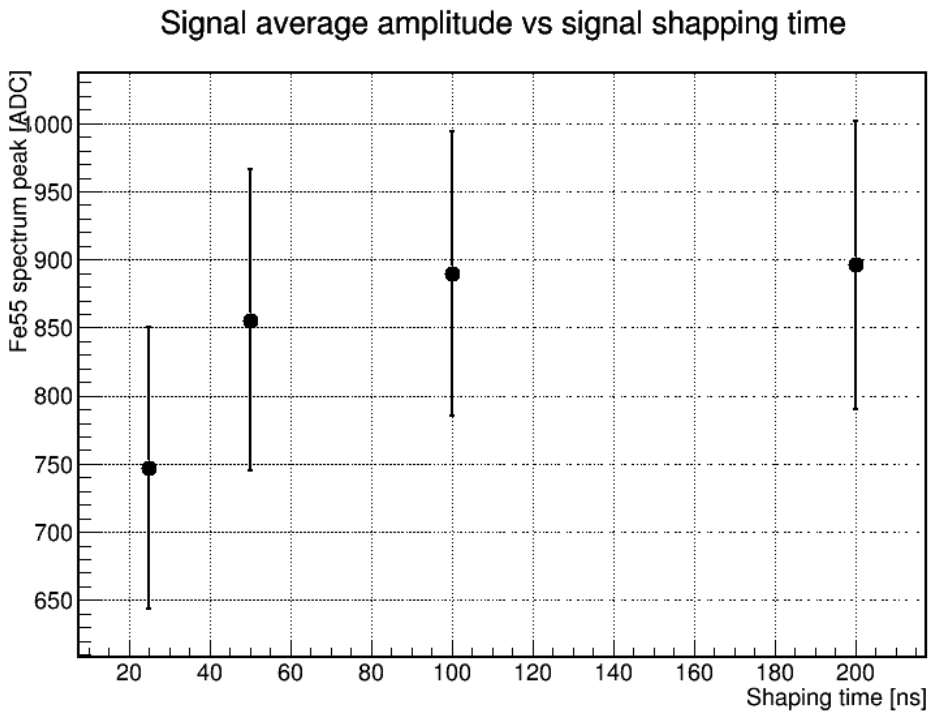
Trying TOF testing during HKS

VMM test

- Built 6 SoLID prototype boards
- Prototype development for data performance, test direct output with detector and X-ray source

Signal gain vs shaping time, gain = 3 mV/fC

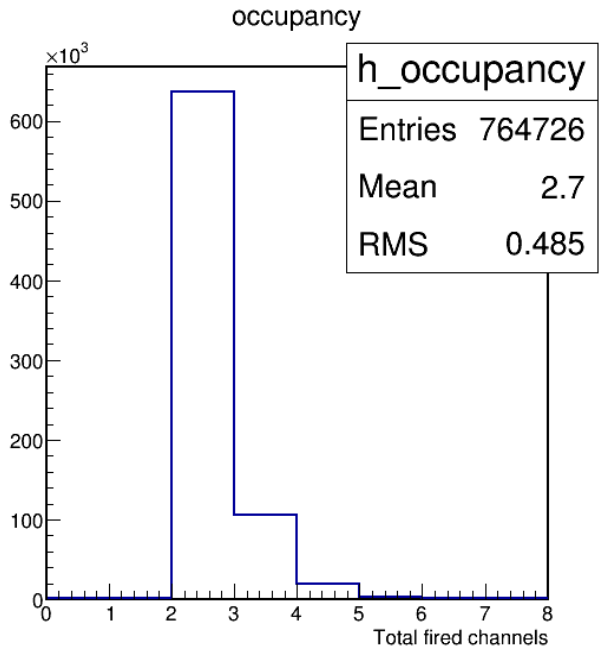


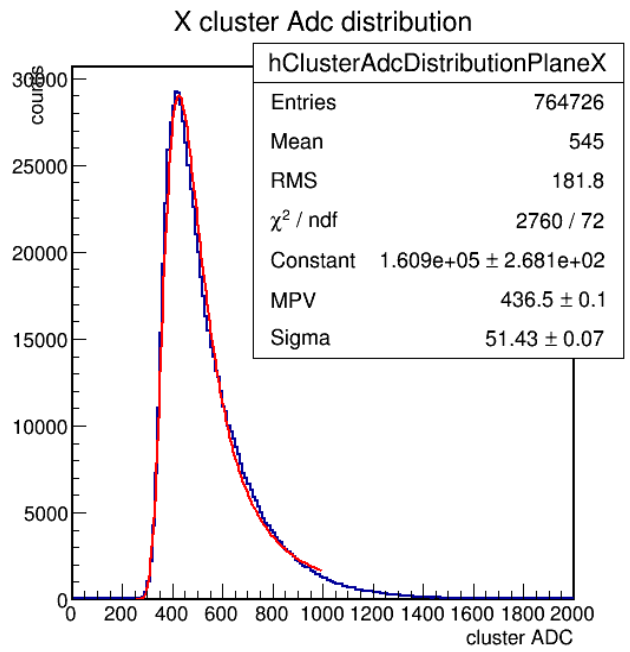


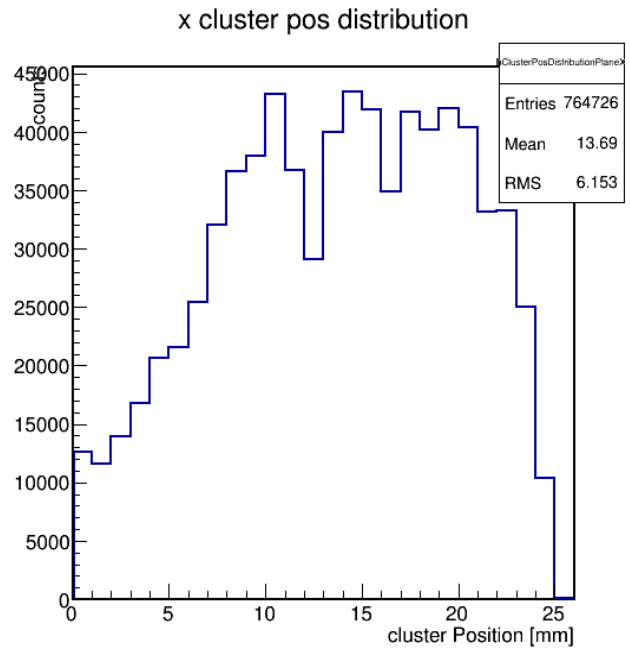
From source data, 25 ns shaping only about 15 % lower than 50 ns, so 25 ns shaping useable

HV =

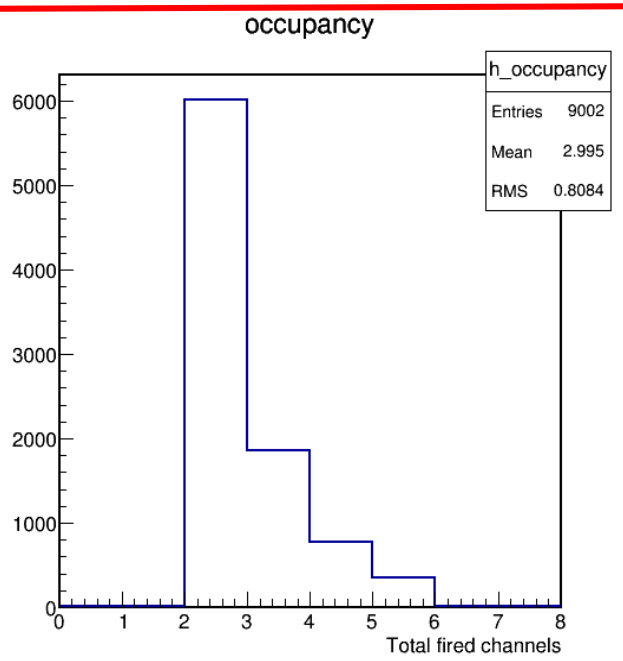
Sr90

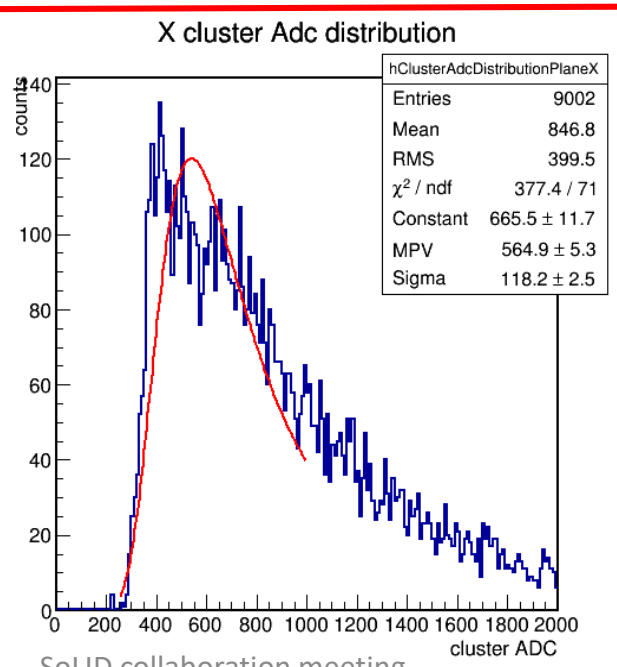


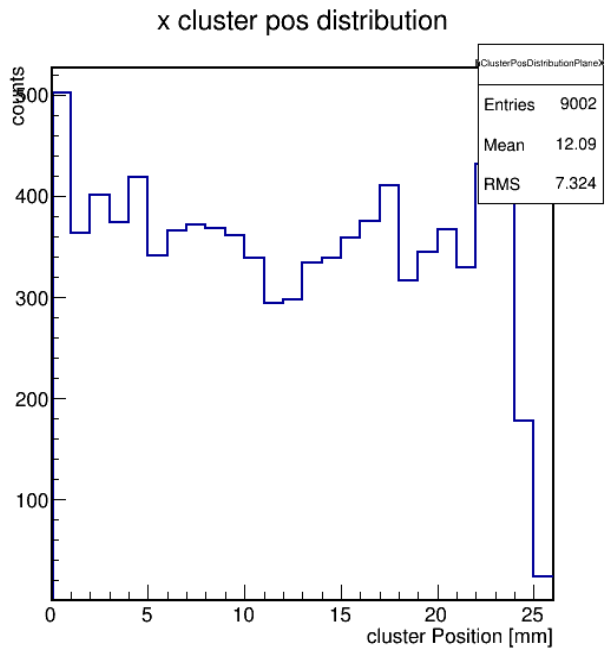




Cosmic







VMM3 prototype board development (Ed)

FPGA for VMM Direct Readout

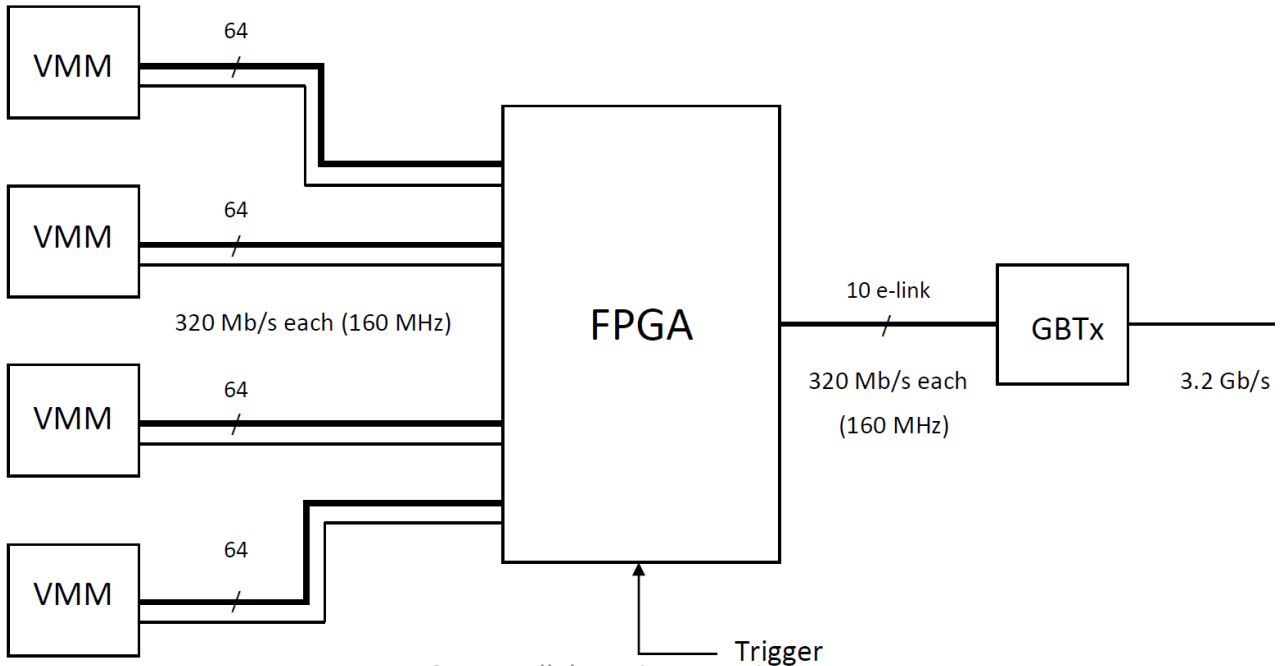
(E.J. 5/28/20)

Proposal

1 FPGA handles direct readout of 4 VMM chips

[64(channels/chip) + 1(clock/chip)] x 2(pins/signal) x 4(chips) = 520 pins (reasonable size, price FPGA)

1 GBTx data link for FPGA output data (10 e-links @ 320 Mb/s = 3.2 Gb/s)



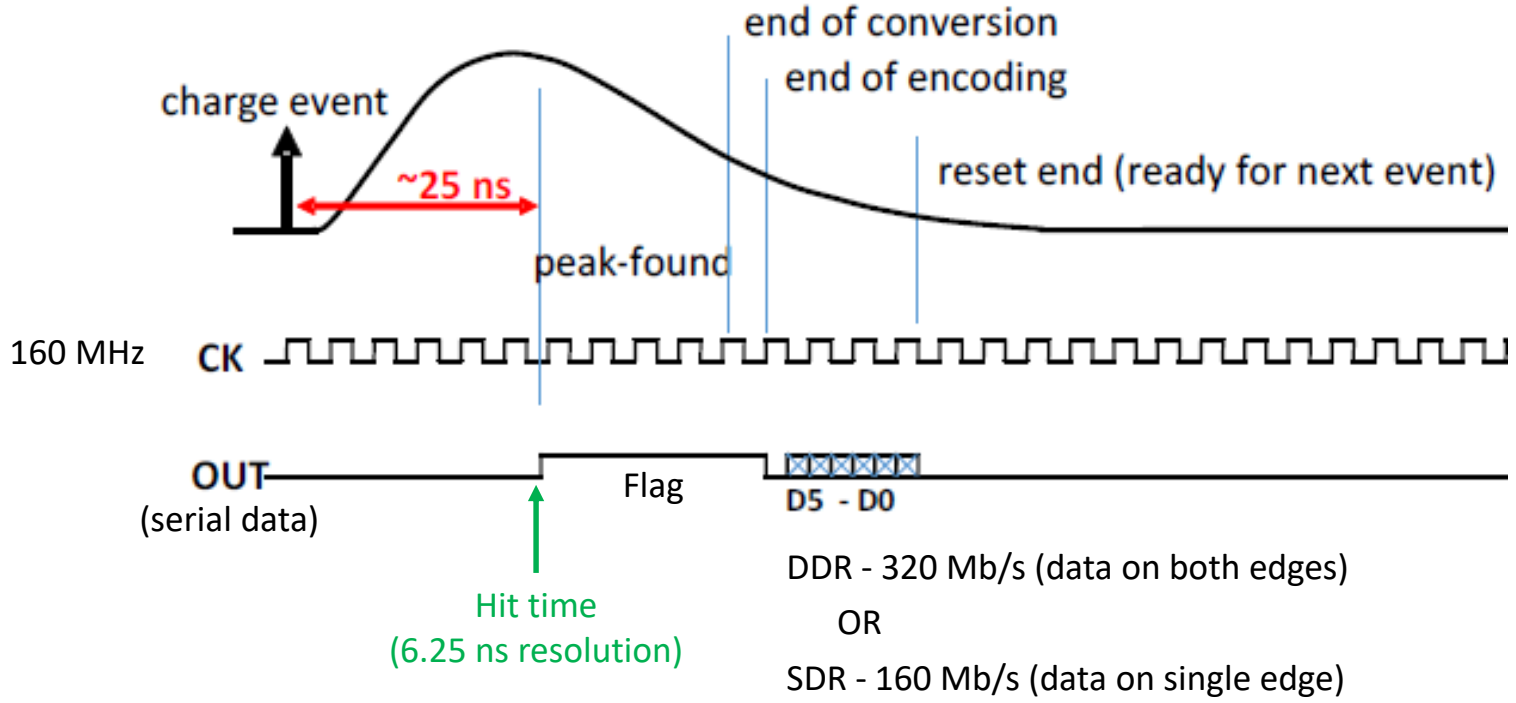
128 channel VMM prototype for SoLID

- Features
  - Fast 6-bit ADC data from each channel allows for high hit rates (~10MHz/ch)
  - Dual readout paths (fiber)
    - 10GbE for low radiation environments (FPGA → SFP+)
    - Readout using CERN rad hard components (FPGA → GBTx → VTRx)
  - Power and signal interface through mezzanine cards
    - Initially use commercial components on mezzanines
    - Later mezzanines with rad hard components – no modification of base board
  - Mitigation of effects of radiation on FPGA by triplicating logic and adding voting circuitry (TMR)

  - Status
    - Commercial component mezzanine boards fabricated
    - Base board fabrication in early May

VMM 6-bit Direct Output data format

Peak amplitude converted to 6-bit value



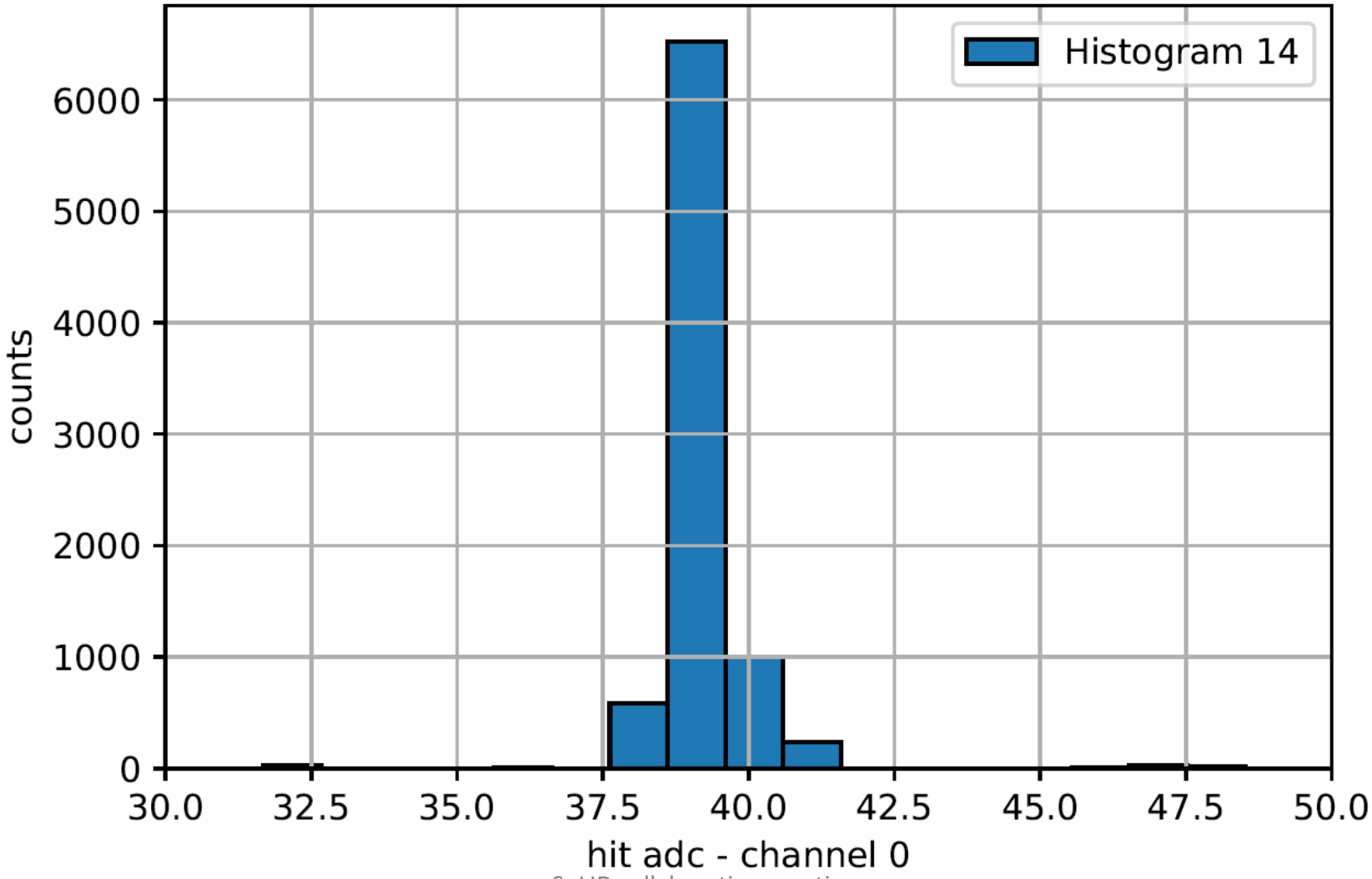
DDR - 320 Mb/s (data on both edges)

OR

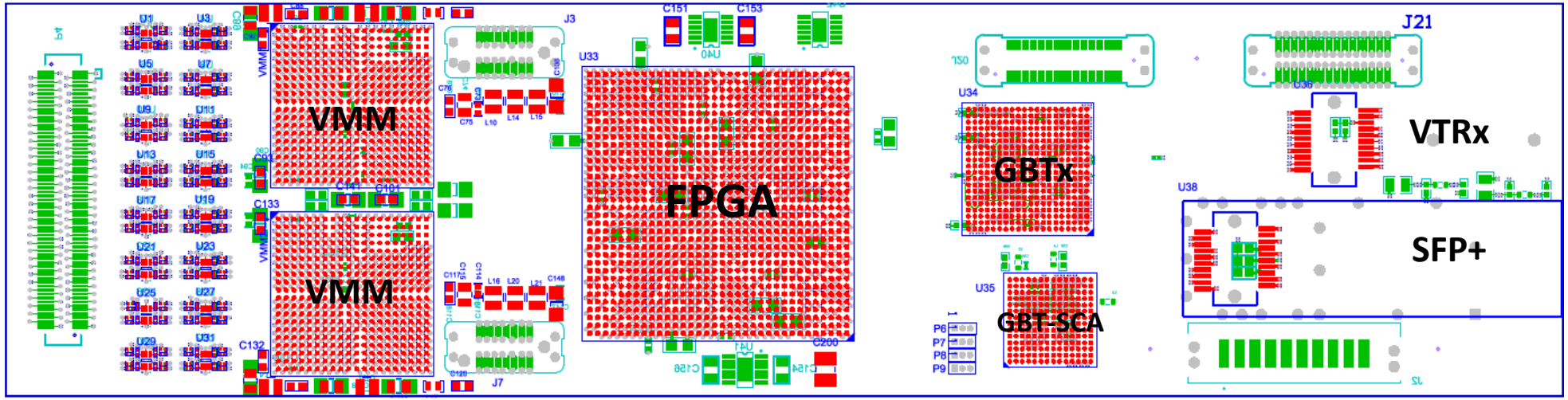
SDR - 160 Mb/s (data on single edge)

VMM 6-bit ADC direct data

(VMM evaluation board read out with Xilinx FPGA development card)



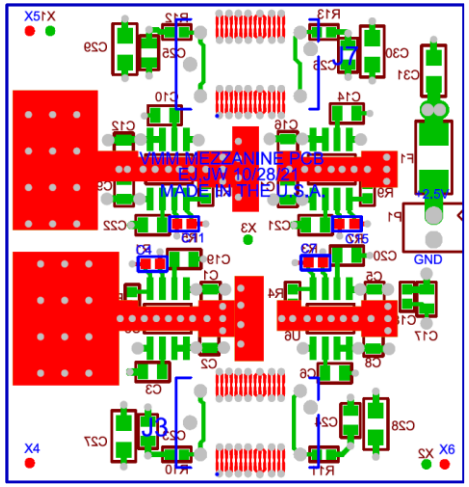
50mm

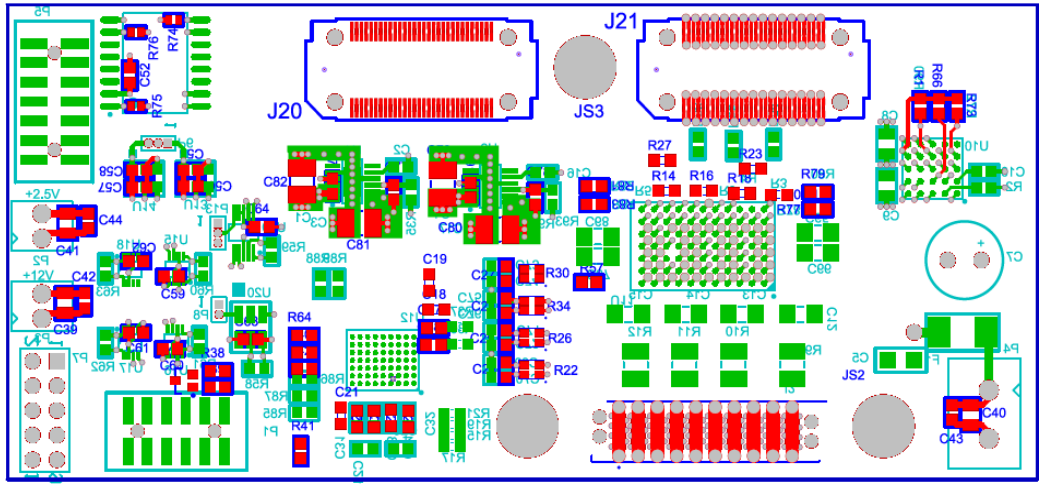


Base board

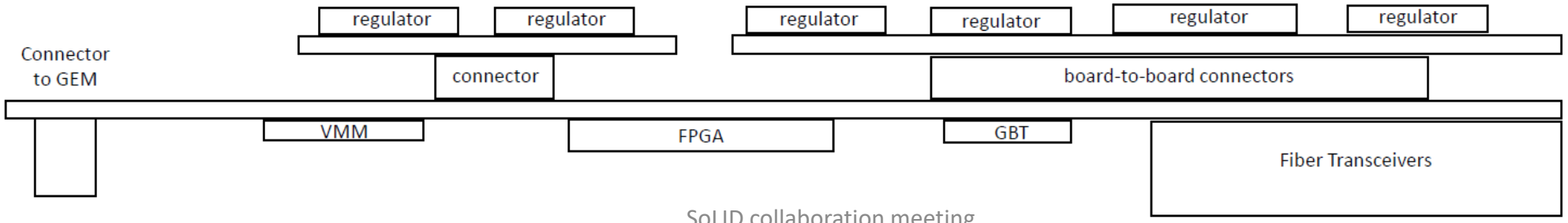
128 channel VMM prototype

VMM power mezzanine

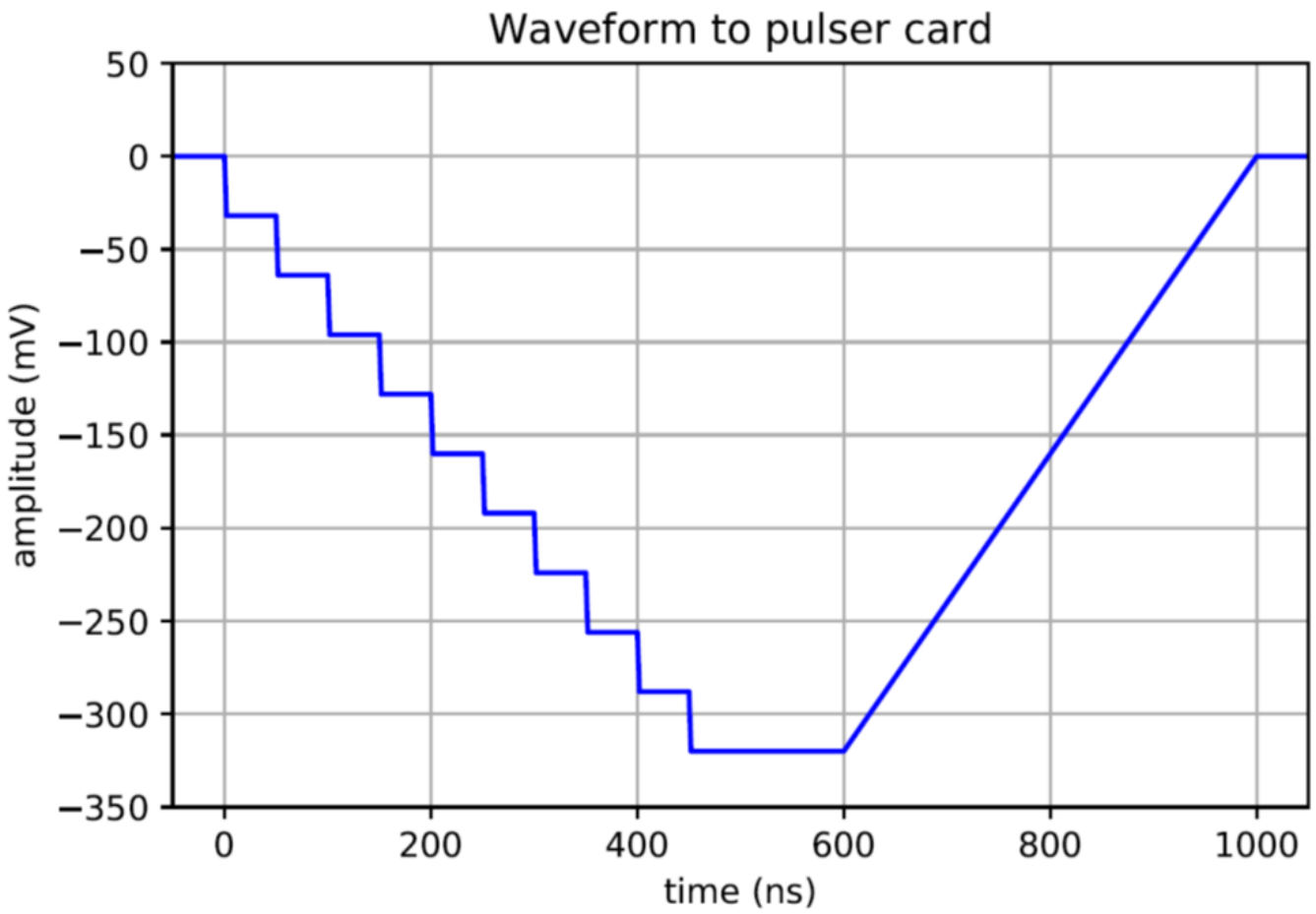


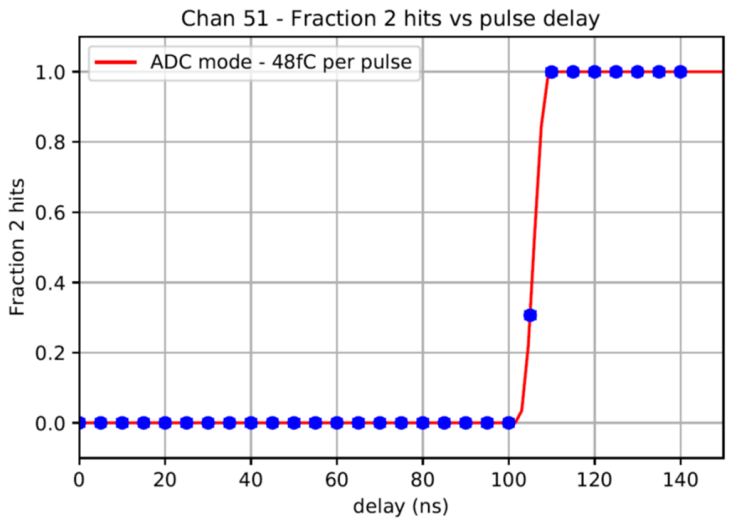


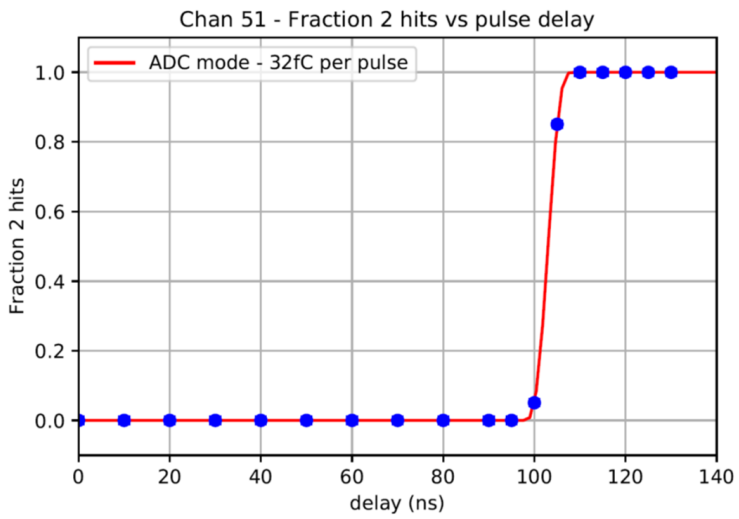
FPGA power mezzanine

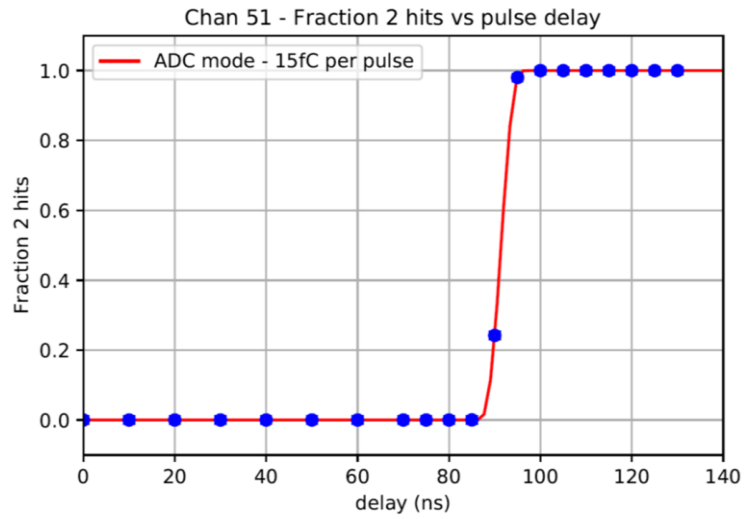


Assembly side view

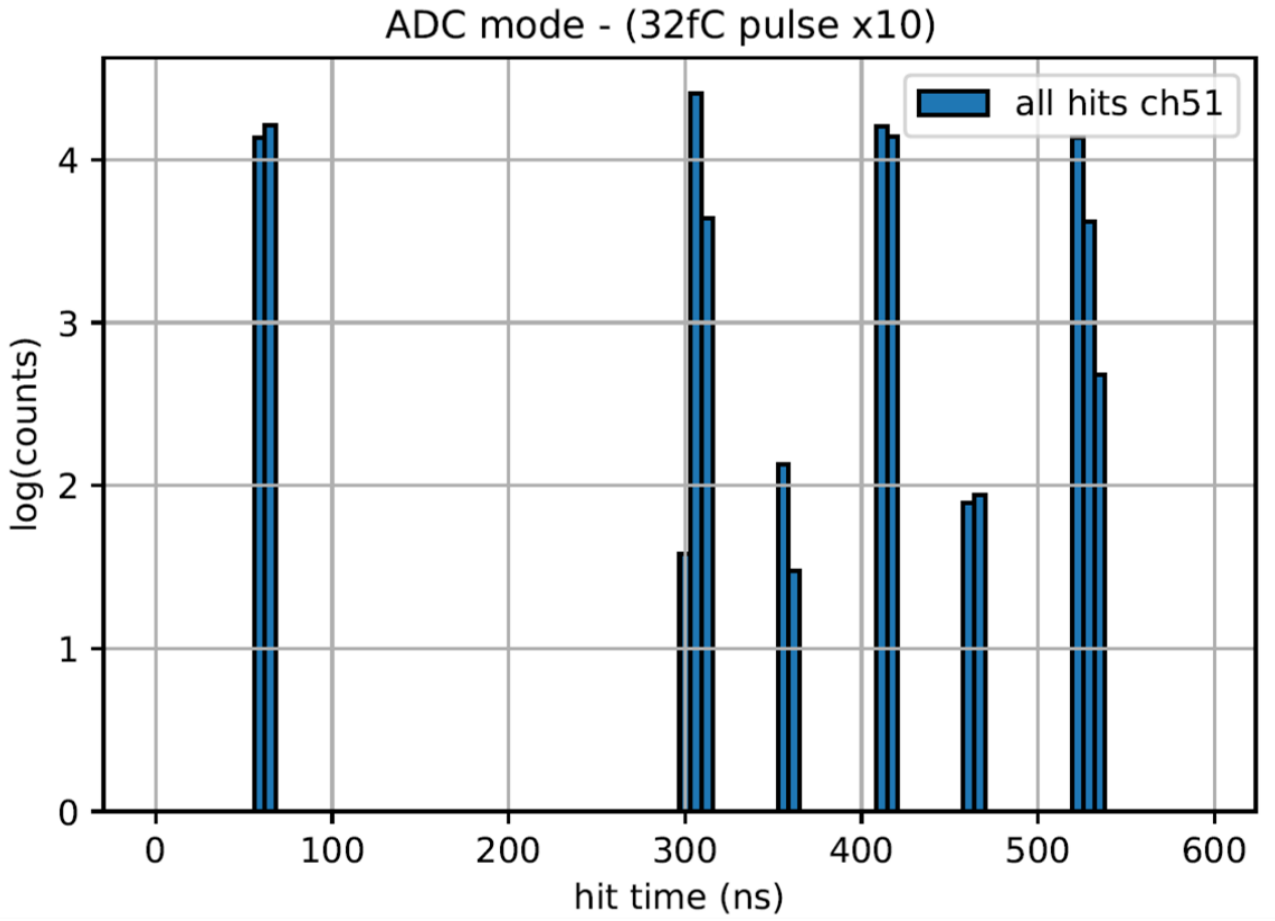

Waveform to pulser card
50
0
−50
−100
−150
−200
−250
−300
−350
amplitude (mV)
0
200
400
600
800
1000
time (ns)


Chan 51 - Fraction 2 hits vs pulse delay
ADC mode - 48fC per pulse
Fraction 2 hits
delay (ns)
0.0
0.2
0.4
0.6
0.8
1.0
0
20
40
60
80
100
120
140


Chan 51 - Fraction 2 hits vs pulse delay
ADC mode - 32fC per pulse
Fraction 2 hits
delay (ns)
0.0
0.2
0.4
0.6
0.8
1.0
0
20
40
60
80
100
120
140


Chan 51 - Fraction 2 hits vs pulse delay
ADC mode - 15fC per pulse
Fraction 2 hits
delay (ns)
0.0
0.2
0.4
0.6
0.8
1.0
0
20
40
60
80
100
120
140

VMM dead time pulser testing



VMM dead time pulser test 6 bit

- Dead time is :

25 ns (peaking time)
+
5 ns (peak finding)
+
25 ns data conversion
+
7 x 6.25 ns data transfer
=
~120 ns

Can go down to ~ 90 ns when using DDR (6.25 / 2)

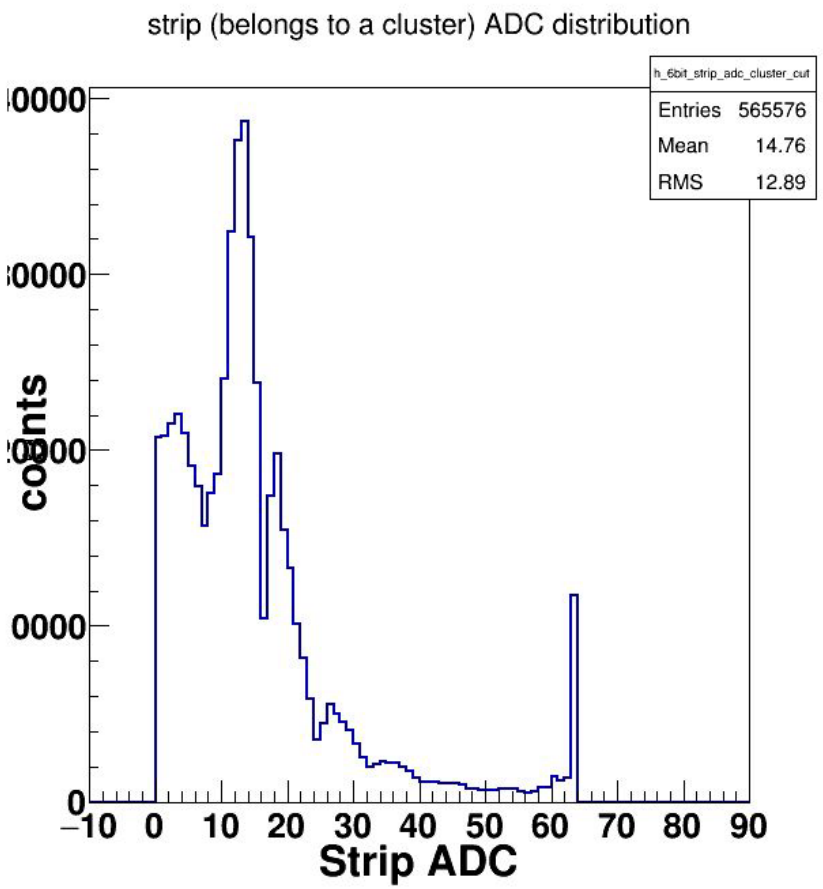
VMM dead time pulser test 10 bit

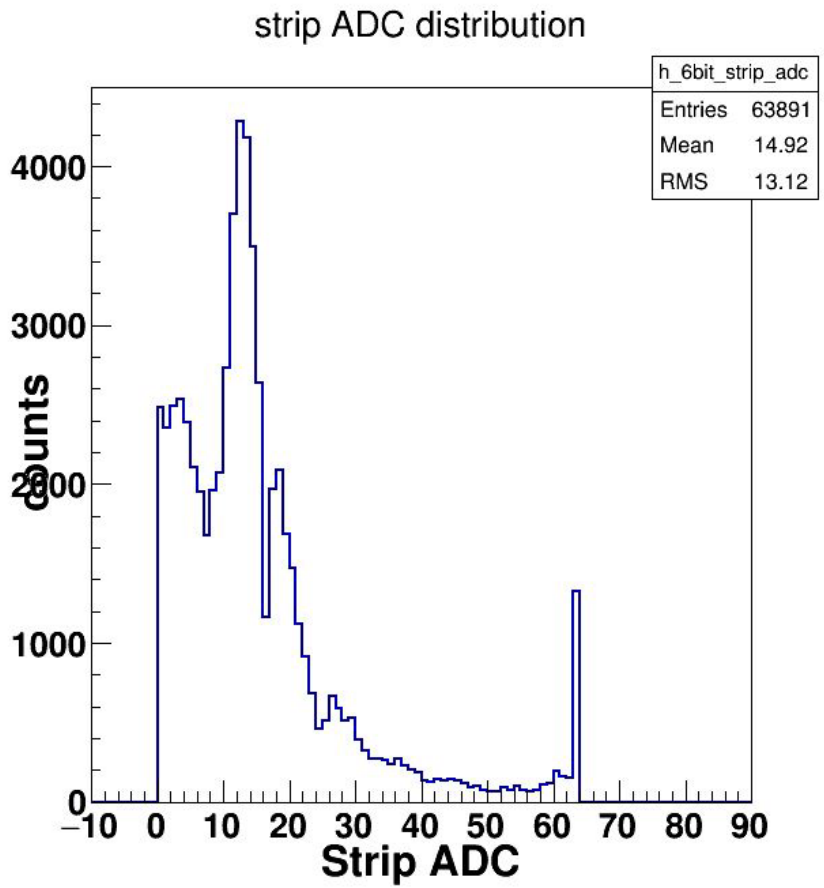
- Dead time is :

25 ns (peaking time)
+
5 ns (peak finding)
+
25 ns data conversion
+
7 x 6.25 ns data transfer
=
~120 ns

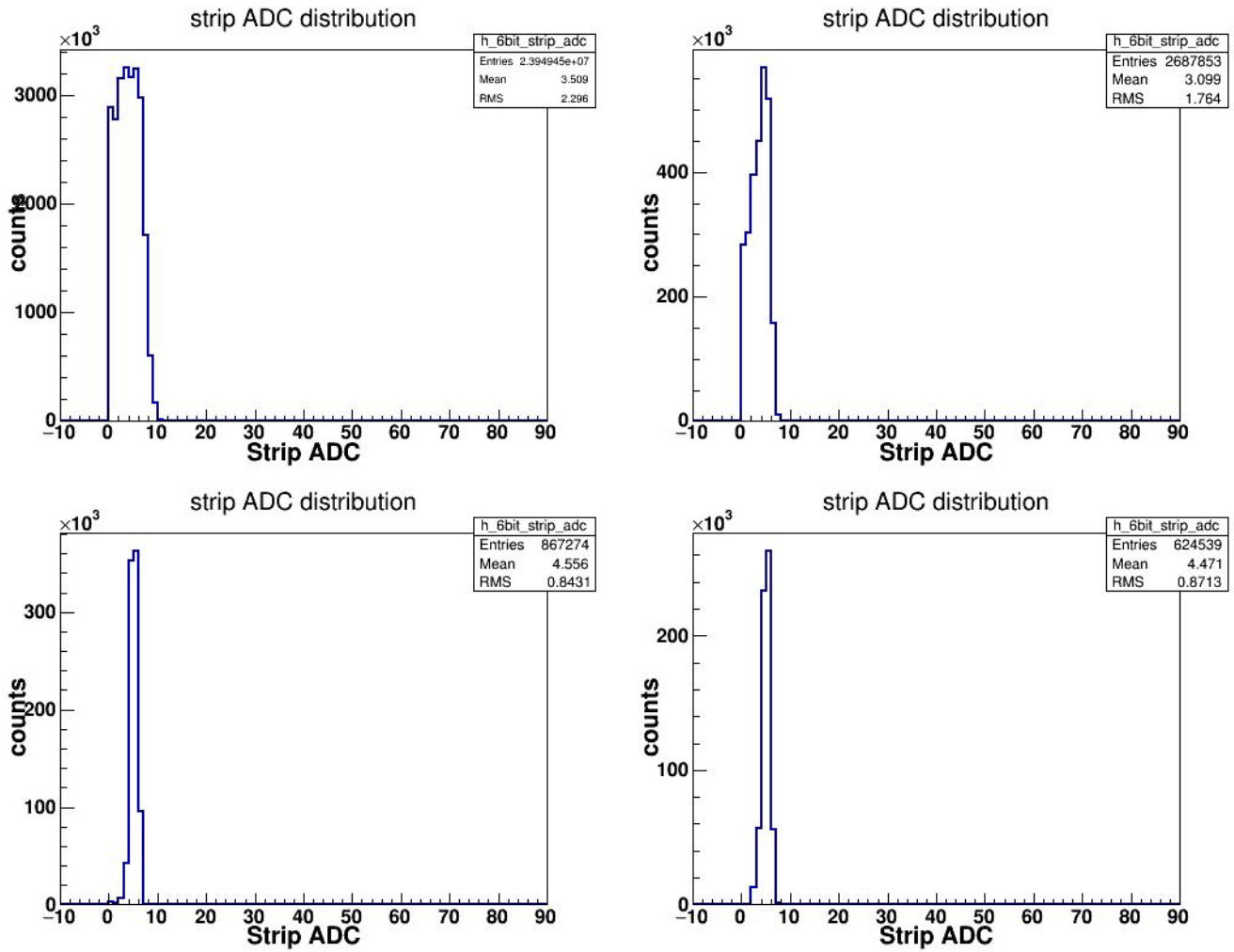
Can go down to ~ 90 ns when using DDR (6.25 / 2)

Sr90 VMM 6 bit 16mV/fC GEM at 4200 V

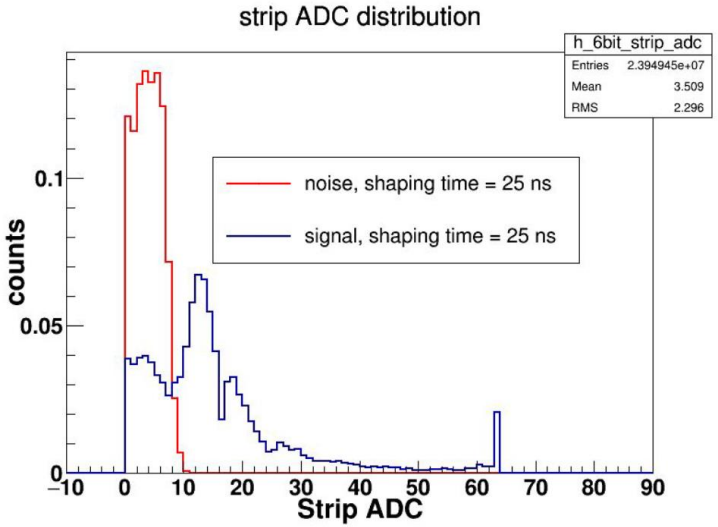


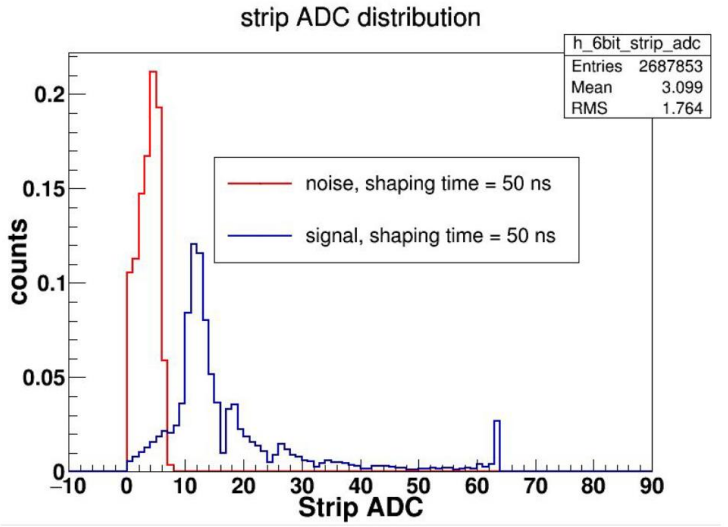


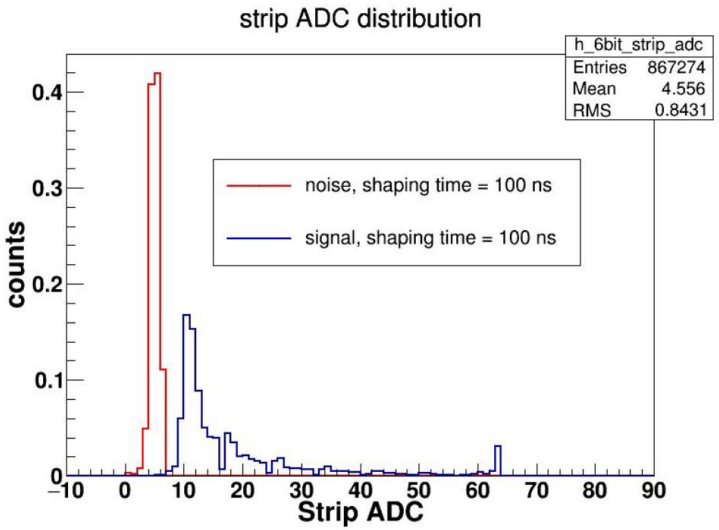
Noise 6 bit 16mV/fC

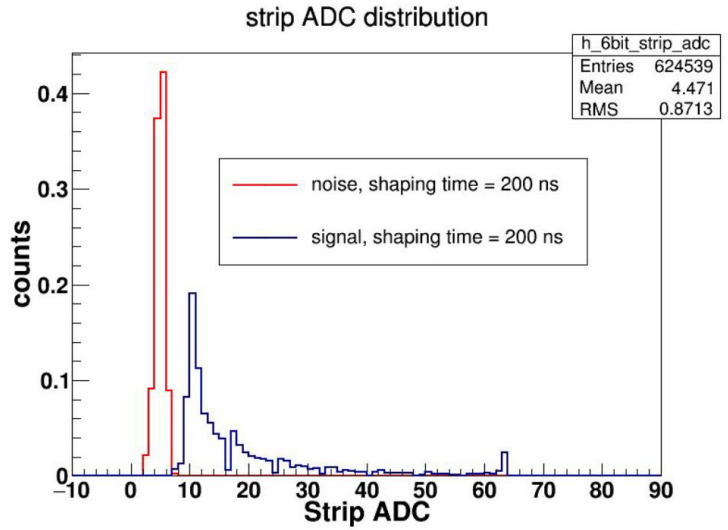


Noise 6 bit 16mV/fC Sr90





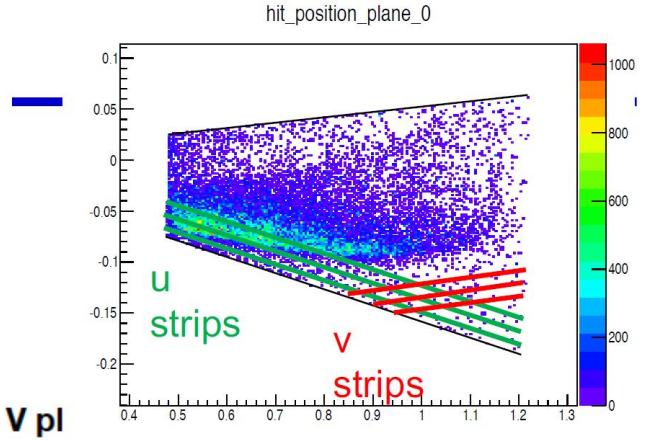




- Amplitude for MIP not change much
- Pedestal width dependent on peaking time

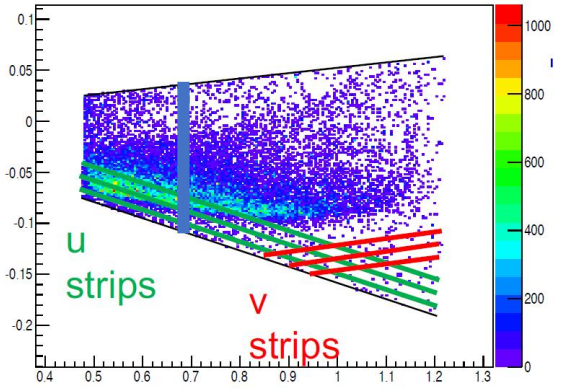
SoLID occupancy

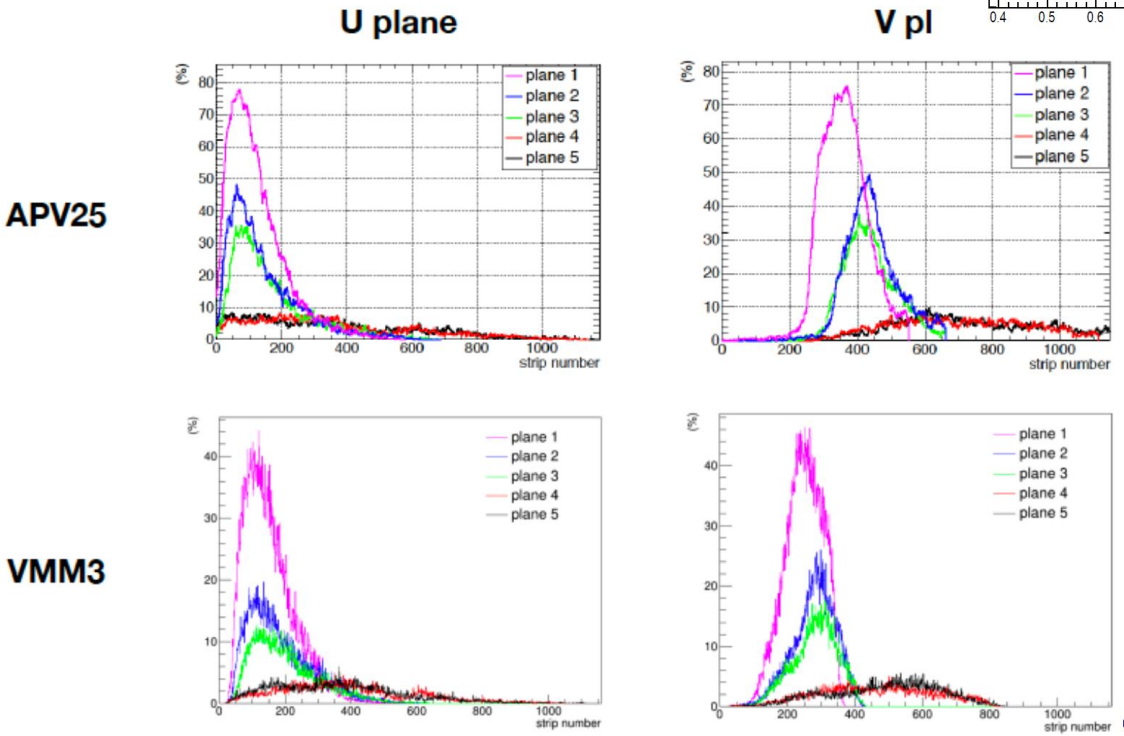
However, we need to be careful – SoLID occupancy is not uniform, hot-spots at small radius



Can lower occupancy with strip splitting ?

Or pixelized readout ?
Is material budget an issue





Conclusion VMM testing so far

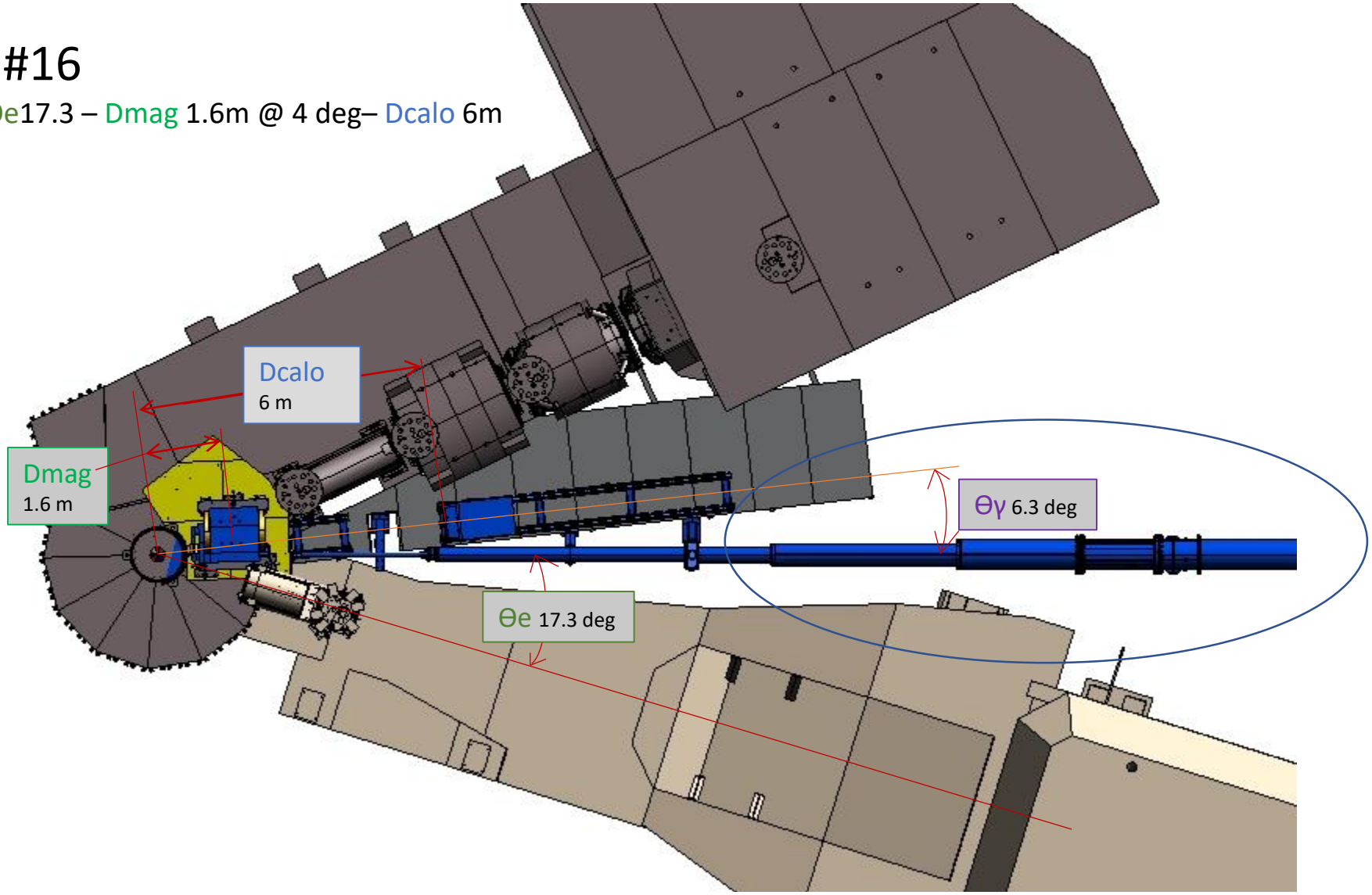
- 90 ns dead time in 6 bit mode
- Some noise seen in prototype
- Noise larger with decreasing integration time not clear 25 ns can be used
- MIP a bit low in dynamic range of 6 bit prototype at 4200 V (can we operate at higher HV ?)
- Implementing 10 bit to cross compare noise with evaluation board
- 250 ns dead time for 10 bit mode
- Setting up in ESB for cosmics
- Difficulties procuring the LV radiation hard parts

Test run

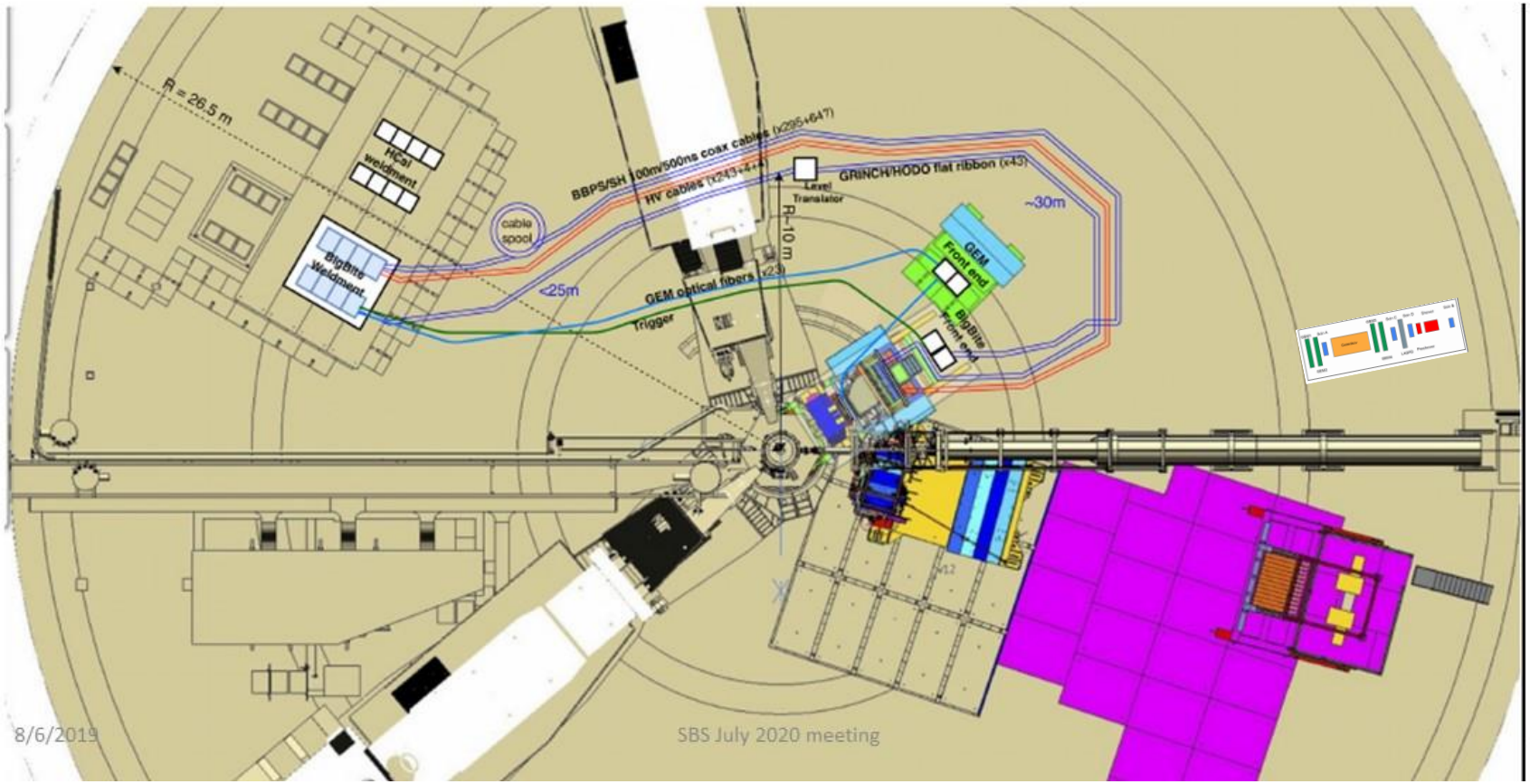
- Build small stand on wheels
  - Can move to any angle without tech support
- Roughly same detector stack as Ecal test run
  - 4 GEMs
  - ECAL
  - Small scintillators to define area for efficiencies and reduce photon background
  - Gas Cerenkov prototype for pion/e
  - Very high radiation rate at small angle

NPS Layout configurations(cont)

- DVCS #16
- Θγ6.3 – Θe17.3 – Dmag 1.6m @ 4 deg– Dcalo 6m



Hall Layout


R = 26.5 m
HCal weldment
BBPS/SH 100mV/500ns coax cables (x295+647)
HV cables (x243+44+4)
Level Translator
GRINCH/HODO flat ribbon (x43)
~30m
cable spool
R~10 m
BigBite Weldment
~25m
GEM optical fibers (x23)
Trigger
GEM Front end
BigBite Front end

Comparison of SAMPA and VMM3

SAMPA

- 32 channels
- Shaping time 80, 160 ns
- 10 bit ADC, 20 MHz ADC sampling
- Threshold zero suppression, Huffman coding
- Data transfer rate: 3.52 Gbit/s max
- Triggered or continuous mode
- Trigger latency up to 9.6 us
- Zero dead time – input channel rate limited by front-end current (35 nA; e.g. 35 fC at 1 MHz)
- Less

VMM3 direct output

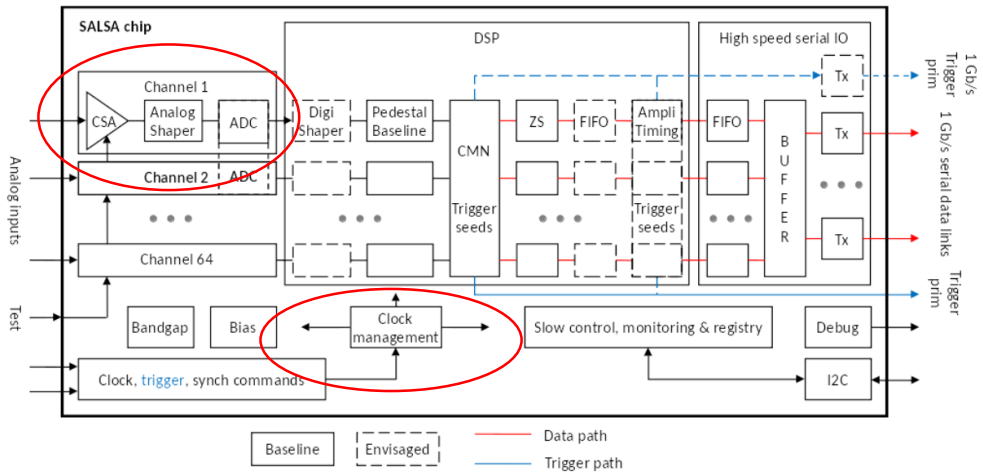
- 64 channels
- Shaping time 25 to 200 ns
- Selectable 6 bit ADC (peak), time over threshold output 160 MHz clock
- Latency up to 16 us
- On board zero suppression
- 320 Mbit/s x 64 -> 1 GBT link 3.2 GB/s
- Max rate per channel : 12 MHz
- Theoretical max trigger rate : 26 MHz
- 4000$ per wafer ~ 1$ per channel
- Radiation hardness ~ 100 MRad

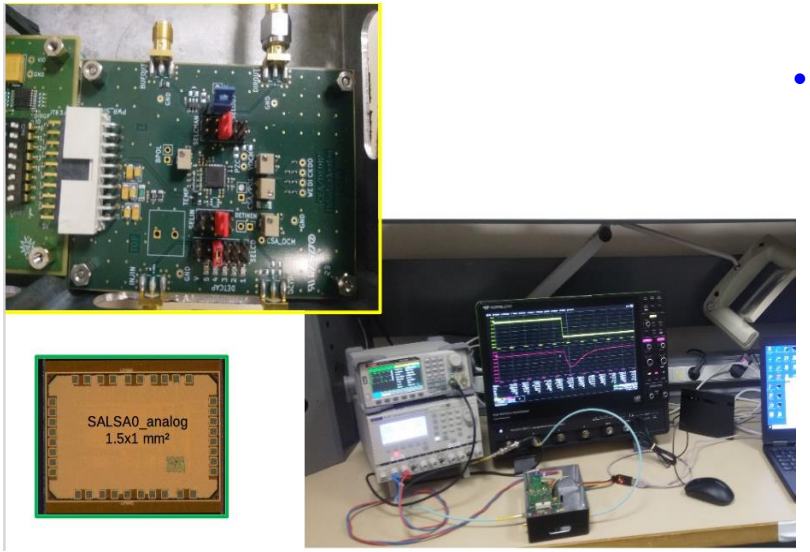
SALSA

- 64-Ch, updated design from SAMPA V5, migrating to 65 nm CMOS.
- Peaking time: 50 – 500 ns
- Inputs: Cin optimized for 200 pF; Dual polarity.
- FADC: 12 bits, 10 – 50 MSPS.
- Extensive data processing capabilities.
- Triggerless and triggered operation.
- Power: 15 mW/Ch
- Gbps links.
- I2C configuration.
- Preliminary target cost 2$
- Should be radiation hard

eRD109 – SALSA (CEA-Saclay, U. São Paulo) (F. Barbosa Streaming Workshop 2023)

MPGD





- 64 Ch
- 65 nm CMOS
- Peaking time: 50 – 500 ns
- Inputs: Cdin<200 pF; Dual polarity
- Rates: ~100's kHz
- ADC: 12 bits, 5 – 50 MSPS.
- Extensive data processing capabilities.
- Triggerless and triggered operation.
- Power: 15 mW/Ch
- Several 1 Gbps links
- I2C configuration

- ASIC Progress Summary:
  - SALSA0_analog and SALSA0_digital blocks submitted and received June 2023.
  - SALSA0_analog performance in agreement with simulation. Some stability issues traced to PCB residues.
  - DSP IP block design in progress.
  - PLL block submitted July 2023.

- SALSA0 (IP blocks): FY23 (June 2023)
- SALSA1: FY23 – FY24
- SALSA2: FY24
- SALSAf: FY25 – FY26
- SALSA: FY26

• Conclusion

- preRD allowed many developments
  - Tested in SBS and NPS experiment

- Capital equipement for DAQ to procure FADC, VXS crates, VTPs – can instrument about 1600 channels : can continue testing for experiments and beam tests
  - GEp5
  - HKS
  - Parasitic measurements

- VMM
  - VMM test with Eval board
  - Small amplitude variation with peaking time
  - Prototype board developed
    - Dead time measure 110 ns for 6 bit
    - Signal to noise marginal at 25 ns peaking time and 4200 V on GEM

- Test beam for VMM
  - Smaller stand
  - Hall A or C
  - Need to procure radiation hard low voltage components
  - Plan for September 2024
- SALSA option might come in time for SoLID