EIC-HPSoC - Project summary and response to reviewers

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10/30/2023

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Summary

"Design, Fabrication and testing of a multi-channel System on a chip for Low-Power High-Density High Timing Precision Readout ASIC for AC-LGADs (HPSoCv3)"

- Response to written questions
- General introduction to project
- First year performance summary and status
- Plan for continuation
- Further Q&A?

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ENABLING INNOVATION

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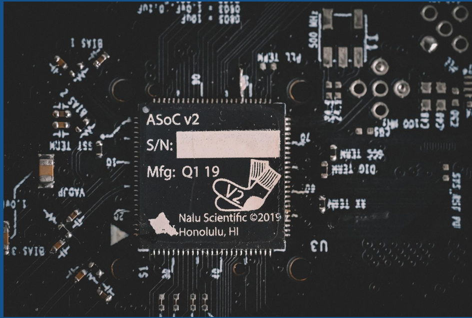

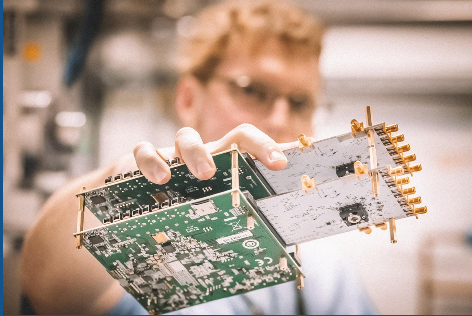

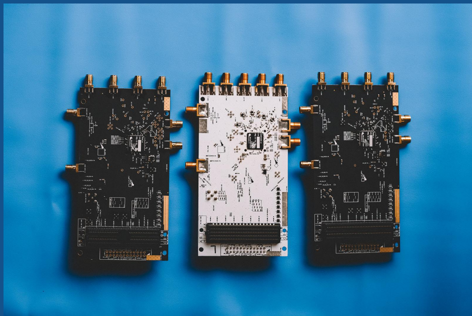

Fast Growing Startup in Honolulu, Hawai'i

Located at the Manoa Innovation Center near U. of Hawaii
20 staff members-diverse background
Access to advanced design tools
Rapid prototyping and testing lab

Technical Expertise

IC design:	Analog + digital System-on-Chip (SoC)
Hardware design:	Complex multi-layer PCBs
Firmware design:	FPGAs, CPUs
Software design:	GUI, analysis, documentation

Scientific Expertise - NP/HEP subject matter experts

Physicists (3x)
Electronics for large scientific instruments

Exclusive Distributor Agreement for North America

Sales of ASICs, eval boards
Enhanced OEM opportunities

Nalu = 'wave' in native Hawaiian language

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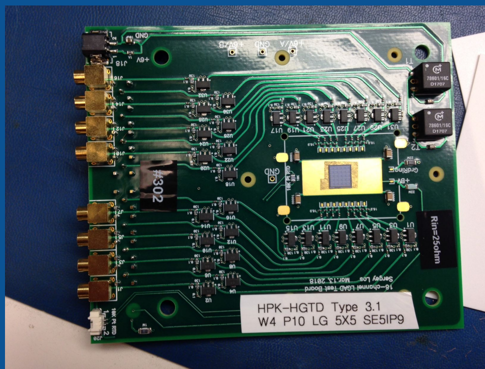

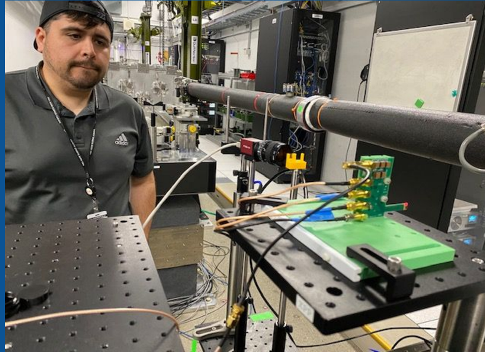

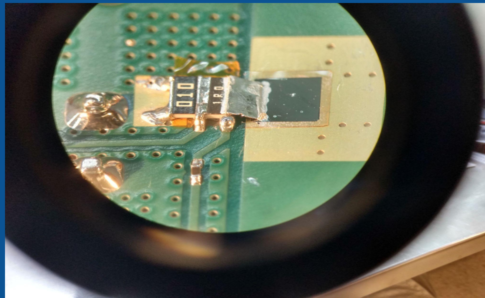

ABOUT SCIPP

The Santa Cruz Institute for Particle Physics (SCIPP) is

- A California state-supported research unit on the UC Santa Cruz campus
- Embedded within an AAU that is also minority-serving (one of only 5)
- Hosts research in Physics, Astrophysics, Life Science and Engineering
- Emphasis on Instrumentation

SCIPP Infrastructure

- Automated precision interconnect systems
- High-bandwidth (10+ GHz) test and measurement
- Benchtop characterization (Beta, alpha, fast-pulsed laser)
- Metrology and precision mechanics

SCIPP Capabilities

- TCAD simulation and sensor design
- High-speed detection systems
- Rapid prototyping
- Bench-test and test-beam based detector characterization
- Electronics design and characterization

SCIPP is internationally renowned as a driver of innovation in the field of nuclear instrumentation and its associated readout

List of Questions

1. How do you envision transition to application in an EIC experiment? What design and implementation steps would be needed?
2. How well did the waveform sampling and digitizing work in Tiny-HPSOC? Were substantial modifications needed for the next generation?
3. Test results are modest. Why only a few hundred events? Is it a trigger issue?
4. Why were the chip bonding issues limiting? Could you use other chips from the submission?
5. Was the power consumption as expected?
6. How will the HPSoCV2 be packaged? Is it intended to be bump bonded (direct bond), and if so, is there budget for this? Does the geometry match existing sensors? Is an interposer needed?

Additional reader questions received less than 2 weeks before the presentation:

7. How does the feature extraction work in more detail? dCFD? Any fitting?
8. Are there plans for patenting or protecting the intellectual property involved in the HPSoC's development?
9. The four-channel prototype will be performance tested in fall 2022. Has this happened yet?
10. Beyond the immediate scope of the EIC, are there potential applications for the HPSoC in other areas of research or commercial sectors?
11. Should this proposal be funded, what are the next steps, how long will they take, and what will be the requested budget to reach the final goal?

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Q1. Transition to EIC experiment? Design and implementation steps needed?

- The work done so far has been fully in view of the expectations for EIC performance requirements. We plan to continue working closely to keep abreast of EIC requirements and evolution (especially in terms of timing, detector geometry, interfacing).
- (Further) Steps as envisioned:
  a. Validate performance of combined amplification/digitization with realistic sensor/sensor arrays.
  b. Prove multi-channel readout performance with 4 channel and then fully integrated 9 channel (this project)
  c. Scale up to larger array and investigate packaging/sensor integration schemes (see below)

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Q2. Waveform sampling and digitizing work in Tiny-HPSOC and modifications?

- First revision of HPSoC (pre-EIC/JLAB involvement) could not be tested as-is:
  - Issues with power shorting on chip - recently linked to wire-bonding issues
  - Design probed and elements modified, expected performance verified in simulation
- HPSoCv2 fabricated during FY23, performance testing
  - Final layout submitted June 2023
  - Chip received Sep 2023
  - Board fabrication completed
  - FW development completed recently (last week)
  - One issue identified in design prevents full evaluation - see below for corrective measures
  - Testing in progress:
    - Validating main components:
      - Sampling array, ramp generator, conversion counter, comparator
    - Full performance estimator (based on experimental results) being developed.
    - Correction of issues completed and design ready for re-submission (expected end of November)

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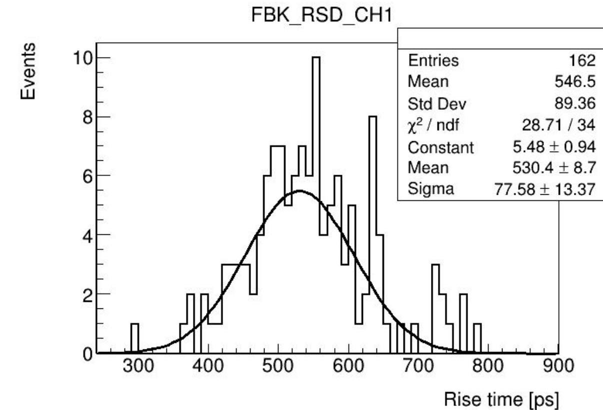
Q3. Test results are modest. Why only a few hundred events? Is it a trigger issue?

If referred to the graph presented in proposal:

- The prototype nature focused on functional fundamentals and initial prototyping in an advanced technology also prohibited the ability to do large sample size automated data taking and statistical analysis
- Data taking for this specific effort was performed as the last part of a SBIR grant in 2021 with limited time available at SCIPP
- Experimental setup was complex:
    - Original plan required use of external buffer that proved to be unstable
    - Data needed to be taken with hand-held scope probe
- Within EIC/JLAB2022 project better probe attachment was included in design - larger data set has been collected (Data in the order of 5000 events used for most recent evaluations)
- In principle new internal trigger implemented in HPSoCv2 (not available with reported data) could be used to facilitate acquisition.



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Q4. Why were the chip bonding issues limiting? Could you use other chips from the submission?

From report: “Only two of the chip channels produced usable data; issues in bonding with the other two channels precluded data-taking with them.”

- Stemmed from the re-use of a previously bonded chip in this set-up. Current evaluations are based on HPSoCv2 and largely supersede previous results.
- Some issues were connected to what is believed now to be a bonding issue (detailed below)

Q5. Was the power consumption as expected?

- Power measurement results on revision 1 (HPSoCv1) were problematic and higher than expected, with unexplained variations between dies. It is now believed that this was an effect of shorts or low impedance paths with wirebonding too close to seal ring conductive structure we identified on revision 2.
- After proper digital configuration and operational setup, power numbers from HPSoCv2 are closer to expected (measured ~24mA for 4 full sampling channel and 5 TIA input stages)
    - Comparator consumption control is critical to keep power to a minimum - nominal settings are used for those numbers
    - Some small adjustment of power possible within TIA/Trigger circuitry - under investigation

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Q6. HPSoCV2 packaging. Bump bonding? Budget for this? Geometry match existing sensors? Is an interposer needed?

- HPSoCv2 (result of previous year effort) was manually die bonded to evaluation boards (calibration and input sensors) by SCIPP personnel, as part of this year's performance
- The next revision (e.g. HPSoCv3 - this proposal effort) will be a larger design (9 channels) with all-included digital control and is expected to be also manually wire-bonded for its evaluation.
    - Redistribution layer is possibly within this technology that allows for bump bonding, but that is also out of proposed budget.
- Analysis of data from v2 and v3 and experiments with different types of sensors (pixel-based, strip-based) will guide the design of the next revisions and the expectations for interfacing (not necessarily limited to bonding) needs. We are looking at different types of sensors including both pixels and strips consistent with EIC's on-going R&D into optimized sensor geometries.

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Q7. How does the feature extraction work in more detail? dCFD? Any fitting?

- The feature extraction mechanism designed and laid out (not implemented in fabbed silicon) during the previous phases of the project is the simplest mechanism:
  a. Use single pass analysis of waveform and estimate crossing position (multiplication and division operation included)
  b. During same single pass perform Riemann approximation of charge with sum of voltage over threshold
- Design was performed mostly to estimate the single channel area requirements - for HPSoCv3 the plan is to use a cost/benefit analysis to study/implement possible variants of the following:
  a. “Digital” CFD through a 2 pass algorithm:
     i. First pass in channel with bracketing of data after calculation of peak.
     ii. Second pass in common cross channel logic with proper threshold validation and use of bracketed data - “complex’ operations (multiplication, division, timing calibration) will be shared among parts
     iii. Medium computational cost (dependent on sharing/rate limitations) - medium performance
  b. “Traditional” analog-like CFD - single pass:
     i. Subtraction between waveforms with different gains and delays
     ii. Simpler implementation (no need for multiply/divide, single pass possible)
     iii. MC simulations show similar performance to “Digital” CFD
     iv. Advantage: simplicity of implementation - disadvantage: potential dependency on signal shape/ shape variability.
  c. Template-based fitting:
     i. Initial peak bracketing pass as in a
     ii. Limited cross-correlation curve with small sample shifts w.r.t. Template. Maximum extraction.
     iii. Advantage: quality of fit implicit (could be used for finer data fusion) - Drawback - computational cost/large sharing between channels (reduced overall hit rate)
- Digital designs in 65nm are very compact and we currently have a reasonable amount of space for adapting

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Q8. Are there plans for patenting or protecting the intellectual property involved in the HPSoC's development?

1. Nalu has received two US patents for its underlying ‘activity detection and waveform digitizing microchip’ designs from previous DOE funded SBIRs.
2. HPSoC development requires design variations to cover density, power and performance needs. Such designs will allow for additional IP filings. Nalu team will seek funds from future FOAs or private sources to protect the IP. Government rights and ownership will apply.
3. UCSC has mostly been involved in sensor integration, testing and support via data analysis which generally create publishable knowhow, but not much IP.

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Q9. The four-channel prototype performance testing happened yet?

As discussed above - overall testing results discussed later:

- Final layout submitted June 2023
- Chip received September 2023
- Board fabrication completed
- FW development completed recently (last week)
- Analog components (TIA and trigger):
  - Calibration results available (some tuning needed)
  - Initial sensor results collected are being analyzed
- Digital design probed
  - internal delay line and timing generation verified
  - Internal conversion clock and counter tested (one issue found and addressed)
  - Sampling array validated
  - Full conversion problem identified - possible path for testing charted and in execution

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Q10. Beyond the immediate scope of the EIC, are there potential applications for the HPSoC in other areas of research or commercial sectors?

- Well suited to 4D tracking systems that will be required for reliable pattern recognition at next-generation colliders (e.g. FCC).
- Tight integration with high timing and spatial resolution sensors beneficial to applications in
  - High frame rate X-ray cameras (e.g. Fusion research)
  - Synchrotron radiation applications - x-ray diffraction in the low keV range
  - Medical imaging (i.e. Ion beam therapy, proton computed tomography (pCT))
  - Dosimetry
  - Homeland security

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Q11. Should this proposal be funded, what are the next steps, how long will they take, and what will be the requested budget to reach the final goal?

- The scope of this proposal is limited to the development of a fully operational version of HPSoC incorporating all analog/mixed signal and digital components required for the full scale chip. Compared to the final device:
  - Expected to cover a basic “tile” of 9 channels with hooks for multi-tile connectivity, communication
  - Manually bonded sensors will be used
  - Fully functional and modular. Performance is expected to be preserved.
- Full design will require:
  - Extensive experimentation with individual tiles
  - Combination of tiles and channels with FPGA resources and eventually on-chip integration
  - Prototyping with larger tile size
  - Investigation of final bonding methodology (wire bonding/interposer choice - please see below for a cartoon view).
  - Expected time to completion (e.g. readiness to engineering/production runs): 1.5-2 extra years.
  - Funding required for high level integration (engineering), fabrication costs (fixed - dependent on size), and bonding (e.g. dependent on bonding requirements) is in the order of ~$500k

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HPSoC - concept and target specs

- State of the art photodetectors (e.g. LGADs) -> excellent spatial and timing precision.
- Limited by existing readout electronics.
- Time-to-Digital Converter (TDC) and time-over- threshold (TOT) readout limitations:
  - Indirect estimate of integrated charge,
  - Limited sub-pixel spatial resolution
  - No correction for pile-up,
  - Sensitivity to sensor aging (radiation)
  - Time errors (timewalk, baseline wander, and waveform shape variations).
- Use full waveform information would solve all issues, but:
  - Expensive in area/power
  - Too large data BW required
- Proposed solution: HPSoC:
  - Full WaveForm Digitization **(WFD)** per pixel,
  - On-chip feature extraction
  - On chip data fusion (sub-pixel spatial resolution)

Parameter	Specification	Comment
Channel no.	100+	(pitch 300-500 µm)
Sample rate	10 GSa/s	
Bandwidth	2 GHz	
No. bits	10	
Supply Voltage	1.0V	2.5V for digital I/O
Timing accuracy	5ps	With calibration
Front-End stage	Embedded TIA	Optimized for AC-LGADs and other fast sensors
Analog buffer length/channel	256	Effectively operating with a 2 banking system to allow for bursty signals
Power/channel	2mW	Trade-off with integration
Integration	System-on-Chip	Digitizer. Feature Extraction, data fusion

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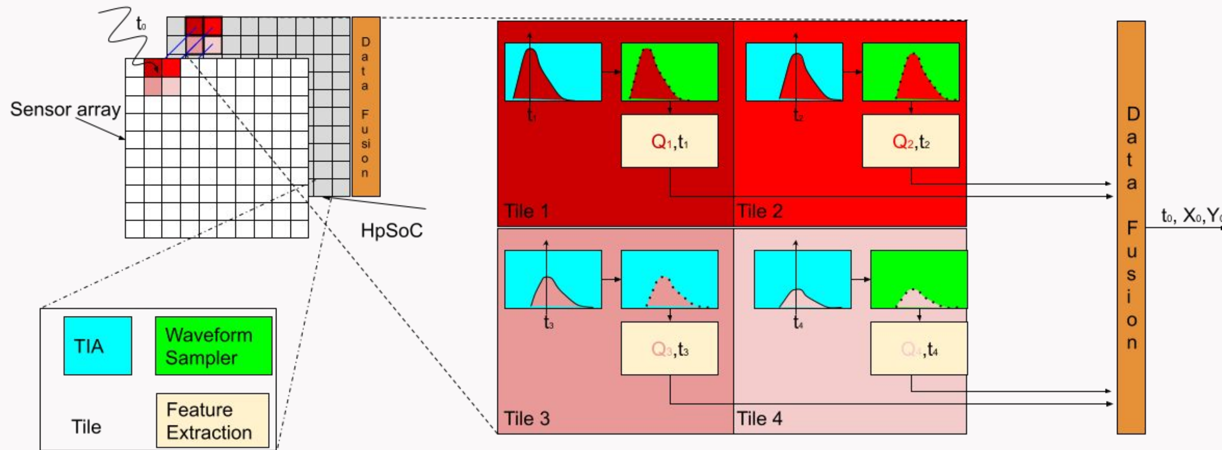
Target Structure

1. Dense sensor array readout (target of ~300um pitch)
2. Modular, independent ("tiles"), per pixel
3. On chip signal amplification (TIA+gain)
4. Continuous waveform sampling and triggered digitization - "ping-pong" operation to avoid deadtime.
5. On the fly timing and amplitude (charge) extraction
6. "Data fusion" and export.



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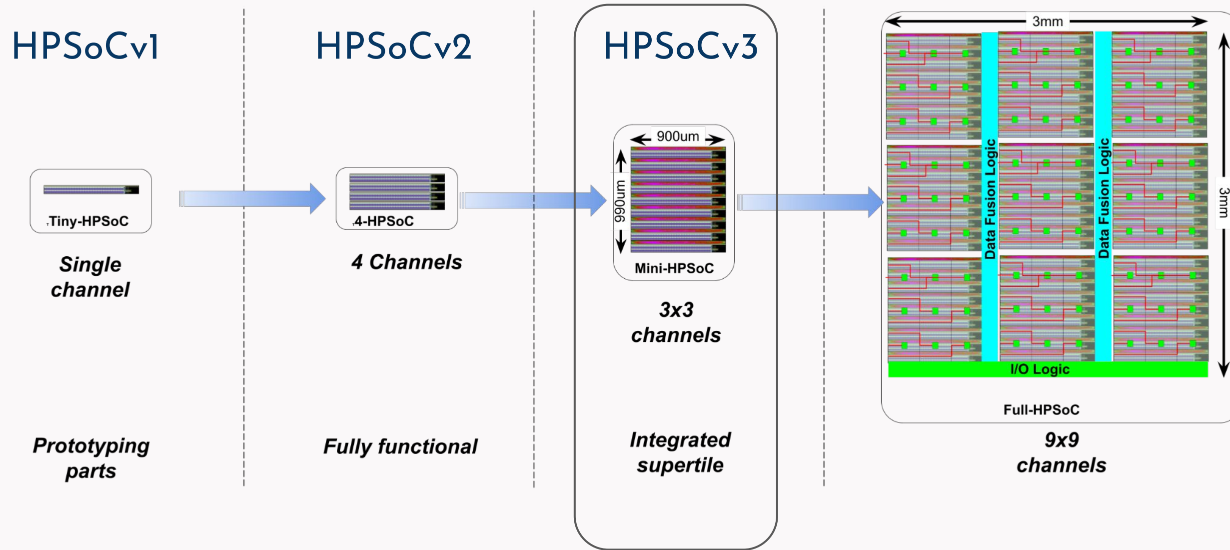
Overall Project Plan



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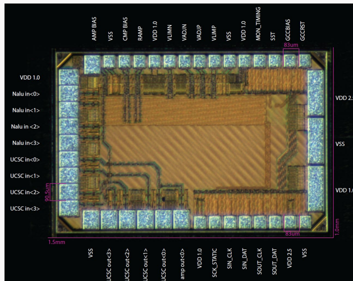
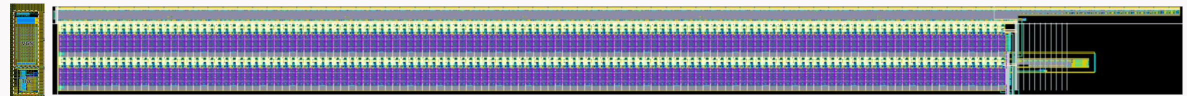
HPSoCv1: channel-level layout

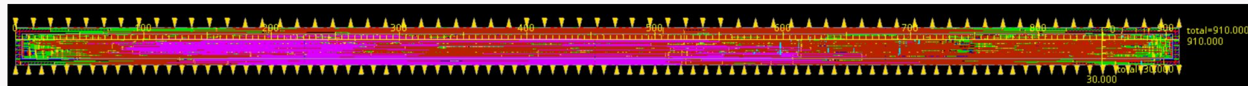
- Front End amplifier - composed of a TIA and gain stage - fabricated and extensively tested by SCIPP
- Sampling array and conversion logic: 3 different versions incorporated in fabricated chip - ready for testing (some supply issues need to be addressed before full evaluation possible)
- Digital control: fully placed and routed design to permit area/power estimation (NOT in fabricated chip):
  - control for channel,
  - readout of digitized data
  - preliminary logic for feature extraction
    - Thresholding (on digitized data) -> for time of arrival estimation
    - Integral over threshold -> for charge estimation



“Tiny-HPSOC” - 1.5x1mm^2 for part prototyping



Front end amplifier and channel layout - approximate size: 900um x 80um for 256 samples.



Fully placed and routed channel control - dimensions are 900x30um^2, including power rails.

HPSoCv2

- Incorporation of 4 channels with independent triggering, self digitization, and improved TIAs based on the result of the previous experience.The main outcome for the FY22 effort was the second version of prototyping channels, along with calibration and sensor test results, of the **full four-channel prototype HPSoC chip**, which implements
    - (a) an **optimized front-end design** informed by the testing results from the initial prototype chiplet,
    - (b) a **full digitizer**,
    - (c) on-chip **autonomous operation**,
    - (d) An evaluation **test board**(s) has been designed and fabricated to permit testing **with EIC-specific prototype LGADs** sensor(s) as well as **calibration signals**.
- The fabrication is finished and the testing and evaluation is being completed now

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HPSoC prototype 2 features

1. 4 channel device
2. Each channel has an optimized front-end with improved TIA performance targeted at AC-LGAD readout
3. Each channel has a waveform digitizer (128x2 samples) following the gain stage:
   a. Digitization at 10 Gsps
   b. Number of converted bits: 10
   c. Note that the original plan had a single group of 128 samples - this was doubled to permit testing of the ping-pong feature to reduce deadtime.
4. Channel can operate independently (i.e. does not require external electronics to perform the digitization)
5. Extra Independent TIA
6. One channel (number 3) has direct access to the digitizer to test its performance independently of the TIA (original plan had a single separate channel, but the adoption of the 2x128samples made it impossible to fit in the allotted space and fabrication budget.

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HPSoCv2 Analog parts

- TIA: objectives:
  - Improve SNR - mostly gain and possibly noise shaping (use signal templates for simulations).
  - Improve input resistance (TIAv1 quite high)
  - Results -> substantial reduction of input resistance (<250ohm DC, ~50 ohm at pulse BW) - adequate gain bandwidth, expected jitter ~10ps, partially controllable/programmable gain
- Ramp Generator:
  - Explored architectures (through simulations):
    - Simple mirror (default/baseline)
    - Cascode mirror
    - Low overhead cascode mirror
    - Triple cascode -> chosen
  - Match with input - rising - channel with 0-0.6V range
  - Need distribution? -> Single ramp per channel - relatively limited number of samples load (256)
- Triggering system:
  - Very simple first attempt - unsuccessful triggering for fast LGAD output.
  - Self-threshold set-up with sensitive 3 stage differential pair architecture -> targeted for expected signal polarity

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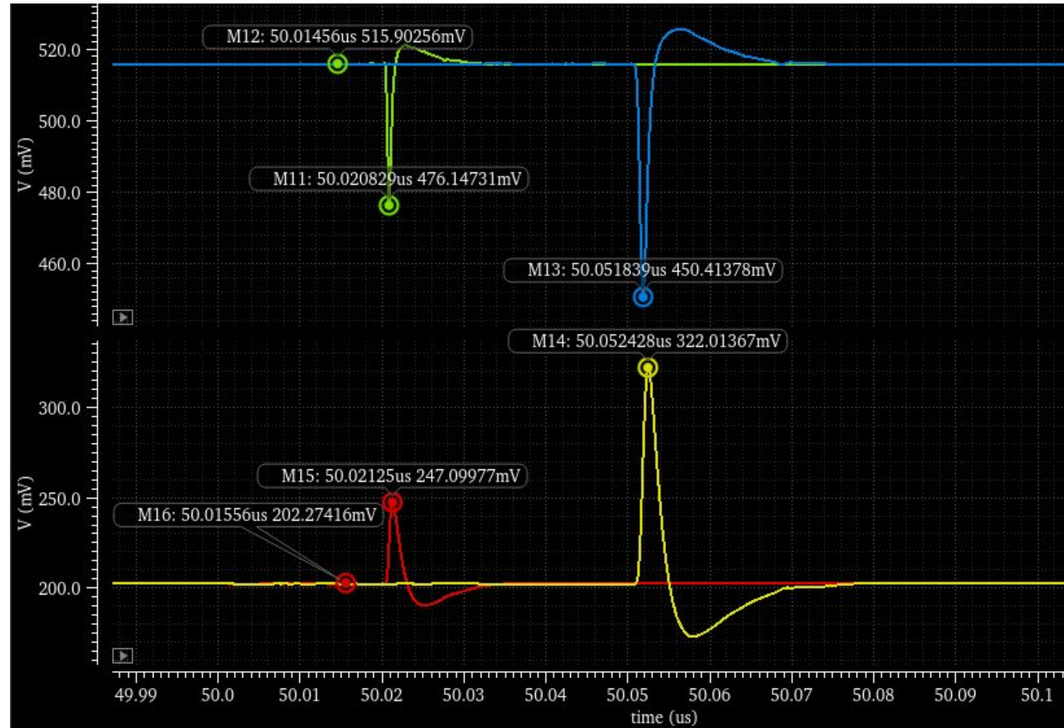
HPSoCv2 TIA simulations including parasitics effects

20um LGAD:

- Risetime(10-90%):450ps
- Peak: 45mV
- Noise upper bound=1mV
- Jitter = 450/45)*1/0.8=12.5ps (v1->13.5ps)

50um LGAD:

- Risetime(10-90%):850ps
- Peak: 120mV
- Noise upper bound=1mV
- Jitter = (850/120)*1/0.8=8.85ps (v1->12.5ps)



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HPSoCv2 Digital Control

- Dual operation:
  - “Manual” - with external control of digitization and readout (and Banking control)
    - to facilitate testing of low level features of digitizer
  - “Automatic”:
    - Uses a trigger to: 1. Switch sampling to secondary bank if not in use 2. Perform full window (128 samples) digitization. 3. Export data using serial interface.
    - Trigger can be external (all channels) or internal (individual discriminator).
- Entire design placed and routed by hand to guarantee symmetrical routing for the timing critical bank switching.

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HPSoCv2 - Submitted design

Full I/O ring to avoid ESD issues

Verification and rule checking complete

1mm

1.5mm

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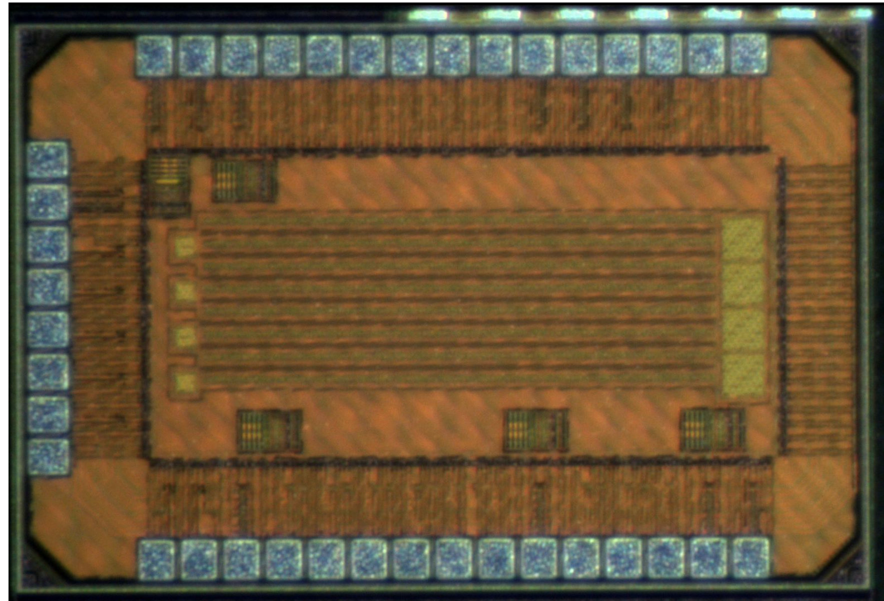
HPSoCv2 - Fabricated chip

Fabrication and shipment on time (~1 week later than expected)

80 chips delivered - 9/01/2023

1mm



1.5mm

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HPSoCv2 - Test Board design

Onboard (Si5341) or external clocking

Support for 2 types of FPGA connections

Ability to bias SCIPP AC-LGADS

Direct board bonding for IC, sensor

Ability to either supply power independently or onboard from derived rails

Mechanically compatible with SCIPP test and beam equipment

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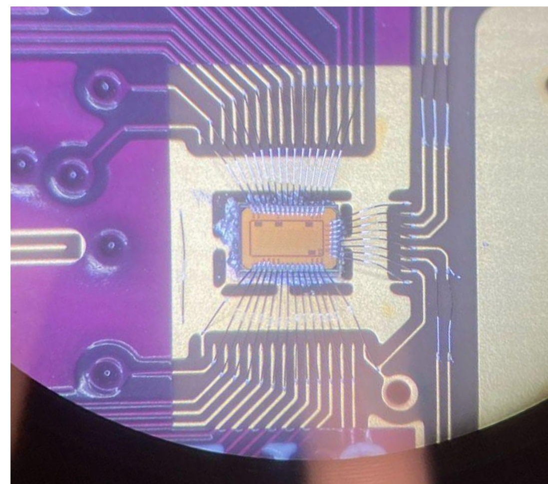
HPSoCv2 - Final test board

The test board was sent out for fabrication on 09/14/2023

Features:

- Layout for Sensor and HPSoC attachment:
  - Fiducial mounting
  - HV distribution
  - Cage fixture for sensor/readout chip complex to reduce RF interference and EMI
  - Minimized additional board/trace capacitances and facilitate wire bonding
- Digital interface signals direct mapped to I/O pin on FPGA connector, for maximal flexibility
- On board clock generation for low jitter timing reference
- Attachment for high input BW oscilloscope probe for separate TiA testing.
- Dual option for FPGA control:
  - Ribbon cable connection for external attachment
  - DIP connector for mini-FPGA board with simple USB cable to minimize connectivity
- Mechanical design compatible with insertion in irradiation setup (SCIPP)



Specs:

ENIG plating and 0.78oz outer copper weights for compliance with Aluminum wire bonding

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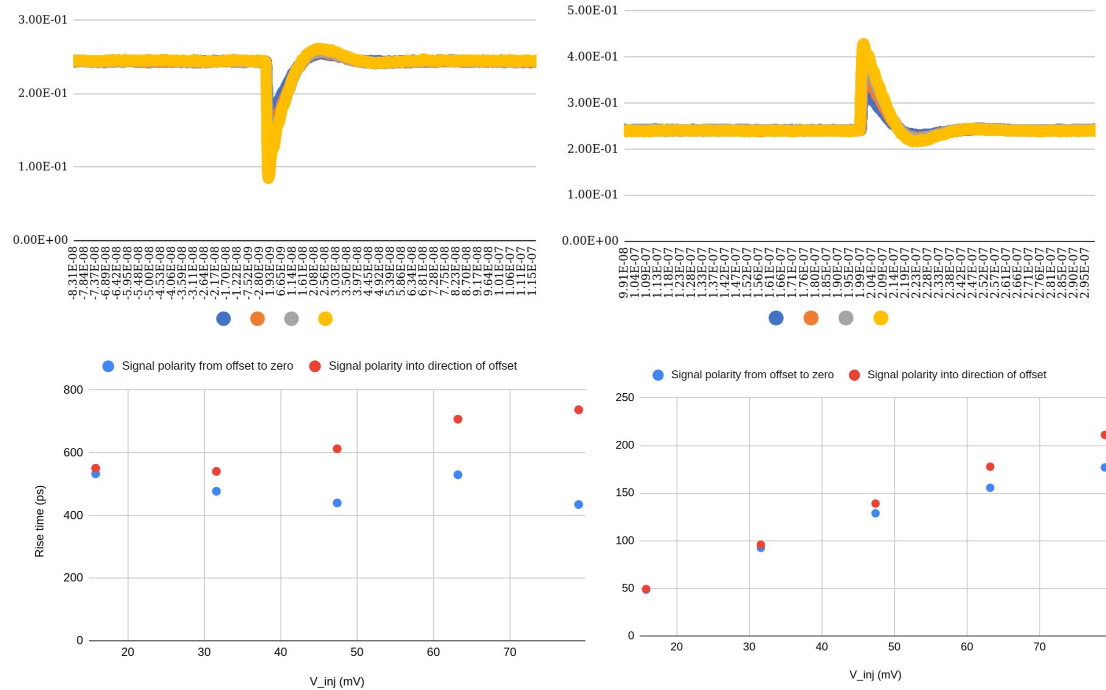
HPSoCv2 - Preliminary TIA Results - calibration signals

- Signal step of different amplitudes applied to a small series capacitor (0.5pF) -> effective charge injected 10fC to 35fC
- Peak output amplitude ~6mV/fC
- Rise time ~500-600ps



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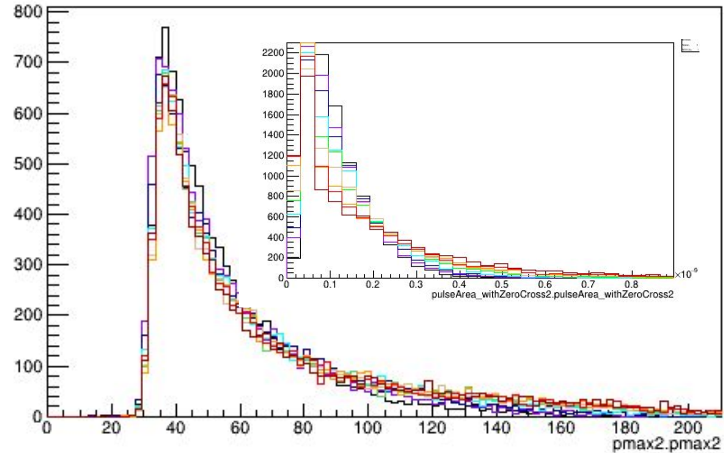
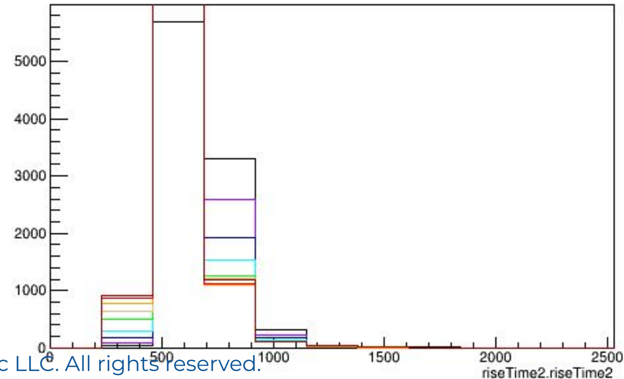
HPSoCv2- Preliminary TIA Test Results - sensor inputs

- Beta Source excitation
- 50-um HPK AC-LGAD sensor, 450 um pad size
- Data from oscilloscope, Self-triggered (Threshold ~20 mV above baseline)
- Peak mode at ~40 mV
- Rise time ~500-600ps
- Current time resolution of ~15ps (with ~1.5mV noise as measured)
  - Some fine tuning required
  - Use of full waveform expected to improve estimate





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HPSoCv2 - Preliminary Digitizer Test Results

- Internal delay line (generation of timing signals):
  - Properly adjustable delay with external biases - initial set point found for nominal 10 Gsps sampling
- Internal conversion clock generation and counter:
  - Adjustable clock from external bias
  - Identified issue with additional loading that reduces conversion speed:
    - Simple buffering introduced for revision to avoid effect.
- Comparator behavior under testing:
  - Power dissipation dependent on proper biasing
  - Nominal value corresponds to close to minimal biasing
  - Initial evaluation of nominal bias with individual sample
- Ramp testing
  - In connection with Comparator - nominal speed ~1 us ramp for full range.

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HPSoCv2 - Preliminary Digitizer Test Results - continued

- Full internal conversion:
  - Identified functional bug in joint control of ramp and counter
  - Makes impossible direct conversion in present chip
- Corrective measures:
  - Bonding of generation I board to evaluate conversion
    - Previous tests inconclusive due to recently identified short with wire bonding.
    - Same channel structure present, can be tested properly
  - Re-submission of “tiny chip” with bug correction:
    - Booked next available round (November 2023)
    - Already generated GDS for fabrication

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HPSoCv2 - Preliminary Digitizer Test Results - continued

- Alternative testing for accuracy/sampling still possible and underway:
  - Individual comparators can be accessed and evaluated
  - Measuring external delays from ramp start to comparator edge used to generate a proxy of conversion
  - Can repeat most initial tests for conversion accuracy and synchronous signals
- “Pedestal” acquisition
  - Feed a DC value on input and measure conversion accuracy
  - Scan DC values and perform voltage calibration
- Synchronous wave acquisition
  - Feed a perfectly synchronized waveform with sampling reference
  - Convert one sample at a time and synthetically reconstructs the waveforms with multiple acquisition - i.e. acts as a sampling oscilloscope
  - It effectively can capture most of the imperfection of the conversion

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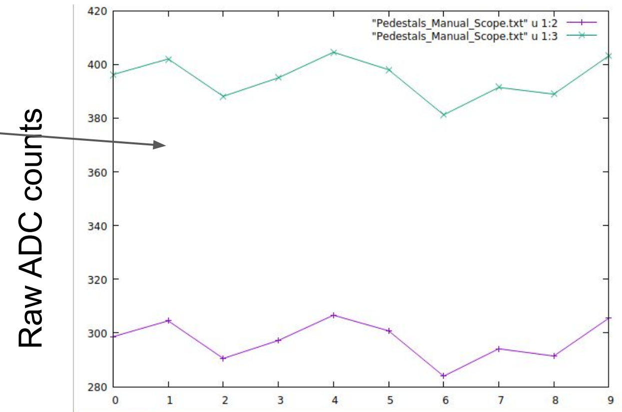
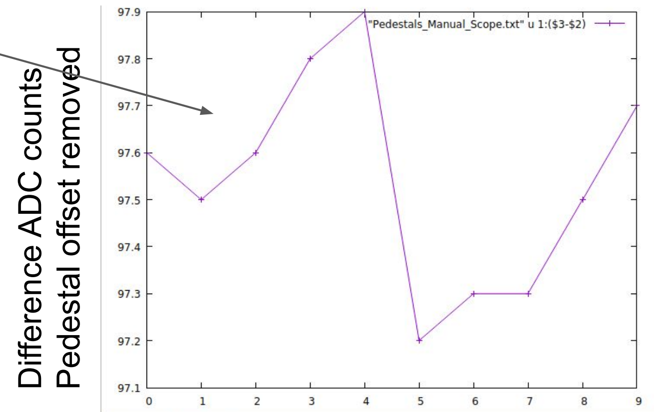
Pedestal Acquisition and subtraction

- Digitized DC inputs at 300mV and 400 mV
- Using the 300mV acquisition as an offset reference and correcting for it, the 400 mV acquisition is within 1mV of 400mV, as expected
- The acquisitions RMS are recorded (over 100 events) to be between 1.3 and 1.6 count RMS





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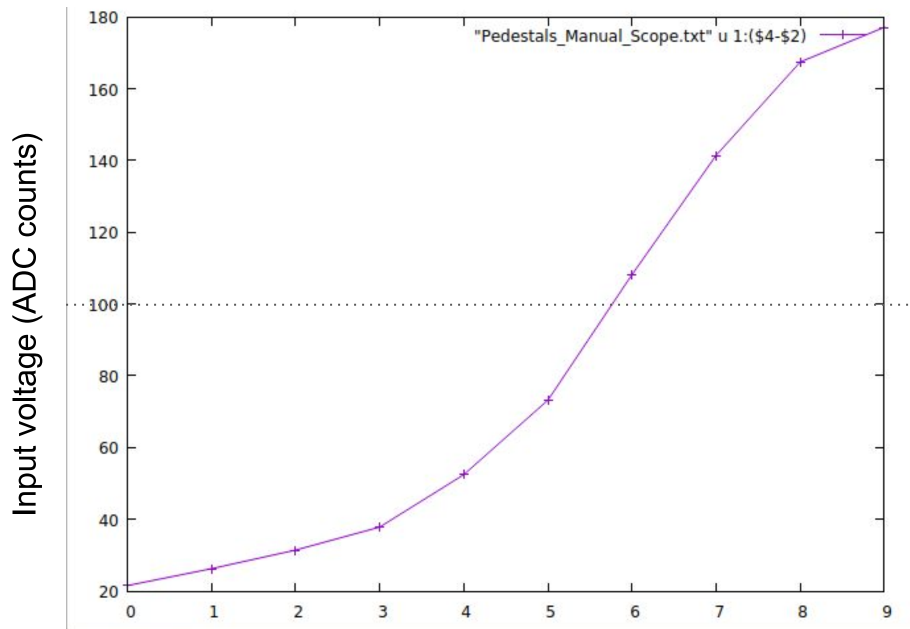
Synchronous signal conversion

- Using multiple acquisition on a tightly synchronized signal:
  - Copy of reference clock guaranteed to be within <1ps from reference clock
- Edge clearly defined - error on voltage estimation within 2 counts - 2 mV
- Cross timing estimation to within **<u>5 ps</u>** on edge only.



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Proposed work

WBS 1. Analysis and high-level design of SoC features: Based on HPSoCv2 prototype measurements, trade-off between performance and computational complexity. Identify existing weak points in the analog implementation and corresponding corrective measures.

WBS 2. Design of the HPSoCv3 9 channel module ("mini-HPSoC"): Design and implement an optimized nine-channel self-contained SoC module. New elements to be worked on:

1. Module level mechanisms for cross-channel triggering and channel coordination.
2. Digital voltage calibration ("pedestal subtraction"), timing and charge parameters ("feature extraction")
3. Channel combination ("data fusion"), packetization and serialization

WBS 3: Integration of test chip, verification and foundry submission

WBS 4: **Evaluation PCB test board design, fabrication and chip testing:**

- Chip packaging and footprint:
- Evaluation PCB test board design: individual channels and cross-channel features (i.e. low level crosstalk, channel to channel timing estimation, charge and position estimation). Will accommodate the new prototype chip and/or EIC-specific prototype sensor(s).

WBS 5: **Firmware Design:** Firmware implemented in an FPGA on the evaluation test board will be required to e.g. configure the chip, provide external triggering, collect and save data at reasonably high rates for the high level tests.

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Sensor level integration

- Current device has been designed with pixel array-based architecture in mind
- This architecture is naturally well-suited for bump-bonding interconnect
- Strip-based sensors are being currently investigated as a promising alternative
- Project at current state is sufficiently flexible to adjust to different sensor configurations:
    - Requires proper evaluation of front end stage (mostly due to effect of input capacitance)- possible with fabricated dies.
    - Can take advantage of modularity of approach.
- Easiest configuration is the duplication of the 9-channel device in a limited linear vertical array, and addition of module to module communication to handle data forwarding. This modularity can be quite convenient for cost purposes as well.

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Conclusions

- The second revision of HPSoC has been designed and fabricated:
  - It incorporates most of the local functionality needed for the final implementation.
- Testing is underway:
  - Pre-amplification seems compatible with high performance readout of state of the art sensors
  - Digitization is expected to be advantageous compared to pure TDC approaches
  - Functional errors precluding full architecture assessment are being addressed with additional testing of present and old prototyping and new fabrication
- Preliminary results are encouraging:
  - Good timing performance of front end
  - At-spec performance of digitizer modules
- Robust planning for future tests and following steps:
  - Digitizer and front end modules will go through an extensive validation with calibration and sensor inputs.
- Design of HPSoCv3 will incorporate:
  - Results from front-end tests
  - Results from further digitizer evaluations
  - Optimization of feature extraction mechanisms based on acquired data
  - Channel fusion information based on experimental data from multiple channels

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