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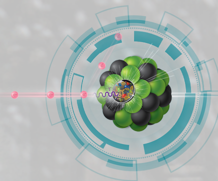

FABRICATION AND CHARACTERISATION OF TI-LGAD DETECTORS FOR 4D TRACKING

Generic EIC-related detector R&D proposals

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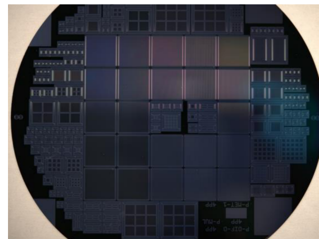
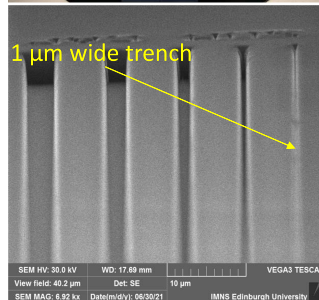


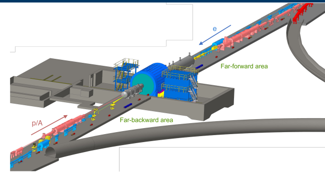


Goal

Develop a viable 55 µm pixelated sensor to match the state-of-the-art capabilities of the Timepix4 ASIC. For use in critical high flux density regions at the EIC.

ABSTRACT SUMMARY

- The proposal focuses on the development of TI-LGADs combined with the Timepix4 ASIC for 4D tracking detectors.
- The primary focus is on a high rate “Far Backward” electron tracker at an upgraded ePIC, or a new detector at a second interaction point at EIC.
- Detector very close to the beam line, giving a very high, beam bunch correlated background from bremsstrahlung and synchrotron radiation.
- The 50 µm pixel size is essential to deliver the required rate capability.
- The ∼30 ps timing resolution from the TI-LGAD will provide an order of magnitude improvement in background rejection.
- Opens running with a luminosity upgrade, and operating in electron + heavy ion experiments where the bremsstrahlung rate increases with Z^2.



- Other detectors such as the trackers in the “Far Forward” subsystems are required to operate with a 30 ps resolution.
- Current technologies are limited by pixel size, sacrificing potential position resolution and rate capabilities.
- The development of a 50 µm pixel TI-LGAD would negate these limitations in future upgrades.
- We are in a unique position to deliver this, having expertise in developing both TI-LGAD and Timepix technologies.
- We have close relationships with both the Medipix Collaboration and Micron Semiconductors.

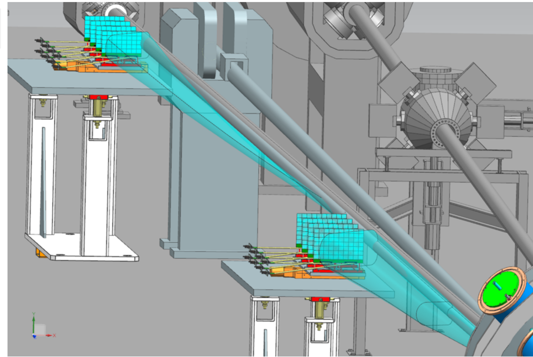
INTRODUCTION - LOW-Q^2 TAGGER APPLICATION

Goal

Develop a viable 55 µm pixelated sensor to match the state-of-the-art capabilities of the Timepix4 ASIC. For use in critical high flux density regions at the EIC.

Low-Q^2 Tagger Support Case

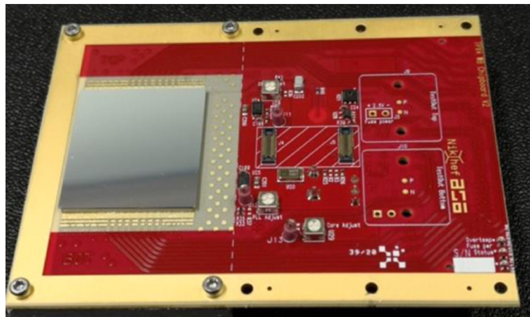
- EIC bunch structure, frequency, luminosity and backgrounds present a very challenging environment.
- Highest flux density and synchrotron backgrounds.
- Timing structure of backgrounds will differ from signals.
- Ideal detector resolution O(20 ps) to match electron bunch length (0.7 cm).
- Of order 99% uncorrelated background hit rejection compared to standard silicon.
- Greatly improved capacity for early data reduction and/or track fitting.



CAD of the Low-Q2 Tagger. From Furletova - ePIC TIC Meeting, 5th Sept 2023

Timepix4

- 30 x 25 mm 512x448 array of 55 µm pixels.
- 4 side buttable through TSVs - large scale, tiled detectors with 100% efficiency.
- data-driven simultaneous timing and energy information.
- 200 ps fine time binning.
- Maximum readout 160 Gbps.
- Mature ASIC.
- Hybrid pixel detector - sensors technology can be transferred to newer ASICs when available (such as VELOPix2 / Timepix5).



Ref: Timepix4, a large area pixel detector readout chip which can be tiled on 4 sides providing sub-200 ps timestamp binning

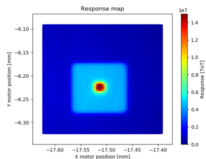
UK LGADS STATUS AND CASE FOR TRENCH ISOLATED LGADS

Beneficial aspects of LGADs

- Higher signal / noise with thinner sensor.
  - Reduced multiple scattering of MIPs.
  - Faster charge collection = lower pileup.
  - Lower efficiency of neutral particle interactions.
- Faster signal rise time.
  - Time of flight track hit matching (4D detector).
  - Rejection of out-of-time backgrounds.

Base LGAD limitations

Low fill factor for pixel sizes below 500 μm.

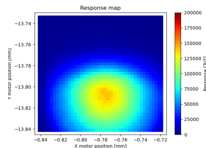


Response of a 100 μm pixel LGAD. Only gain in pixel center.

Ref: Maneuski - iWoRiD 2022

Inverse LGAD (iLGAD)

Demonstrated solution to low fill factor but double sided fab.



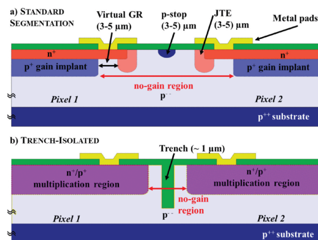
Response of a 55 μm pixel iLGAD. Uniform gain across pixel.

Ref: Maneuski - Pixel 2022

Why Trench-Isolated LGAD?

Several emerging LGAD adaptations address the small pixel limitation.

- Doesn't require specialised ASIC (like e.g. AC-LGAD)
- Only requires single sided processing (e.g. double sided iLGAD process ⇒ may result in low yield)
- Fast maturing through simulation and tests.

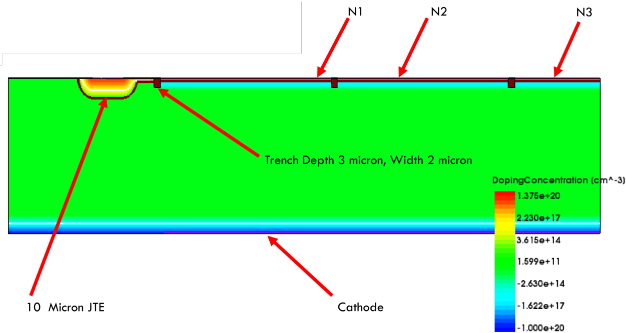


Comparison of standard and TI-LGAD structures.

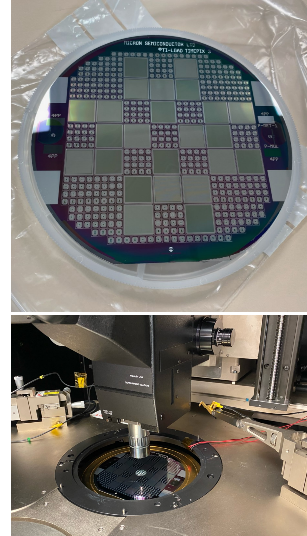
Ref: Trench-Isolated Low Gain Avalanche Diodes (TI-LGADs)

TRENCH-ISOLATED LGADS - STATUS

- Full process simulation has been carried out in TCAD, verified to mirror the processes at fabricators, Micron Semiconductors.
- Trenching done at Scottish Microelectronics Center, Edinburgh.
- Received first wafers of 200 μm thickness.
- Presently carrying out CV / IV probing and gain measurements.



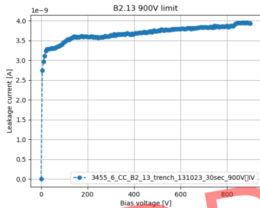
TI-LGAD E-Field from TCAD simulation. Ref: Friday - Thesis 2023

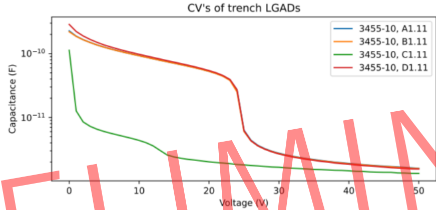


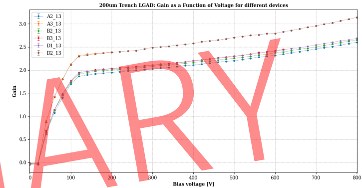
TI-LGAD wafer being probed in Glasgow.

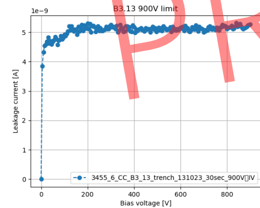
UK TRENCH-ISOLATED LGADS STATUS

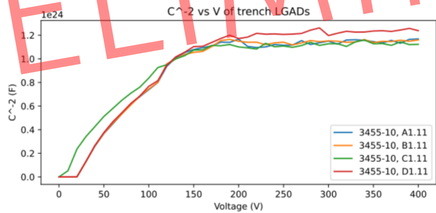
First results from IV, CV and gain probe tests on lowest doping wafer. Conducted in Glasgow, October 2023







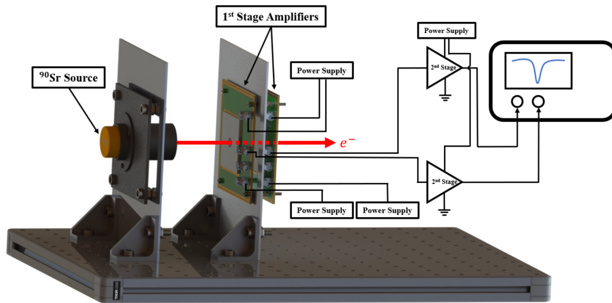




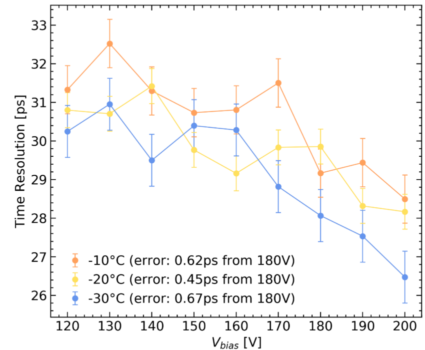
PRELIMINARY

UK STANDARD LGAD TIME RESOLUTION

Measurement of Micron fabricated standard LGAD pad using ^{90}Sr source, carried out in Glasgow.



An illustration of the setup to measure time resolution.

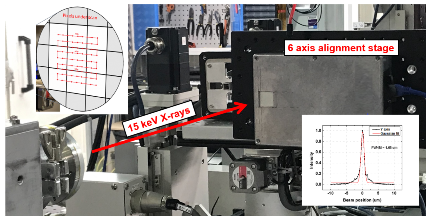


Measurements of Micron LGAD timing resolution.

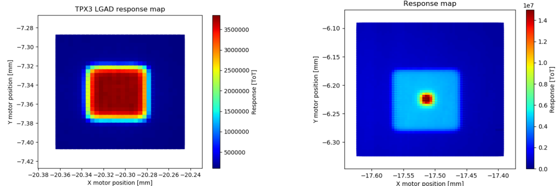
Ref: 26.5 ps Time Resolution Using 50 µm Low Gain Avalanche Detectors Fabricated by Micron Semiconductor Ltd.

TIMEPIX3 - STANDARD LGAD DEVICES TESTED AT DIAMOND VS SIMULATION

Standard LGAD bonded to Timepix3 ASIC and tested at Diamond Light Source, November 2019



Experimental setup at Diamond Light Source facility

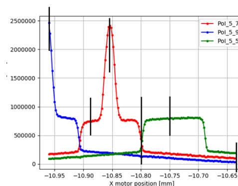


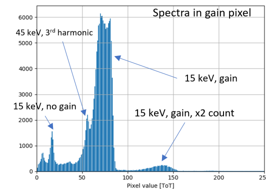
Response of 55 µm (left) and 110 µm pixel (right) LGAD bonded to Timepix3 ASIC.
Ref: Ref: Maneuski - iWoRiD 2022

Simulation verification of fill factor

Pixel pitch	Simulated FF	Measured FF
55 µm	0.0%	0.0%
110 µm	11.5%	9.5%

Ref: Moffat - Thesis 2020



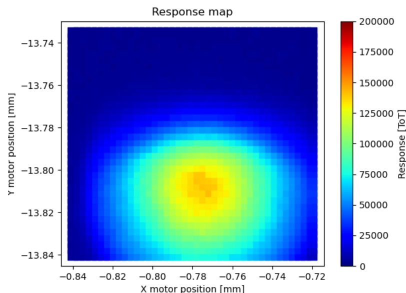


Ref: Maneuski - iWoRiD 2022

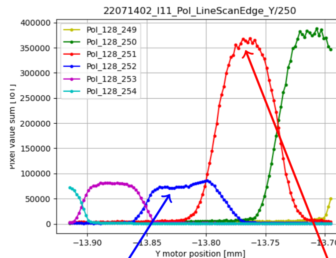
iLGAD bonded to Timepix3 ASIC and tested at Diamond Light Source, July 2022.

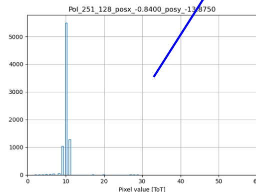
Timepix3 55 µm pixel - iLGAD test results

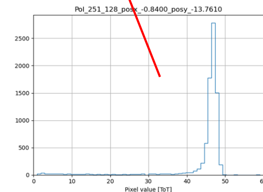
- Step function pixel response
- Convoluted with finite beam size
- Uniform gain achieved



2D response of iLGAD across Timepix pixel. Ref: Maneuski - Pixel 2022

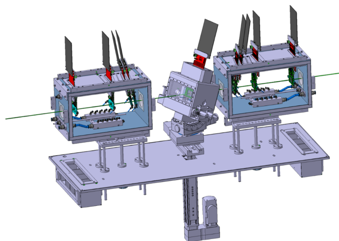


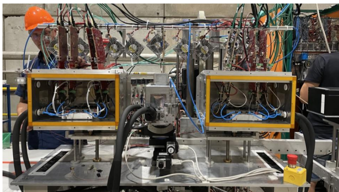




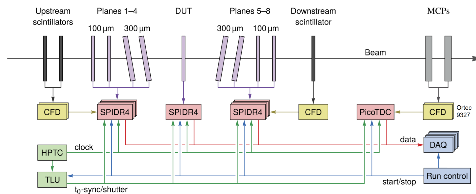
Line scans showing gain in iLGAD pixels compared no gain pixels.

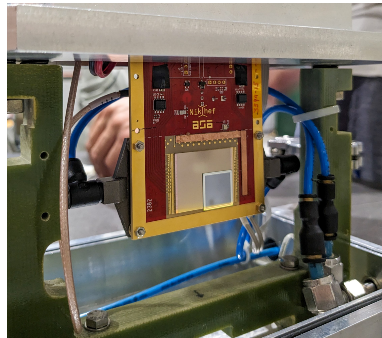
- Successful tests of iLGAD (Timepix3 dimensions) bonded to a Timepix4 ASIC in August 2023.
- Data not yet made public.





CAD and picture of the Timepix4 telescope installed at H8 beamline at SPS, CERN.





Timepix4-iLGAD device as DUT

Ref: *https://ep-news.web.cern.ch/content/spotlight-hybrid-pixel-sensors*,

WORK PACKAGES

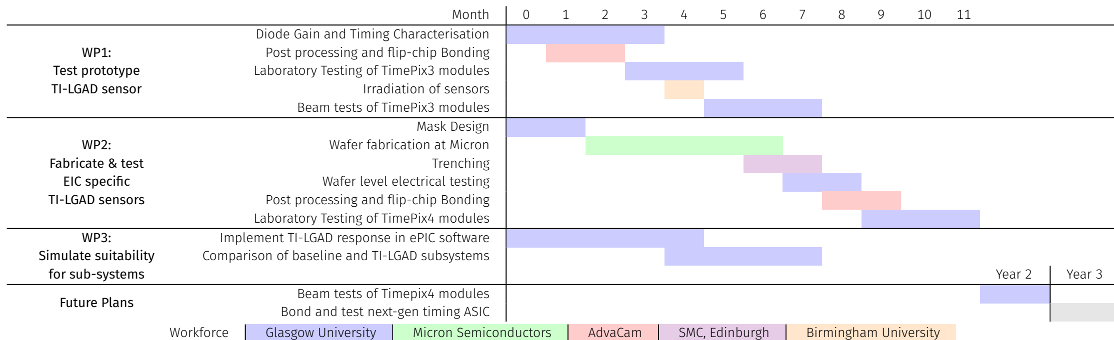
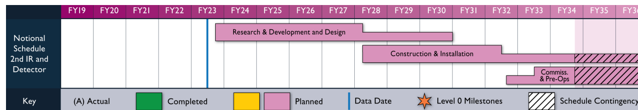


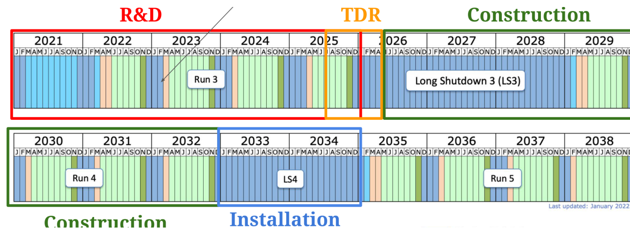
Table 1: Deliverable schedule.

OUTLOOK

- On fulfilment of this work, TI-LGAD technology should be mature for production of Timepix4 modules for the ePIC Low-Q^2 tagger.
- Far-forward, far-backward and electron polarimetry are envisioned as potential benefactors of this work as upgrades or at Detector 2.
- Notional timeline of Detector 2 and possible upgrades align with Medipix/CERNs next generation of large scale fast timing ASIC - VeloPix2/Timepix5.
- Micron fabrication planned to include PicoPix geometry. (Velopix2 prototype aiming for 20 ps timing resolution and extreme radiation hardness.)



Notional EIC 2nd detector schedule. Ref: 1ST INTERNATIONAL WORKSHOP ON A 2ND DETECTOR FOR THE EIC



LHC schedule. Ref: VELO Upgrade 2 Workshop

REVIEWER Q&A

REVIEWER QUESTIONS: 1

Question 1 - Are you aware that multi-pixel TI-LGAD exists?

We are aware of developments at BNL, FBK, CNM, HPK, etc. We attend RD50 meetings and aware of fabrication developments and characterisations within the collaboration.

To our knowledge only our group has demonstrated functional 55 µm LGAD device flip-chipped to a TPX3 ASIC, both LGAD and iLGAD.

Our next goal is the TI-LGAD concept bonded to a TPX4 ASIC which we hope to pursue with the help from EIC funds.

Question 2 - AIDAInnova TI-LGAD includes TimePix geometry. What will a production at MICRON add to this?

We have long standing collaboration and very good links with the commercial vendor Micron Semiconductor Ltd. we have access to their full process which allows us to optimise their process using TCAD simulations.

This opens access to the full process parameters and close collaboration allowing us to find the best fabrication architecture without the need to fabricate an excessive number of devices.

We have a strong feedback loop in place where we perform the simulations, Micron the fabrication and the two groups perform the post fabrication device characterisation including SIMS analysis of the doping profiles, IV, CV, X-rays, TCT, Synchrotron.

We believe we are best placed to investigate small pixel Ti-LGAD with TPX4 concept as we have been a member of the MPX collaborations for since its inception (MPX1, MPX2, MPX3 and MPX4).

Question 3 - How would the probe testing be done? Are there structures designed to provide information on gain and isolation characteristics?

Cleanroom: Our cleanroom has a 200 mm Wentworth probe station with temperature-controlled chuck and controlled humidity environment. We routinely test LGAD and ATLAS ITk sensors there. The setup if fully automated for wafer level testing. We invested in pattern recognition system which will be installed this month allowing automatic testing of diced devices.

Test structures: One of the biggest concerns with the trench isolation is the uniformity of the trench over the wafer. We have test structures distributed over the full wafer surface to map trench performance as a function of position.

Fabricated devices: Diode structures are separated into two parts with a trench. We will measure the isolation as a function of depletion voltage using electrical (on probe station) and TCT (laser).

New device structures: For future fabrication runs we plan to add structures to look at deeper, wider and multiple trenches. Map over the wafer.

Device gain: we have pad diodes with transparent entrance widows for TCT (laser): different pad sizes and the use of small arrays allow easy characterisation of gain of a pixel matrix without the need for flip-chip.

Question 4 - What is the division of work between RD50/Timepix and this proposal?
Question 5 - The Timepix3/4 process seems to be an integral part of the R&D. What parts are unique to EIC? Is the work in ”Test Prototype TI-LGAD sensor” partially paid by R&D funds?

Previous work was funded by the UK research council and LHCb, no funds obtained through other means. But this funded the production of LGAD wafers, iLGAD wafers and first lot of TI-LGAD wafers. This allowed to validate fabrication process, benchmark TCAD vs. Micron fabrication process, characterise gain / timing, demonstrated small pixel design functionality. We used Timepix3 as a platform to demonstrate pixellated sensor characteristics.

In this bid we aim to prove the TI-LGAD device functionality to EIC requirements, including those flip-chipped to TPX4. The new devices and all further characterisation discussed in the proposal will be funded from this bid.

REVIEWER QUESTIONS: 6-7

Question 6 - Are both flip chip runs included in this proposal?

Yes, both flip-chip runs are funded in the proposal. In addition to this, we will look at doing more flip-chip in house using our newly purchased FC150 flip-chip machine to reduce cost and produce more devices to characterise.

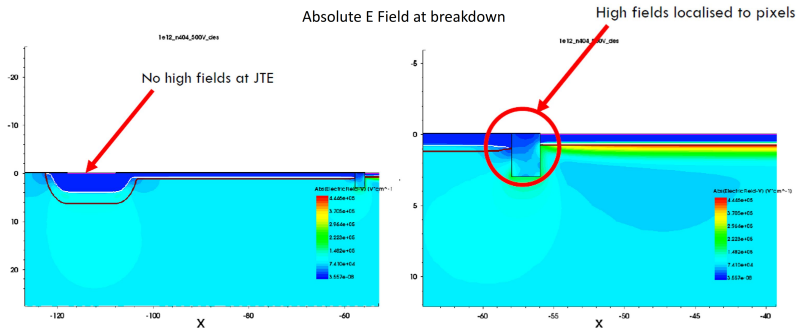
Question 7 - How would the work proceed if this proposal is not funded?

There will be no fabrication run specific to EIC requirements or focus to deploy the technology at the EIC. Effort to characterise existing devices would likely to be reduced until further funding is secured.

Question 8 - Does the TCAD indicate any limitations on gain / breakdown related to the trench depth or spacing? Can you show the TCAD E field map?

We studied various parameters of the trench before proceeding with fabrication. Some conclusions are:

- Wider trenches have slightly higher breakdown.
- Deeper trenches have slightly higher breakdown.
- JTE essential at the physical edge of the device, parameters optimised.



Ref: Friday - Thesis 2023

REVIEWER QUESTIONS: 9-10

Question 9 - Do you plan to study various trench fill materials? Is thermal oxide the only one studied in the base plan? Are other methods consistent with the processing?

We only plan to study trenches with thermal oxide which is considered ideal. The trench aspect ratio makes filling of the trench difficult. Thermal oxide will also remove any initial defects in the silicon trench as the silicon is turned into silicon oxide to fill the trench.

Question 10 - Why the mix of 6 epitaxial (epi) and 12 float zone wafers? Aren't the epi wafers the ones that would be used for the experiment?

The 6 epi + 12 FZ are the wafers that are in production and funded by the UK research council to allow us to get the first look at the trench isolation using the Micron process. These wafers don't have TimePix4 devices. For this initial run the float zone wafers were cheaper and easier to obtain to allow the trench to be optimised, and then the epi wafers were used for the thin devices.

Only epi to be used for the new fabrication run funded by this proposal which include the TimePix4 devices.

Question 11 - In reference 15 it states ”*It is worthwhile to note that even the safest layout in TI-LGAD has IPD lower than 15 μm. Due to these characteristics of TI-LGADs, they are the ideal candidate for segmented LGADs with a pixel size of 100 μm, achieving FF higher than 84%*” How do you plan to achieve your 2-3 micron goal?

We have a different fabrication architecture which will reduce the no gain distance between the pixels to the dimension of the trench, after filling with thermal oxide.

Reference 15 - Characterization of novel trench-isolated LGADs for 4D tracking

COSTING

BACKUP - PROPOSAL COSTING FY24

The total request is $157000

Item	Cost ($)
Fabrication	64000
Flip-chip	27500
Proton Irradiation	7500
Travel	8000
Consumables	5000
Equipment	10000
TimePix4 ASICS x 20	16000
TimePix4 PCB x 20	9500
SPIDR4 - TimePix4 readout	9500

Table 2: Breakdown of the funding request

Costing	100%	80%	60%
Wafers fabricated	12	8	6
Wafers postprocessed	6	3	3
Proton Irradiation	Yes	Yes	No
Beam Tests	Yes	Yes	Lab only

Table 3: 80% and 60% costing reduction