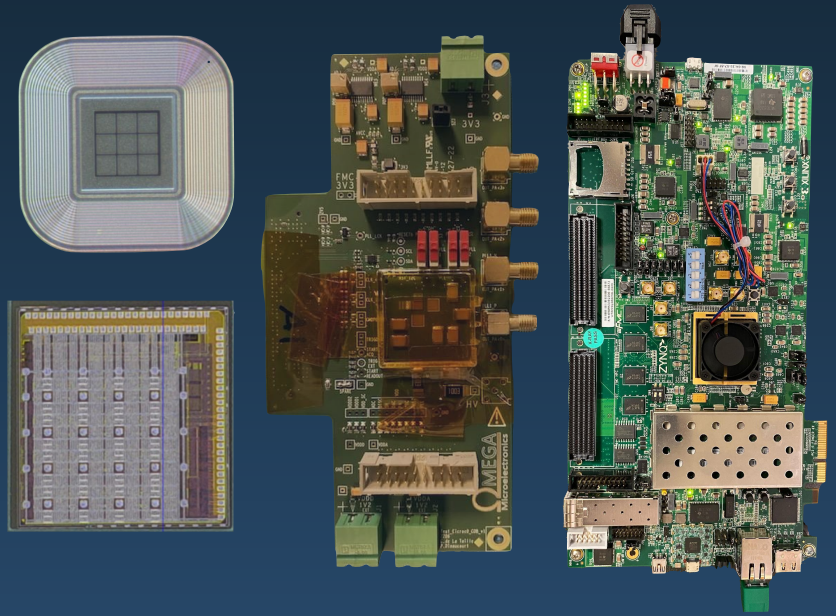
R&D of 4D Detectors with EICROC and AC-LGAD at EIC consolidating a US-Japan Consortium

EIC-Related Generic R&D Proposal Review Meeting



Japanese Members:

Kenta Shigaki (Hiroshima Univ.)

Satoshi Yano (Hiroshima Univ.)

Yoshiyuki Miyachi (Yamagata Univ.)

Yuji Goto (RIKEN)

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Alessandro Tricoli (BNL)

HAMAMATSU

Review Questions

- What would be the effect on EICROC testing if this project were not funded?

EICROC testing is an essential part of the development and validation of the AC-LGAD sensors for the EIC detectors. The EICROC chip is designed to read out the pixelated AC-LGAD sensors for the Roman Pots, which require high time resolution and low power consumption. However, the same chip may not be compatible with the strip AC-LGAD sensors for the Barrel TOF, which have larger capacitance and different geometry. Therefore, this project aims to test the feasibility of using EICROC for strip sensors, by modifying the AC-LGAD geometry and optimizing the EICROC parameters. This would avoid the need for a separate ASIC design and fabrication for the strip sensors, saving time and resources. This approach is a mitigation to the risk for the current strategy of a separate chip design for AC-LGAD strip sensors, which will also save time, effort and in turn money. (exploratory component, if not funded this compatibility part will not be explored.)

Review Questions

- One of the aims is to improve the design of the EIROC ASIC, but there are no collaborators from the Omega group. Why?

The Omega group is already collaborating with BNL and other US institutes, as well as with Japanese institutes, supported through fundings from eRD109 consortia. The Omega group relies on the feedback and results from these consortia to improve the EICROC ASIC design. The goal of this proposal is to strengthen the US-Japan collaboration in the EIC TOF project, by leveraging the expertise and facilities of both countries in AC-LGAD sensor development and testing. The PIs of this project already have a strong and established relationship with the Omega group, and have regular meetings with them to discuss the EICROC ASIC performance and issues. The PIs will also share their results and findings with the Omega group, as well as with other EIC consortia, to contribute to the overall improvement of the EICROC ASIC design.

Review Questions

- How would the project lead to continuing involvement by Japanese groups in EIC? Are there specific contributions envisioned?

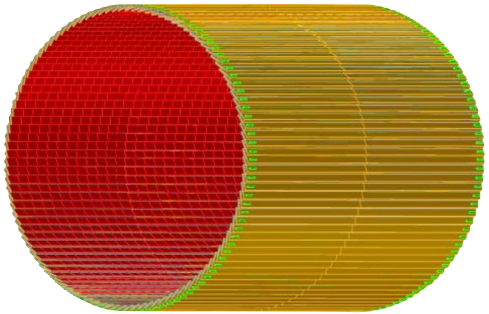
HPK is the most reliable large-volume producer of silicon detectors for collider physics experiments and specifically for AC-LGADs. HPK's proximity to Japanese institutions is a significant advantage for large-scale sensor production for EIC projects. However, without an established base in Japan and expertise, securing funds from Japanese national agencies is challenging. This project, if funded, will allow the Japanese institutes to collaborate with the established BNL group in AC-LGAD R&D, enabling the Japanese groups to establish local facilities, work with US institutions, and closely collaborate with the Japanese vendor HPK. This strong partnership will enhance their funding prospects, facilitating their contributions to the EIC project from national agencies in Japan. We anticipate robust involvement from Japanese groups, national agencies, and Japanese vendors across various aspects of future EIC projects.

More specifically Japanese groups aim to play key roles in Barrel TOF construction for the ePIC TOF project. They're currently taking leadership roles in this project and plan to expand their involvement in mechanical design, electronics, software, and simulation aspects in the future.

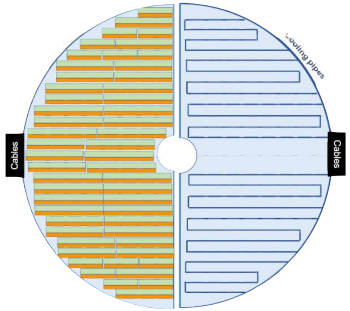
Background: AC-LGAD application at EIC

Improve spatial, similar time resolution to previous incarnation (AC-LGAD) various applications at EIC

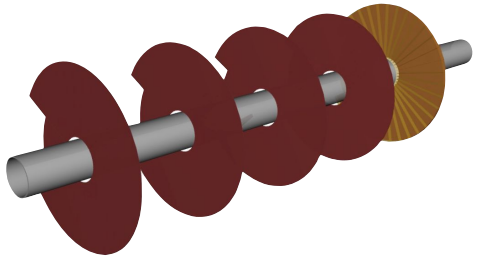
Barrel TOF (strips)



Forward TOF (pixel)



B0 tracker (pixel)



Roman/OMD (pixel)

	Area (m^2)	Channel size (mm^2)	# of Channels	Timing Resolution	Spatial resolution	Material budget
Barrel TOF	10	0.5*10	2.4M	30 ps	30 μm in $r \cdot \varphi$	0.01 X0
Forward TOF	2	0.5*0.5	8.8M	25 ps	30 μm in x and y	0.05 X0
B0 tracker	0.07	0.5*0.5	0.28M	30 ps	20 μm in x and y	0.01 X0
RPs/OMD	0.14/0.08	0.5*0.5	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.

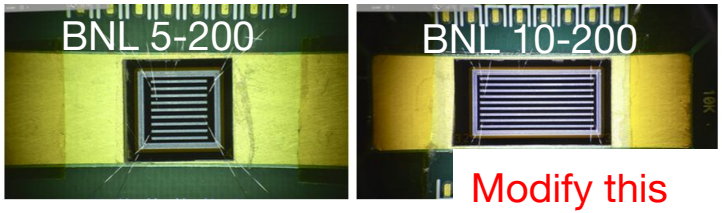
AC-LGAD devices has the potential to enhance EIC detectors' capabilities in a significant way, with eRD112 and eRD109 groups spearheading the R&D of this technology

Open areas for generic R&D: ASIC compatibility of long-strip sensor, large area sensor production

Background of the planned project

BNL and Hamamatsu Photonics (HPK) sensors

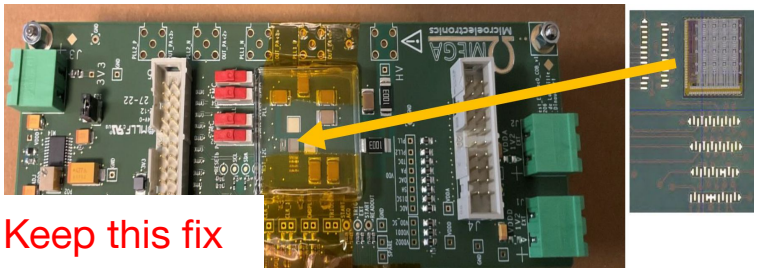
long strip sensors (100 µm pitch), 10x0.5 mm^2



Modify this

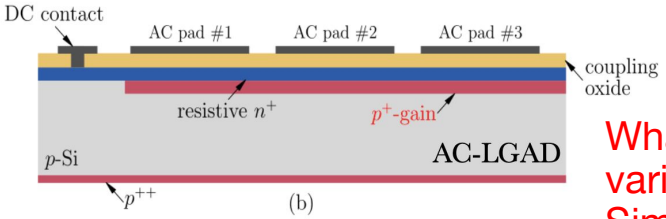
Compatible ?

ASIC EICROC: IJCLab, Ecole Polytechnique/Omega and CEA



Keep this fix

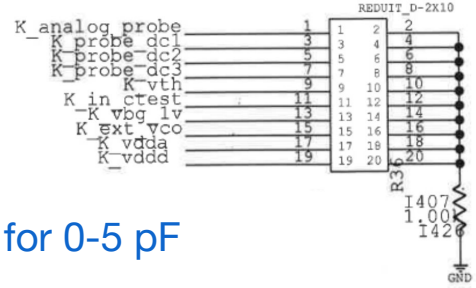
Strip sensor requirement for EIC:
20 pS time & 30 µm spatial resolution



What can be varied? Simulation?

EICROC is designed for Roman Pots (pixel sensor) but provides a range of tolerance for capacitance (Pre-Amp ~1pF) & impedance to be compatible with a range of other sensor geometries

Limited tuning possible



Major goal: find compatible strip sensor with EICROC which is optimized for 0-5 pF input range of capacitance (C_{det}), Sig/Noise scales with C_{det}

Objective of the planned project

- Project Context:
  - Feasibility of using EICROC ASIC (originally designed for 500 micron pitch pixel sensors) for strip sensors, by modifying the AC-LGAD geometry and optimizing the EICROC parameters (minimal modifications to design).
  - Risk mitigate a completely separate ASIC design for the strip sensors by fulfilling ePIC physics requirements
  - Foster expertise in Japan to facilitate continuing investment in EIC in particular to strip-sensor based detectors, by providing training and collaboration opportunities for Japanese researchers and institutions.
- What is needed:
  - BNL's expertise on testing full readout chain for sensor+ASIC+prototype RDO, including design, fabrication, simulation, integration, and analysis.
  - Primary training of workforce development for Japanese collaborator, including hands-on experience, knowledge transfer, and technical support.
- Tools:
  - A test stand for sensor+ASIC+RDO system, Xilinx kit for EICROC and ePIC DAQ interface
  - A radiation source & test beam for sensor+ASIC exposure

Proposed Research and Methods

Main tasks:

- Sensor Procurement: Acquire strip sensors from previous HPK productions with various geometries, different lengths (1 mm to 2 cm), and metal sizes to vary the detector capacitance. Some BNL sensors may also be used for comparison.
- Active Thickness Variation: Obtain sensors with different active thicknesses (20-50 μm) to assess their effect on readout speed and time resolution, aiming for ~20 ps.
- Resistivity Variations: Acquire sensors with varying resistivities in the n+ (resistive) layer.

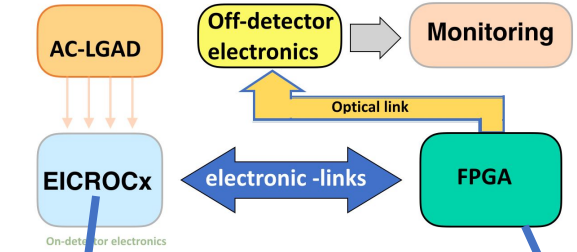
Performance testing:

- EICROC Evaluation: Test EICROC with AC-LGAD sensors, varying geometric parameters, and assess performance in terms of time resolution, gain, noise, power consumption, signal sharing and radiation tolerance.
- Compatibility Assessment: Identify the compatibility region for sensor geometry that ensures EICROC meets requirements, such as for applications like barrel TOF.

Details:

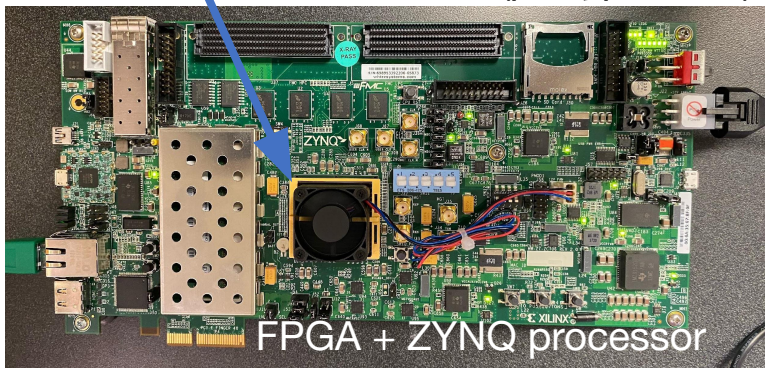
- TCAD Simulations: Utilize TCAD simulations to explore sensor designs and provide feedback to HPK for future fabrication.
- Performance Measurements: Conduct measurements of charge collection and time resolution using beta particles from a 90Sr source and infrared pulsed laser light (1056 nm)
- Test-Beam Facilities: campaigns at the FNAL Test-Beam Facility (FTBF) with 120 GeV protons and with ~1 GeV electrons in Japan

Full readout chain at BNL and in Japan

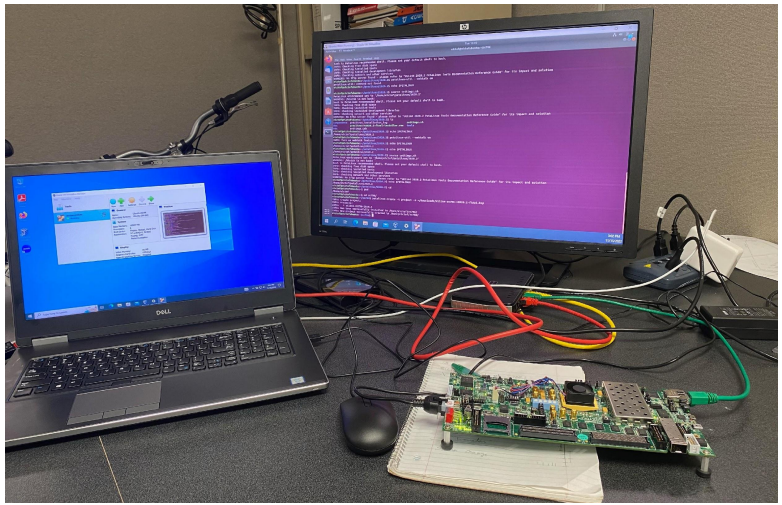



EICROC0 ASIC on carrier board

Xilinx dev kit at (protype RDO)


FPGA + ZYNQ processor

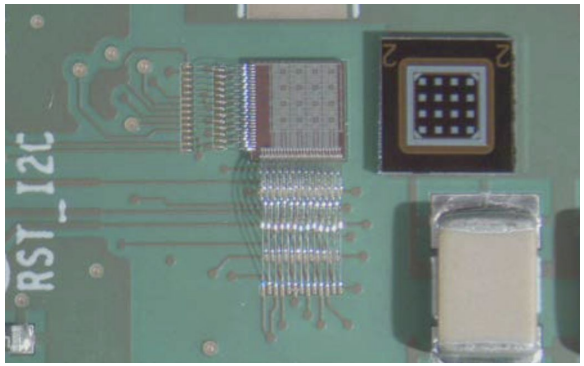
Setup at BNL



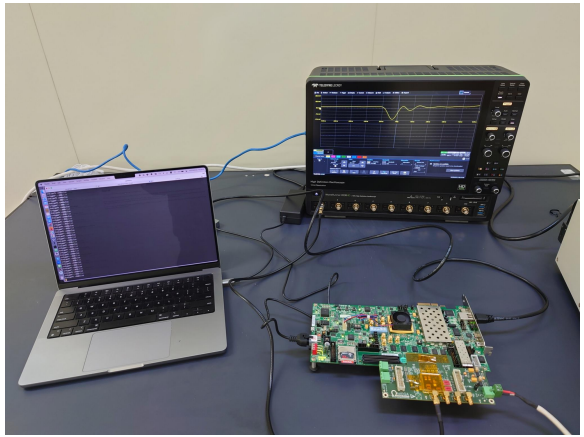
- The full readout chain requires: procuring a sensor and EICROC ASIC mounted on a carrier board custom which is connected to a prototype RDO board. BNL group has set up the full stand in collaboration with the French IJC Lab, we are setting the same in Japan

First set of results: Japanese member visit to BNL

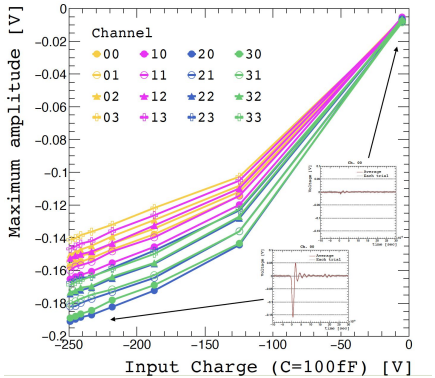
ASIC + Sensor on carrier board

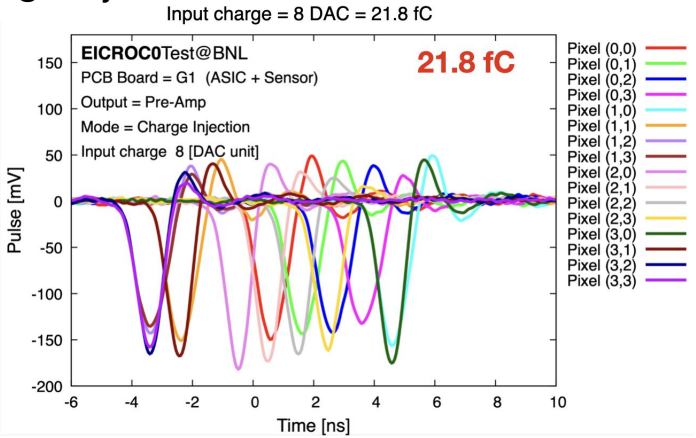


Setup at Hiroshima Univ.



ASIC response to charge injection

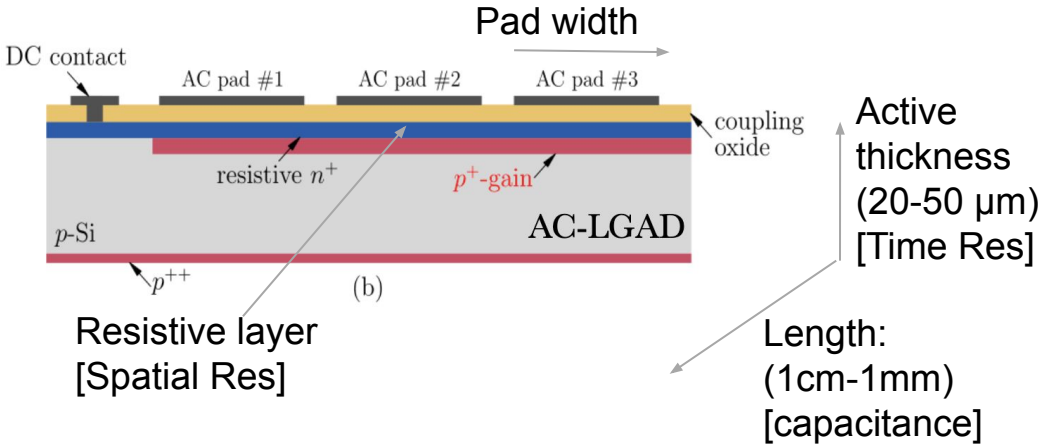




- EICROC Evaluation: With the help of the BNL group we have been able to perform the first EICROC0 ASIC testing without the sensor and setup a test stand in Japan.
- We have procured one sensor+ASIC+prototype RDO in Japan and about to start characterization of full chain
- Future plan is to expand the testing with various sensor geometries

What is our next plan on testing & analysis

1. Procure BNL & HPK sensors for various geometries



2. Test the module assembly with beams using beta particles, IR laser, and protons (FNAL) or electron (in Japan) at different facilities, and study its charge collection, time resolution, charge sharing, and space resolution

3. Find the range of applicability with the EICROC keeping EIC requirement of time (20 ps) and 30 μm applications

4. Perform TCAD simulation to optimize the sensor configuration
5. Submit new HPK sensors for EIC with improved geometries (leveraging other funding sources for this submission)

Responsibility of the BNL & Japanese groups

US - BNL:

- Get EICROC chips and Carrier Boards from IJCLAB/Omega
- Assemble EICROC chips and HPK's AC-LGADs on Carrier Boards
- Test modules before shipping to Japan
- Train and instruct Japanese colleagues on module testing
- Liaison with IJCLAB/Omega and ASIC designers

Japan - Hiroshima:

- Coordinate activities in Japan
- Set up and perform system and module tests
- Test and evaluate strip modules with different designs
- Study sensor designs using TCAD simulations and inform HPK

Japan - Yamagata:

- Test and evaluate pixel modules with different designs

Japan - RIKEN:

- Lead discussions to acquire sensors from HPK

Japan - Shinshu:

- Prepare and conduct test beam in Japan

Deliverable, project timeline

BNL deliverables:

- Provide EICROC chips, Carrier Boards, and AC-LGAD sensors from previous batches (Month 1)
- Assemble and test 5 modules with EICROC chips and AC-LGAD sensors (Month 2-3)
- Ship 4 modules to Japan and keep 1 module at BNL (Month 3)
- Train Japanese colleagues on equipment, software, firmware, and device testing (Month 2-8)
- Produce 5 more modules with new AC-LGAD sensors for this project (Month 8-10)

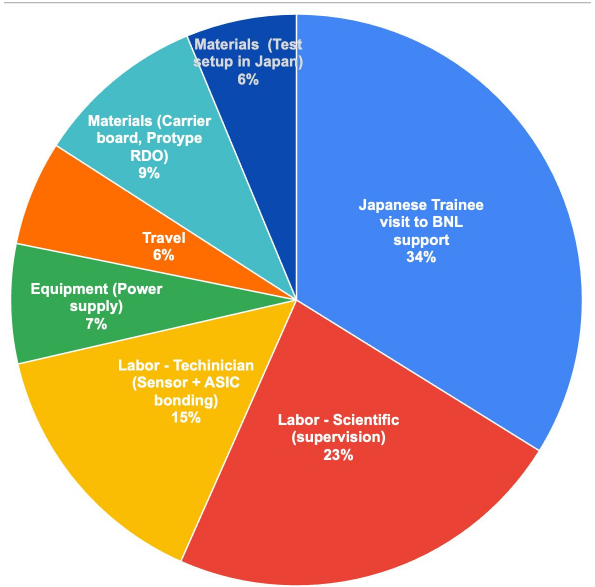
Japanese deliverables:

- Set up equipment, software, and firmware (Month 2-4)
- Characterize BNL-made modules with EICROC chips and AC-LGAD sensors (Month 4-10)
- Study AC-LGAD designs using TCAD simulations (continuing effort)
- Join HPK submission to produce more AC-LGADs for EICROC1 (Month 6-8)
- Characterize BNL-made modules with new AC-LGAD sensors (Month 10-12)

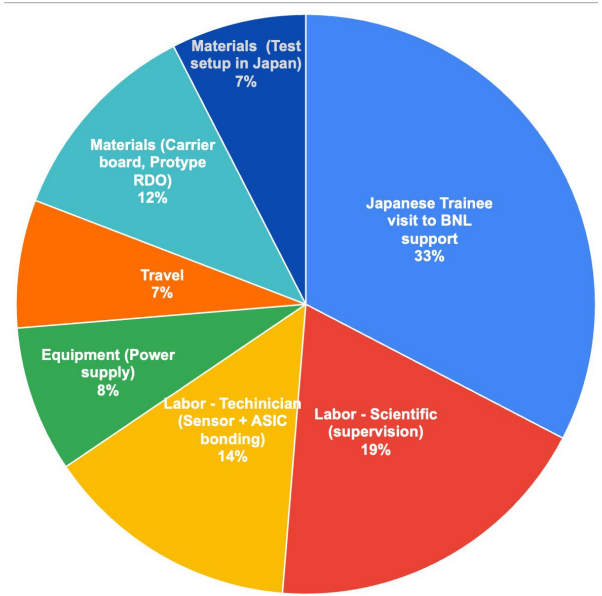
Shared deliverables:

- Participate in test-beams at FTBF and ELPH (schedule depends on availability)
- Disseminate results to the particle physics community & provide feedback to EICROC developers (Month 10-12)

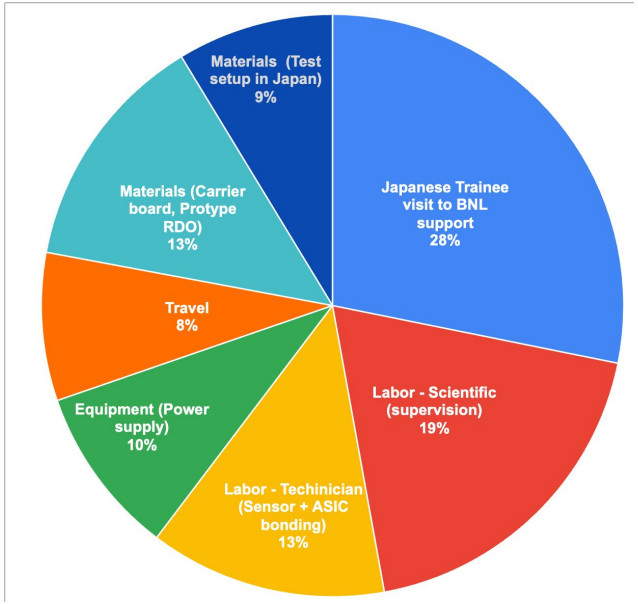
Funding requests (overhead included)



Nominal (152 K)



-20% cut (127 K)



-40% cut (108 K)

Fund requested for training Japanese students/participants and device fabrication at BNL to jump start efforts in Japanese institute

Summary

- Goal: To test the feasibility of using EICROC for strip sensors with AC-LGAD, avoiding the need for a separate ASIC design for strip sensors for EIC application

- Motivation: Strip sensors have important applications in EIC, such as barrel TOF, and require fast and precise timing and charge measurements, but cost and risk are high for a new ASIC design and production

- Approach: Modify the AC-LGAD geometry and optimize the EICROC parameters to match the strip sensor requirements, and test the performance of the modules using various radiation sources and beams

- Collaboration: US-Japan consortium, leveraging BNL's expertise in AC-LGAD R&D, HPK's proximity and production capability, and Japanese groups' involvement and leadership in ePIC TOF project

- Impact: Risk mitigation for a separate ASIC design for strip sensors, saving time and resources; development of local facilities and expertise in Japan, facilitating future communication and collaboration with HPK; enhancement of funding prospects and contributions from Japanese national agencies and institutions to the EIC project (ePIC & det-II)