Brookhaven National Laboratory

U.S. DEPARTMENT OF ENERGY

Large-Area Monolithic Active Pixel Sensors Combining High Spatial and Temporal Resolution – committee presentation meeting

Dominik Gorni

10/30/2023

PART 1
Committee comments

Question #1

Are there engineering, physics, or computer science faculty at universities who would be interested in collaborating on some aspects of this R&D? In general, this would seem like a way to increase the number of senior person-months per year devoted to arguably important generic R&D without increasing the cost so much that it is out of reach of the current program.

Answer

We are open for collaboration. Instrumentation Division has a long tradition of collaboration with the universities around the US, e.g.:

- Yale University (*Photon Detector Readout Electronics for nEXO*)
- Yale and Princeton Universities (*Co-design Center for Quantum Advantage C2QA*)
- Columbia University / Nevis Lab (*ATLAS lAr Calorimeter ALFE ASIC-COLUTA ADC*)
- University of Pennsylvania (*Rubin Observatory - LSST*)

Some ad-hoc ideas for shared, supplemental efforts, while more can emerge:

- Simulation of whole sensors latency with event-driven readout using physics data generators;
- Investigation of the original data grabber and RSU-to-StaveEnd transmission, existing for framed-readout, and its adequacy for the event-driven readout, and potential redesign;
- Happy to host grad, PhD students and postdocs on-site in ASIC design (process specific) and testing work.

Note: Good communication between BNL and potential collaborators is required due to utilization of IPs, created at BNL, fabrication process requiring NDA;

Question #2

It is not clear to me how a person with 0.02 FTE can be effective. The highest FTE in this project is <0.2 which is also low. Which tasks does each person do? This breakdown would be necessary to judge if the required task could be performed with the assigned FTE value.

Answer

- While generic R&D aims at demonstrations of feasibility and suitability of the proposed technologies, it is constrained in the total distributable budget for all projects, so **we adjusted to the expectations and plan to achieve the initial stages of the R&D efforts.**
- To advance to a manufacturability readiness level, more funding should be requested, but we do not see ability of getting such a chunk from the generic R&D portfolio, therefore follow-up on this “actual seed” will need to be requested in the upgrades-time, but we hope to start the project, gain tracking and visibility.
- This concept is beyond the ePIC SVT baseline, nevertheless the team possess momentum and the same fabrication process is used, so less overhead than in starting from scratch.

Sum of FTE		Reporting Year		Reporting Year		Reporting Year	
LaborType	Name	2024	Grand Total	2024	Grand Total	2024	Grand Total
SCIENTIFIC	PINAROLI,GIOVANNI	0.07	0.07	0.06	0.06	0.04	0.04
	MANDAL,SOUMYAJIT	0.02	0.02	0.02	0.02	0.01	0.01
	DEPTUCH,GRZEGORZ W	0.02	0.02	0.02	0.02	0.01	0.01
	ASCHENAUER,ELKE C	0.02	0.02	0.02	0.02	0.01	0.01
PROFESSIONAL	GORNI,DOMINIK S	0.18	0.18	0.14	0.14	0.11	0.11
POST DOC	POST-DOC	0.05	0.05	0.04	0.04	0.03	0.03
Grand Total		0.36	0.36	0.28	0.28	0.21	0.21

Responsible for design and simulations of the **analog part**

Supervision of the design, technical assistance

Supervision of the physics side

Responsible for design and simulations of the **digital part**

Responsible for simulations on the **physics side**

Note: funds are limited, thus allocations aims at covering, even shallowly, the most critical tasks needed to achieve technology demonstration; individual names may change.

Question #3

How does the proposed solution compare with other event-driven readout designs such as the MuPix chip (https://arxiv.org/abs/2002.07253) which achieves timing < 10ns ?

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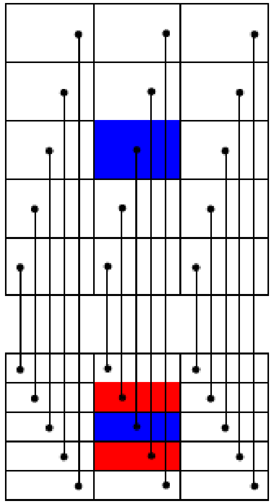
Answer

- **MuPix is not even driven**; it only stores hit is peripheral cells, measures time of arrival and amplitude and cells wait for being scanned.

Readout Buffer

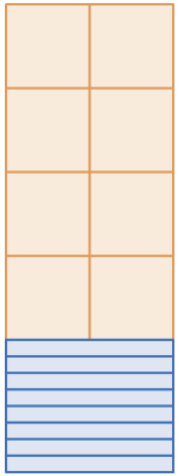
- Each pixel has its own readout buffer cell
- Contains different circuits for these purposes
  - time measurement
  - amplitude measurement
  - address signal generation
  - temporary storage of the hit information
    (10 bit time stamp and 5 bit second time stamp for time over threshold calculation)
  - priority ordered readout
  - hit bus signal generation
- One readout buffer column (500 buffers) connected to two pixel columns (500 pixels)
- Size readout buffer cell 5 µm x 160 µm

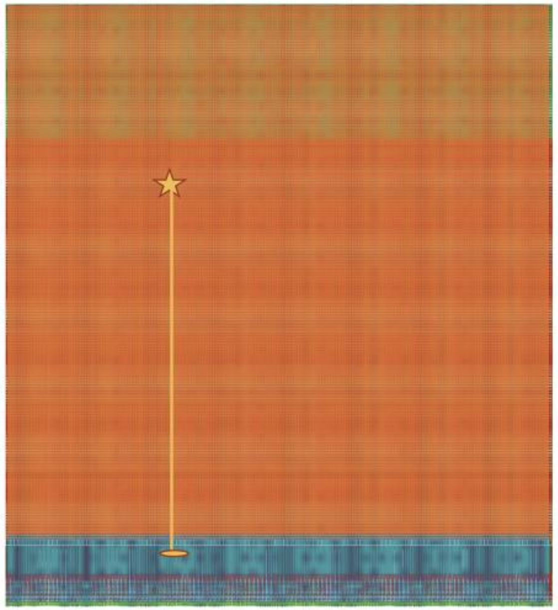
MuPix10 (cern.ch)



Signal flow through the MuPix10 – from the pixel to the readout buffer

- Particle generates electron-hole-pairs in the pixel diode
- Small signal amplified with PMOS amplifier in pixel
- Analogue signal transmitted via a long line to the readout buffer cell





Design and Features of MuPix10 Alena Weber 22

- MuPix still utilizes priority encoding at the end for readout of the cells
- the readout circuitry is spatially separated from the active pixel matrix and there is one readout cell for every pixel in double column structure (old scheme), resulting in **big periphery circuit – highly disqualifying for EIC SVT!**

- **Every pixel individually routed to periphery**, that is feasible for O(50um-80un) but impossible at O(20um) and with process with 6 metal layers
- Alone readout cells are >2um in height each, occupying all more area than entire readout in ALICE-ITS3 sensors

Answer cont.

Definition of Event-Driven Readout:

Event-Driven Readout is a data processing approach and transmission method, where data is automatically localized and forwarded to the output in an automated manner without the need for manual prioritization, intervention or intermediate storage. This approach ensures that data is transmitted without corruption or delay caused by collisions with other data, transfer of which was either previously initiated or during the transmission pf the data in question. This method guarantees efficient, seamless data transmission without explicit, hidden, or apparent priority assignments.

Readout, in which sources of data report to external storage cells (and these cells extract time-of arrival and amplitude information thanks to locally running clocks, data converters, etc.) and, then, these cells are scanned for presence of data is not Event-Driven.

Currently in HEP or NP community there is no Event-Driven Readout developed or used other than here presented EDWARD protocol.

X-Y reporting is prone to ambiguities
Token Passing is polling readout method with unpredictable time to localize data
Priority-encoder based methods require snapshotting of frames
Time-encoded methods, such as CERN-proposed DPTS, are prone to ambiguities, prone to process dispersions and biases changing timing and require time-to-digital converters for obtaining position from time or delay information

Question #4

Funding this proposal will not produce a working prototype. What is the path forward in subsequent years?

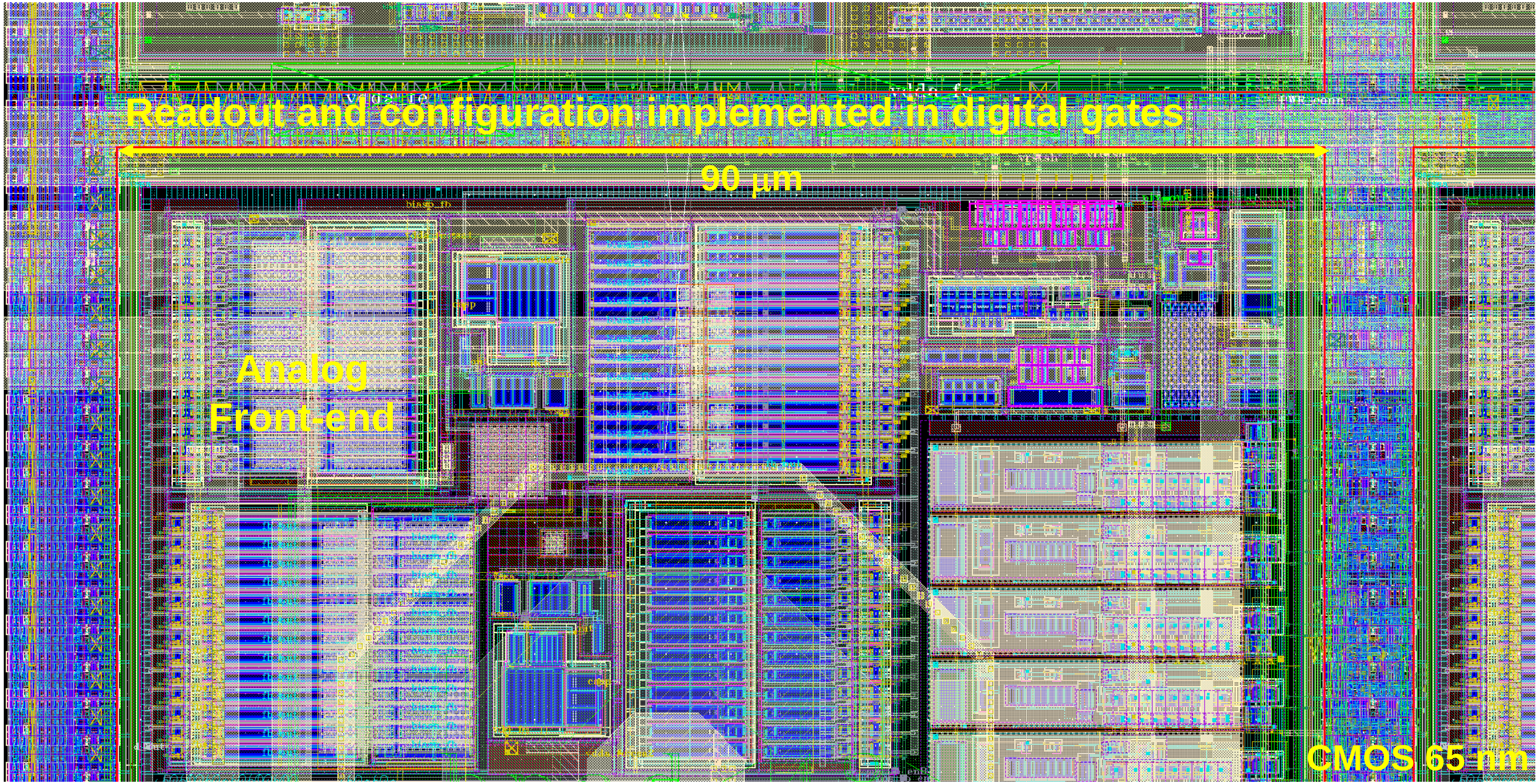
Answer

- **Yes, the requested funding is insufficient to complete the design and prototyping;**

- We know that:
  - the concept's general viability has been demonstrated in X-ray hybrid pixel detector prototypes at BNL;
  - how to successfully transition to O(20um) monolithic pixels needs to be undertaken;
- Within the scope of this proposal, our intention is to work on:
  - tailoring of the concept for implementation together with AFE in O(20um) monolithic pixels
  - setting up methodology and CAD/EDA flow to match the needs, e.g., evenly distribute resources of the event-driven protocol in the matrix of O(20um) pixels,
  - developing scalable readout skeleton and building blocks (FE, configuration, etc.) in TPSCo65nm process,
  - forging understanding of the proposed technology among potential users,
  - sharing the findings and form collaborations, even with other groups who may be preferring working on other then TSPCo65nm process;
- Universality of the planned development will allow flexible and independent of specific form factor and manufacturing process use in the future.

Answer cont.

Flash view of implementation in X-ray pixel Readout ASIC, challenge of translation to monolithic O(20um) pixels



about 4,000 transistors / pixel (100 ×100 μm^2), 20 : 80 analog : digital

Answer cont.

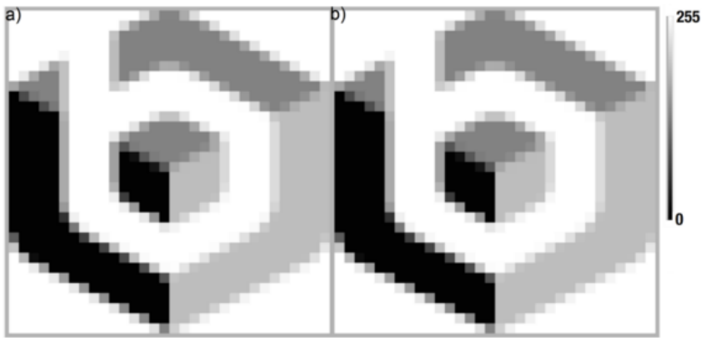


Figure 6: The number of readouts for all pixels represented in a form of an intensity map a) as programmed using the I2C-SPB interface b) as actually read out from the pixels; no difference between them is observed.

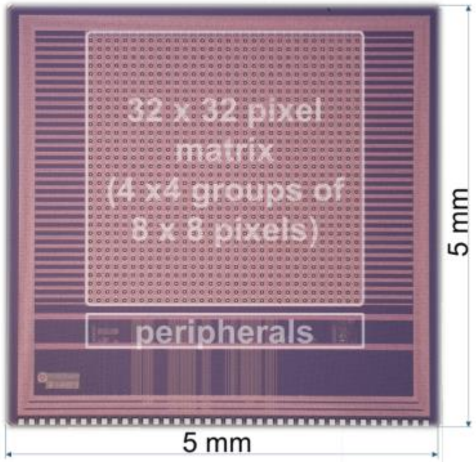


Figure 1: A microphotograph of the 3FI65P1 ASIC with the locations of the matrix of pixels and the peripheral circuitry together with the dimensions of the ASIC marked.

PART 2
Proposal overview

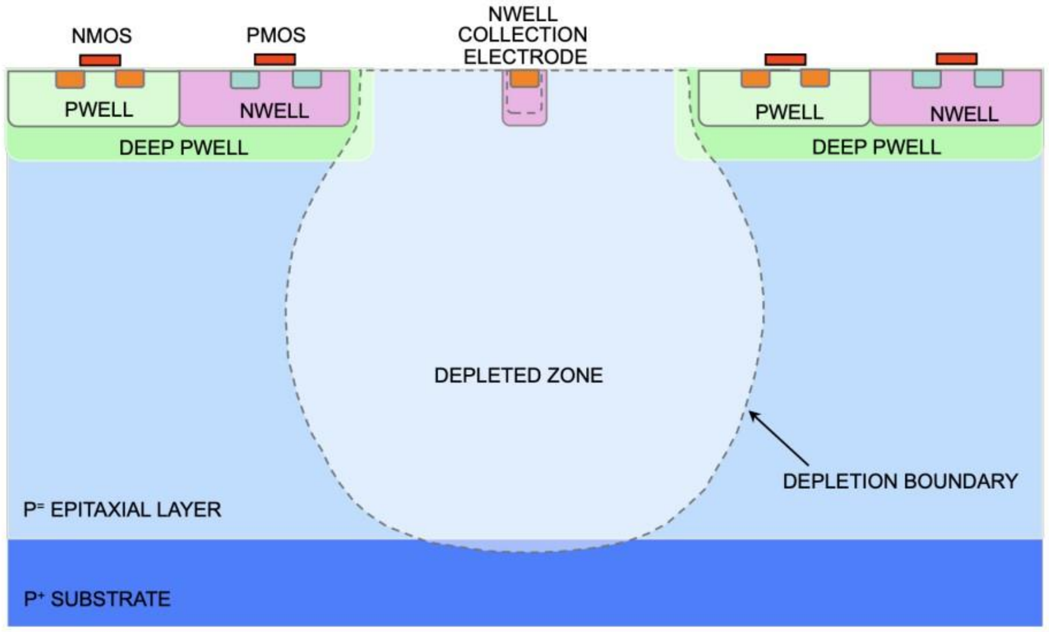
Motivation

Improve design to the EIC requirements based on the existing ALICE ITS3 design – baseline for ePIC SVT inner layers:

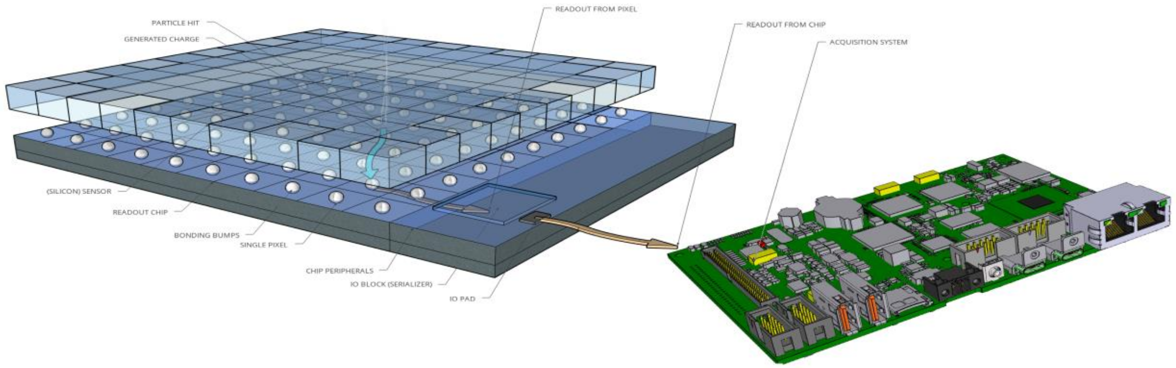
- **improved timing resolution (sub-microsecond, on the order of ~100 ns),**
- low mass,
- low power

MAPS

- The **material budget** and **spatial resolution** requirements of the EIC Vertex and Tracking Detector are only fulfillable by the **Monolithic Active Pixel Sensors (MAPS),** built as Si large-scale chips;
- MAPS **combine the sensor matrix and readout circuitry in one silicon substrate**, unlike the hybrid sensors, where the sensor matrix and readout circuitry are split in two separate silicon pieces;



MAPS example
https://doi.org/10.1016/j.nima.2017.07.046



Hybrid pixel sensor example

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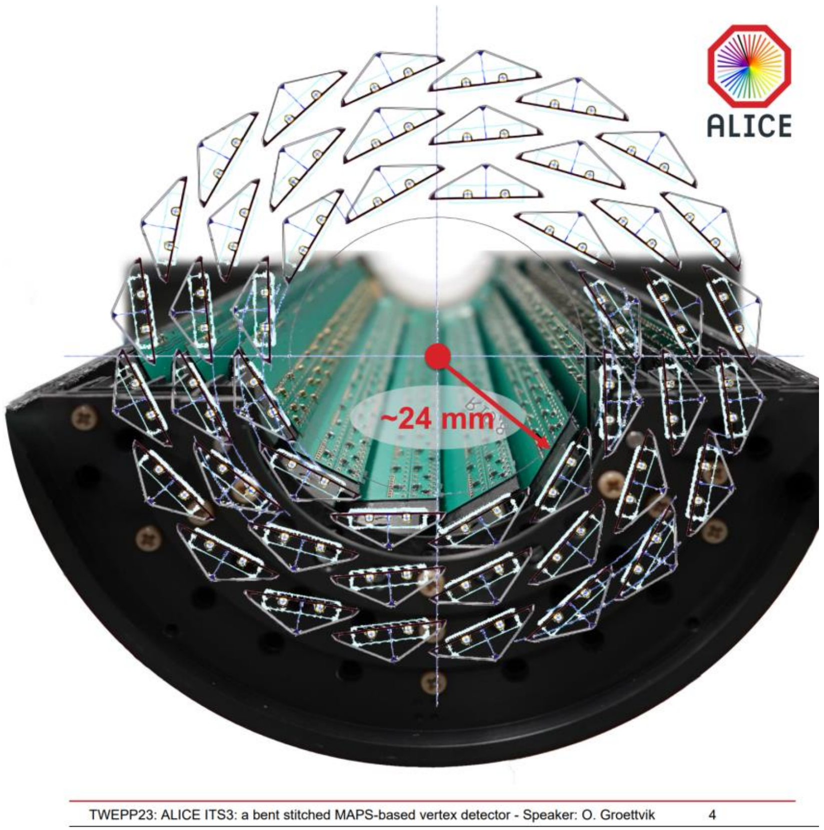
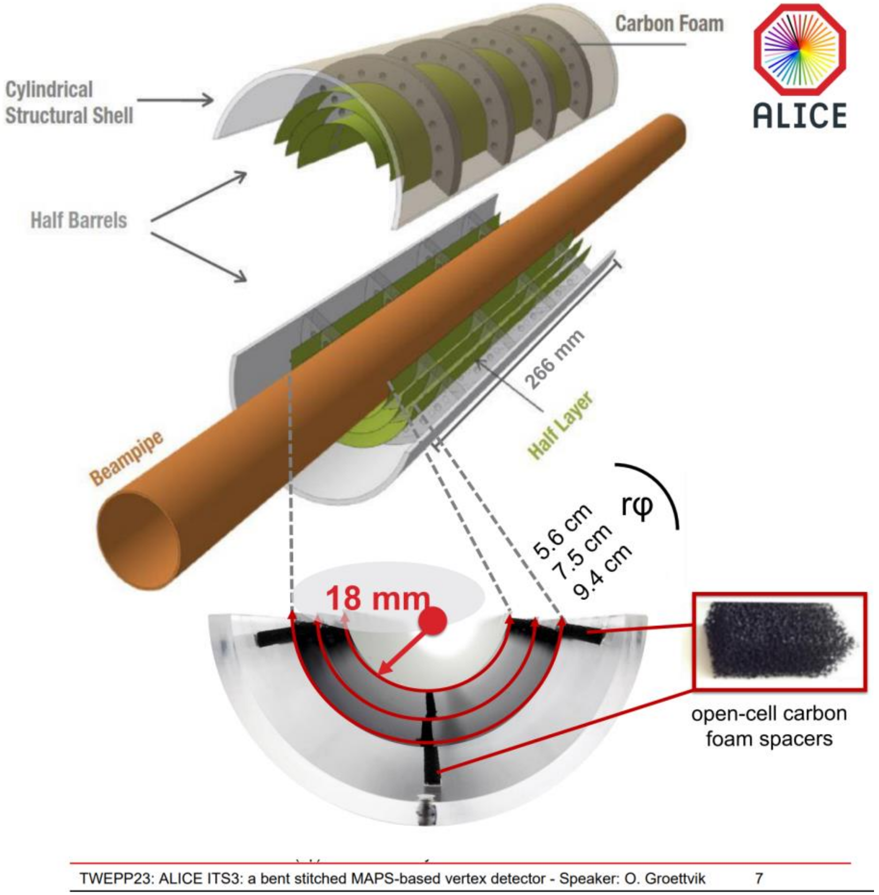
ALICE-ITS3



ITS2

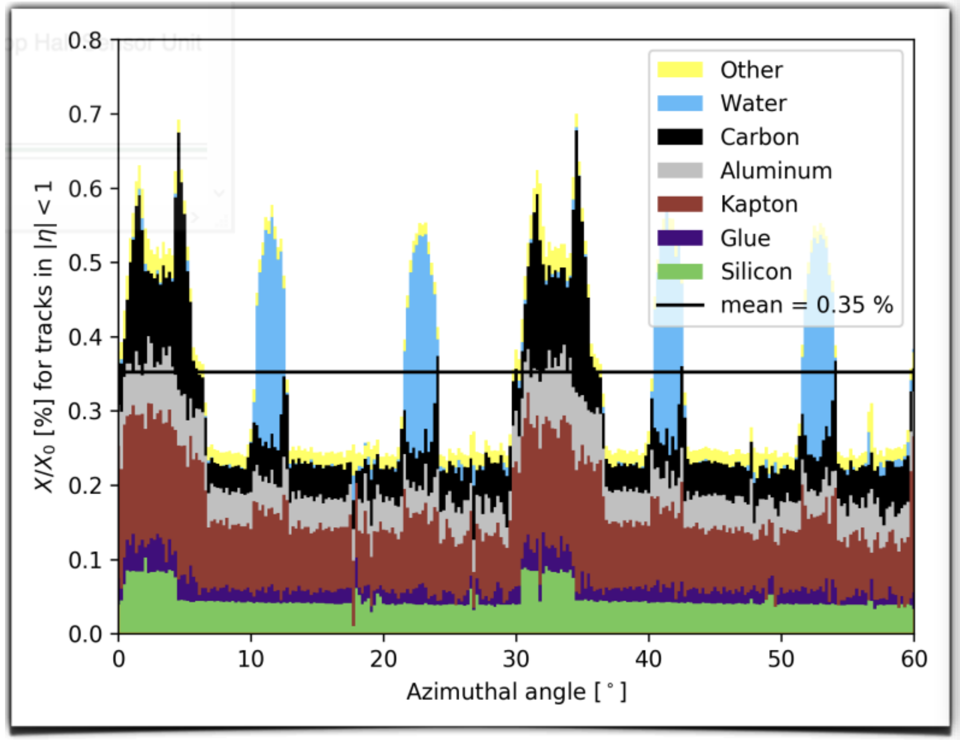


ITS3 → ePIC SVT fork

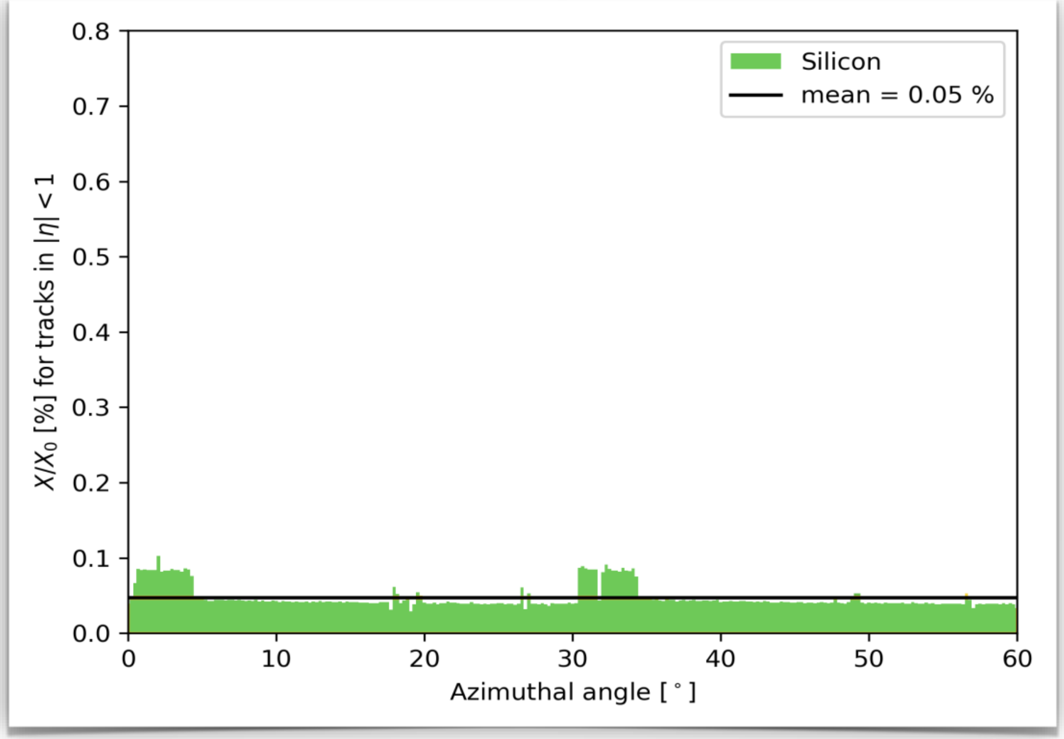
Main goals:

- reduction of power consumption,
- coverage by multiple layers
- reduction of material budget
- elimination of water cooling (in favor of air cooling)

ALICE-ITS3



ITS2



ITS3 → ePIC SVT fork

- Remove water cooling
- Remove the circuit boards
- Reduction of cabling
- Reduction of mechanical support

[TWEPP 2023 Topical Workshop on Electronics for Particle Physics (1-October 6, 2023): ALICE ITS3: a bent stitched MAPS-based vertex detector · Indico (cern.ch)]

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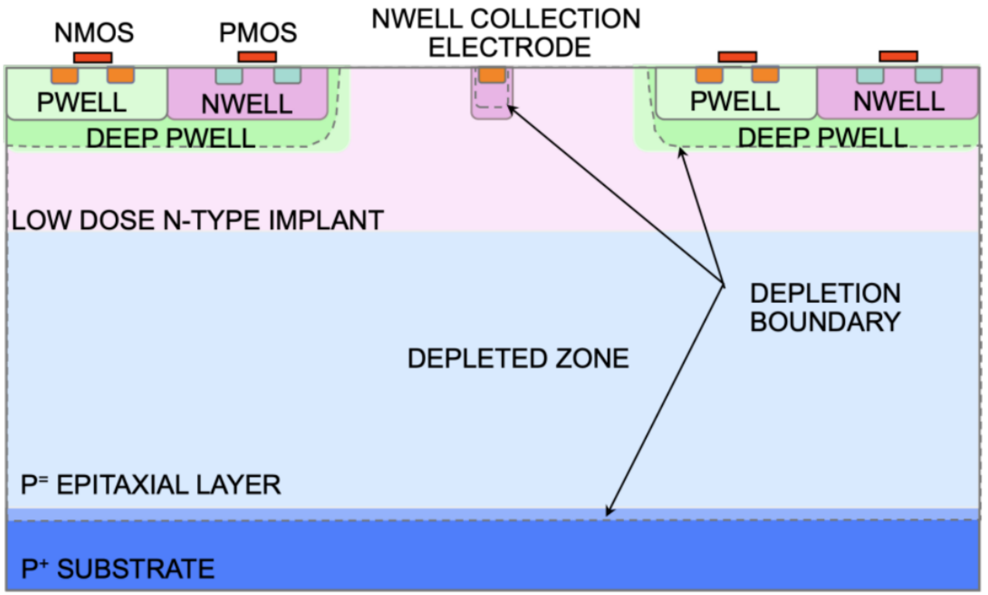
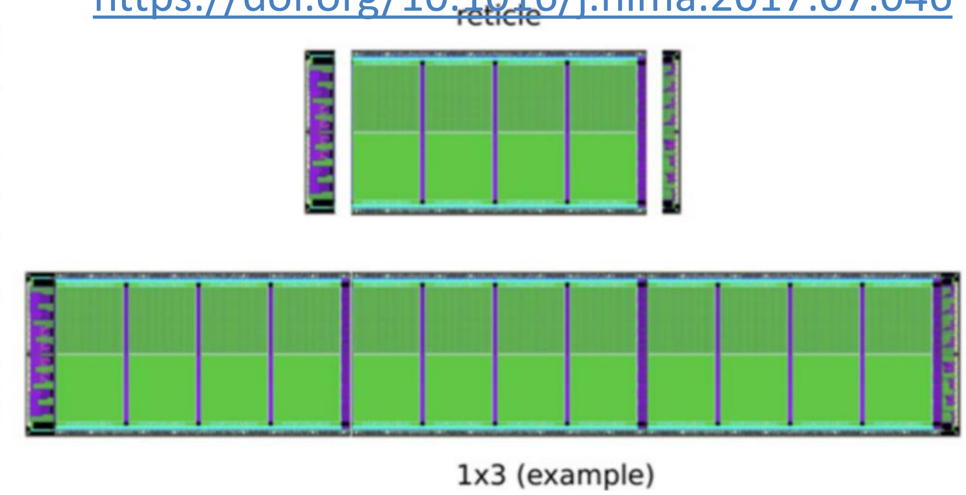
TPSCo 65nm

- The TPSCo (Tower Partners Semiconductor Co.) 65 nm process is the state-of-the-art CMOS process for image sensors.
- TPSCo65nm is continuation of Tower-Jazz 180nm, which was successfully used for all layers of the ALICE-ITS2.
- Stitched sensors (wafer size)



Example of modification of standard proces allowed in TPSCo 65nm

https://doi.org/10.1016/j.nima.2017.07.046



Stiching example

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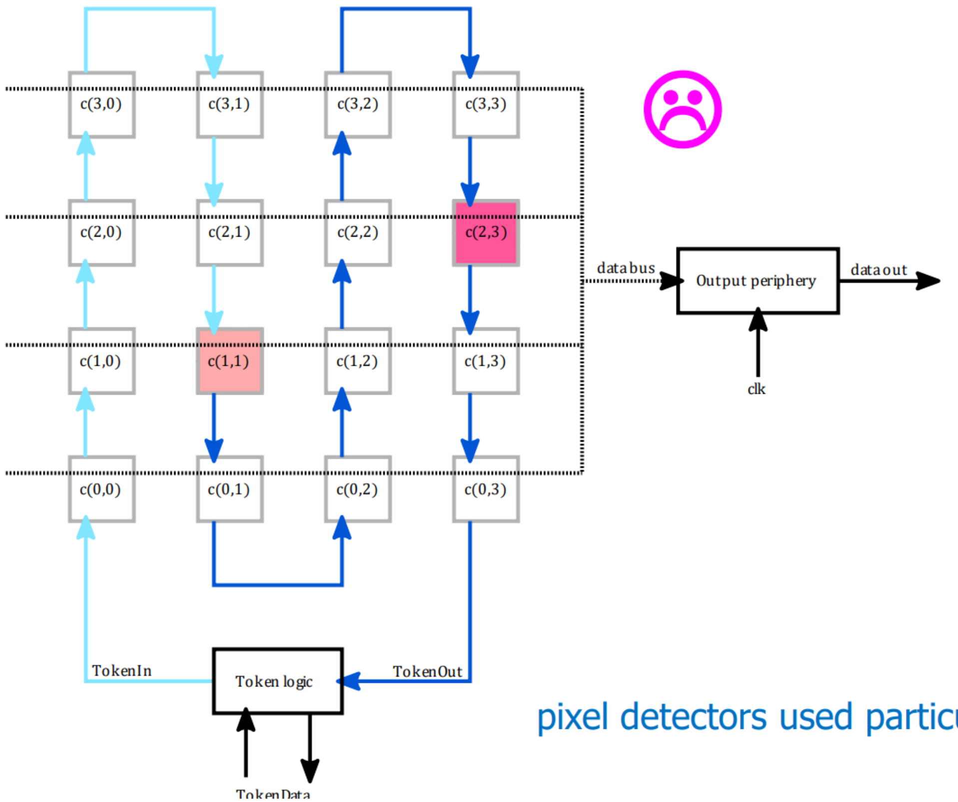
Common Readout Schemes

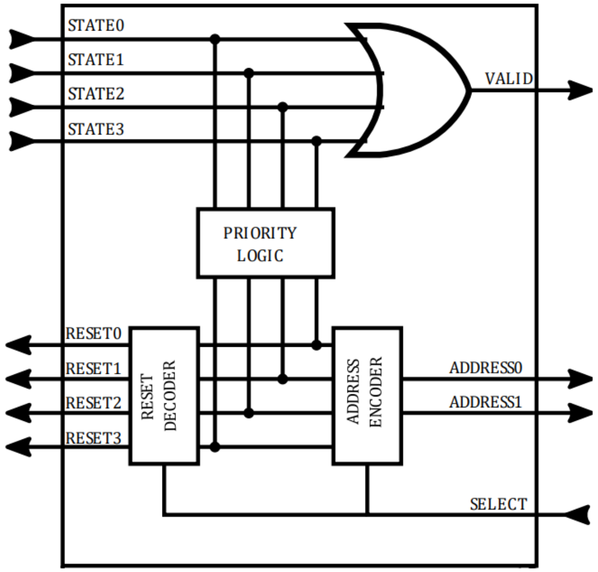
Token passing:

- varying latency (hit first or last pixel in the scan chain)



Priority encoder:

- suited only to framed (snapshoted) readouts



pixel detectors used particularly in fluorescence imaging needs to be event-driven read out

Continuous readout: we are interested in reading signal while they arrive

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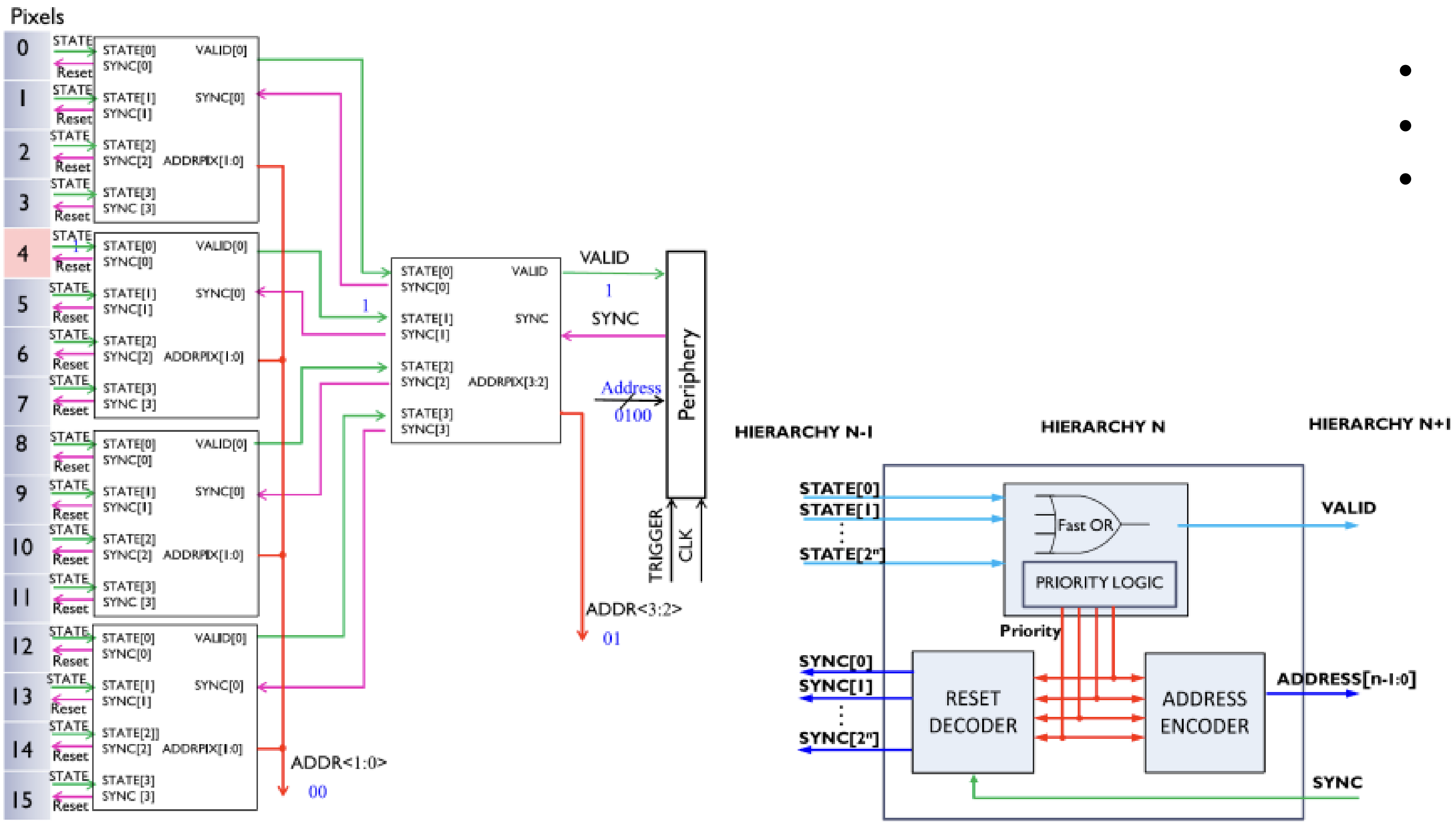
ALICE readout - AERD



(a) (b)

- **Priority encoder**
- Frame snapshots (2 us – 10 us)
- Improvement is not anticipated due to operational mode limitations.

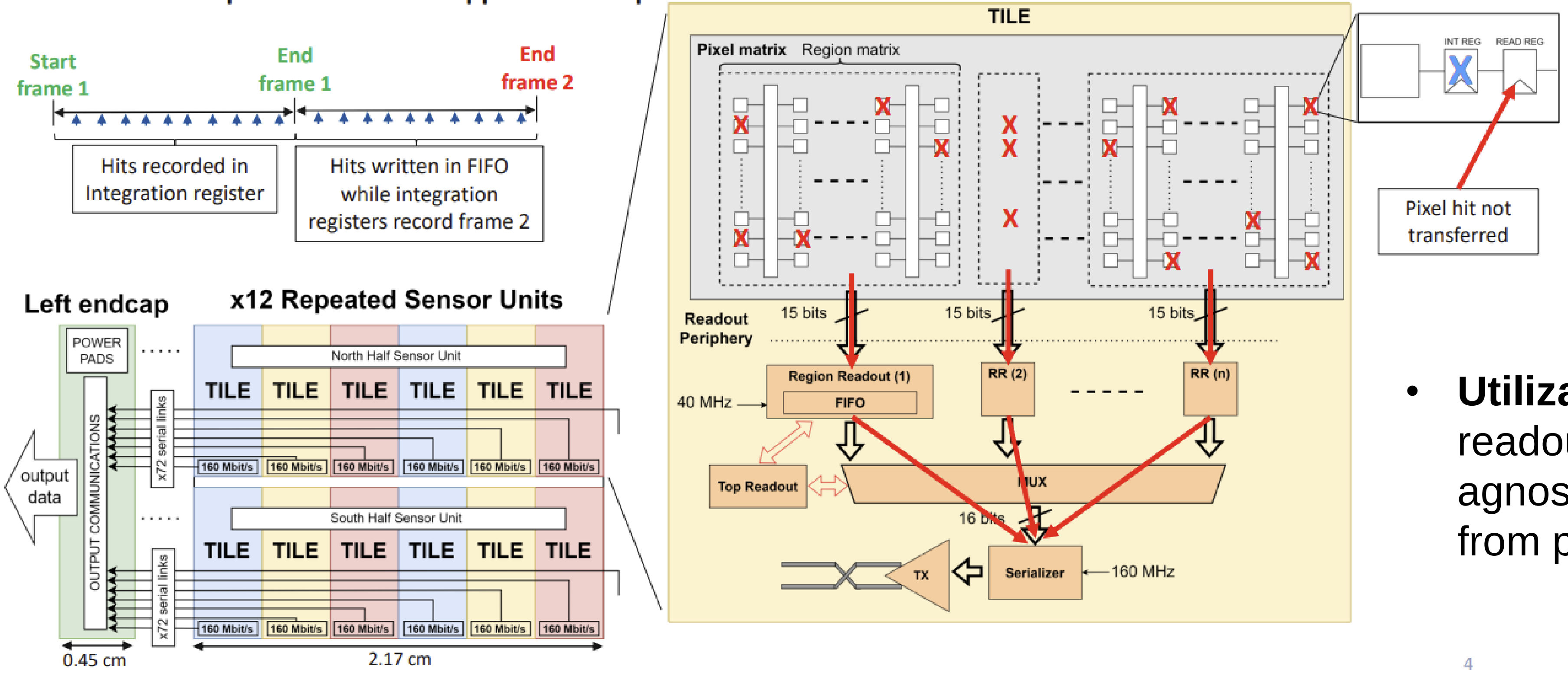
AERD in ALICE-ITS3

On-chip readout scheme

Continuous trigger-less solution

- Hits sent in time stamped packets (**frame packet**)
- **Frame packets must be shipped out completed**

Collision information may be lost depending on the number of detected hits

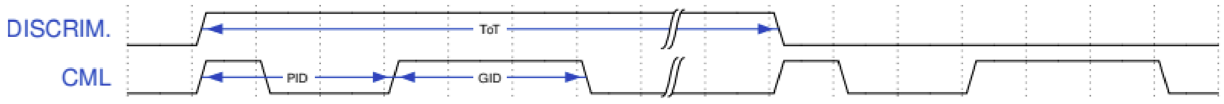


- **Utilizable platform** with readout periphery largely agnostic of how data from pixels is flowing in;

[TWEPP 2023 Topical Workshop on Electronics for Particle Physics (1-October 6, 2023): Model and analysis of the data readout architecture for the ITS3 ALICE Inner Tracker System · Indico (cern.ch)]

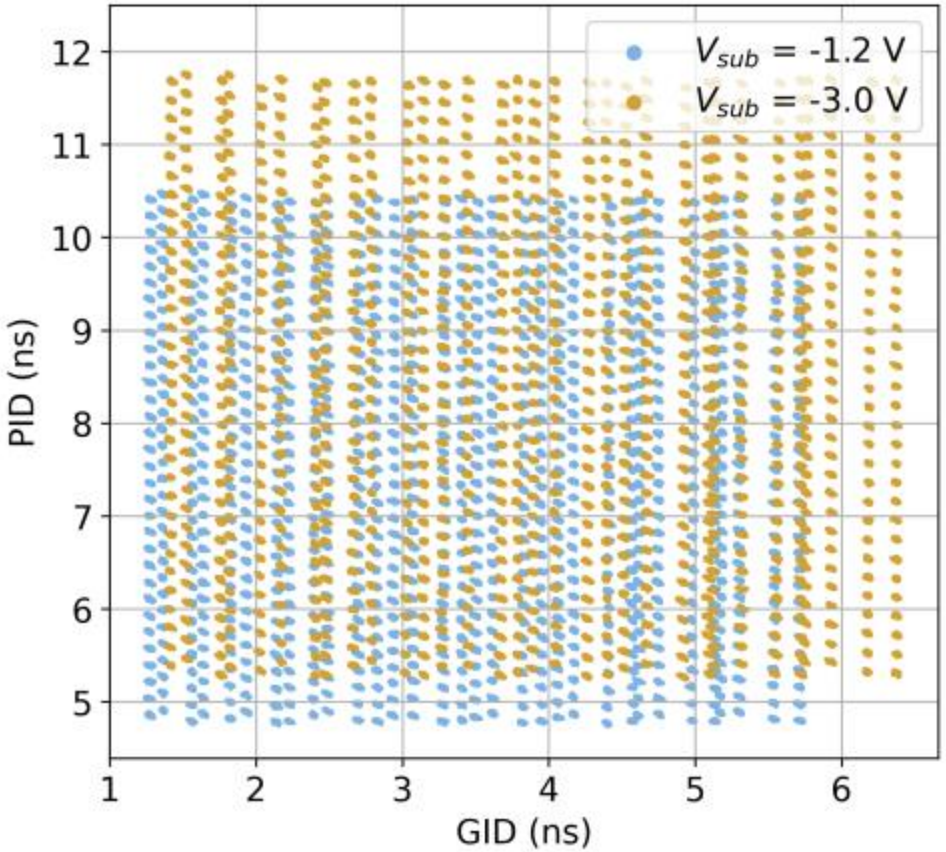
DPTS idea

Awareness of the **limits of the priority-encoder-based readout** is apparent and research on event-driven readouts is commonly carried out, but no success so far, e.g.:



The Digital Pixel Test Structure (DPTS) is CERN's MAPS prototype MAPS in TPSCo65 nm process by CERN. DPTS encodes position in the time-domain position:

- in-pixel discriminators trigger address generators to send two consecutive pulses on the CML outputs with a duration based on the pixel positior
- duration of the first pulse is fixed,
- time distance between the two pulses encodes th pixel position in a group of columns (PID);
- duration of the second pulse encodes the column group position in the matrix (GID).



VERY SENSITIVE to any differences (including ageing) of operation points, biases, etc.

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Digital Pixel Test Structures implemented in a 65 nm CMOS process (arxiv.org)

EDWARD – Event Driven With Access and Reset Decoder

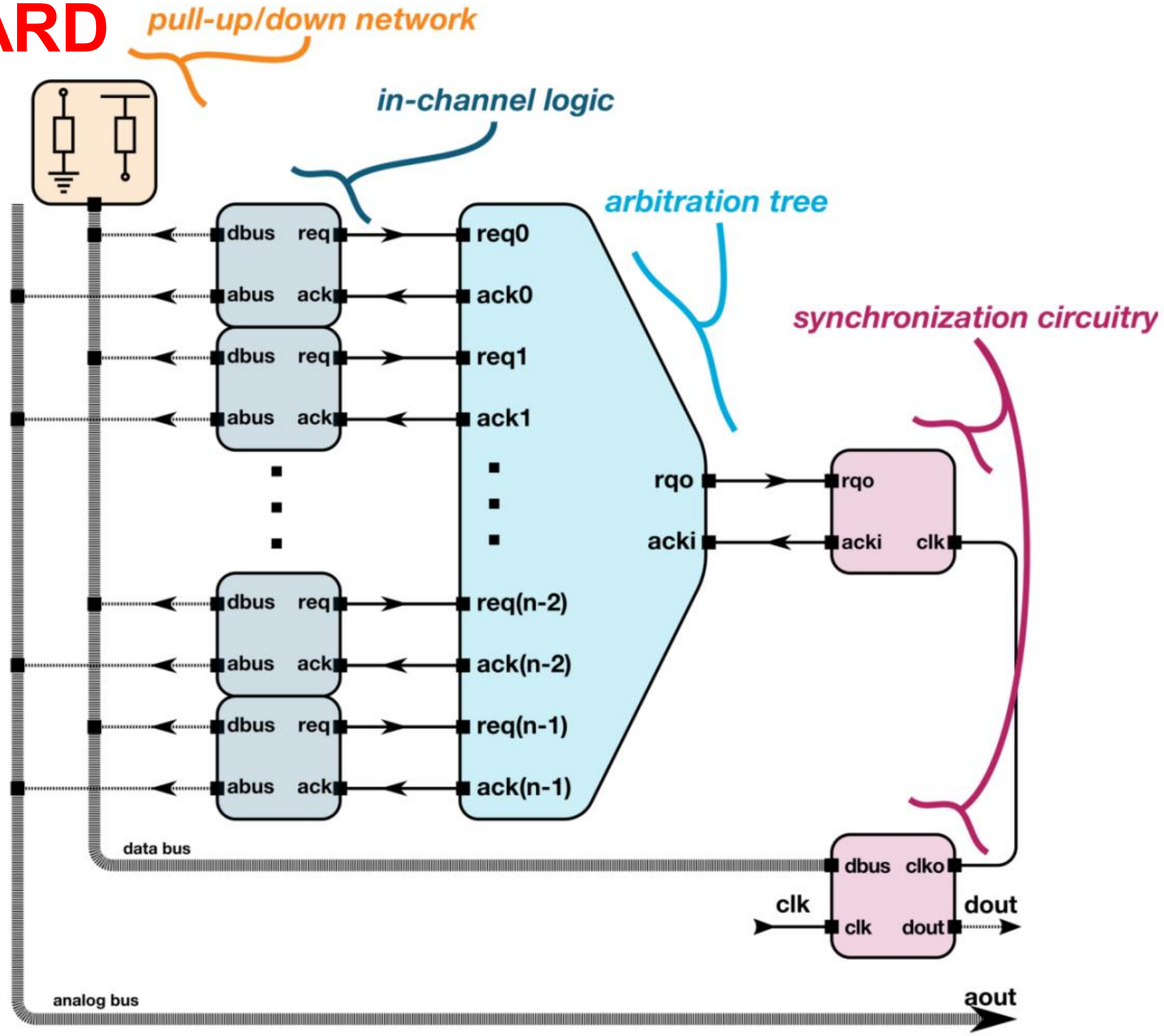
no success so far, **except BNL's EDWARD**

Reset decoder provides guaranteed readout time for each transaction, and no dead time between them

No need to provide a clock to each pixel - requests can be sent asynchronously

Uninterrupted access to data within a pixel

No priority encoder



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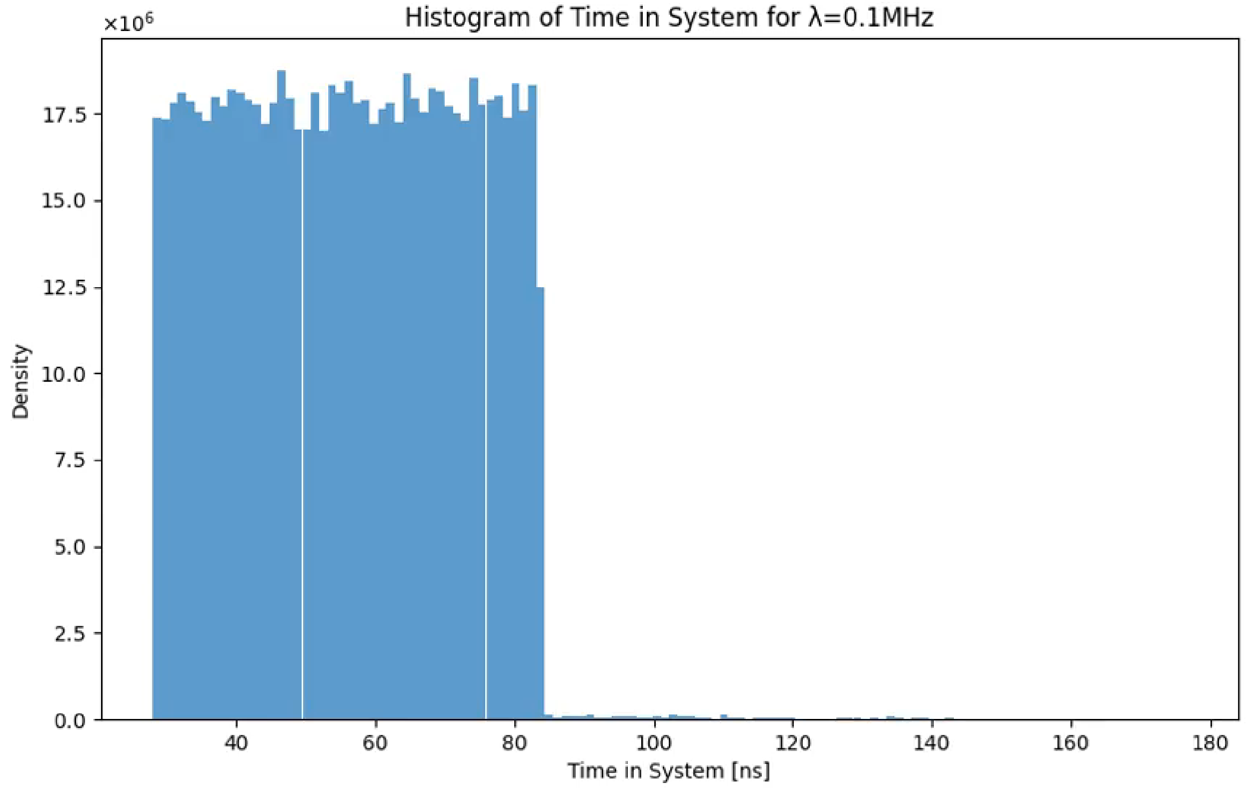
Gorni, D. S., et al. "Event driven readout architecture with non-priority arbitration for radiation detectors." *Journal of Instrumentation* 17.04 (2022): C04027.

Readout latency in EDWARD (delay) -1

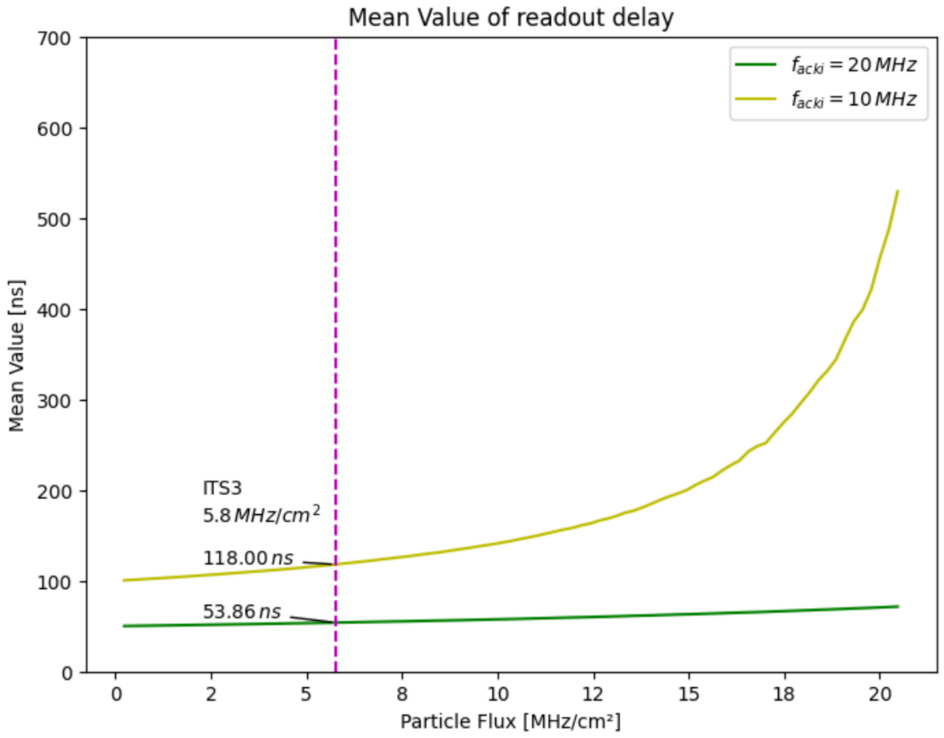


Assumptions in the example:

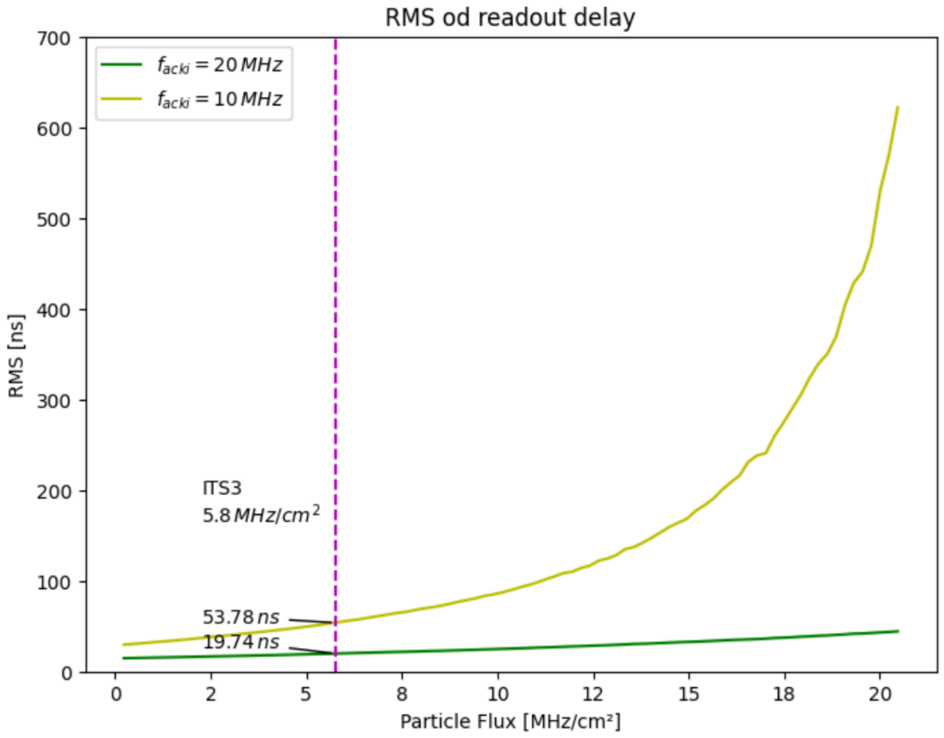
- 1024 independent pixels with Poisson process generator (rate λ);
- readout clock equal to 250 MHz/14 = 17.86 MHz

Readout latency – time passed from generating the event to latching data in the periphery

Readout latency (delay) – 2



(a)

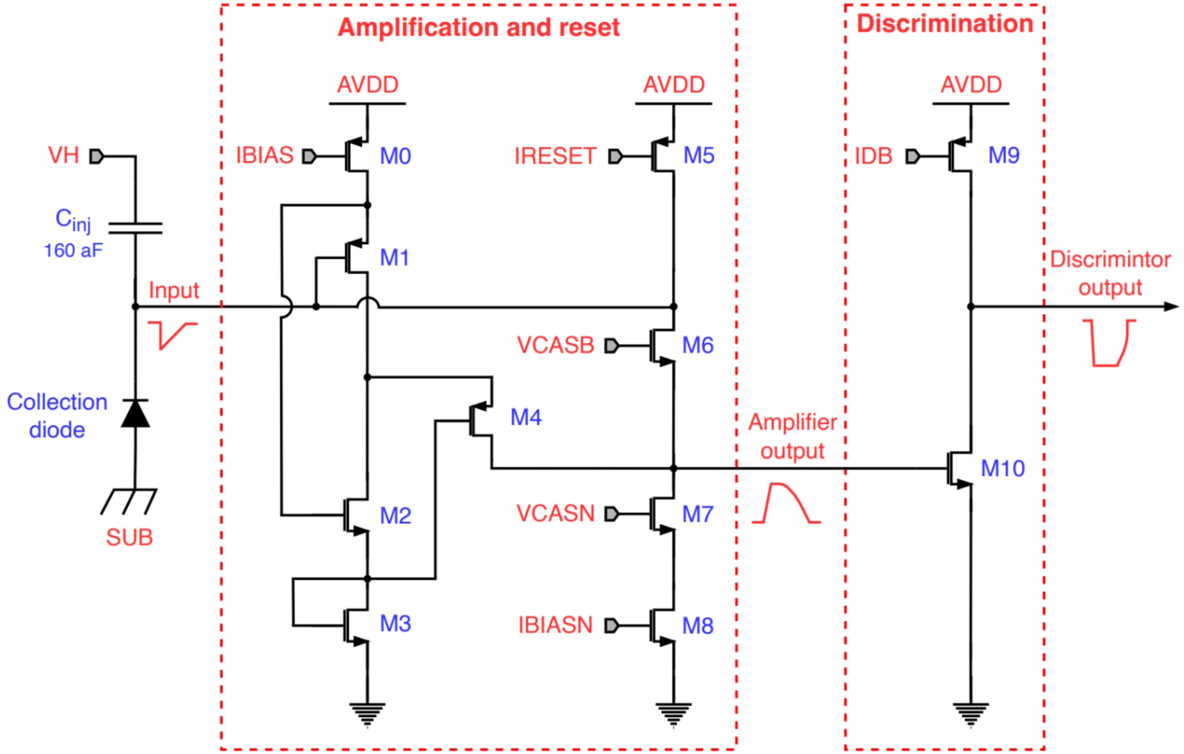


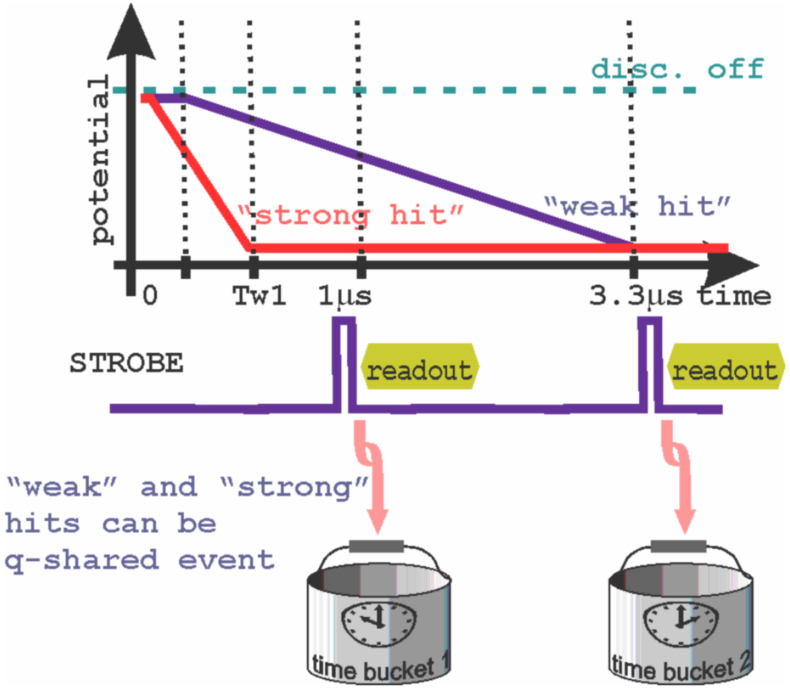
(b)

The mean and RMS of readout latency as a function of particle flux (~event generation) for different readout clock speeds.

Low-Power Front-End Design

ALICE-ITS3 – modified ALPIDE FE





ALPIDE's Front-End is suitable for framed readout but it is not enough beyond:

- Time-Walk is shaded by frame durations;
- hand-shake with priority-encoder-based readout uses global STROBE;
- does not amplify input charge;
- needs directly maximizing charge-to-voltage conversion what is slow.

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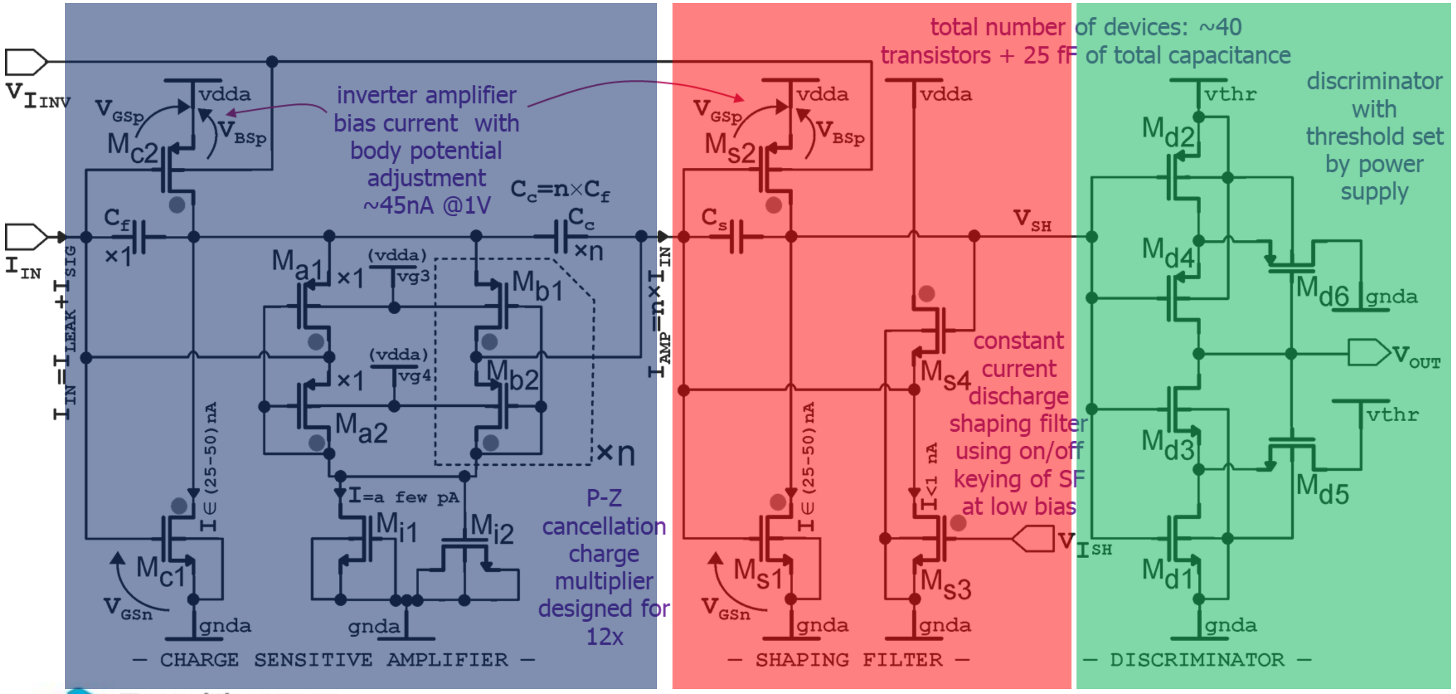
Low-Power Front-End Design

ALPIDE ➡ ALICE-ITS3 Front End:

- does not amplify charge but needs to create voltage amplitude large enough to discriminate;
- high-gain stage operates at low current but does not allow increase of transconductance with signal;
- It is still composed of three stages.

Q-amplifying FE developed in Electron Microscopy LDRD at BNL



Q-amplification | I-const. discharge | discriminator

Direction for proposed FE paved by Electron Microscopy MAPS LDRD at BNL using SCFET amplifier for charge multiplication:

- Low DC bias with signal-dependent increase (low power X0 nW),
- Capacitive arithmetic charge multiplication;
- Fast rise time and constant current discharge,
- Discriminator with hysteresis and threshold applied as power supply
- Minimal (2) number of biases,

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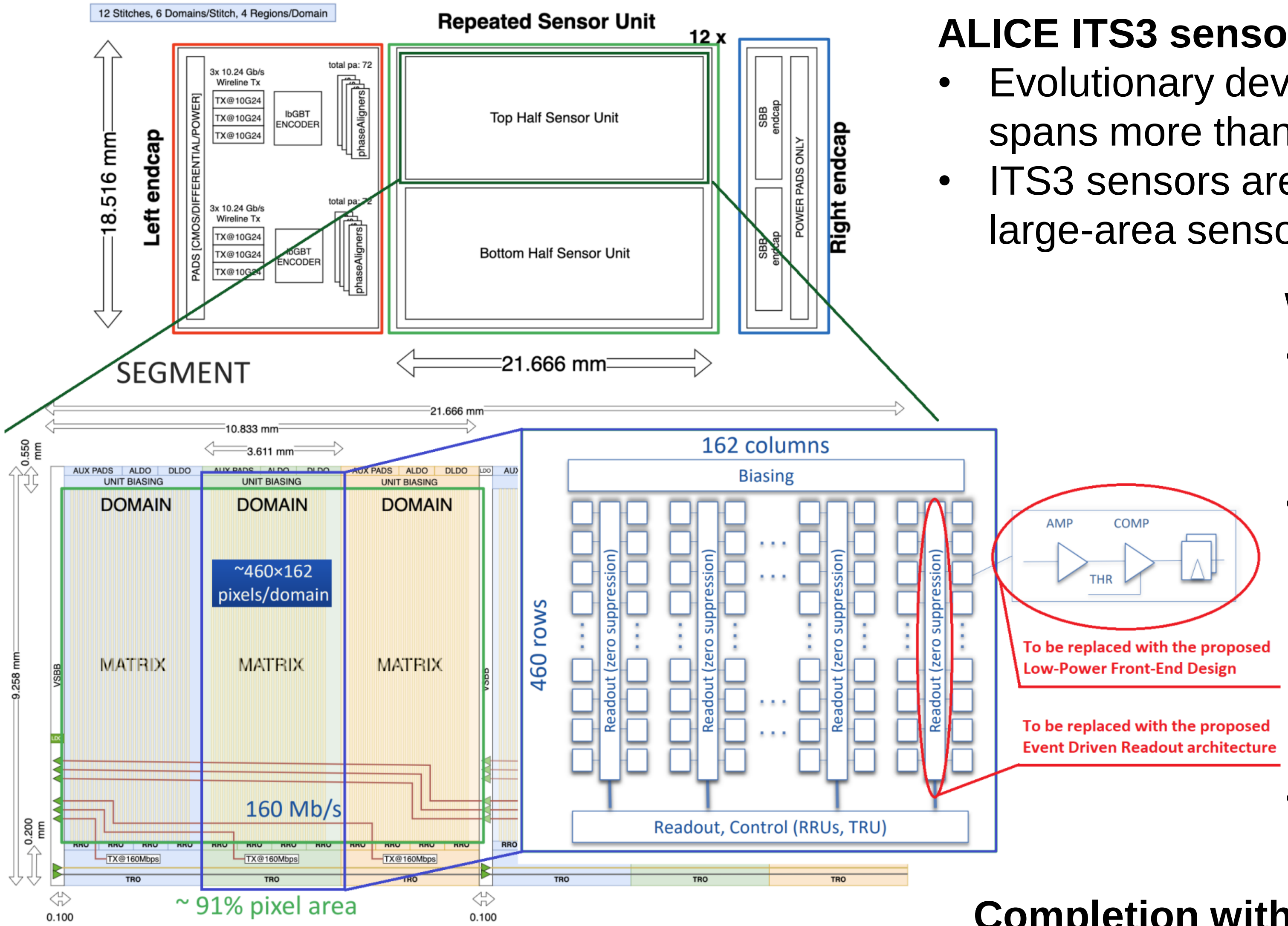
Plan for substituting ALICE ITS3 RSU



ALICE ITS3 sensors – baseline for ePIC SVT:

- Evolutionary development of ALICE-ITS2 / ITS3 sensors spans more than a decade and carries degree of legacy;
- ITS3 sensors are not finalized and efforts of getting large-area sensors operational are significant.

We favor risk and effort minimization:

- Repeated Sensor Unit (RSU) plug to peripheral transmission blocks (@160Mbps/domain);
- Priority-Encoder and EDWARD both produce addresses of hit pixels and minimal effort should be required to substitute RSU with priority-encoder-based readout by RSU with EDWARD – this will be studied!
- Adaptation of the interface is good ground to work with **the universities**

Completion with Front-End and interface:

- LP charge amplification and simple discrimination

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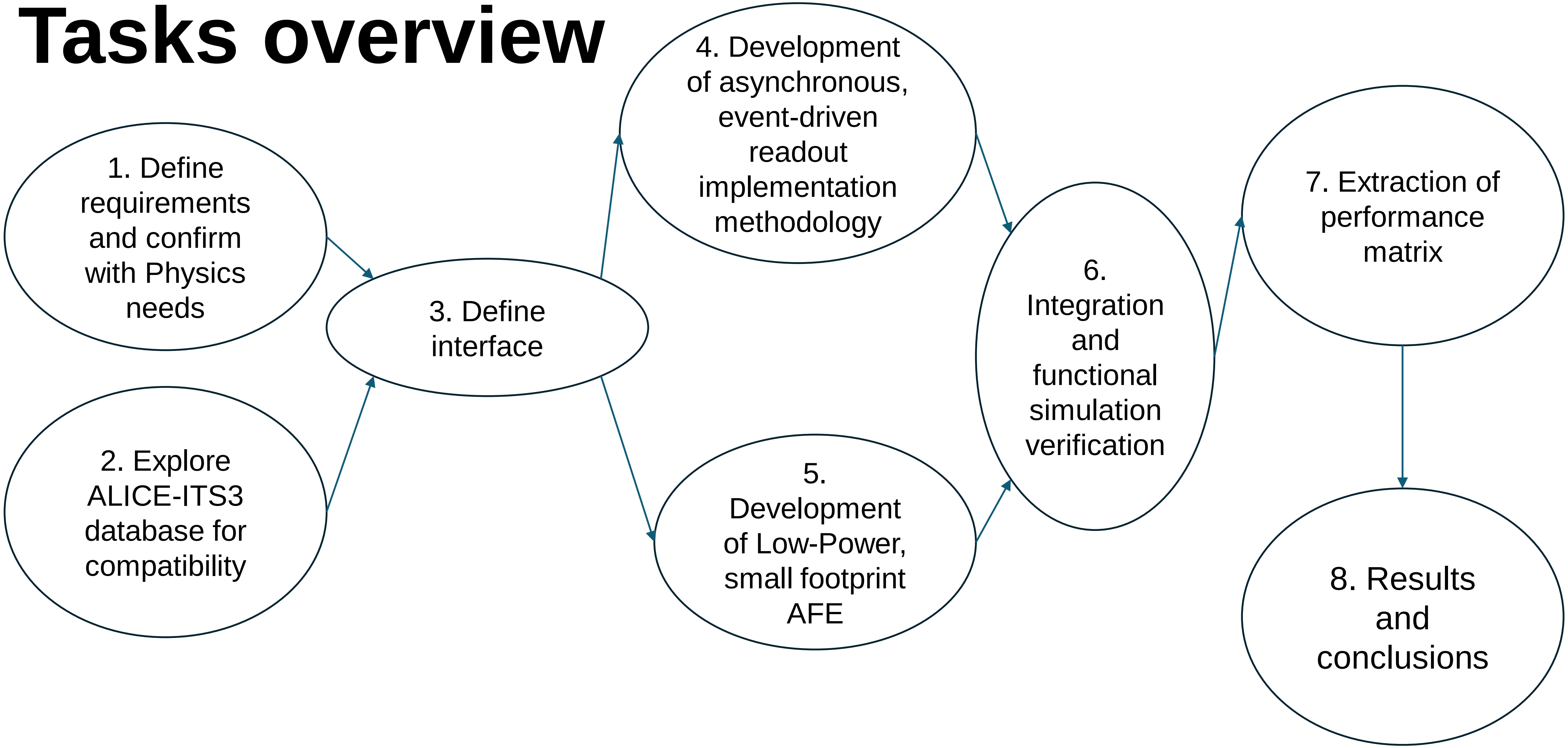
Tasks overview



EDWARD and CSA with SCFET are
BNL's patent pending technologies

PART 3
Q&A

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Backup

Tasks overview

Quoted as in proposal:

- Task 1: Determine detector operating conditions, requirements and needs to compare the capabilities of the ITS3 detector with the proposed new solution.
- Task 2: ITS3 database exploration and environment configuration.
- Task 3: Development of architectural adaptations in the detector database.
- Task 4: Integration of EDWARD readout architecture into the database.
- Task 5: Incorporating Low Power AFE into the database.
- Task 6: Functional verification of the detector with the new circuits.
- Task 7: Comparison of the performance obtained with the assumptions made.
- Task 8: Creating the proposal of the new SVT detector which exploits the advantages of the increased timing resolution and low power design.

Tasks overview cont.

Table 2: Proposed project timeline

Month	Task 1	Task 2	Task 3	Task 4	Task 5	Task 6	Task 7	Task 8
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								

Deliverables

The key project deliverables are summarized below for the following budget scenarios:

- **Scenario 1**: Realistic nominal budget (baseline budget).
- **Scenario 2**: Nominal budget minus 20%.
- **Scenario 3**: Nominal budget minus 40%.

Deliverable	**Scenario 1**	**Scenario 2**	**Scenario 3**
Documentation of the design requirements	Month 3	Month 3	Month 3
Design and simulation results of the RSU with the proposed readout circuitry	Month 11	Month 11	Month 11
Design and simulation results of the RSU with the proposed AFE	Month 11	Month 11	N/A
Comparison report with proposal of the new SVT detector	Month 12	N/A	N/A

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Budget

			NOMINAL BUDGET		NOMINAL BUDGET - 20%		NOMINAL BUDGET - 40%	
Sum of Amount			Reporting Year		Reporting Year		Reporting Year	
Cost Type	Group Break Descr	Description	2024	Grand Total	2024	Grand Total	2024	Grand Total
Direct Costs	BNL Direct Labor	Base Labor	$ 59,703	$ 59,703	$ 47,798	$ 47,798	$ 35,809	$ 35,809
		Base Labor - Research Assoc	$ 4,929	$ 4,929	$ 3,907	$ 3,907	$ 2,970	$ 2,970
	BNL Direct Labor Total		$ 64,632	$ 64,632	$ 51,705	$ 51,705	$ 38,779	$ 38,779
	Departmental Charges		$ 10,496	$ 10,496	$ 8,397	$ 8,397	$ 6,298	$ 6,298
Direct Costs Total			**$ 75,128**	**$ 75,128**	**$ 60,102**	**$ 60,102**	**$ 45,077**	**$ 45,077**
Indirect Costs	Indirect Overheads-Project G&A	VAB Common Institutional Recov	$ 33,031	$ 33,031	$ 26,425	$ 26,425	$ 19,818	$ 19,818
		VAB G&A Recovery	$ 7,783	$ 7,783	$ 6,227	$ 6,227	$ 4,670	$ 4,670
	Indirect Overheads-Project G&A Total		$ 40,814	$ 40,814	$ 32,651	$ 32,651	$ 24,488	$ 24,488
	Indirect Overheads - LDRD		$ 4,058	$ 4,058	$ 3,246	$ 3,246	$ 2,435	$ 2,435
Indirect Costs Total			**$ 44,872**	**$ 44,872**	**$ 35,898**	**$ 35,898**	**$ 26,923**	**$ 26,923**
Grand Total			**$ 120,000**	**$ 120,000**	**$ 96,000**	**$ 96,000**	**$ 72,000**	**$ 72,000**

Sum of FTE		Reporting Year		Reporting Year		Reporting Year	
LaborType	Name	2024	Grand Total	2024	Grand Total	2024	Grand Total
SCIENTIFIC	PINAROLI,GIOVANNI	0.07	0.07	0.06	0.06	0.04	0.04
	MANDAL,SOUMYAJIT	0.02	0.02	0.02	0.02	0.01	0.01
	DEPTUCH,GRZEGORZ W	0.02	0.02	0.02	0.02	0.01	0.01
	ASCHENAUER,ELKE C	0.02	0.02	0.02	0.02	0.01	0.01
PROFESSIONAL	GORNI,DOMINIK S	0.18	0.18	0.14	0.14	0.11	0.11
POST DOC	POST-DOC	0.05	0.05	0.04	0.04	0.03	0.03
Grand Total		**0.36**	**0.36**	**0.28**	**0.28**	**0.21**	**0.21**

Sum of Hours		Reporting Year		Reporting Year		Reporting Year	
LaborType	Name	2024	Grand Total	2024	Grand Total	2024	Grand Total
SCIENTIFIC	PINAROLI,GIOVANNI	130	130	103	103	78	78
	MANDAL,SOUMYAJIT	36	36	28	28	21	21
	DEPTUCH,GRZEGORZ W	36	36	31	31	21	21
	ASCHENAUER,ELKE C	36	36	28	28	21	21
PROFESSIONAL	GORNI,DOMINIK S	311	311	248	248	189	189
POST DOC	POST-DOC	95	95	75	75	57	57
Grand Total		**643**	**643**	**513**	**513**	**387**	**387**

Sum of Months		Reporting Year		Reporting Year		Reporting Year	
LaborType	Name	2024	Grand Total	2024	Grand Total	2024	Grand Total
SCIENTIFIC	PINAROLI,GIOVANNI	0.84	0.84	0.67	0.67	0.51	0.51
	MANDAL,SOUMYAJIT	0.24	0.24	0.19	0.19	0.14	0.14
	DEPTUCH,GRZEGORZ W	0.24	0.24	0.21	0.21	0.14	0.14
	ASCHENAUER,ELKE C	0.24	0.24	0.19	0.19	0.14	0.14
PROFESSIONAL	GORNI,DOMINIK S	2.10	2.10	1.67	1.67	1.27	1.27
POST DOC	POST-DOC	0.60	0.60	0.48	0.48	0.36	0.36
Grand Total		**4.26**	**4.26**	**3.40**	**3.40**	**2.56**	**2.56**