Slim Edge for LGADs

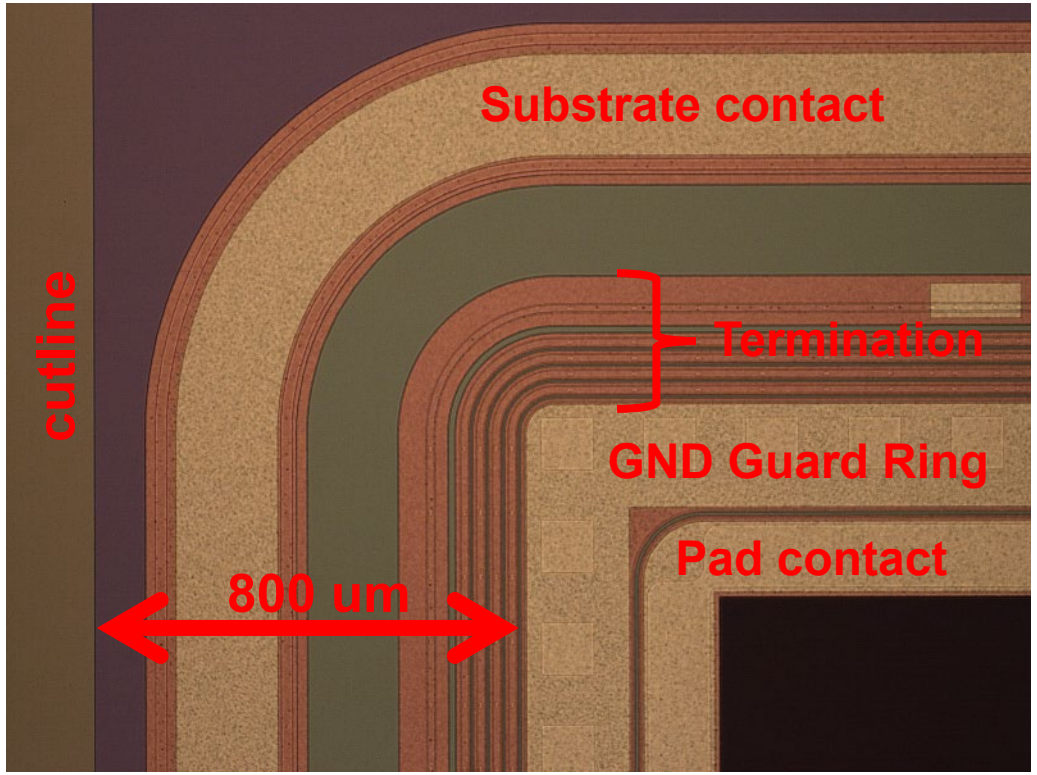
Gabriele Giacomini

EIC-Related Generic Detector R&D Proposal Review Meeting

October 20th 2023

Answers to reviewers' questions - 1

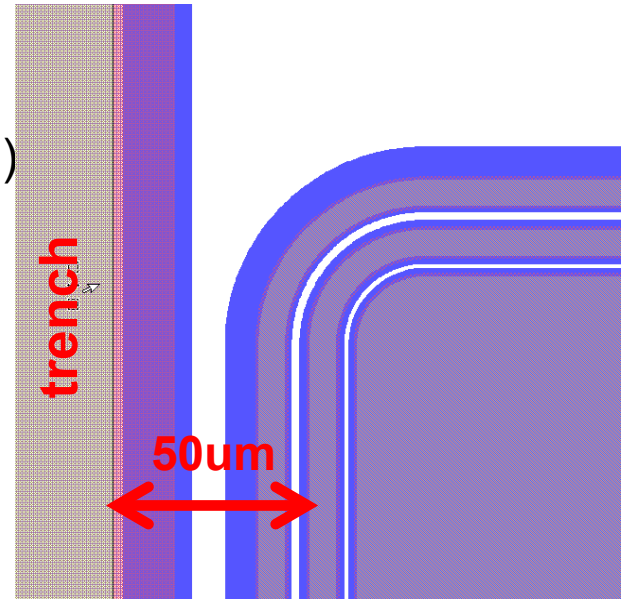
Explain in more detail the designs of the edges.

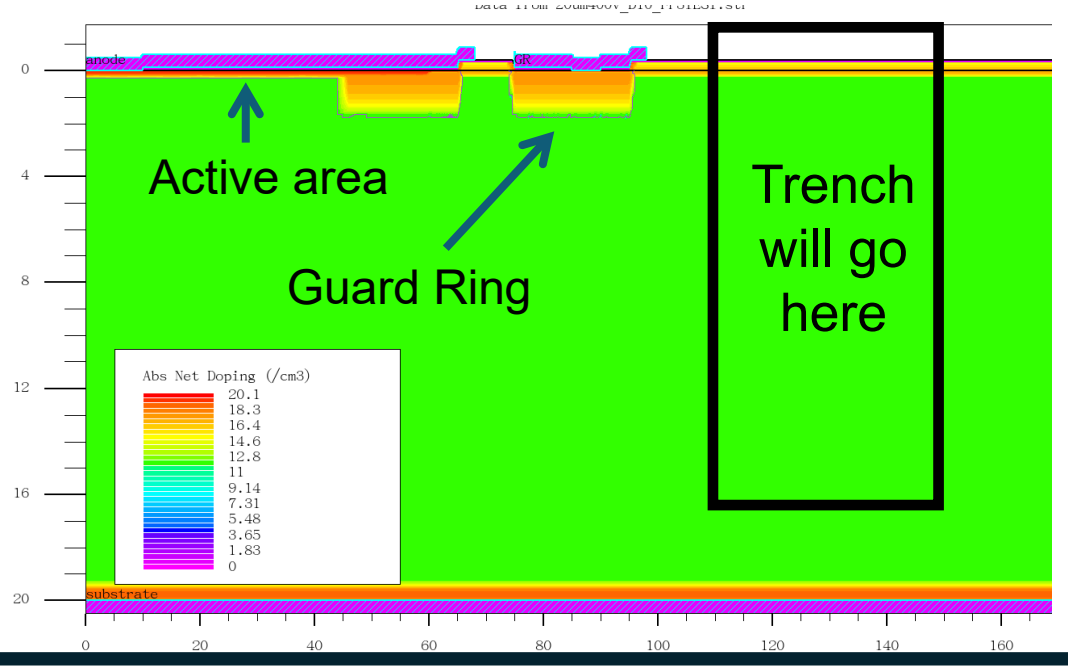


Standard termination,
even for a 20um thick substrate

Modified termination:

(several variants will be designed)
- termination down to 1 floating guard Ring
- shrinking (or elimination) of grounded GR
- Substrate contact smaller and closer



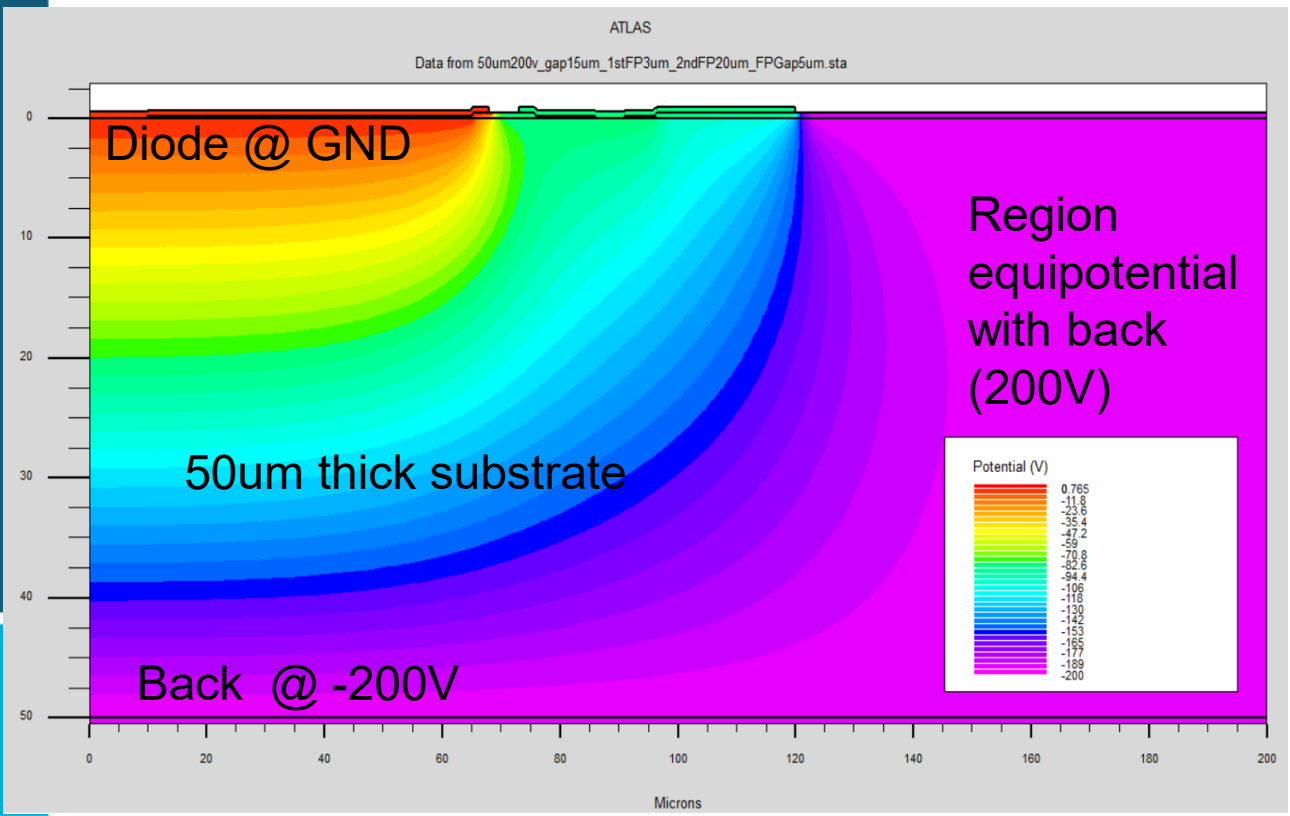


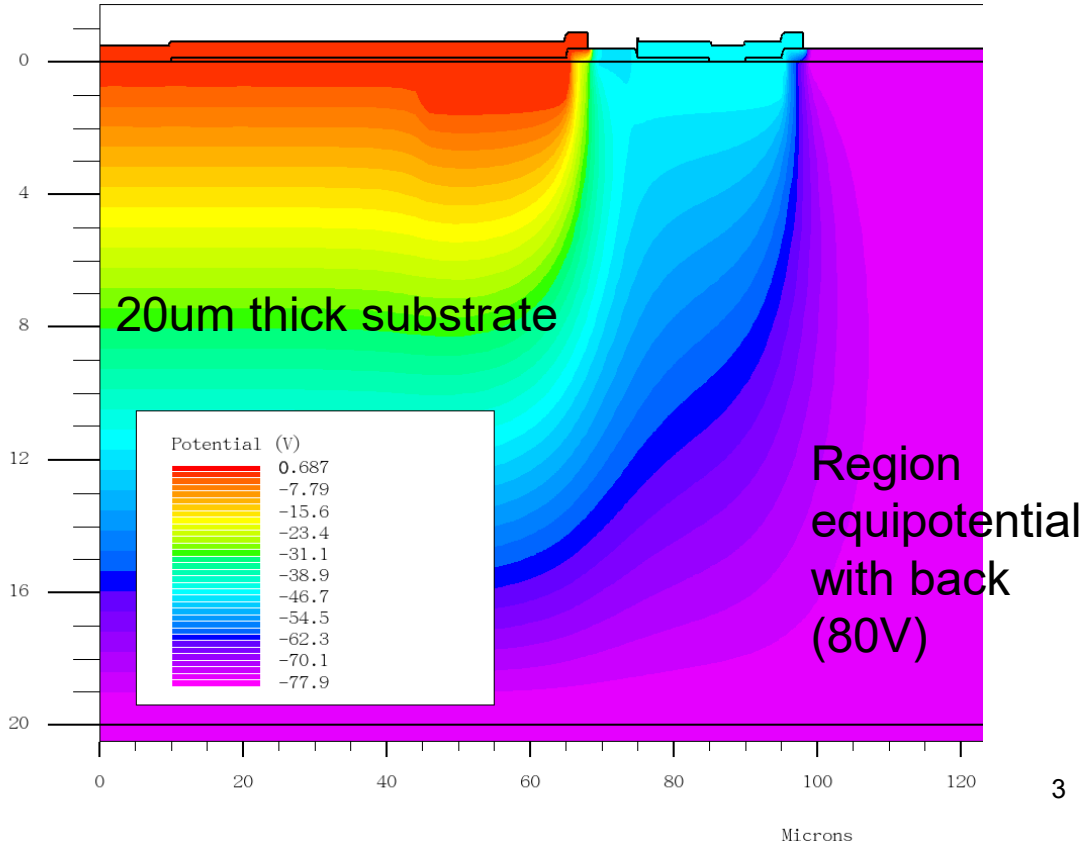
Brookhaven National Laboratory

Answers to reviewers' questions - 2

Is simulation supporting your choices?

Yes, a great deal of TCAD simulations was already carried out by a SULI student this summer (J. Duncan, U, Memphis).
Depletion region hardly extend beyond one GR which is within 50 um from grounded area, even at high voltages.





Answers to reviewers' questions - 3

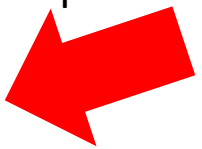
What designs won't be implemented between 100% and 60% financing?

The 4" wafers will be populated with many different designs, to push the limits of the different technologies. The wafers will have a common lithographic mask set, so all designs that we can think of will be implemented.

However, the number of techniques that will be explored to have slim edges will be reduced accordingly.

100% : KOH etch w and w/o alumina deposition, RIE w and w/o alumina deposition, DRIE, …

60%: no DRIE or other ideas which will mature during the projects

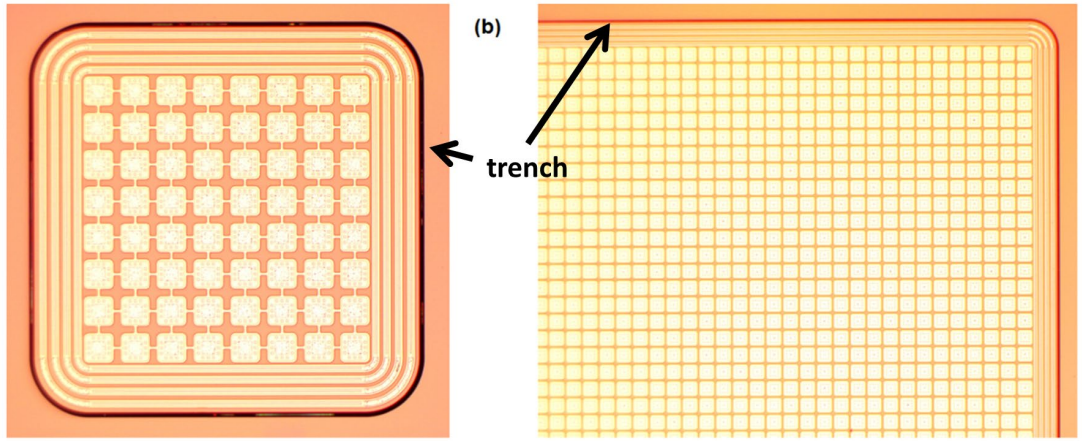


Brookhaven National Laboratory

Answers to reviewers' questions - 4

Why do you not include DRIE (Deep Reactive Ion Etching) in the program? Such a machine may not be available at BNL but they are widely available at University fabs. Inclusion would make the project more complete.

Although we don't have experience in DRIE, we can certainly profit from this project to gain some.
DRIE will require – beside the facility – a furnace for boron diffusion (not a BNL either, but we are users of, for example, Cornell Nanoscale Facility https://www.cnf.cornell.edu/ - so the process can be carried out at Cornell), and PECVD filling to planarize the surface and allow several other lithographies (contact opening, metal, passivation opening).
It is certainly a very elegant and working solution, but it takes some effort (need 100% of funding).



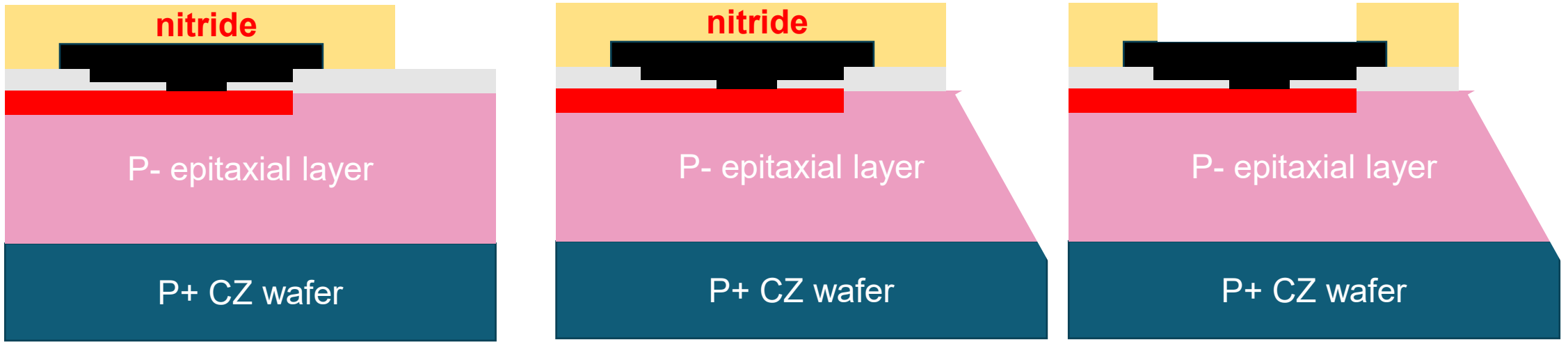
[1] L. Pancheri et al *2016 JINST 11 C12018,*
https://iopscience.iop.org/article/10.1088/1748-0221/11/12/C12018

Answers to reviewers' questions - 5

What lithography is needed after the trench etch? Can it be the last step?

Yes, passivation opening will be the last step.
To resist the KOH attack, a layer of nitride (~ 100nm – already tested) will be deposited. Then we have to open the nitride in the pads area, for testing and contacting. This requires litho.

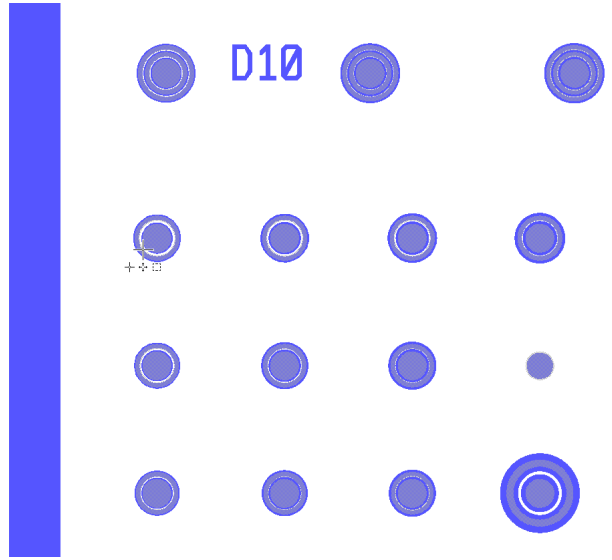
Example of process

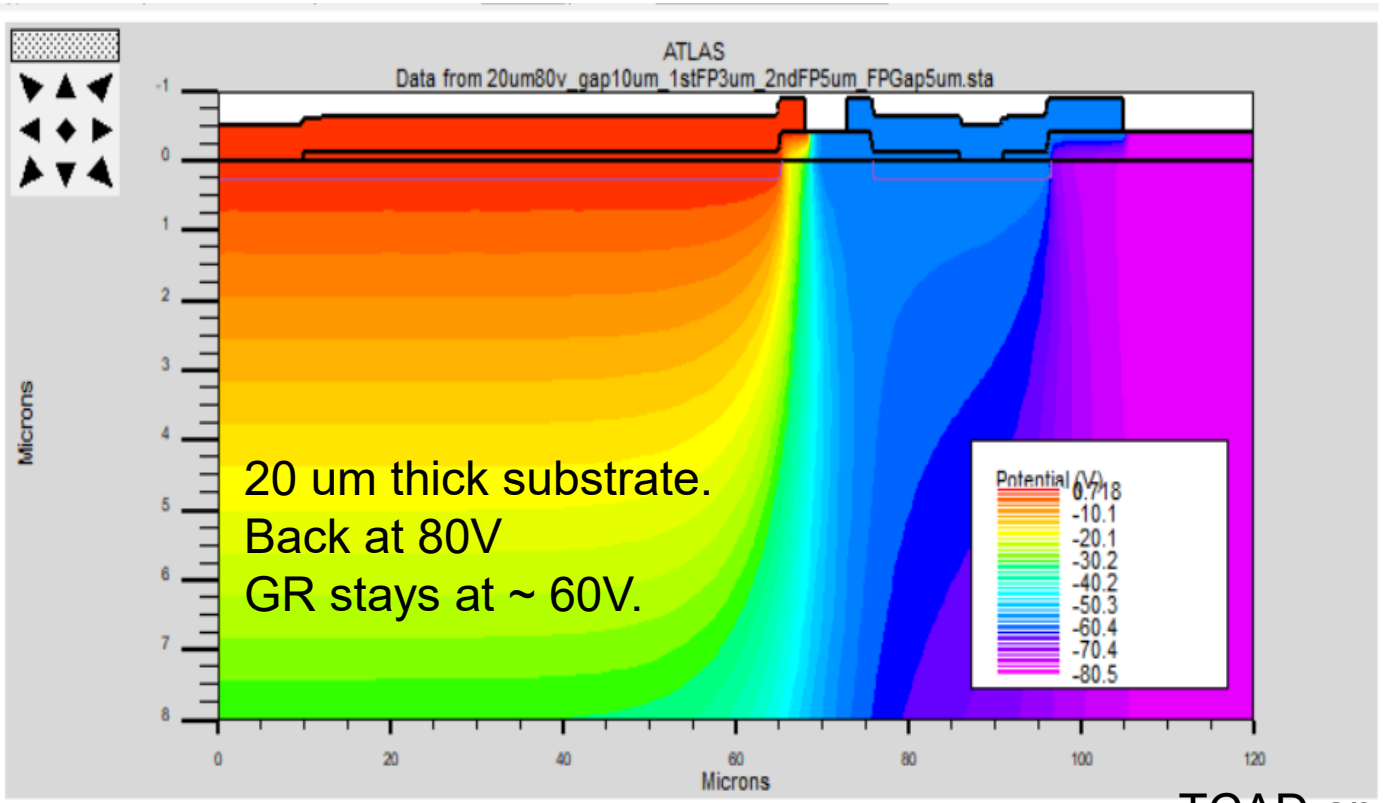


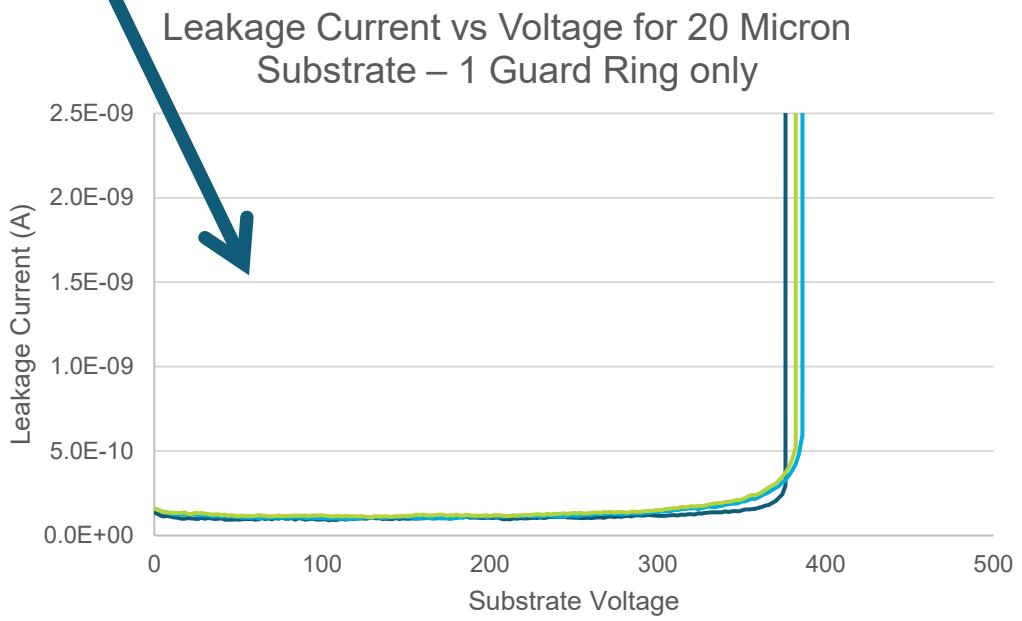
Answers to reviewers' questions - 6

What guard ring geometry do you plan to use? How much space does it take?

In the wafer, there will be placed many design variants, however we'll focus on few GRs, closely spaced, order of ~ 50um or less.
TCAD simulations suggests that, if the substrate is thin, GRs are hardly biased at all.
Measurements on test structures tell that 1 GR is enough to sustain very high voltage.







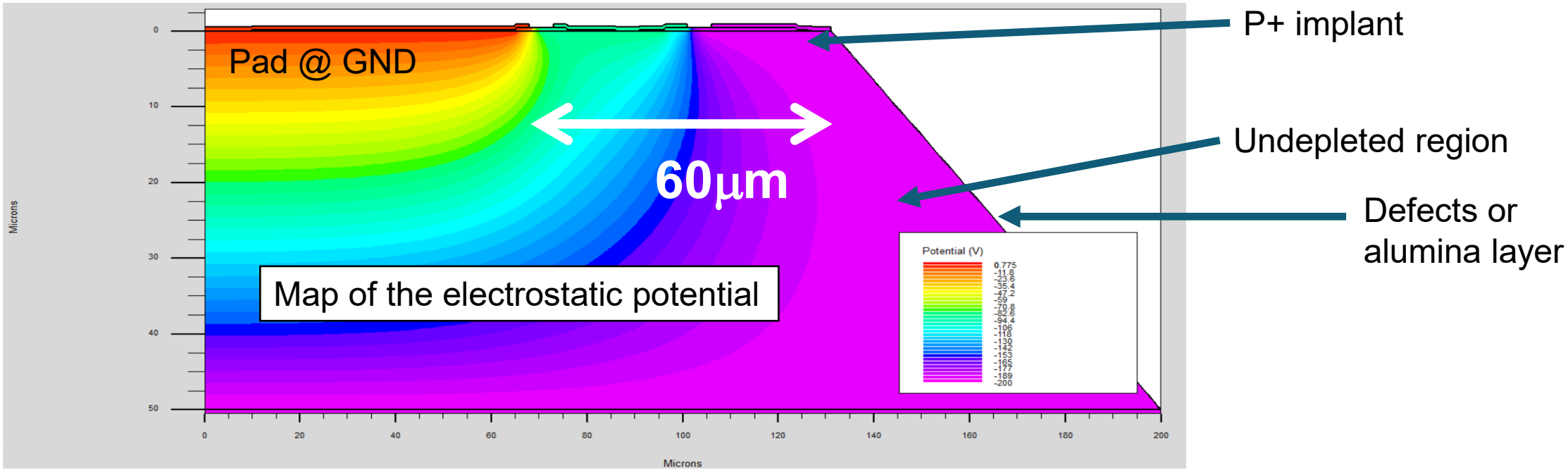
TCAD and I-V by J. Duncan, U. Memphis, SULI 2023

Answers to reviewers' questions - 7

Can the trench be used to isolate the backside from the front so that the front side is at ground potential?

Not in the present plan: both the substrate and the epitaxial active layer are p-type.
The voltage applied to the back propagate to the front side because of:

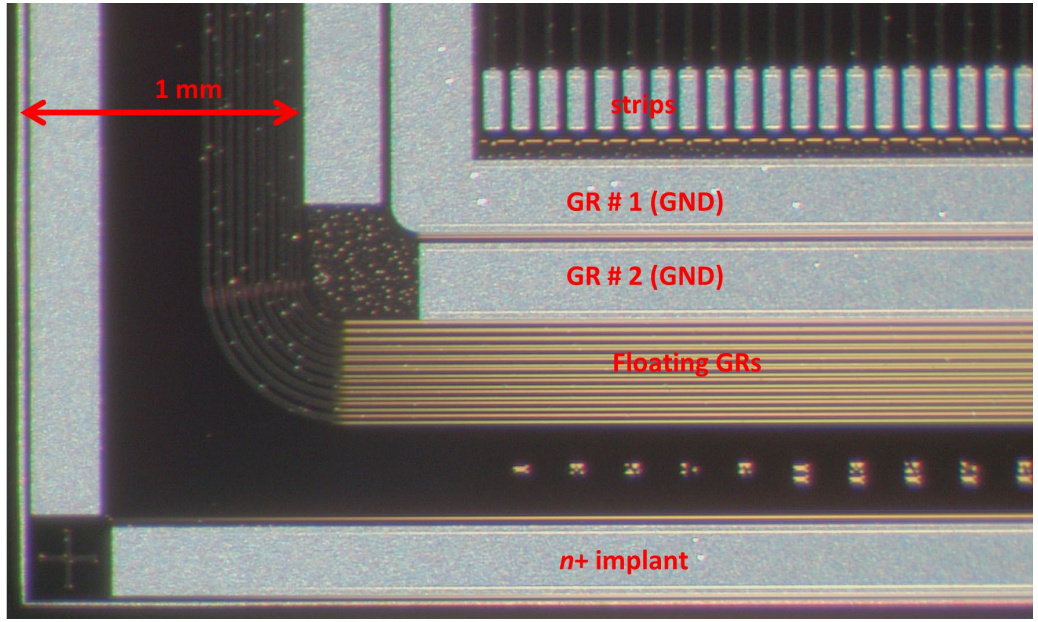
1. the etched/diced wall of the scribeline/trench due to defects
2. by the hole accumulation layer induced by the alumina passivation layer.
3. by the undepleted region at the border (equipotential to the back).
4. at the top surface, at the edge of the device, a p+ layer terminate the surface and is equipotential to the back.



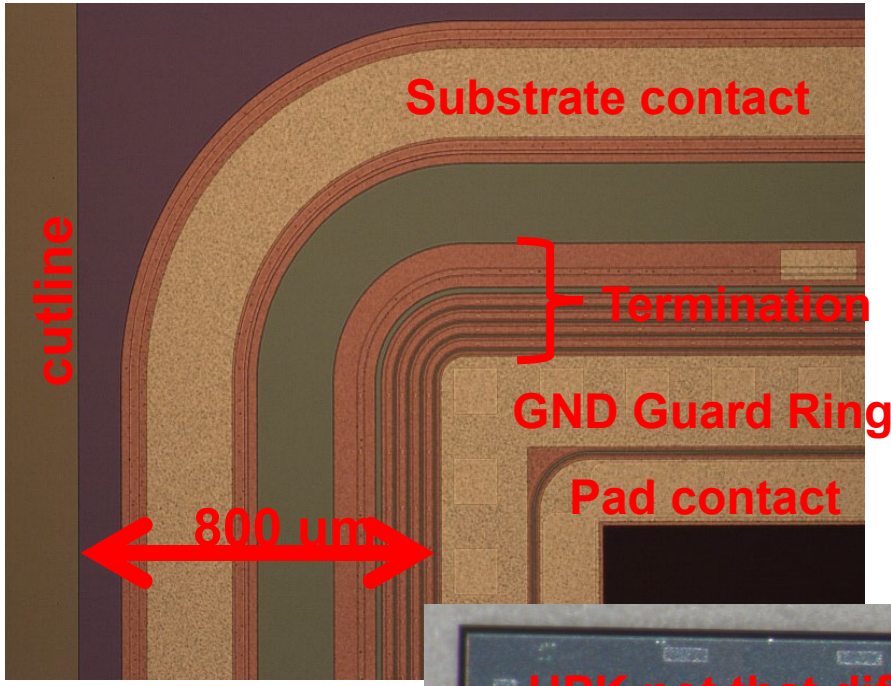
Project description

Standard Termination for silicon sensors

Strip sensor on 300-um thick substrate



Low-Gain Avalanche Diode on 20um thick



Scribeline/Cutline placed at 3x (substrate thickness) to avoid depletion region touching defect-full cut.

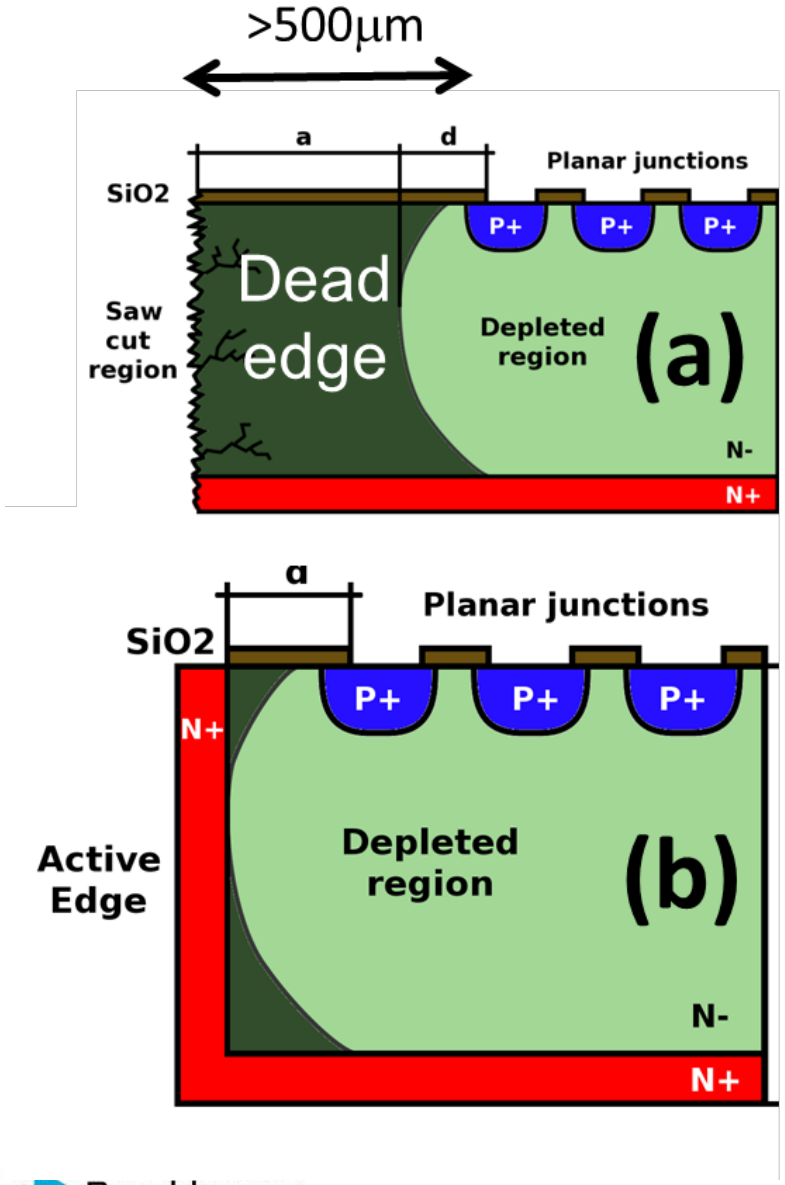
→ 1mm from active area

While LGADs are built on thin substrates, the 1mm “rule-of-thumb” is present in all devices by all manufacturers.

Can we cut-down the distance?

Brookhaven National Laboratory

Active edge



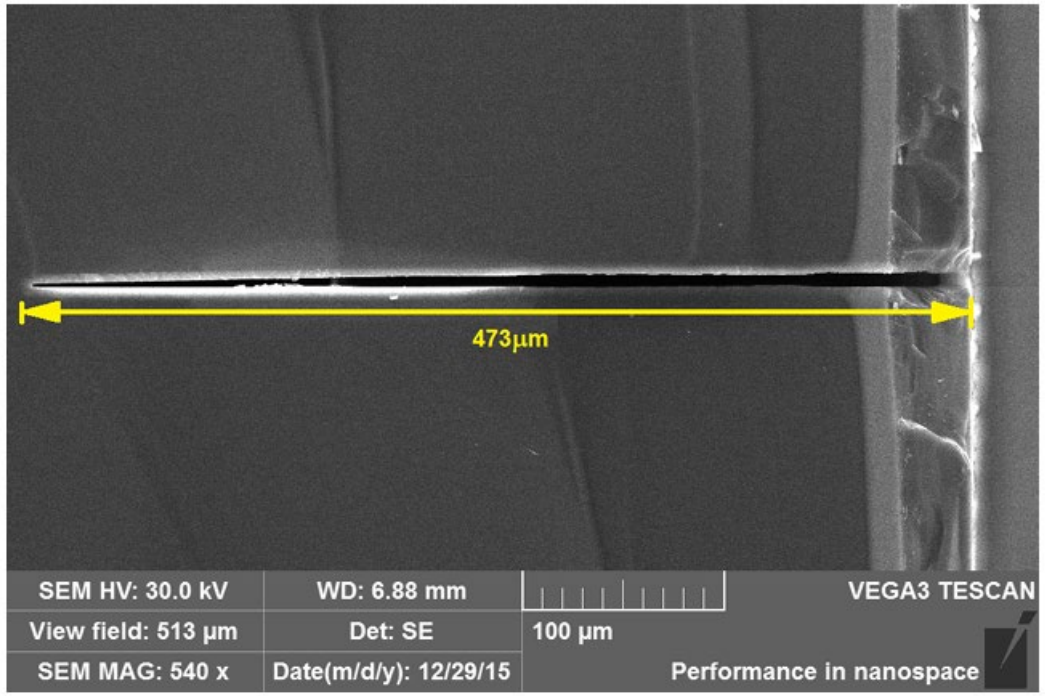
Depletion region must stay away from the defect-full scribeline, or a large current injected into the device.

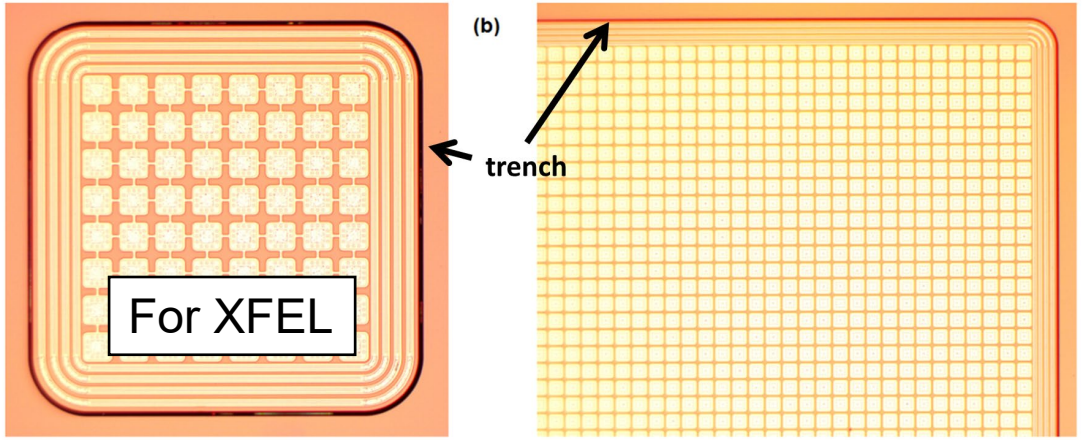
If cutline are “passivated”, defects are shut down and they do not act as generation center → no leakage current even if depletion region extends up to the cutline

The standard way to passivate is by etching a vertical trench (Deep Reactive Ion Etching – DRIE) and doping.

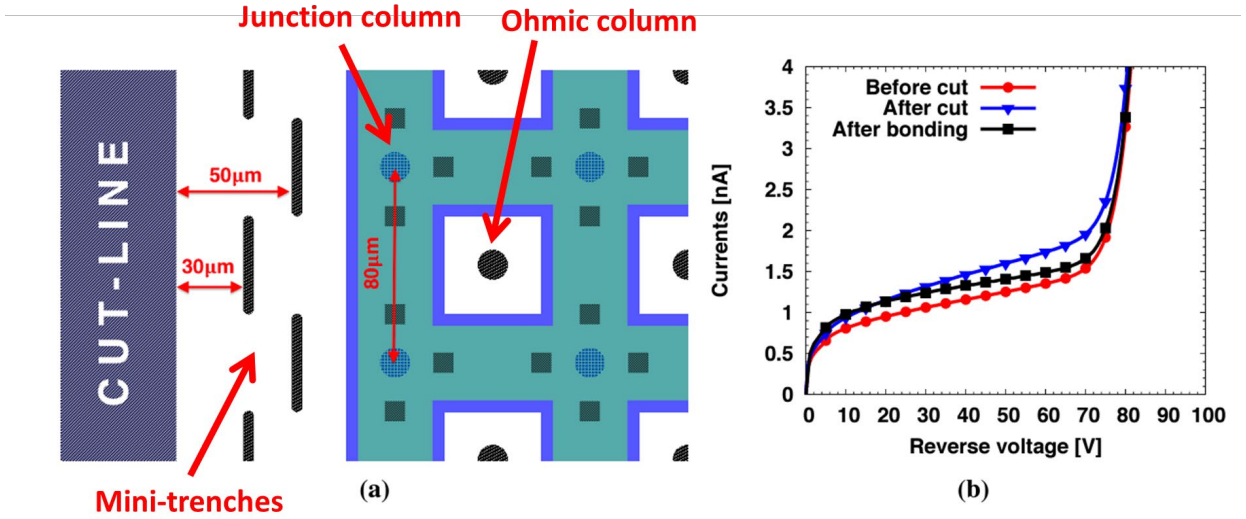
Trench etching by DRIE

Classical method, used for a few PS/HEP experiments on thick wafers (~ 500 – 100 um)





L. Pancheri et al *2016 JINST 11 C12018*



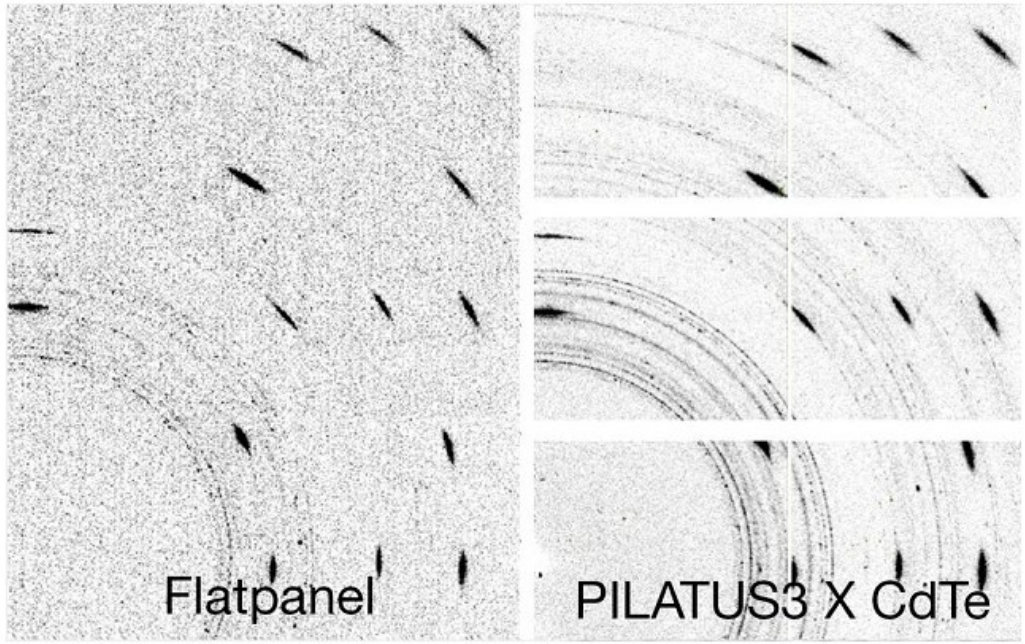
R&D at FBK(Trento , Italy) towards ATLAS IBL, **M Povoli et al 2013 JINST 8 C11022**

Brookhaven National Laboratory

Why go with Slim Edge?

When tiling sensors, dead areas appear w/o slim edges

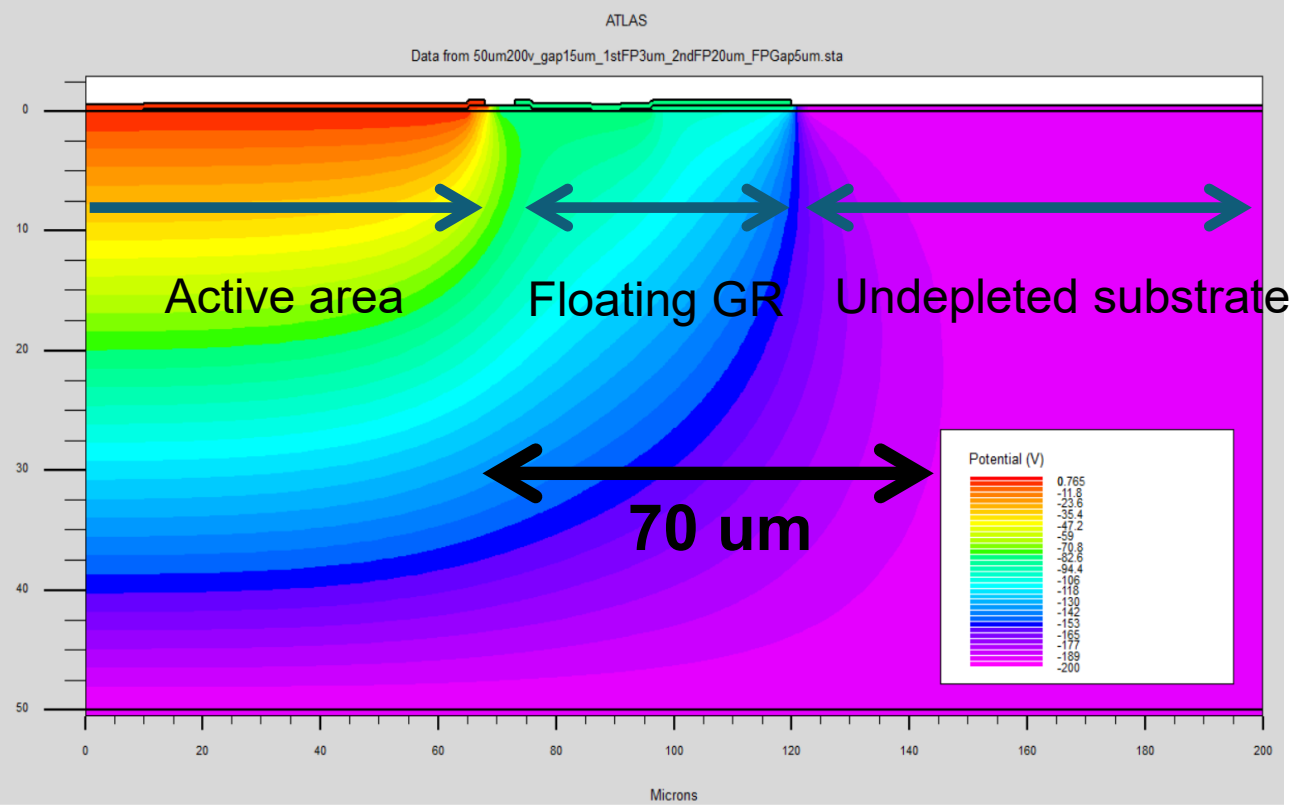
Powder diffraction experiment



Slim edges for:

- Minimize dead areas
- Facilitating tiling
- Smaller devices for the same Fill Factor
  - (particularly critical for LGADs, which suffer from low yield)

Case for thin substrates



In thin (20-50um thick) substrates, depletion region extends ~ 50um, as space is needed to allocate the GR (lithographic constrains).

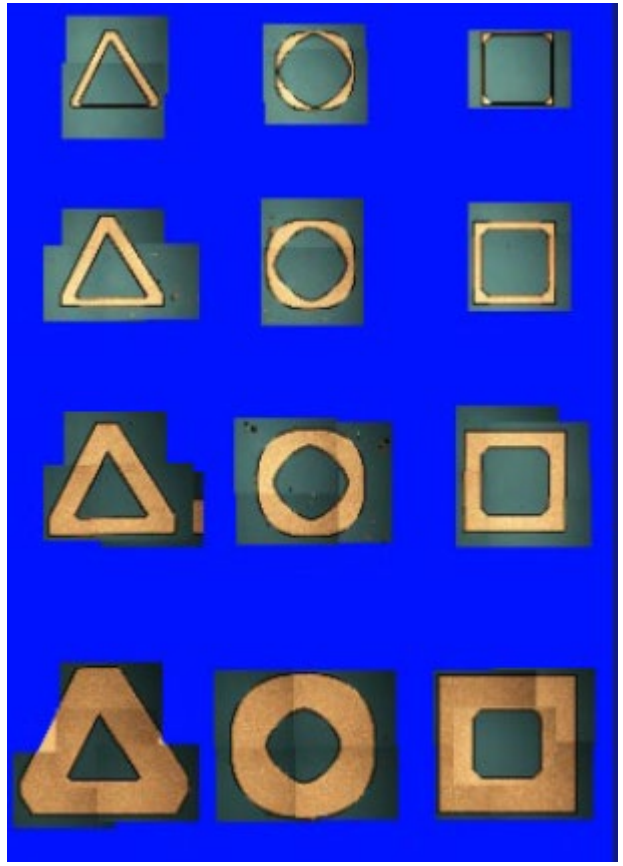
In the undepleted region, a cutline can be placed. No need of any treatment (to be tested)?

Most likely, need to produce a clean cut and passivation.

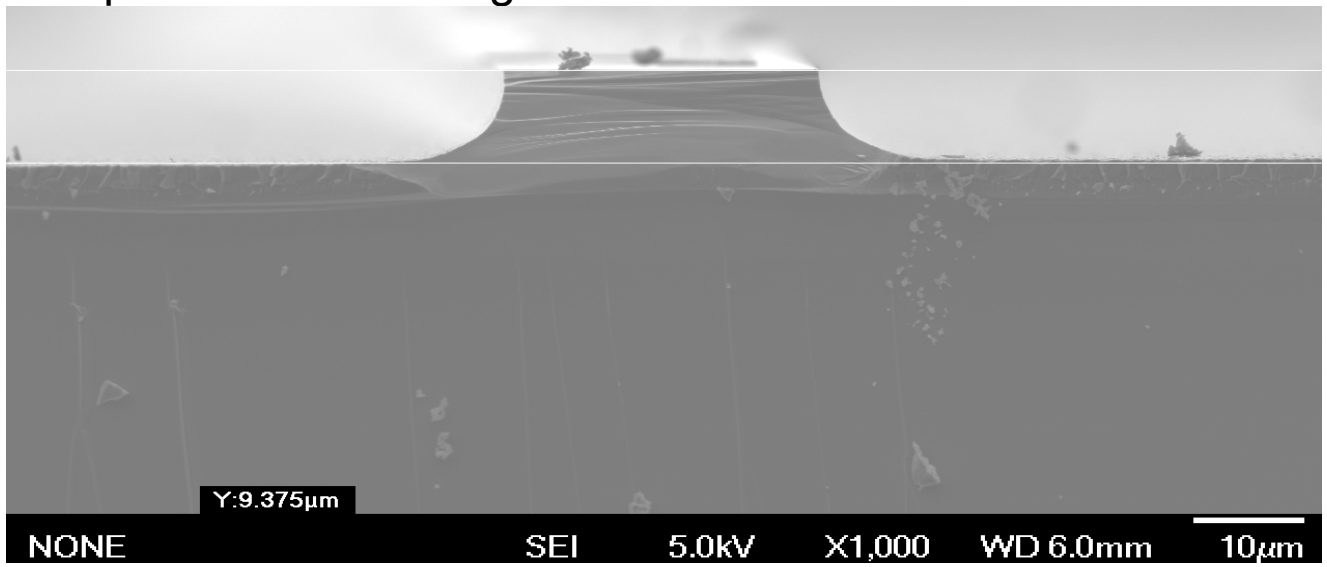
DRIE is the standard option (known to work) but other means may be good enough to achieve the same result.

Trench etching

- Chemical etching (KOH)
  + alumina passivation



- RIE silicon etching
  proved to be enough for thin substrates.



- Cleaving, laser dicing, …

Passivation of Atomic Layer Deposition of aluminum oxide available at BNL.
Used to induce a hole accumulation layer at the Si/AlO interface.

Fabrication

All fabrication carried out in class-100 clean room at BNL, except for:

- nitride/alumina deposition (CFN at BNL)
- DRIE + boron diffusion – if funds allow – at Cornell
- Ion implantation

4” wafer populated with a large number of (small area, ~ mm^2) test structures, differing for number of Guard Rings, distance from the scribeline, termination structure, trench etching method, …

Testing

Current-voltage at the probe station for basic functionality
Transient Current Technique to assure charge collection efficiency.

Budget

- one year project

- 100% budget is 130k (overhead included),
  mainly labor (2 weeks PI, 1 month clean-rom engineer, 2 months tech)

  - 80-60% scenario:
    - work reduced accordingly to fit the budget
    - less exploration of slim edge techniques

month 1-2: production of photolithographic masks and definition of the clean-room process

month 3-4: silicon substrates ready for trench etching

month 5-6. first wafers completed with trenches

month 7. static characterization of device and next plans laid down

month 8-9. Deliverables: method #2 for trench etching/passivation

month 10. static characterization of device

month 11 -12. additional methods for trenching, reports/papers.