

Hypernuclear DAQ

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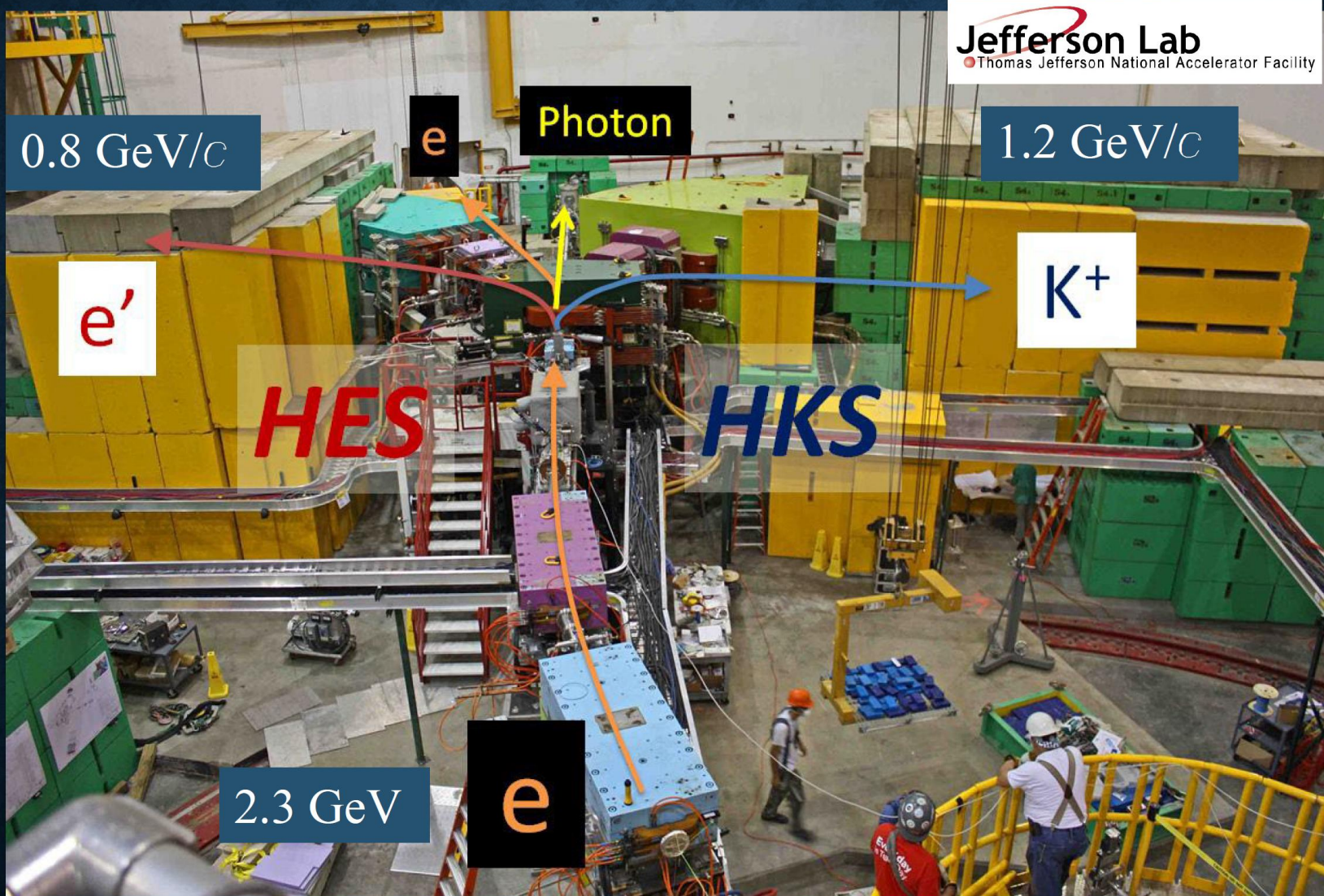
ERR preparation meeting

November 14th 2023

Outline

- Experiment overview
- Channel count
- Overview pipelined electronics
- Trigger overview
- To do
- Conclusion

Experimental setup for E05-115 (2009) at JLab Hall C



PARTICLE DETECTORS

HES

e^-



TOF walls
(Plastic scintillators)

Cherenkov detectors
• Aerogel ($n=1.05$)
• Water ($n=1.33$)

Drift chambers

K^+
 p, π^+

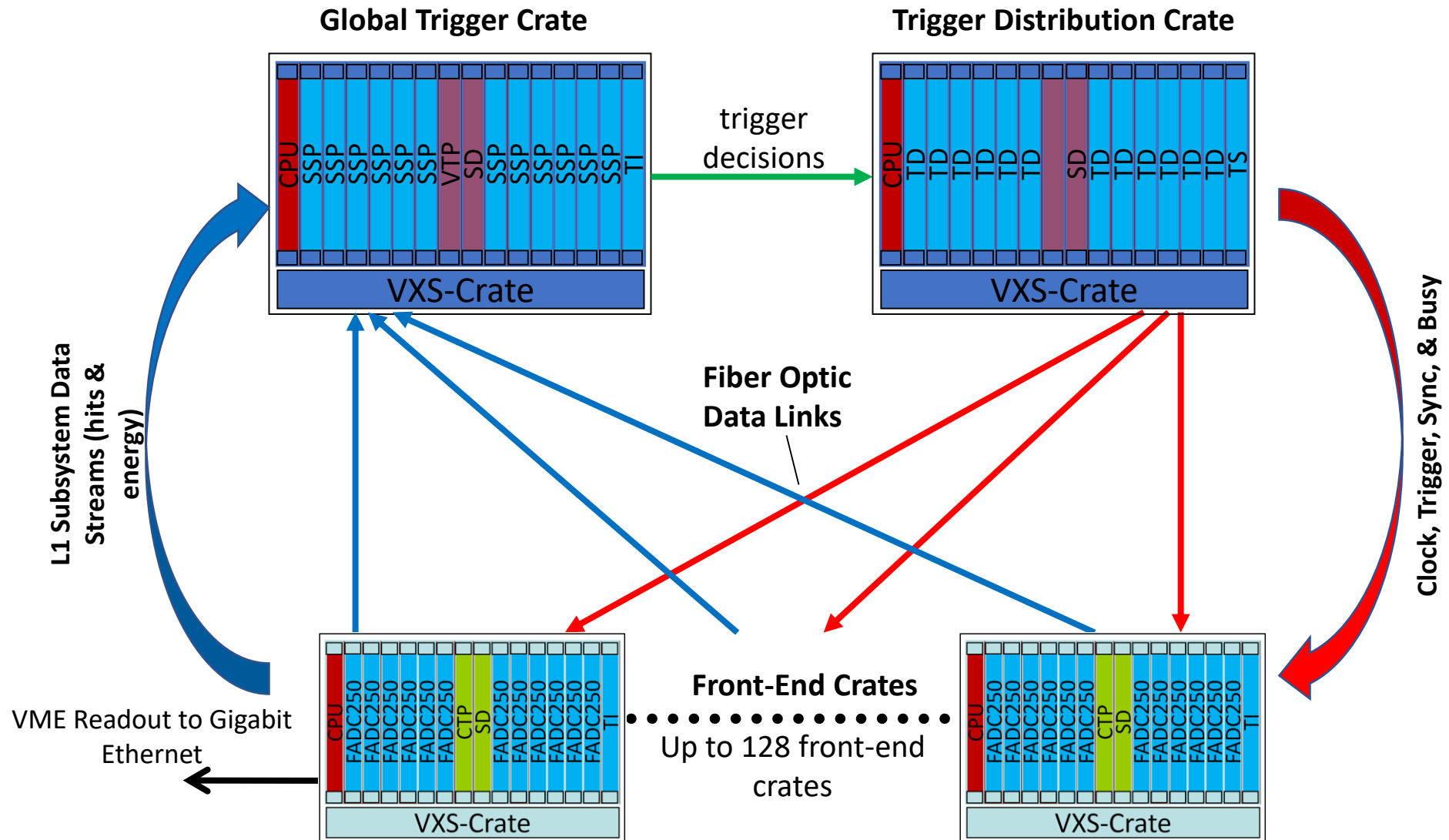
HKS



Channel count

	Detector	Current status	No. of channels		Ready?
			ADC	TDC	
HKS	Drift Chambers	To be tested	N/A	360 + 360	Yes
	TOF counters	All PMTs were checked	88	88	
	Aerogel Cherenkov	Test done	42	42	
	Water Cherenkov	New boxes under construction	48	48	
HES	Drift Chambers	To be tested	N/A	1098+360	
	TOF counters	To be tested	116	116	

Level 1 & Trigger Distribution

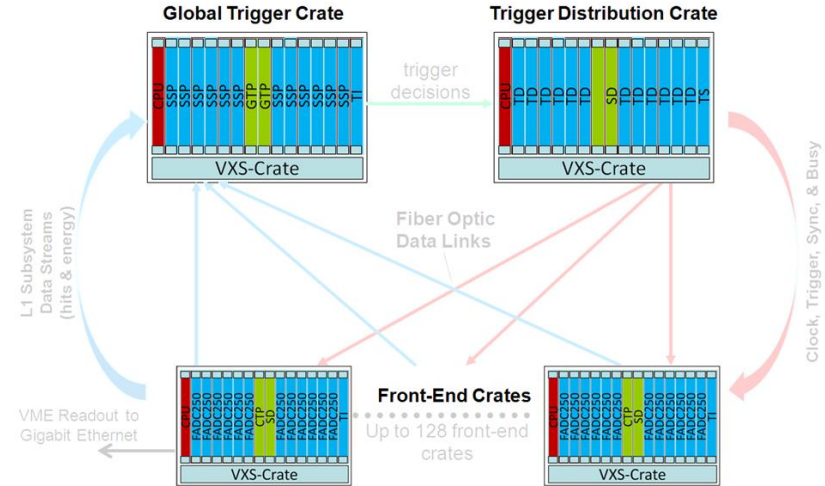


Crate Level – Signal Distribution

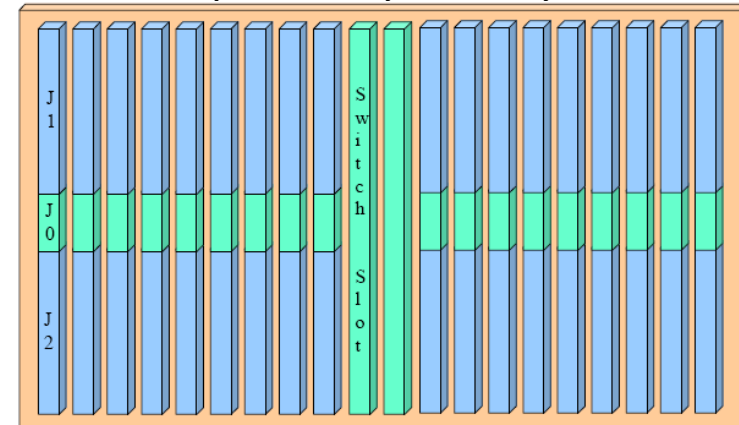
- VXS Based, 20 Slot Redundant Star Backplane
- VME64x backplane w/VXS (VITA 41 Standard) provides standard with high speed serial extension (new J0 connector)
- 18 Payload slots w/VME64x, 2 Switch slots
- Each payload slot has 8 high speed capable links (10Gbps each) to both switch slots

Crate Level Use:

- VME64x used for event readout
- VXS: Low jitter clock & trigger distribution
- VXS: Gigabit serial transmission for L1 data streams to switch slot for processing

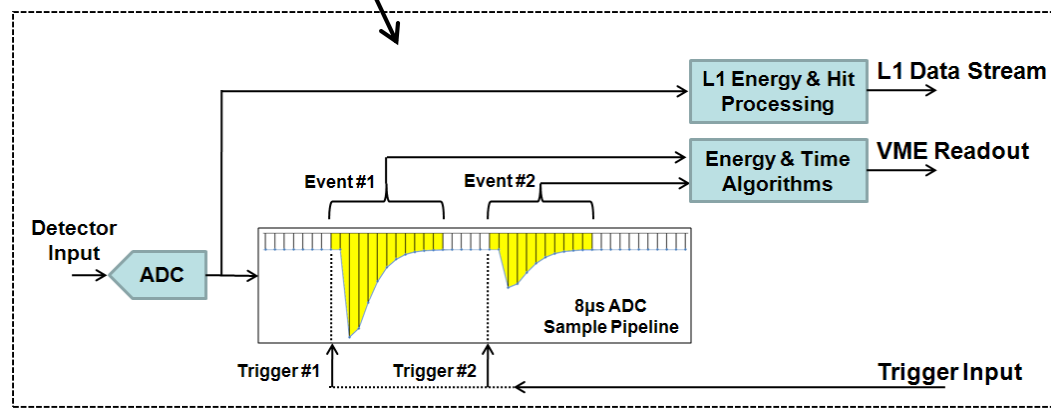
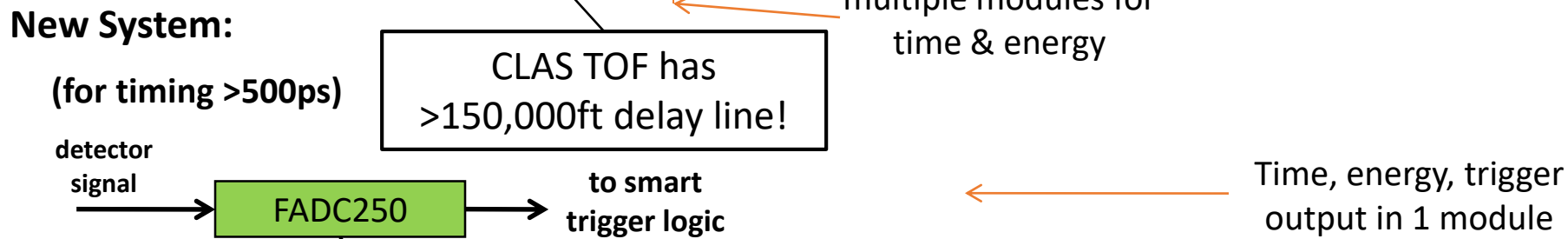
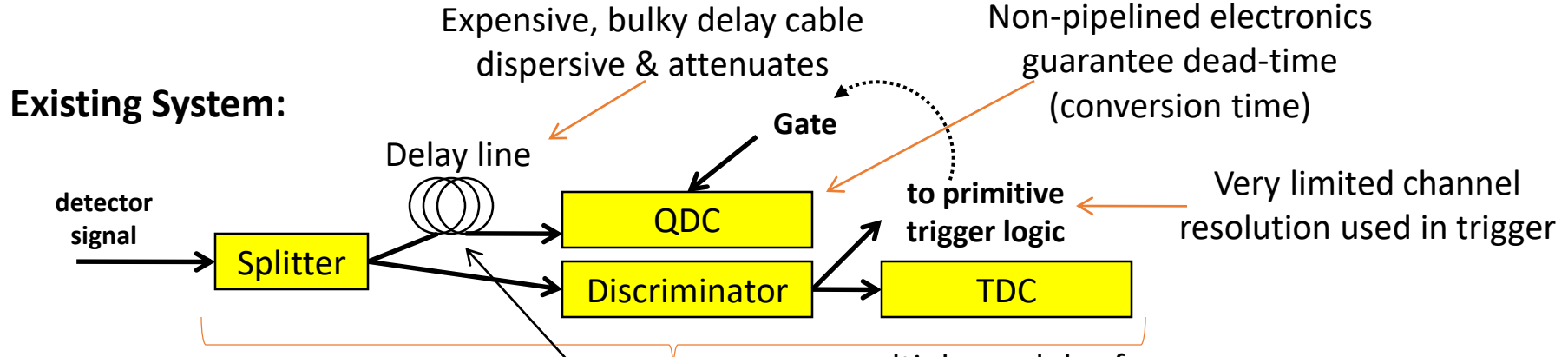


VXS Backplane Physical Layout:



VXS (VITA 41 standard)
VME64x + high speed
serial fabric on J0

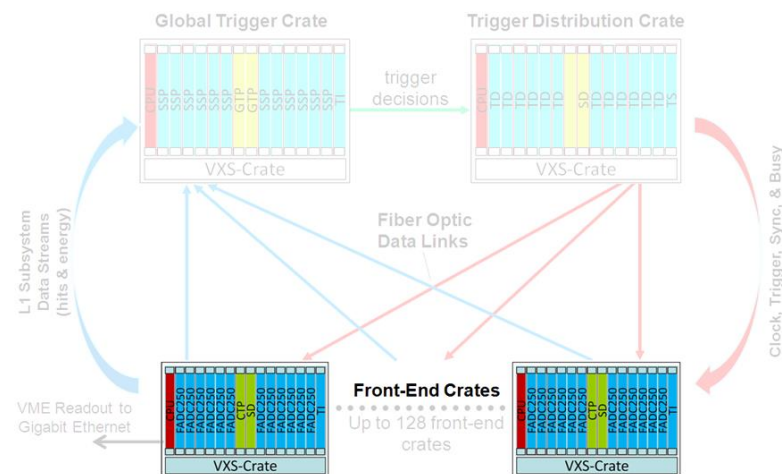
Capturing the Pulses...



- Pipelined sampling, readout, & trigger -> no dead-time
- Digitization retains original signal integrity
- Long pipeline allow more time for complex triggers

Front-End Electronics: fADC250

- 16 Channel 12bit, 250Msps Flash ADC
- 8 μ s raw sample pipeline, >300kHz sustained trigger rate (bursts @ ~15MHz)
- Post-processing in customizable firmware to extract time, charge, and other parameters minimizing event size
- Module supports 2eSST VME transfers at 200MB/s transfer rate
- Large event block sizes (>100) to minimize CPU interrupt handling
- VXS P0/J0 outputs 5Gbps L1 data stream (hit patterns & board sum)
- Used in existing 6GeV program:
 - Hall A BigBite
 - Upgraded Hall A Moller Polarimeter



JLab-fADC250:



Channel count

	Detector	Current status	No. of channels		Ready?
			ADC	TDC	
HKS	Drift Chambers	To be tested	N/A	360 + 360	Yes
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FADC = $88 + 42 + 48 + 116 = 294$ channels = 19 FADCs = 2 VXS crates (NPS)

V1190 = 2268 channels = 18 V1190 = 1 VME64X crate (HMS/SHMS/SBS could use CDET VETROC)

TOF = 204 channels = 7 V1290 = 8 F1 = 3 VETROC (SBS GRINCH)

Will be running during Moller : NPS,SBS,SoLID hardware available, most likely enough FADCs

Can use HMS/SHMDS electronics

BPM rasters : 2 FADC

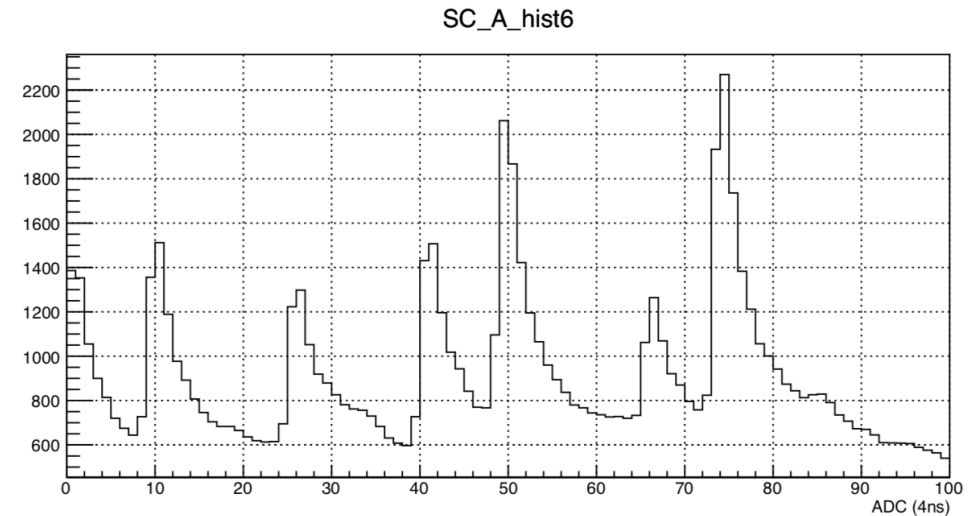
Trigger rates

Target	Areal density [/(g/cm ²)]	Beam intensity (/ μA)	HES rate (/kHz)	HKS rate (/kHz)			Accidental coincidence ^(*) (/kHz)
			e'	π ⁺	K ⁺	p	
⁶ Li	100	50	120	22	0.27	28	1.0
⁹ Be			140	21	0.26	27	1.8
¹¹ B			170	21	0.25	26	2.1
²⁷ Al			930	20	0.24	25	10.5
⁴⁰ Ca	150	20	1100	26	0.31	33	14.8
⁴⁸ Ca			940	25	0.31	32	13.8
²⁰⁸ Pb			1300	8.2	0.24	10	4.9

(*) Assuming,
HES: 30 ns width
HKS: 200 ns width

Data rates

- Rough estimates
 - HKS = 1 MHz
 - HES = 1 MHz
 - Coincidence = $1\text{MHz} \times 1\text{MHz} \times 20\text{ns} = 2\text{KHz}$
- Plan for up to 20 KHz desirable
- If no waveform could take 200 KHz
- Using CODA3 and event blocking should be doable (similar to CLAS12) will be tested during NPS
- Need to evaluate detector occupancies
- If useful can record full FADC waveforms



Example scintillator SoLID beam test

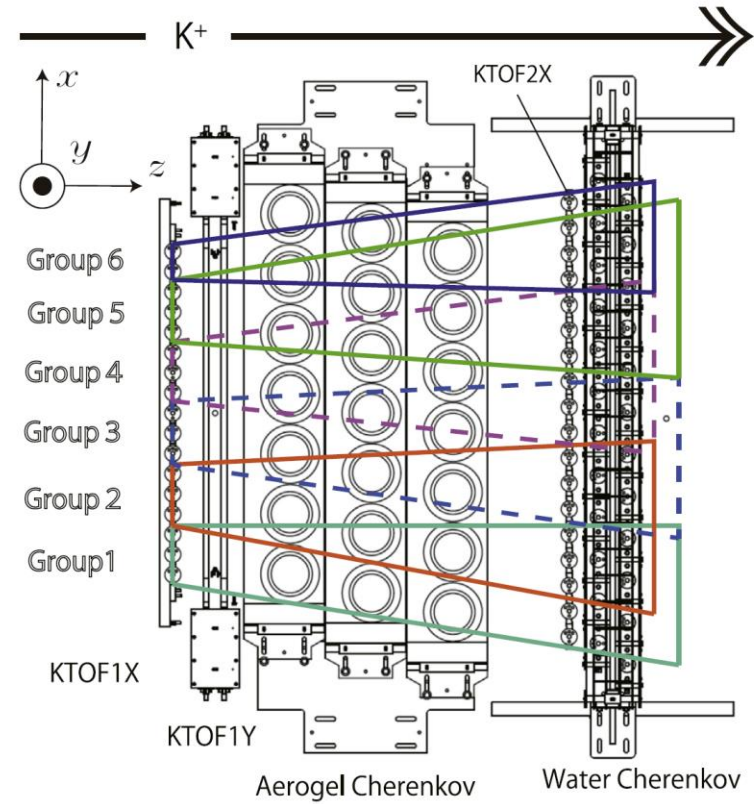
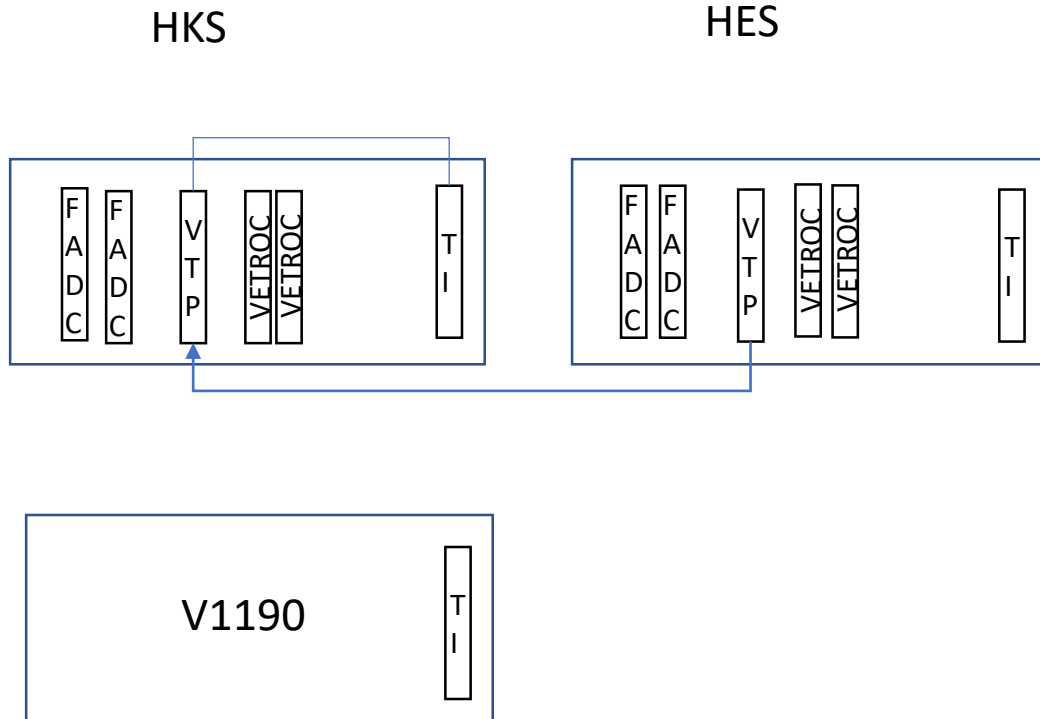
Data rates with full sampling

- Event size
 - 57 kB with 40 samples 100 % occupancy
- Max trigger rate : 15 KHz
- Data rate : 860 MB/s
- Tape : 12 PB

Data rates with time / integral

- Event size
 - 13 kB with time and amplitude 100 % occupancy
- Max trigger rate : 15 KHz
- Data rate : 190 MB/s
- Can be handled now
- Tape : 2.6 PB

Trigger



Can program VTP for coincidences between scintillators
If use VETROC instead of V1190 could add Drift Chamber to trigger

Additional electronics

- Beamline info
 - Target BPM
 - Raster
 - 1C12 BPM cabling

To do / Testing

- Bench testing and testing with detector VETROC
- Setup FADC trigger with VTP
- Setup testing in ESB

Additional detectors

- MCP PMTs
- MRPC
- Would need dedicated new electronics

Conclusion

- HKS and HES
 - FADC = $88 + 42 + 48 + 116 = 294$ channels = 19 FADCs = 2 VXS crates
 - V1190 = 2268 channels = 18 V1190 = 1 VME64X crate
 - TOF = 204 channels = 7 V1290 = 8 F1 = 3 VETROC
 - Could use HMS/NPS/SBS hardware
- CODA3 with event blocking should allow 20 kHz trigger rate (200 KHz with time and amplitude)
- Digital trigger using FADC and VTP
- If use VETROC instead of V1190 can include in L1 trigger (High res TOF and Drift Chamber)

Backup

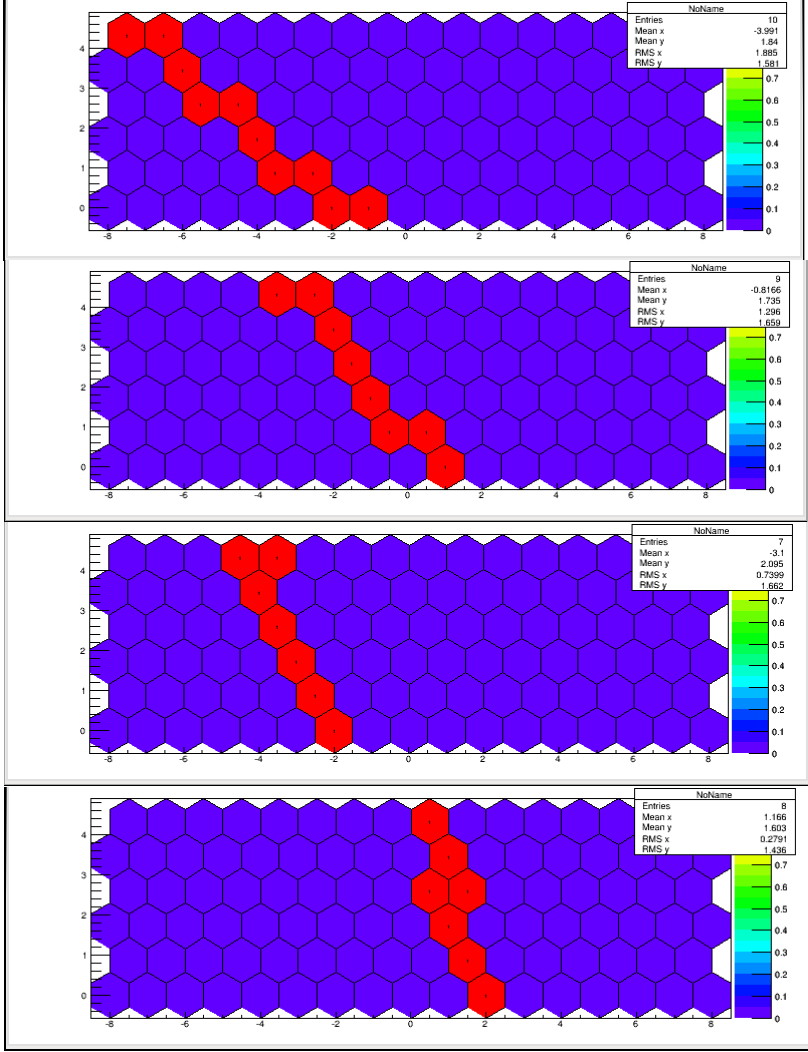
CLAS12

Detector	Can be in trigger?	Will be in trigger?	Trigger Algorithm
ECAL/PCAL	Yes	Yes	U/V/W Clustering
DC	Yes	Yes	Segment Position/Angle Finding
CTOF/FTOF	Yes	Yes	Hit based
HTCC/LTCC	Yes	Yes	Hit based
FT	Yes	Yes	3x3 Clustering
CND	Yes	No	N/A
SVT	Yes	No	N/A
RICH	Yes	No	N/A
MicroMegas	No	No	N/A

- CLAS12 triggering will support geometric matching (e.g. drift chamber segment points to clusters, etc...)

Drift Chamber Segment

sweeps angle and wire offset:



valid segments are binned into common angle, VHDL file/ equations auto generated:

```

CAUsers\braydo\LAB\Desktop\dcsegfinder.vhd - Notepad++
File Edit Search View Encoding Language Settings Macro Run Plugins Window ?
dcsegfinder.vhd
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.std_logic_arith.all;
4  use ieee.std_logic_unsigned.all;
5
6  use work.utils_pkg.all;
7
8  -- Note: This source is auto generated by dctrackbin.C
9  -- This VHDL file should be modified/regenerated by changing the .C source.
10
11 entity dcsegfinder is
12     generic(
13         DC_ARRAY_START : integer := -7;
14         DC_ARRAY_STOP  : integer := 6
15     );
16     port(
17         CLK           : in std_logic;
18
19         SEGMENT_THR   : in std_logic_vector(2 downto 0);
20         DC_ARRAY       : in slv6a(DC_ARRAY_START to DC_ARRAY_STOP);
21
22         SEG_HIT_A     : out std_logic_vector(15 downto 0)
23     );
24 end dcsegfinder;
25
26 architecture synthesis of dcsegfinder is
27     function seghitsum(hits : std_logic_vector) return std_logic_vector is
28         variable result : std_logic_vector(2 downto 0);
29     begin
30         result := (others=>'0');
31         for I in hits'range loop
32             if hits(I) = '1' then
33                 result := result + 1;
34             end if;
35         end loop;
36         return result;
37     end seghitsum;
38 begin
39     SEG_HIT_A(0) <=
40     '1' when SEGMENT_THR <= seghitsum((DC_ARRAY(-1)(0) or DC_ARRAY(0)(0)) & (DC_A
41     '0';
42
43     SEG_HIT_A(1) <=
44     '1' when SEGMENT_THR <= seghitsum((DC_ARRAY(-1)(0) or DC_ARRAY(0)(0)) & (DC_A
45     '1' when SEGMENT_THR <= seghitsum((DC_ARRAY(-1)(0) or DC_ARRAY(0)(0)) & (DC_A
46     '1' when SEGMENT_THR <= seghitsum((DC_ARRAY(0)(0) or DC_ARRAY(1)(0)) & (DC_AR
47     '0';
48
49     SEG_HIT_A(2) <=
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60
61
62
63
64
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VHSIC I length: 20797 lines: 178 Ln: 1 Col: 1 Sel: 0 UNIX ANSI INS
    
```

Drive



segment



x14 DCRB

condition



70Gbps
(DC Hits)

GTP: prototype VXS concentrator card

- Receives all DC hits from DCRB
- Searches for track segments and reports position/angle to next trigger stage
- VTP (mentioned later in talk) will be used in CLAS12

- Scope like interface on GTP allows real-time display of found segments by trigger logic
 - Cosmic event shown where only 1 segment was the trigger condition



FADC deadtime with waveforms

