THE UNIVERSITY OF CHICAGO | Biological Sciences Division

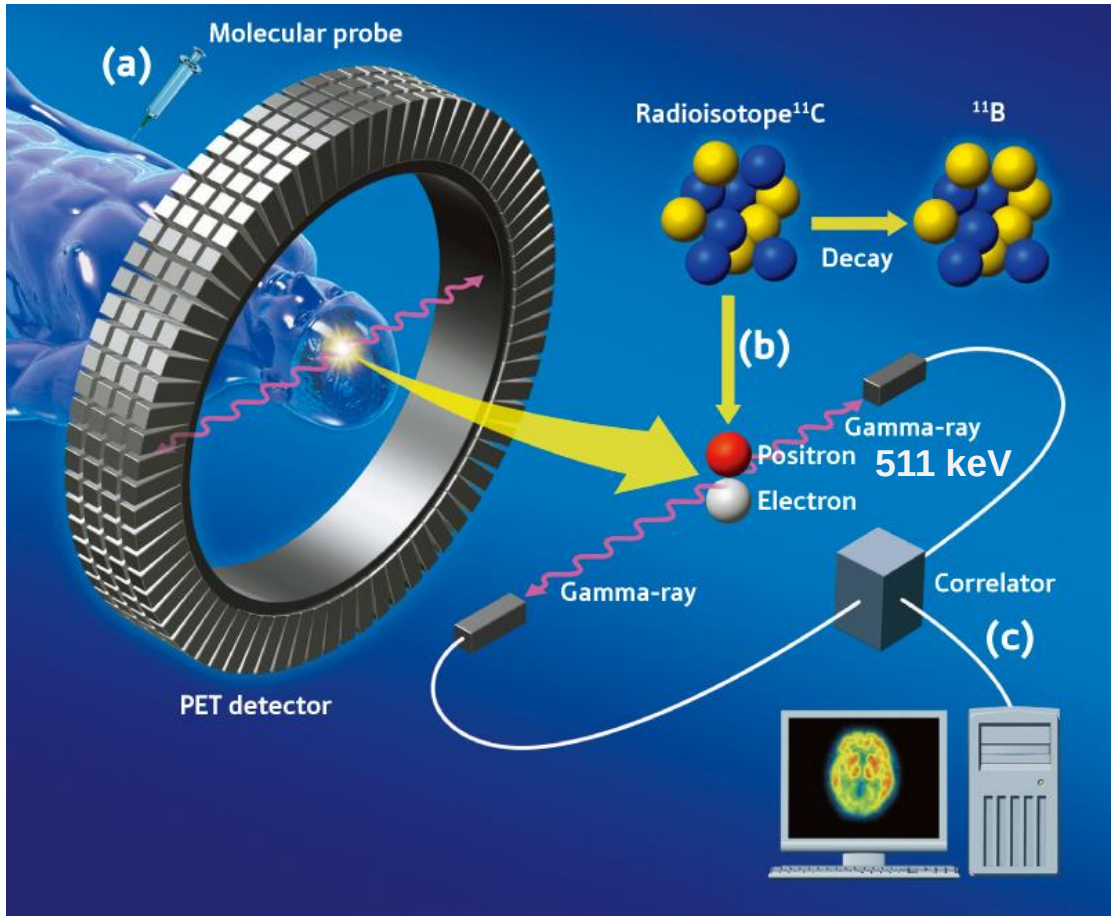
Electronics and Data Acquisition:

State-of-the-art Challenges and Emerging Technologies

2nd Joint DOE/NIH Workshop, March 16-17, 2024

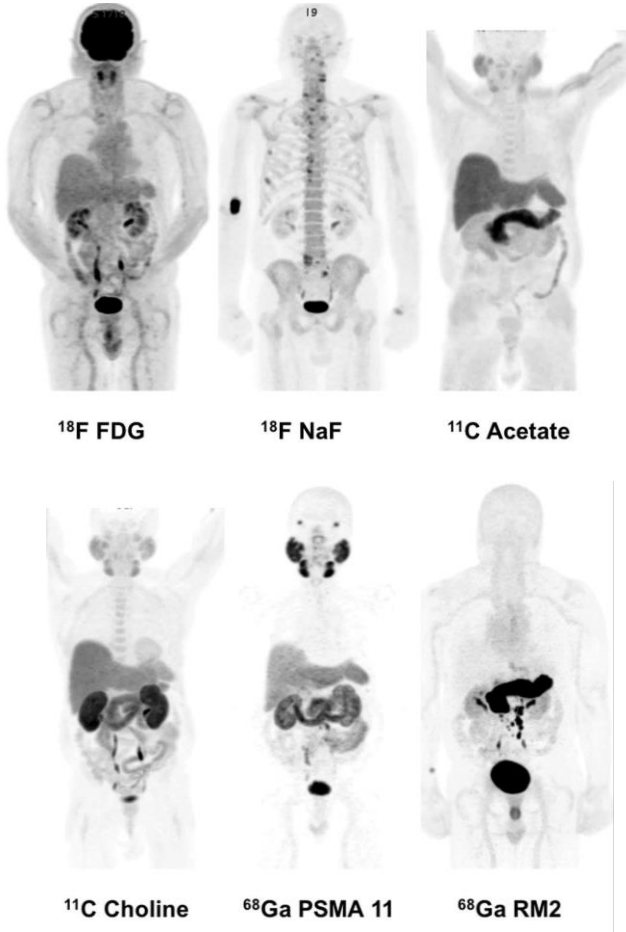
Chien-Min Kao, PhD, Department of Radiology

Principle of Positron Emission Tomography (PET)



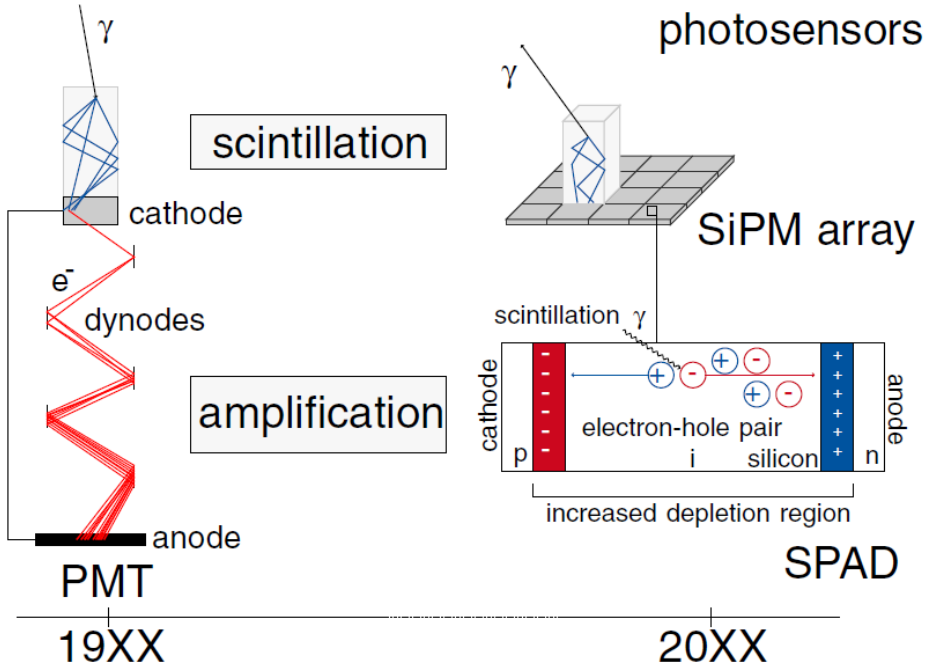
Courtesy of Guen Bae Ko

BRIGHTONIX IMAGING



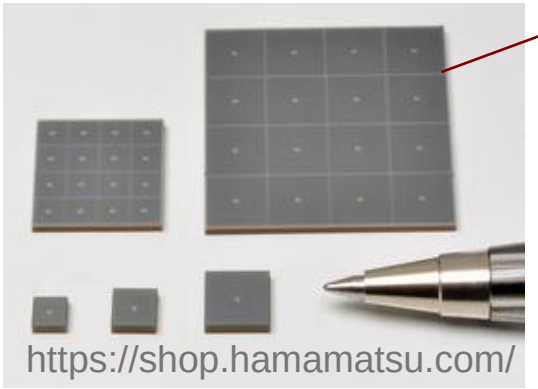
Courtesy of Prof. Iagaru A (Stanford)

PMT based ➔ SiPM based

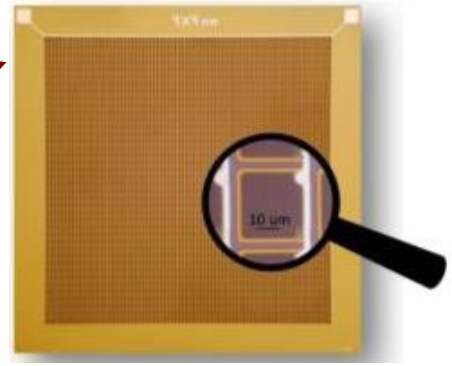


V. Nadig et al , EJNMMI (2022)

https://www.siemens-healthineers.com/



https://shop.hamamatsu.com/



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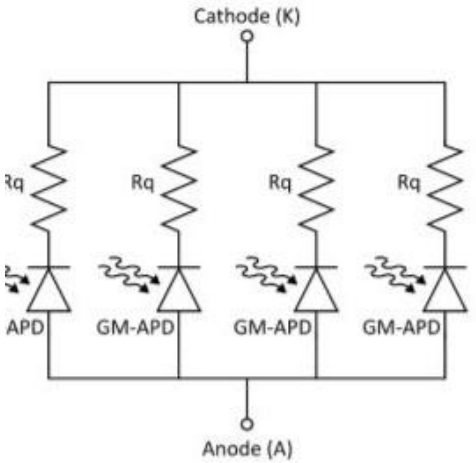
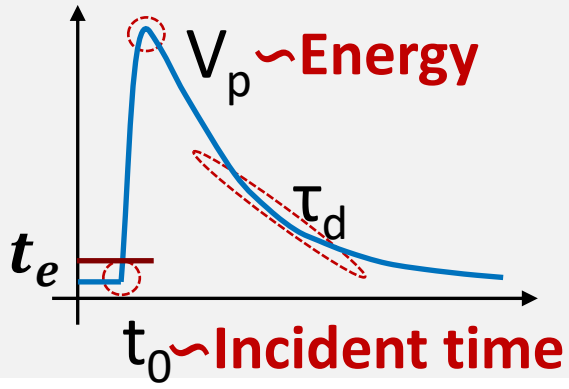


equivalent circuit

high-resolution, TOF PET, PET/MRI, insert, compact organ-specific PET

SiPM Readout Electronics for PET

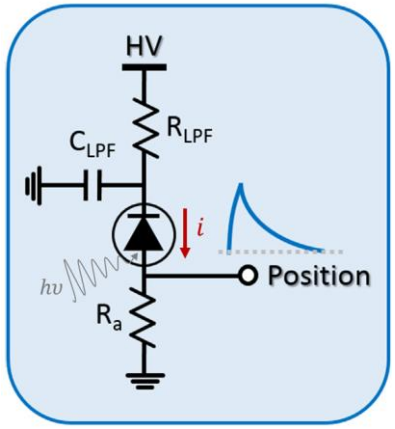


$$s(t) = \begin{cases} 0, & t < t_0 \\ ae^{-b(t-t_0)}(1 - e^{-c(t-t_0)}), & t \geq t_0 \end{cases}$$

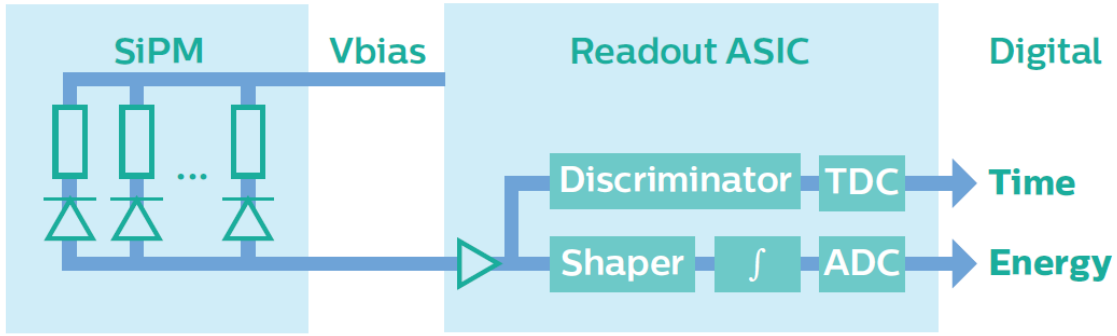
Amplitude · Decay · Rise · Incident time

Courtesy of Guen Bae Ko

Courtesy of Guen Bae Ko



Park et al, PMB (2017)



Philips manual

current mode preamplifer for low input impedance ➔ sharper leading edge

✓ TOF PET

most charge in the slow tail ➔ needs a long integration time

ASICs for SiPM

P.P. Calo et al, NIMA (2019)

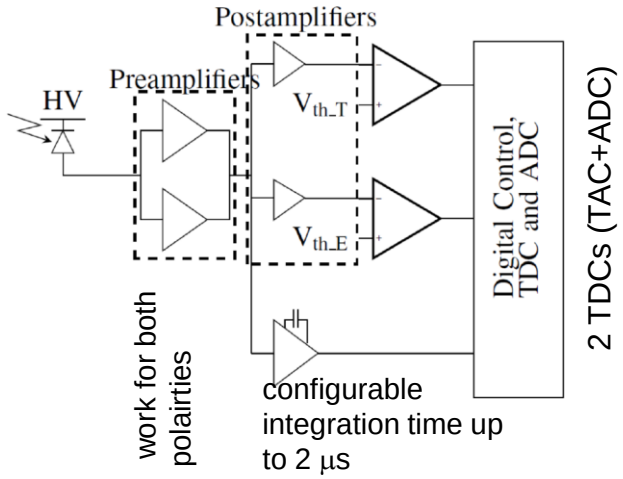
chip	Time resolution	Power consumption	Note
SPIROC	1 ns rms	25 μW/ch	voltage mode; 0.35 μm, 50Ω input impenedance, inverting voltage amplifier; a CRRC^2 shaper with selectable shaping time, x1 or x10;a bipolar fast shaper with shaping time of 15 ns for generating trigger; power pulsing to reduce power consumption
EASIROC	<0.3 ns rms	4.84 μW/ch	voltage mode, similar to SPIROC
PETIROC	trigger jitter 46 ps, 1x1 mm^2 Hamamatsu MPPC, fast laser	3.6 mW/ch	voltage mode; SiGe, high bandwidth f_t>60Ghz; slower shaper for energy and an RF common emitter preamp with 10Ghz gain-bandwidth product and a fast discriminator
PETA3	190 ps FWHM CRT, 3x3x5 LYSO, 3x3 mm^2 FBP SiPMs	32 mW/ch	voltage mode; 50Ω; x20; fully differential voltage amplifier for the fast time channel
NINO	64 ps rms SPTR, Hamamatsu S13360-3050CS biased at 62V	20 mW/ch	current mode; differential front-end, open-loop common gate current follower; 1.5 ns rise time for a single fired microcell, 100 ps rms jitter for a 3x3mm^2 Hamamatsu MPPC with 1.5V overvoltage
STIC3	67.1 ps rms SPTR, Hamamatsu S13360-3050CS	25 mW/ch	current mode; differential front-end, open-loop common gate current follower;
TOFPET2	95 ps rms SPTR, Hamamatsu S13361-3050E-04, biased at 7.5V overvoltage	<10 mW/ch	current mode; regulated common gate transimpedance amplifier to save power

Data Acquisition (DAQ) System for PET

PETSYS

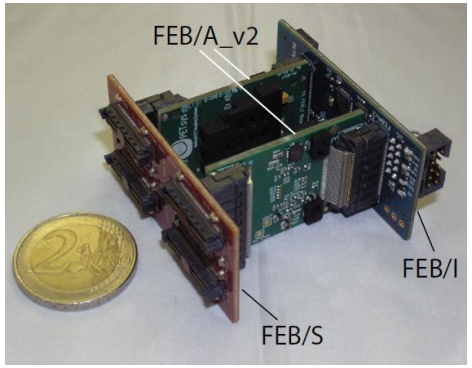
TOFPET2

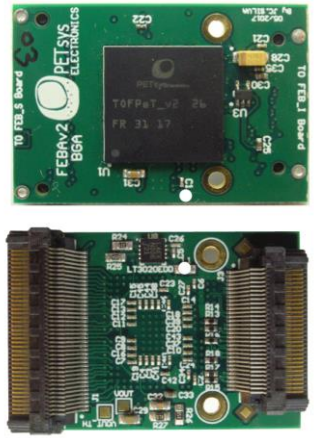
- CMOS, 64 ch
- top-level scheme of one channel



- time-over-threshold (tot) or energy integration (qdc) mode
- 5 – 8.2 mW/ch

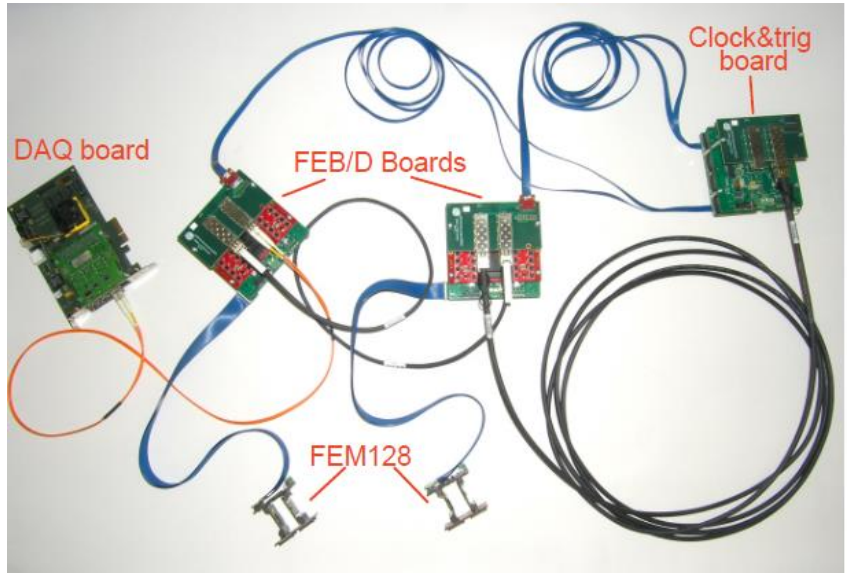
FEB/A_v2





FEM128

- 2 FEB/A_v2: 64ch TOFPET2 ASIC, temperature sensor
- 1 FEB/S: connection adaptor
- 1 FEB/I: communicate with FEB/D

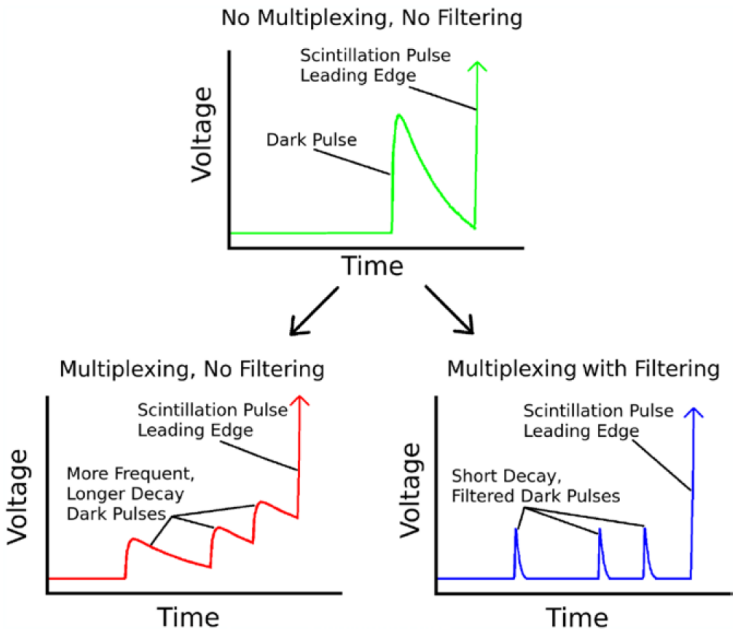


- FEB/D-1024 support up to 8 FEM128
- Up to 32 FEB/D-1024 can be daisy chained to a single DAQ input

Methods to improve timing

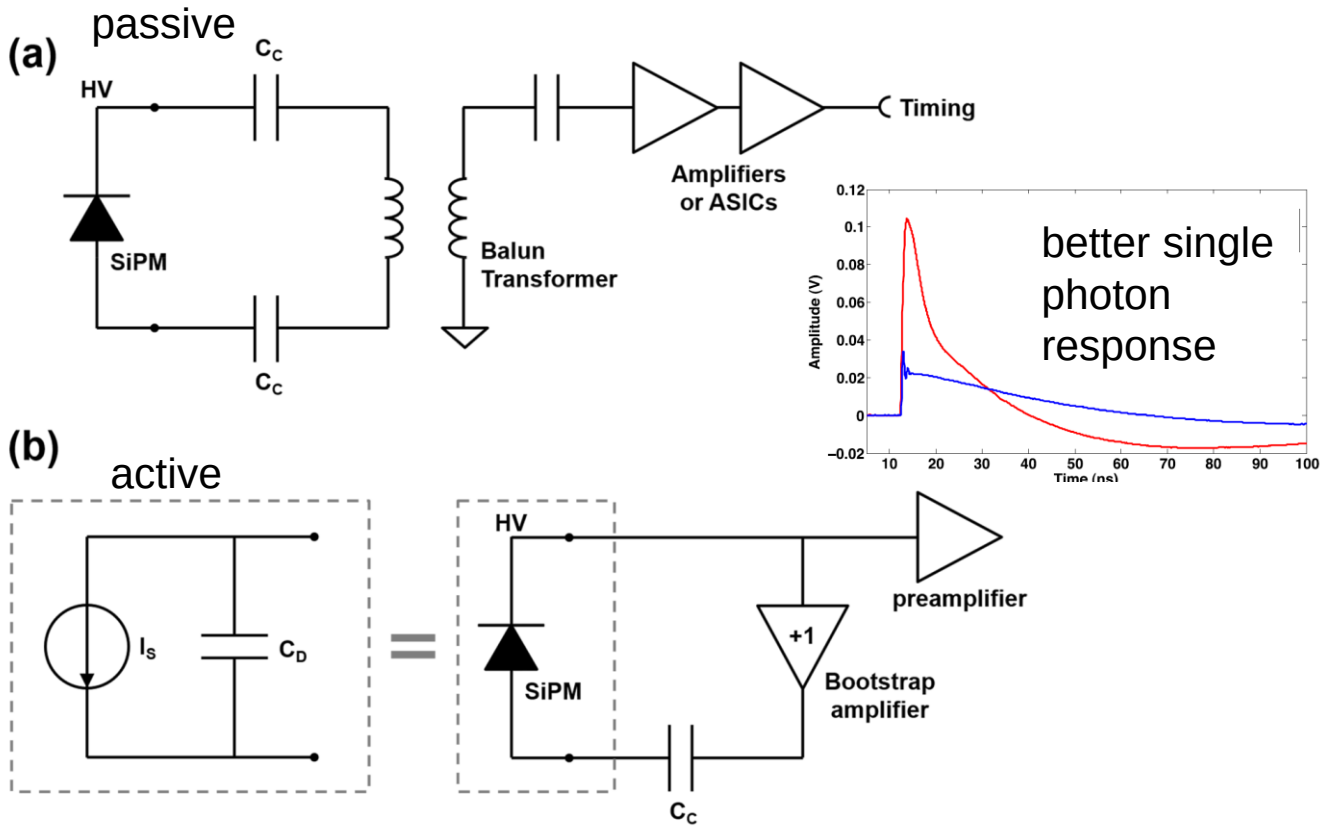
Analog high-pass filtering

High-pass filter leads to improved timing: better SNR on fast leading edge



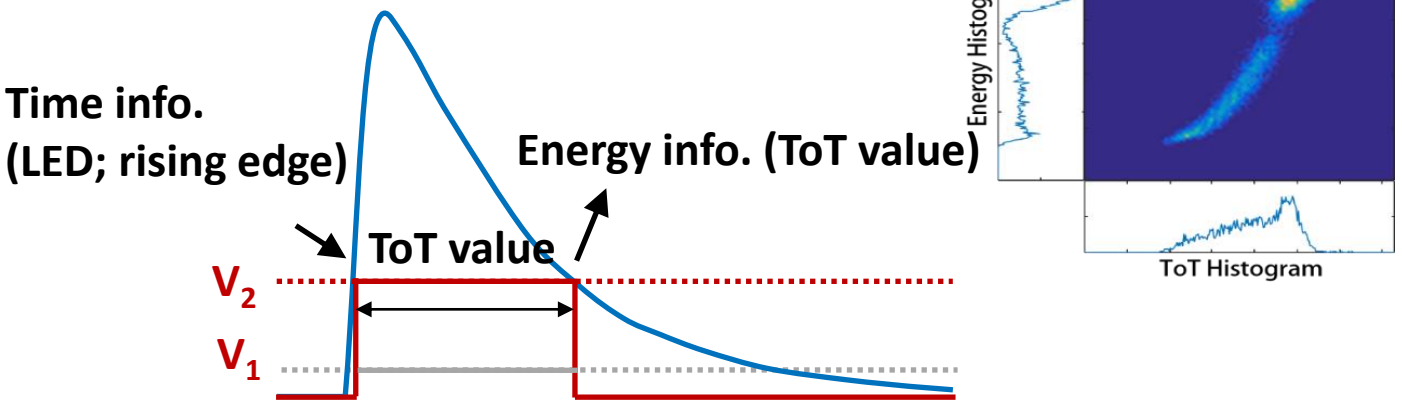
High-pass filter with pole-zero cancellation for baseline correction

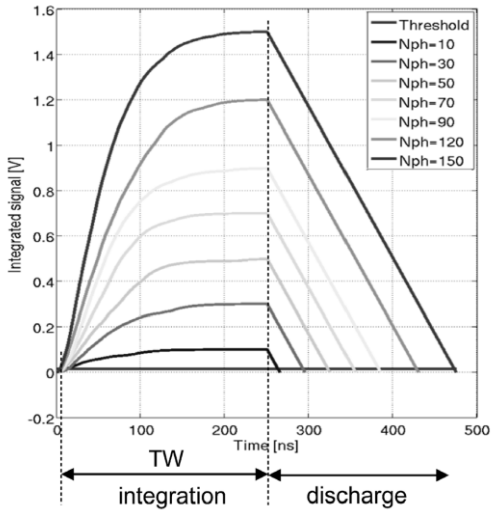
Bootstrapping techniques



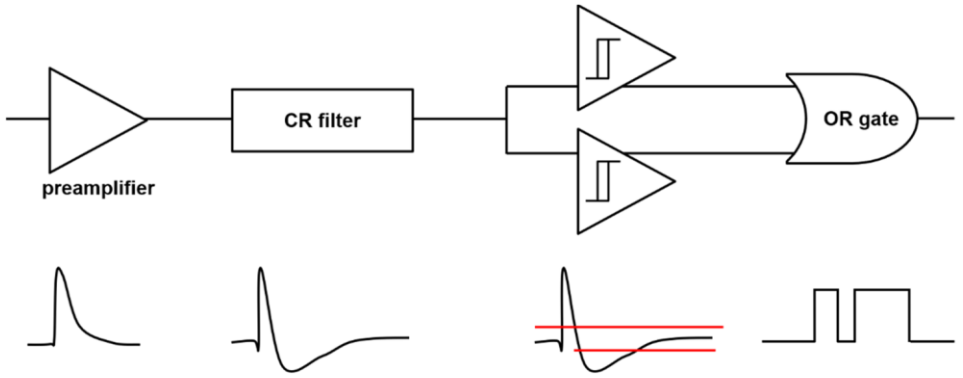
Data Acquisition Electronics

Time-over-threshold (TOT)





linearized TOT



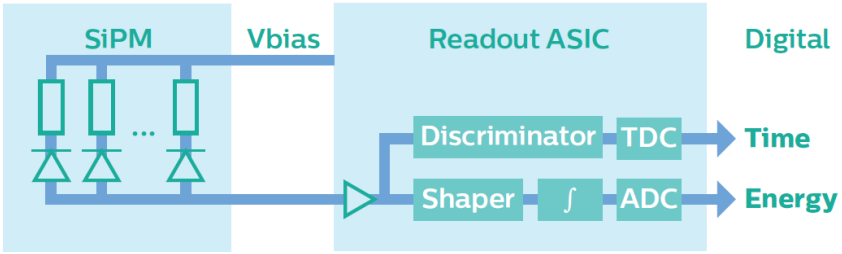
using bipolar shaper

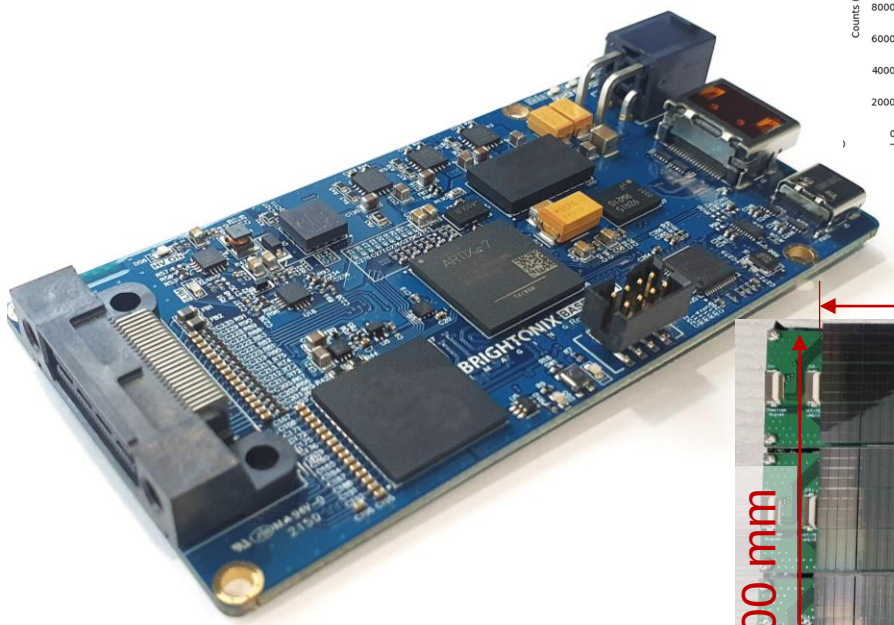
- Cost effective (using simple comparator + TDC)
  - reduced dead time
- ToT value ∝ log (Energy)
- relatively poor energy resolution, but acceptable for PET when using 1:1 coupling and bright scintillators

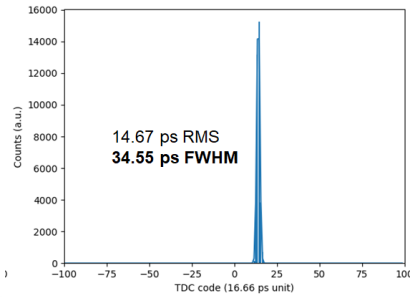
Courtesy of Guen Bae Ko

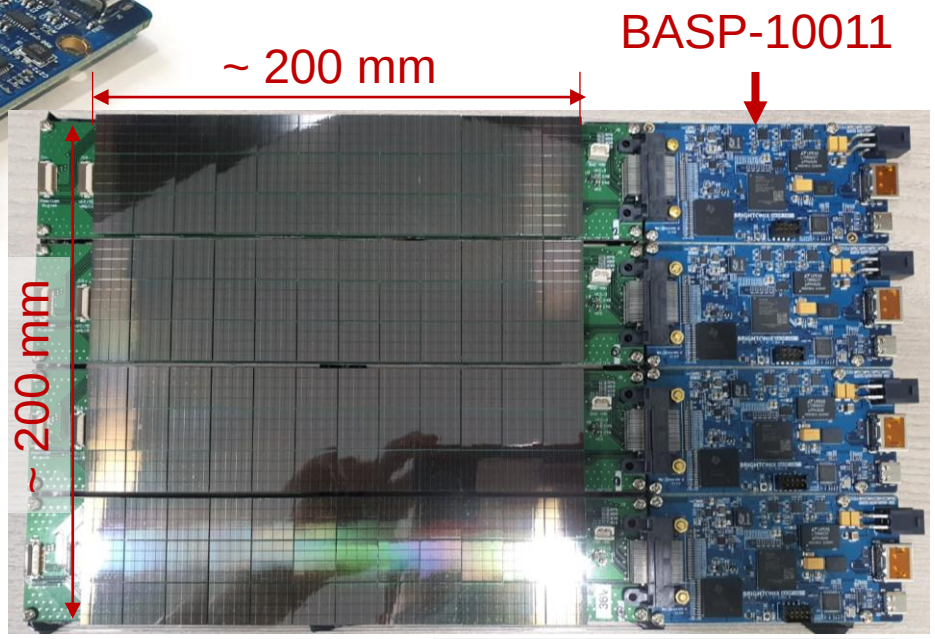
BRIGHTONIX IMAGING

BASP-10011 Compact general purpose 16 channel DAQ module









Large area detector

Features

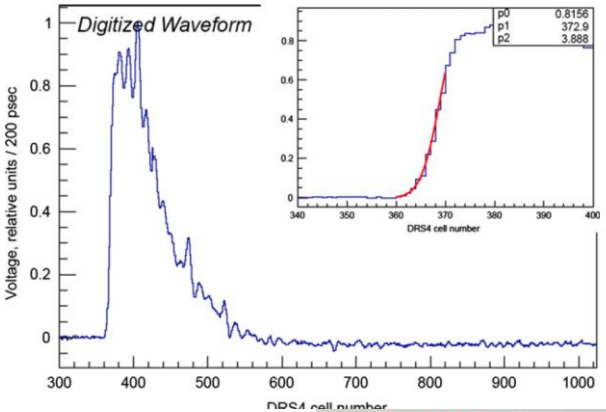
- 1 channel HV output (40-70 V, up to 300 mW)
- 1 channel DAC output (0 – 2.5V, up to 20 mA)
- **16 channel ADC** with analog gain (12-bit, 80 MSPS)
- **16 channel FPGA-based TDC** (16 ps LSB)
- 4 channel slow ADC for temperature monitoring
- 5V and 12V power supply output for front-end circuit
- High throughput with LVDS serializer (up to 2.4 Gbps)
- **Expandable with Brightonix Signal Multiplexer Board (up to 32 modules)**
- **USB 3.0** interface (up to 1.6 Gbps)

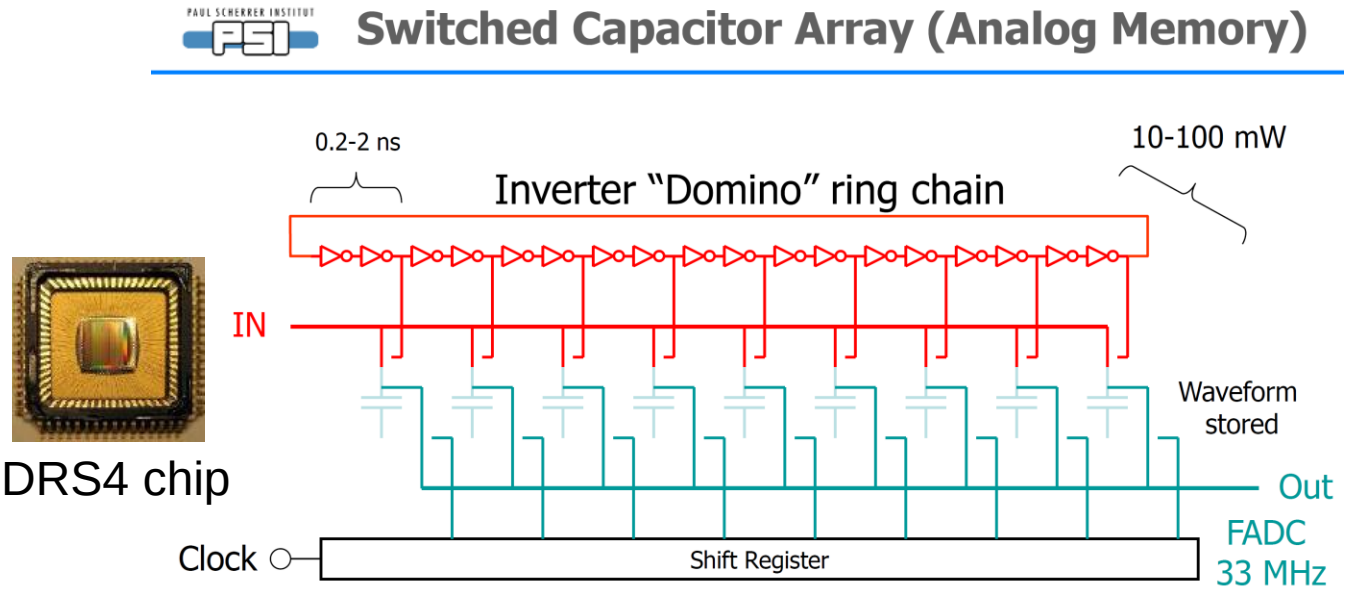
Applications

- PET/SPECT detector
- Gamma spectroscopy
- Compton camera
- General purpose data acquisition
- Various academic research

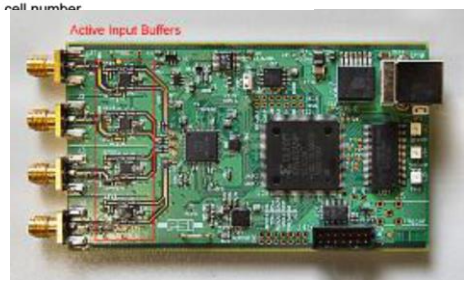
DAQ Electronics

Waveform Sampler (Switched Capacitor Array)





DRS4 chip



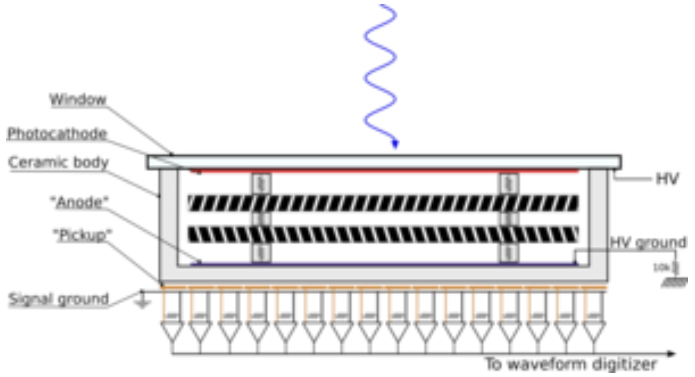
PSI
DRS4 eval board, 4 ch

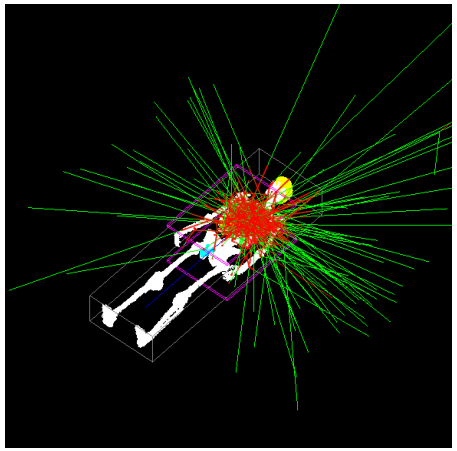
CAEN
VME 32 ch; NIM 16 ch, desktop 16 ch

- **12 bit, up to 5 GHz**
- **8+1 channel, 1024 samples/ch**
- **digital, nontrivial post pulse processing (e.g. noise filtering, baseline correction, pulse pile-up correction)**

DAQ Electronics

Waveform Sampler PSEC4





6 ch, 256 samples, 4-15 GS/s

- Hardware + (lots of) firmware required for system integration of ASICs.

2x RJ45 connectors for flexible system operation (1 clock + 7 LVDS data lines up to 800 Mbps per line)

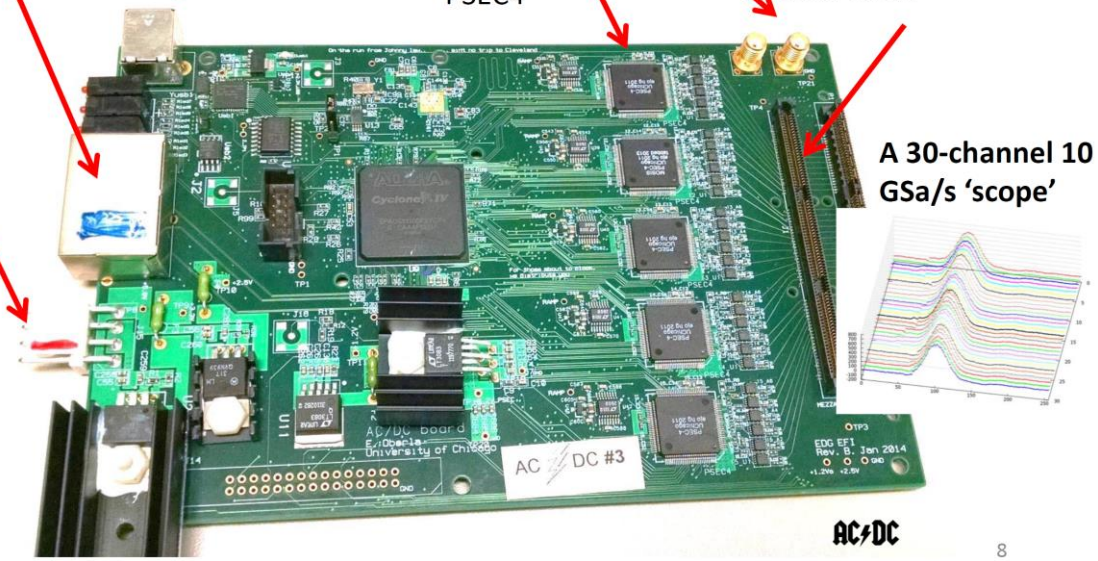
USB 2.0 for standalone operation

Calibration pulse input

Signal conditioning mezzanine / signal input. Plugs into LAPPDs with ribbon coax cable

30 channels of PSEC4

5V power ~1.5A



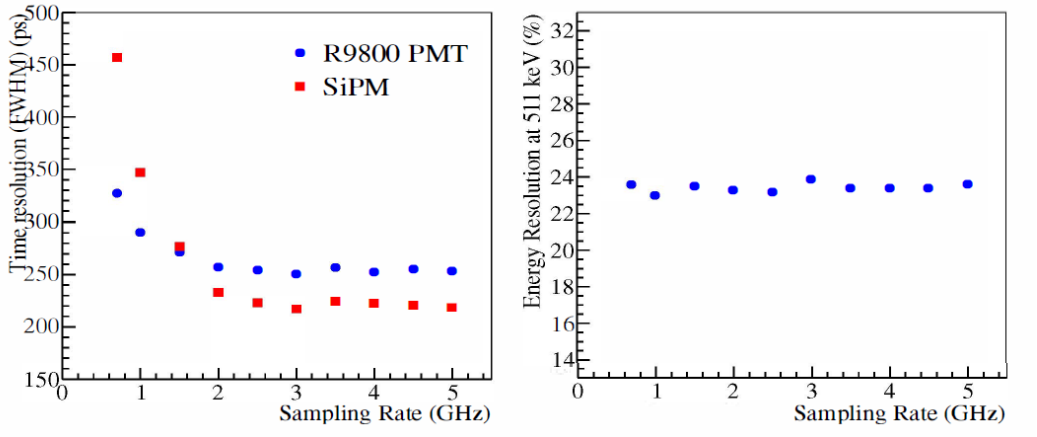
A 30-channel 10 GSa/s 'scope'

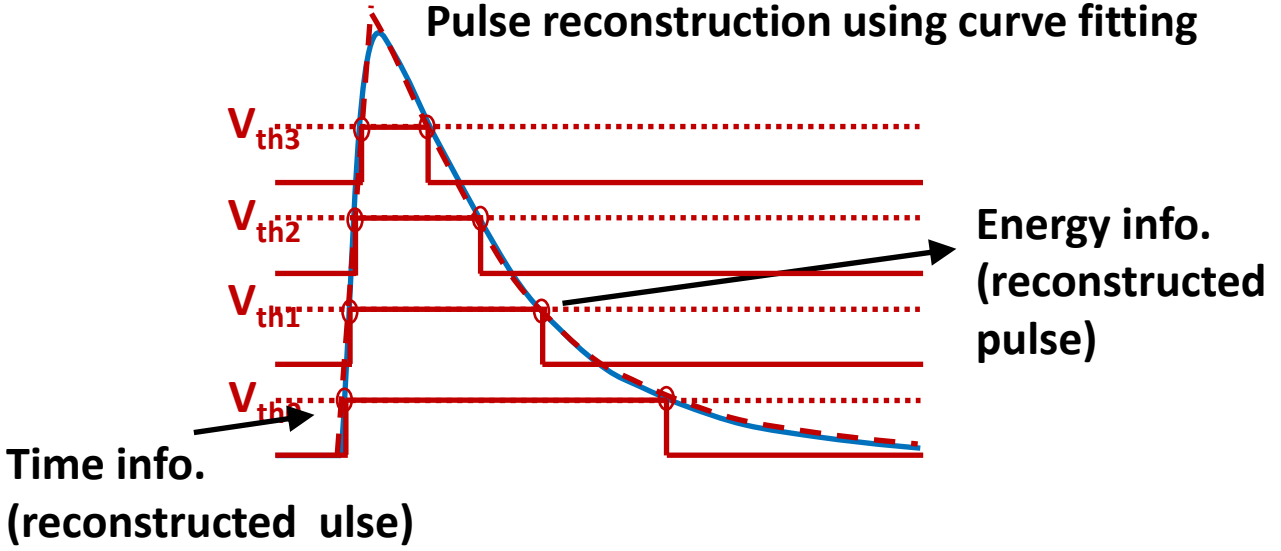
PSEC4a: 6 ch, 1024 samples, 2-11 GS/s

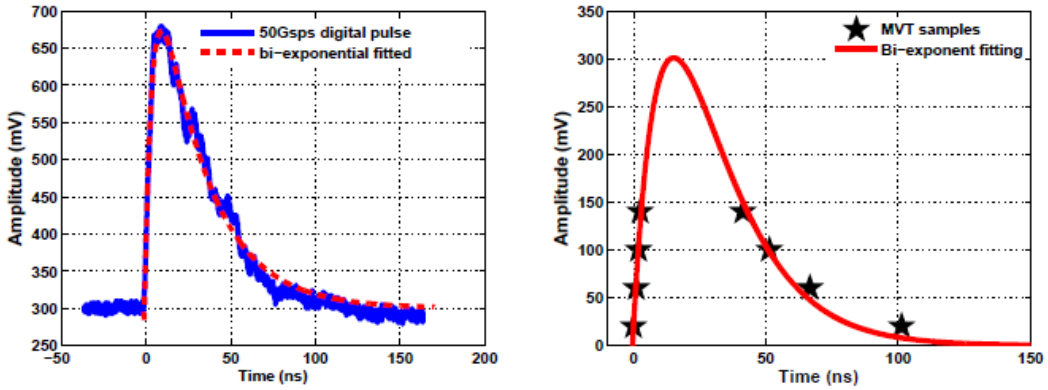
http://psec.uchicago.edu

DAQ Electronics

Multi-Voltage Threshold (MVT)



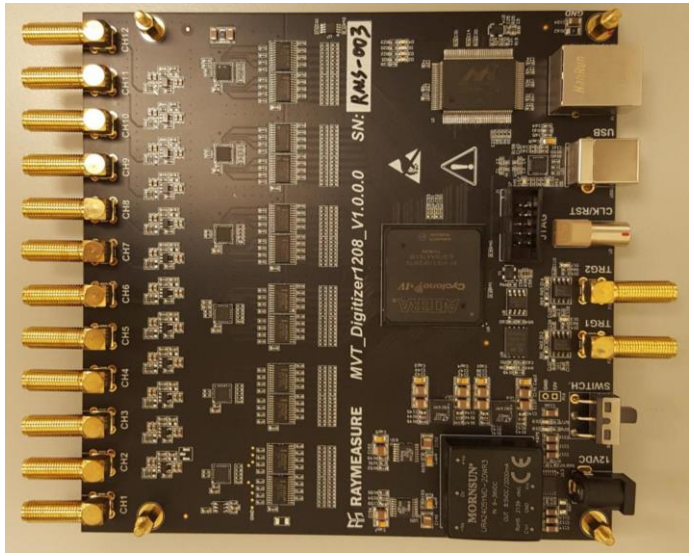




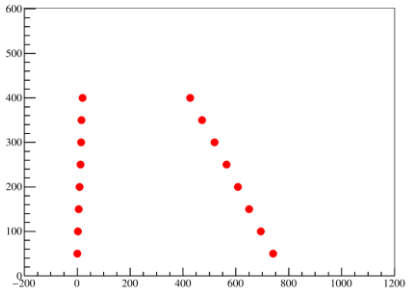
- can reconstruct pulse shape
- improve energy linearity

Data Acquisition Electronics

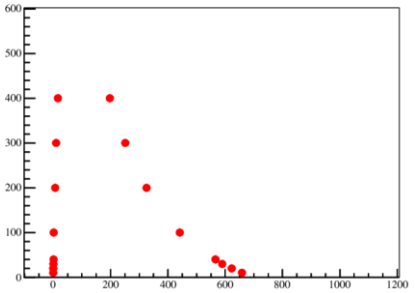
Multi-Voltage Threshold (MVT)



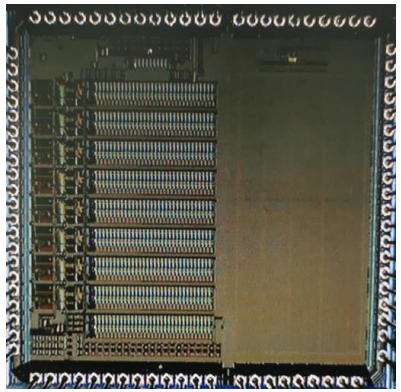
FPAG based
12 ch board, 8-level

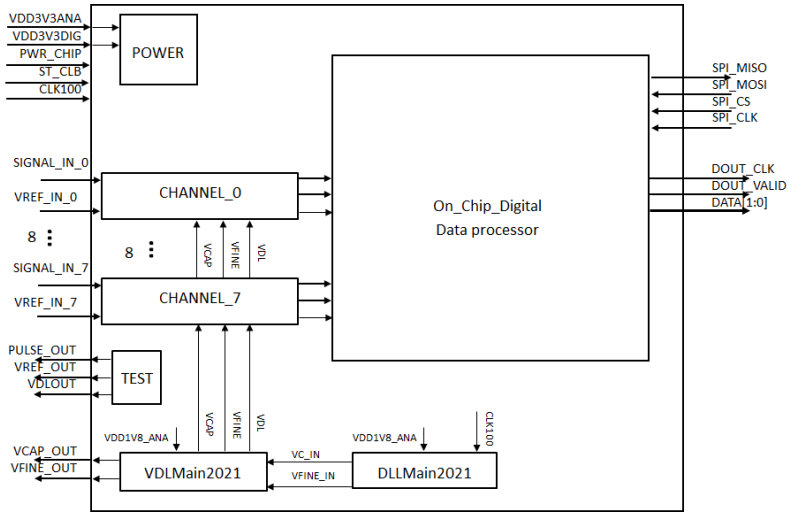


Test pulse



Scintillation pulse





MVT22-8 chip

- 8 ch, 4 level
- time res. ~60 ps between two channel

Courtesy of Prof. Q. Xie (HUST)

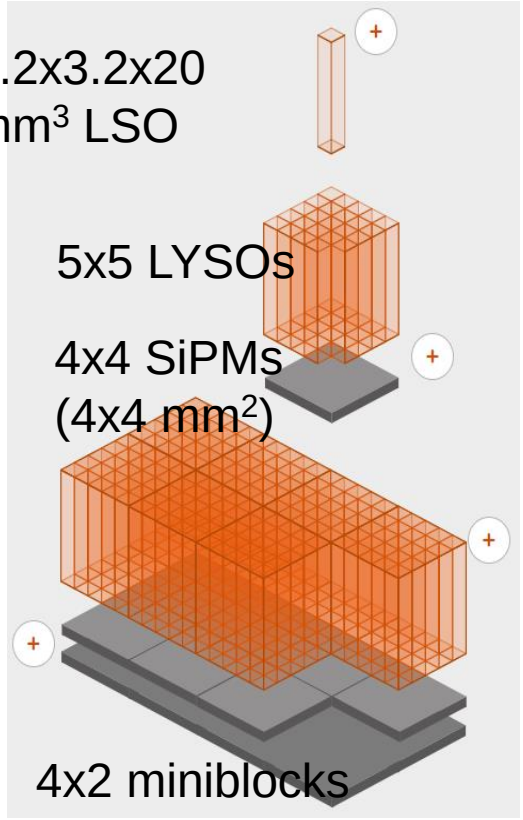
Commercial PET systems

Siemens Biograph Vision

~214 ps (Siemens)
~225 ps (Prenosil et al, JNM (2022))

Siemens UDR:

- 2x2 miniblocks => one elec. channel, 1 TDC, 4 ADCs
- 2 elect. Channel
  - ➢ 200 LSOs, 128 SiPMs (1.5625 ratio)



Detector electronics assembly (DEA):

- 2x8 UDRs
  - ➢ 3,200 LSOs, 2,048 SiPMs

Biograph Vision 600:

- 19 DEA on 82cm dia. Cylinder
- 26.3 cm length
  - ➢ 60,800 LSOs, 19*2,408=38,912 SiPMs

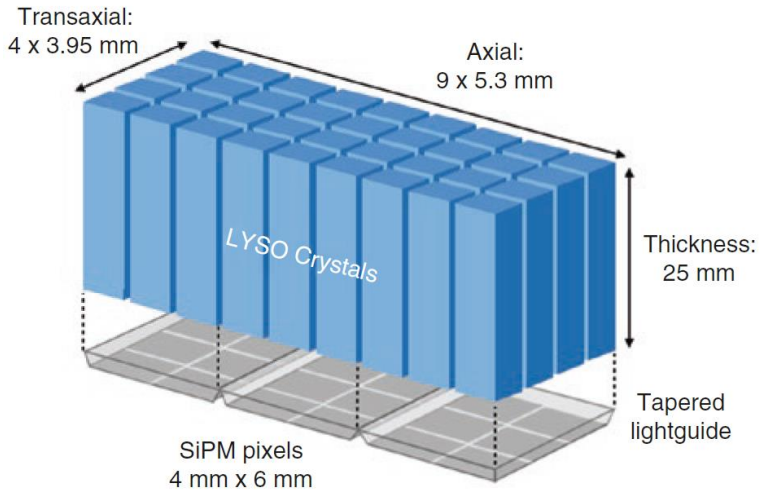
Biograph Vision Quadra

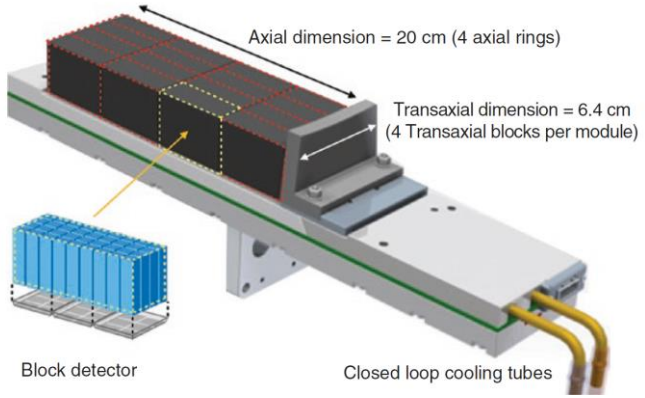
- 106 cm length
  - ➢ 243,200 LSOs, 155,648 SiPMs

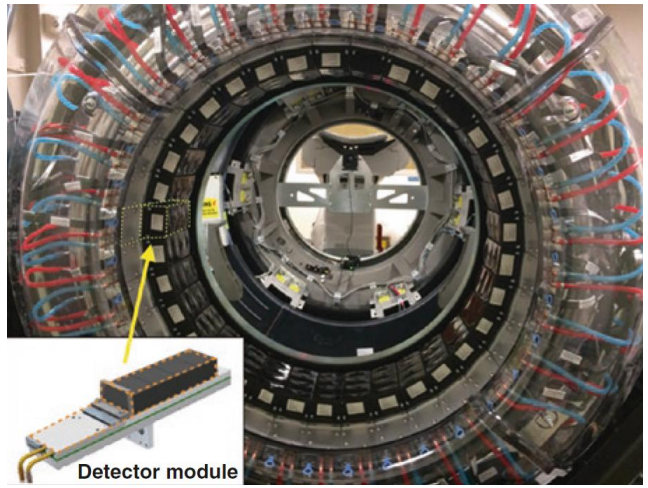
https://www.siemens-healthineers.com/

Commercial PET Systems

GE Discovery MI/Signa ~385 ps (Levin et al, IEEE TMI (2016))







- 4x9 LYSO crystal (3.95x5.3x25 mm^3)
- 3x6 Hamamatsu SiPMs, each 2x2 mm^2
- Light sharing multiplexing, tapered lightguide (36 LYSOs ➔ 18 SiPMs)
  - ➢ 36 LYSO s, 18 SiPMs (2:1 ratio)

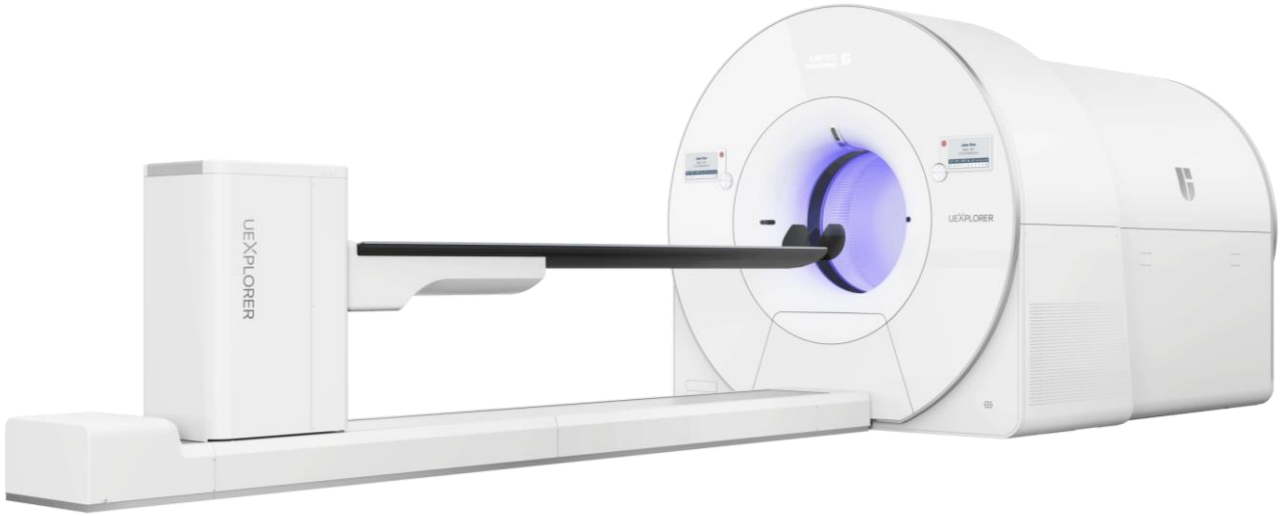
- detector module = 4x5 detector blocks for 25 cm length
  - ➢ 720 LSOs, 360 SiPMs

- D-MI: 34 detector modules on 74.4 cm dia. Ring
  - ➢ 24,480 LYSOs, 12,240 SiPMs
- Signa (PET/MR): 28 detector modules on a 62.4 cm dia. ring
  - ➢ 20,160 LYSOs, 10,080 SiPMs

Hsu and Levin (2020) in *Advances in PET*

Commercial Systems

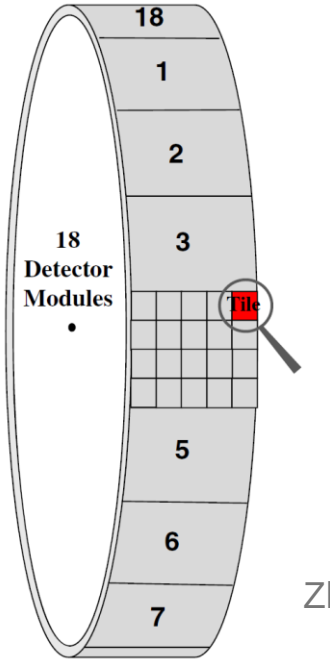
UI uExplorer ~412 ps (Spencer et al, JNM (2021))

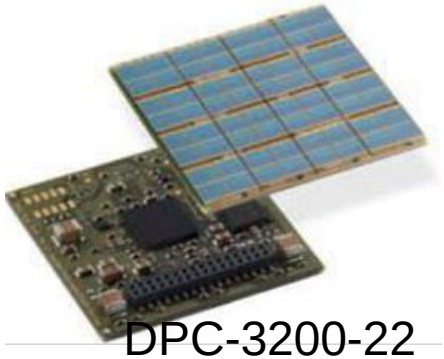


- Detector block = 7x6 LYSO array of 2.76x2.76x18.1 mm^3 ➔ 2x2 SiPMs of 6x6 mm^2 SensL J-series SiPMs
  - ➢ 42 LYSOs, 4 SiPMs (10.5:1 ratio)
- Detector module = 5 (transaxial) x 14(axial) detector blocks
  - ➢ 2,940 LYSOs, 280 SiPMs
- Unit = 24 detector modules, 24.02 cm long, 78.6 cm diameter
  - ➢ 70,560 LSOs, 6,720 SiPMs
- 8 units ➔ axial length 194 cm
  - ➢ 564,480 LYSOs, 53,760 SiPMs

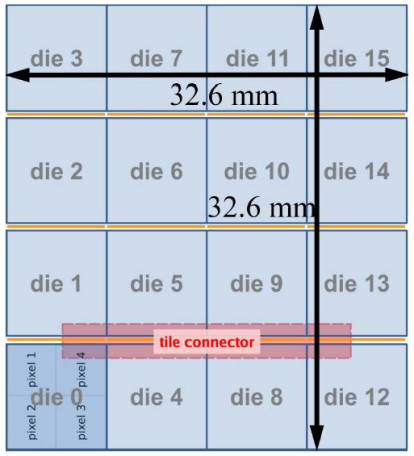
Commercial PET Systems

Philips Vereos ~315 ps (Miller et al, JNM (2015))

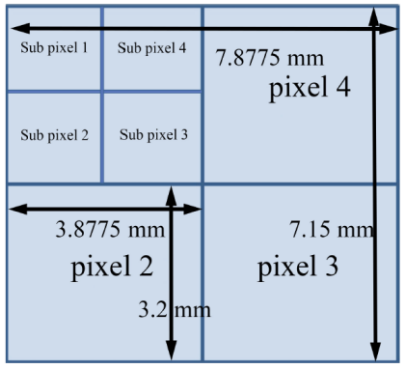




DPC-3200-22
8x8 dSiPMs



Liu et al, JINST (2016)



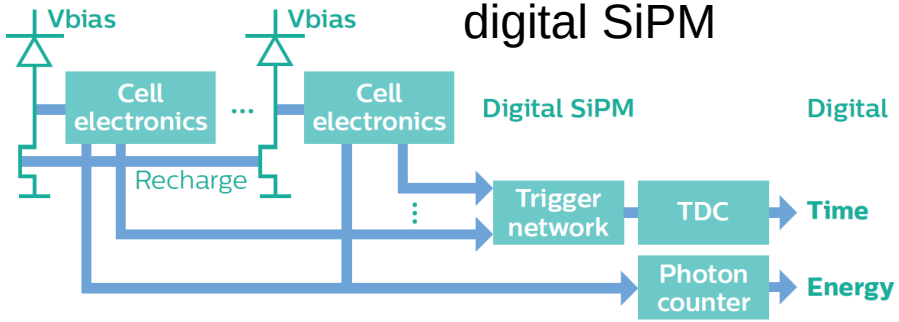
Zhang et al, EJNMMI (2018)

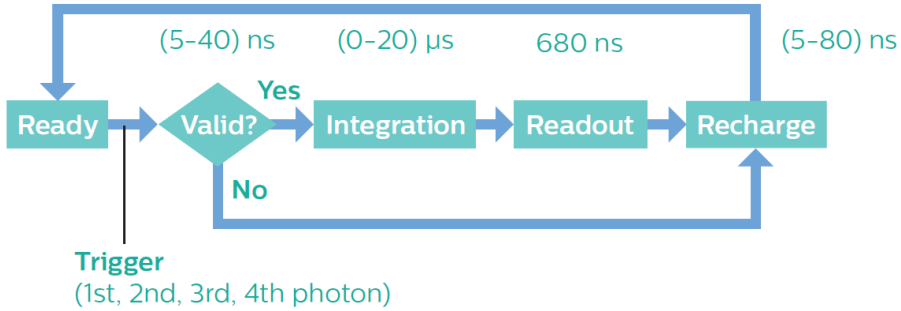
18 detector modules
- 5x4 DPC sensors
- 40x32 array of 4x4x19mm^3 LYSOs
- 1,280 dSiPMs/module
- 23,040 dSiPMs total

2x2 pixels
- 3200 APDs/pixel
- Pixel has individual counter

4x4 independent dies, but share 2 TDCs and produce 1 time stamp

digital SiPM





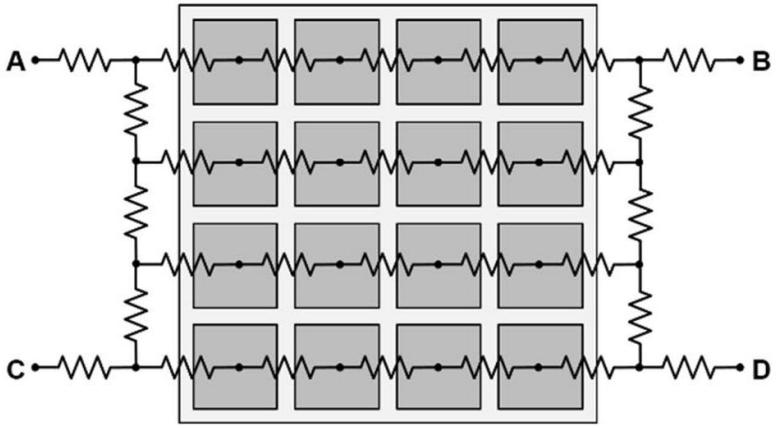
Philips Manual

Multiplexing Readout

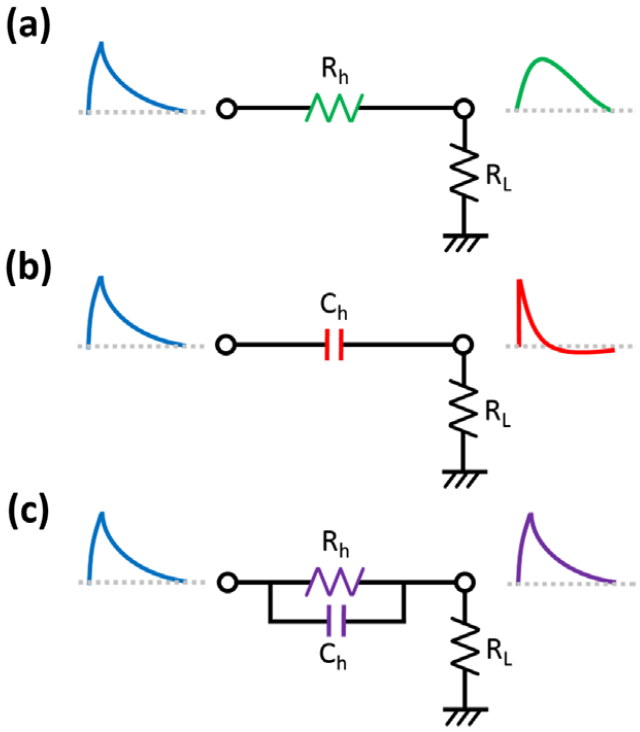
Park et al, Biomed Eng Lett (2022)

Charge modulation based

Discretized positioning circuit (DPC)

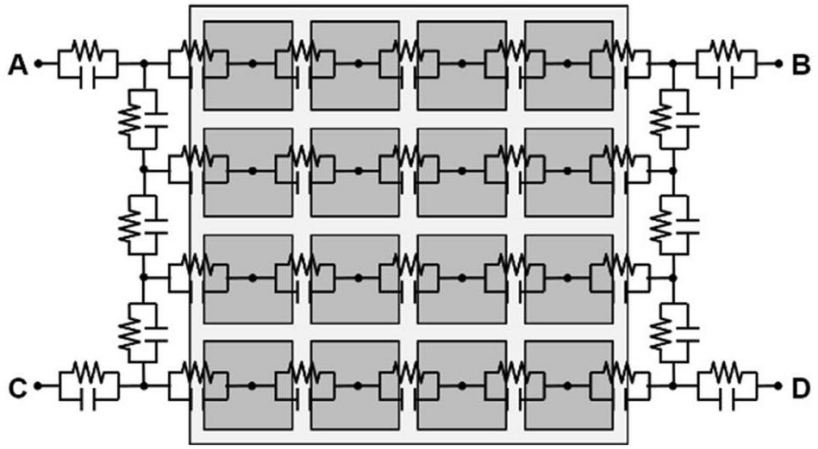


- Z=A+B+C+D; X=(B+C)/Z; Y=(A+B)/Z
- suitable for compact module
- undesirable RC delay
- Resistors ➔ capacitors: better timing



Park et al, PMB (2017)

hybrid DPC



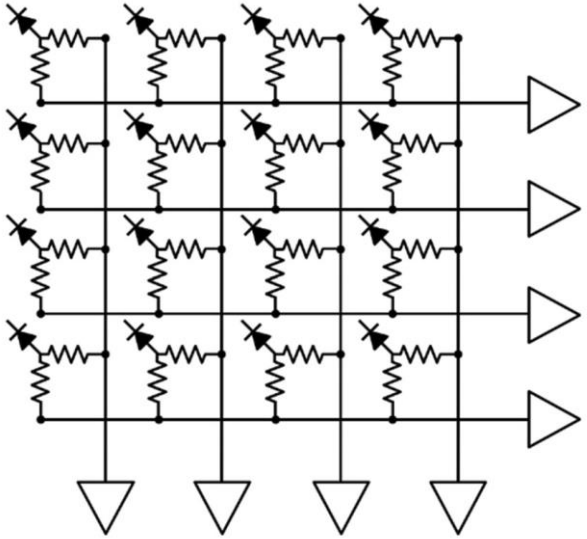
- improved timing
- shape uniformity

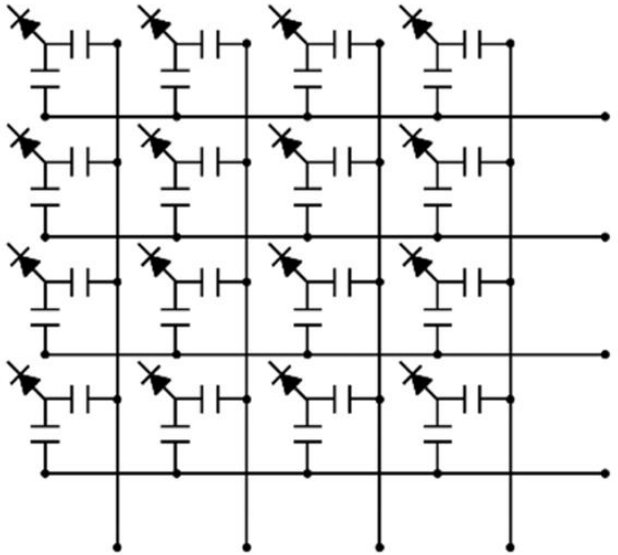
Multiplexing Readout

Park et al, Biomed Eng Lett (2022)

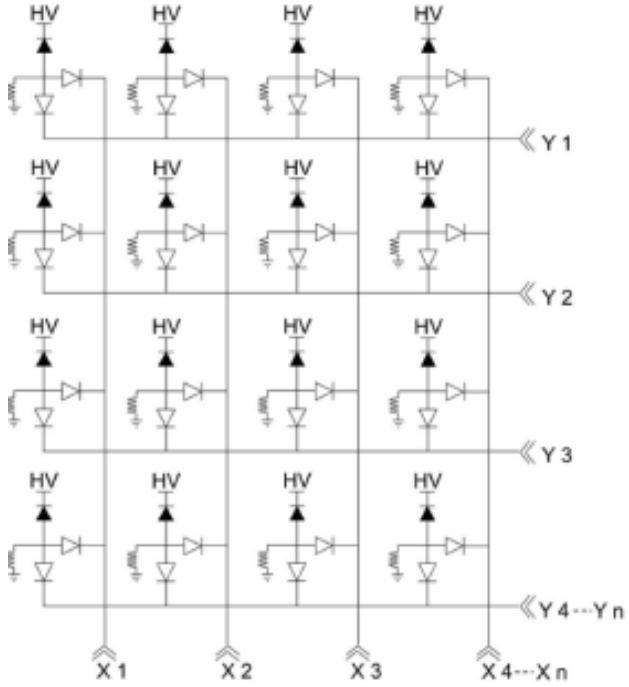
Charge modulation based

row-column sum





- performance > DPC but more preamp and readout channels
- capacitor–based has better timing
- cross talks between channels



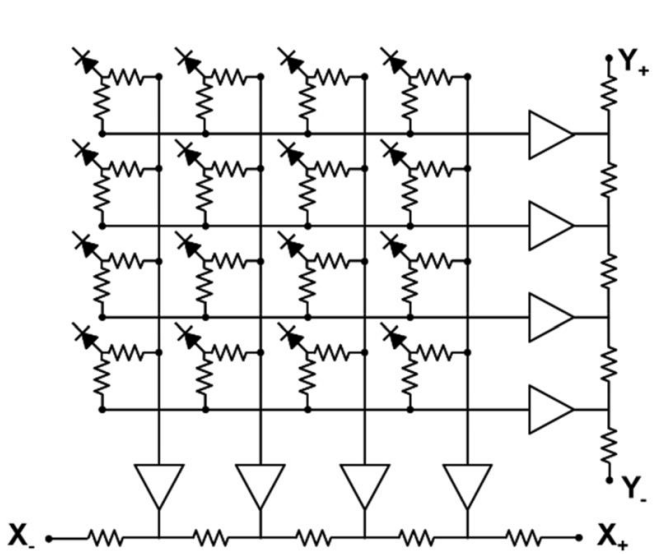
- Use diodes to reduce cross talks

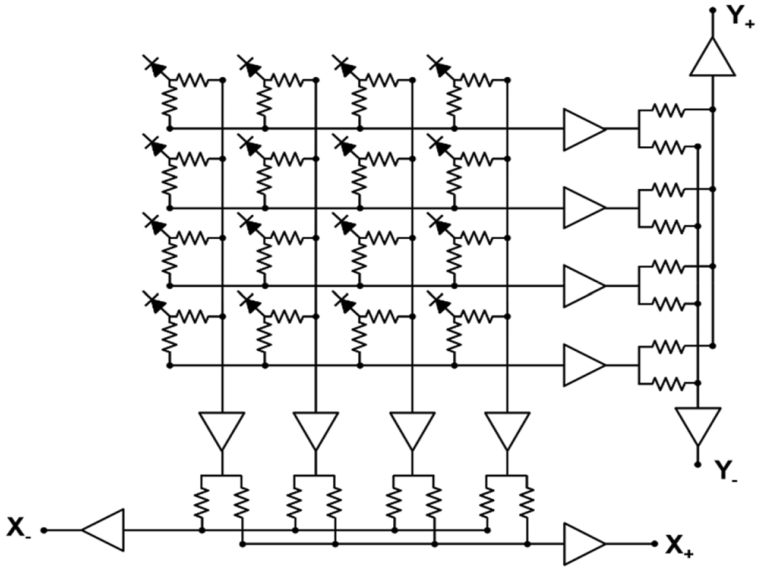
Multiplexing Readout

Park et al, Biomed Eng Lett (2022)

Charge modulation based

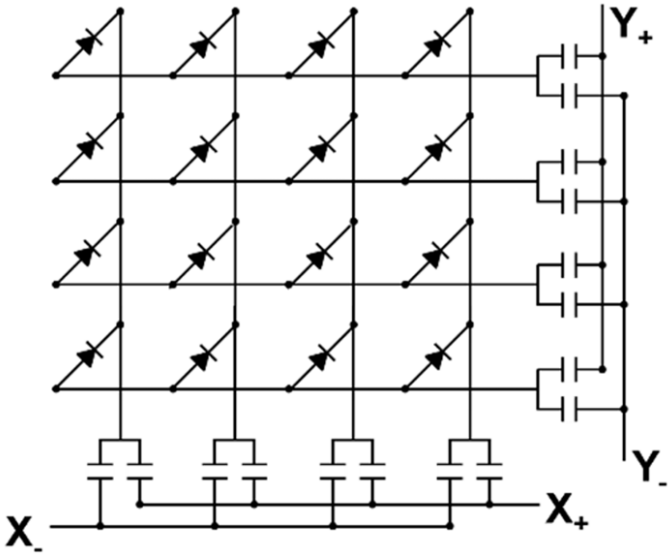
symmetric charge division (SCD)





- row-column sum + 1d resistive chain
- reduce # readout channels

Cross-strip capacitive coupling

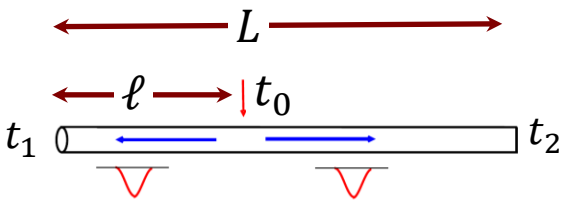


Multiplexing Readout

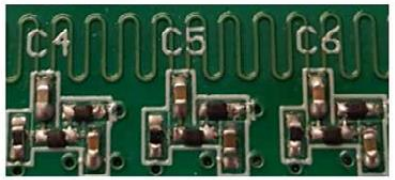
Park et al, Biomed Eng Lett (2022)

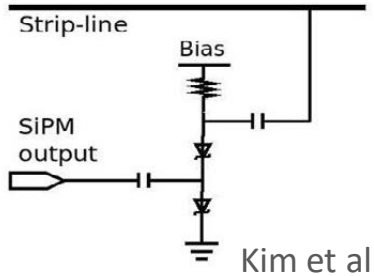
Time modulation based

Stripline readout

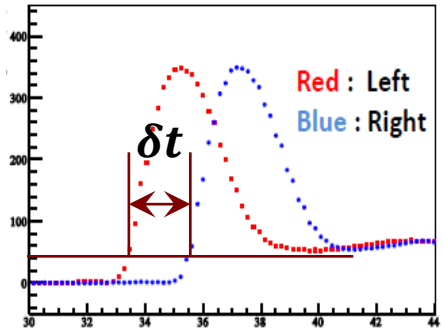


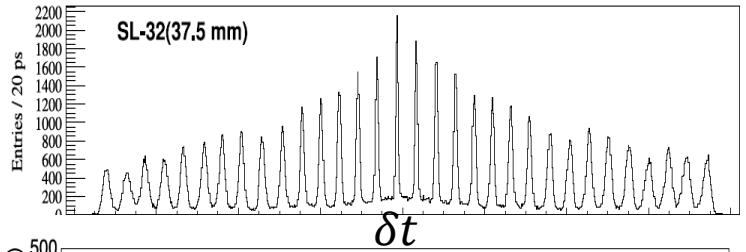
$$\delta t = t_1 - t_2 = 2\ell/v$$

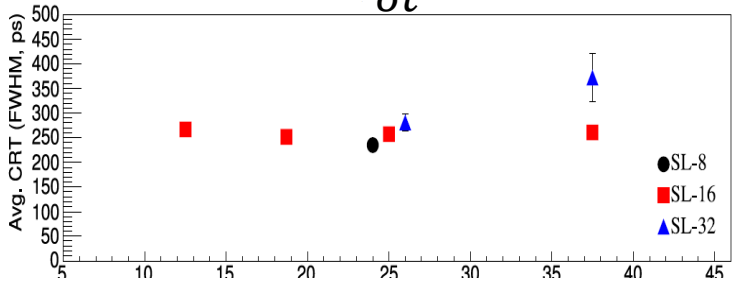




Kim et al , NIMA (2020)

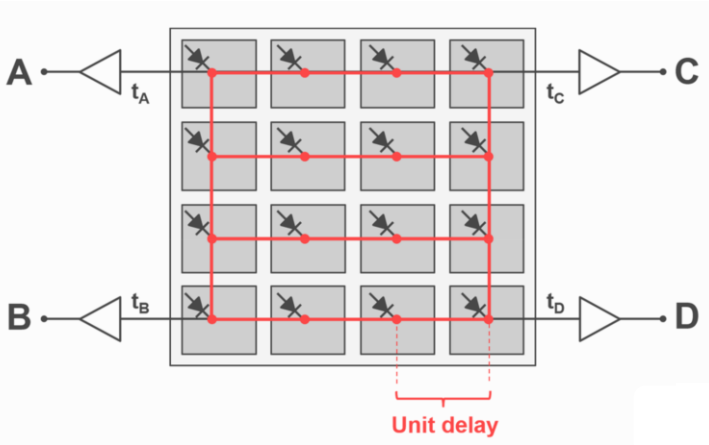


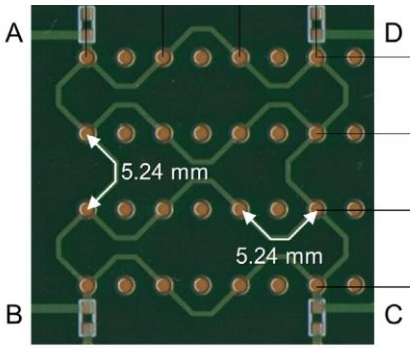




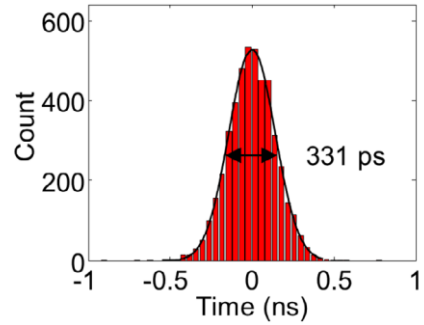
Trace length

delay grid multiplexing





$$x = ((t_A - t_C) + (t_B - t_D))/4$$
$$y = ((t_B - t_A) + (t_D - t_C))/4$$

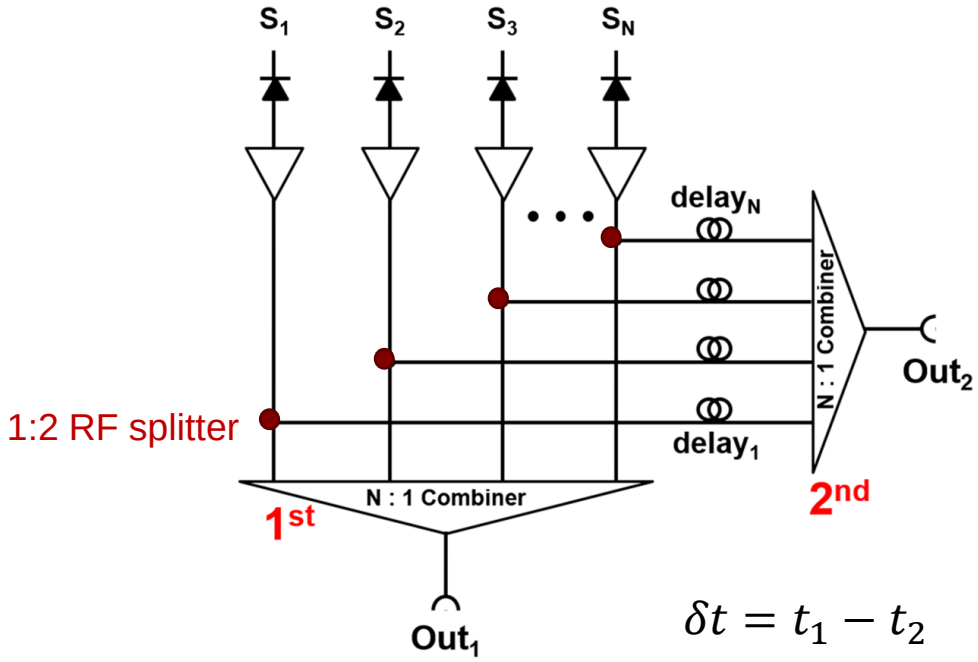


Multiplexing Readout

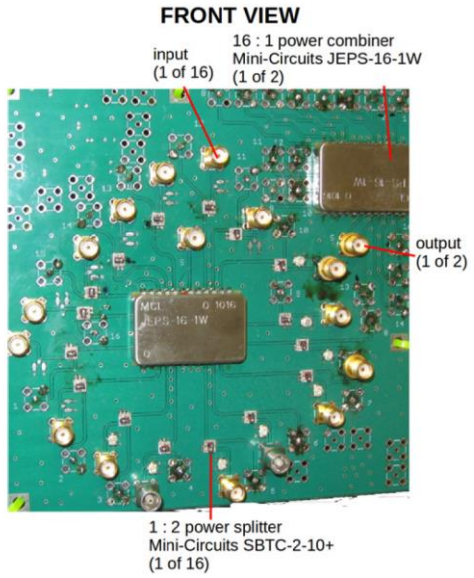
Park et al, Biomed Eng Lett (2022)

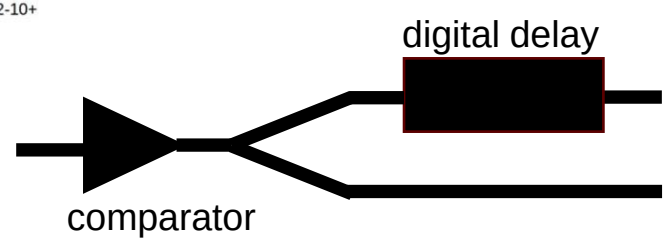
Time modulation based

electrical delay line multiplexing



$$\delta t = t_1 - t_2$$

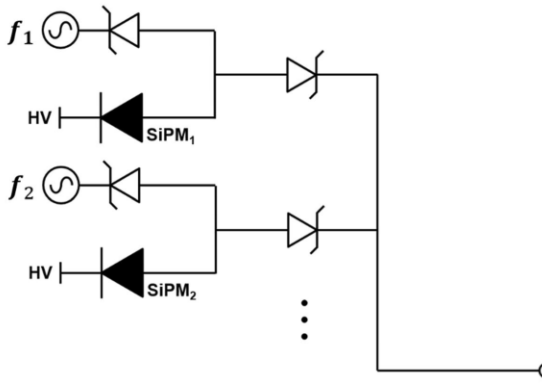


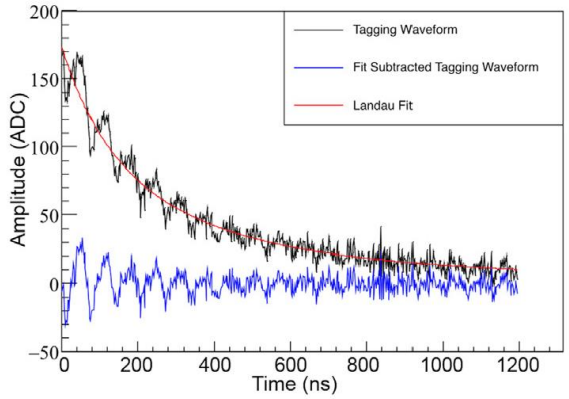


Multiplexing Readout

Park et al, Biomed Eng Lett (2022)

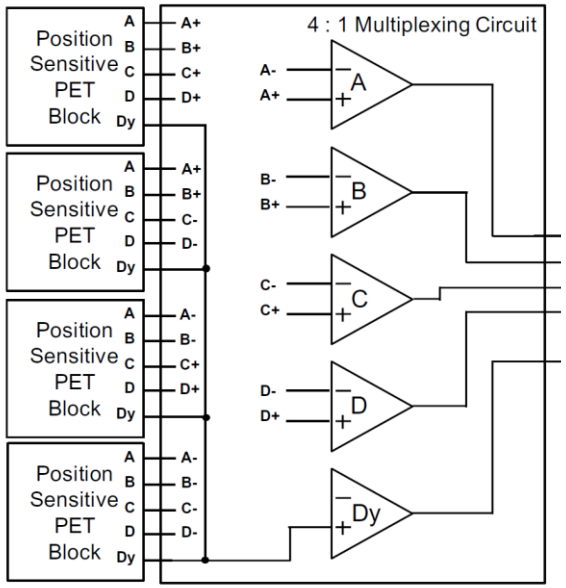
Frequency modulation based

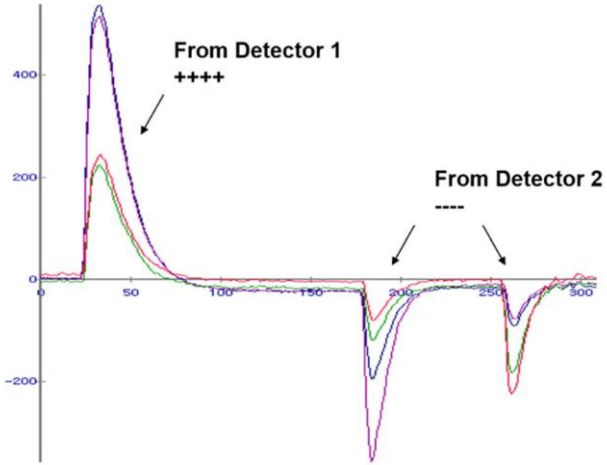




- Single sinusoid source per SiPM → scalability?

Polarity modulation based





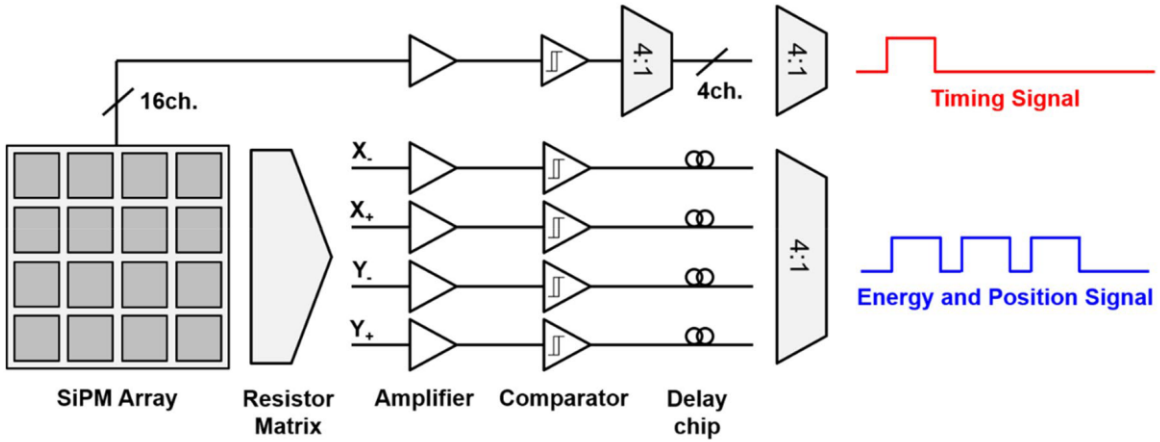
Multiplexing Readout

Park et al, Biomed Eng Lett (2022)

Digital modulation based

- Early digitization allows better performance
- Digital multiplexing can be based on FPGA

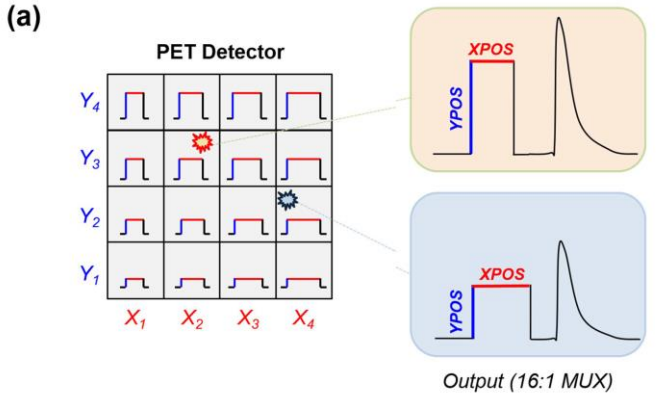
digital pulse sequence generation



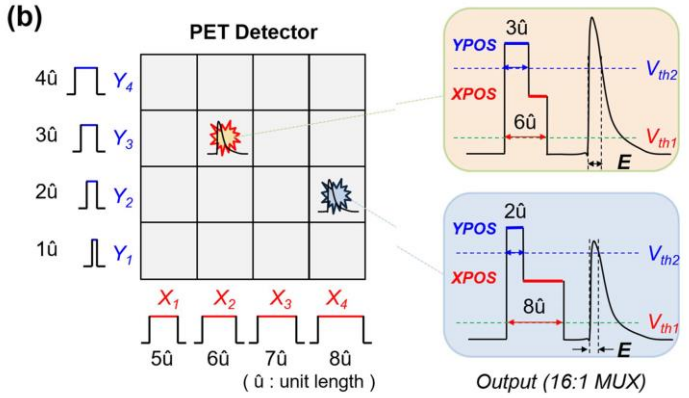
+500 ns

Multiplexing ratio 16:2

Pulse-tagging



use ADC

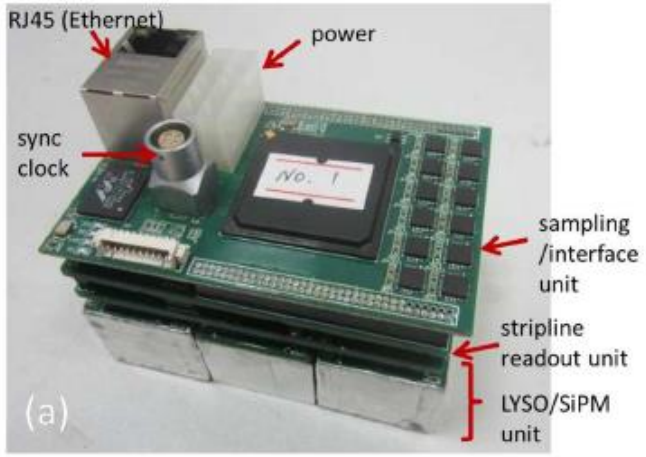


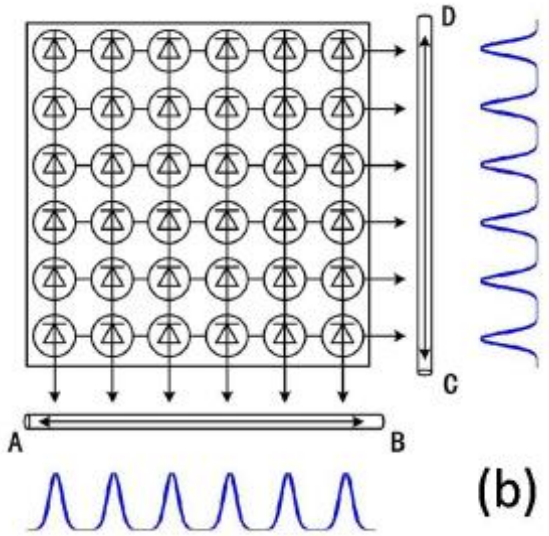
TDC only

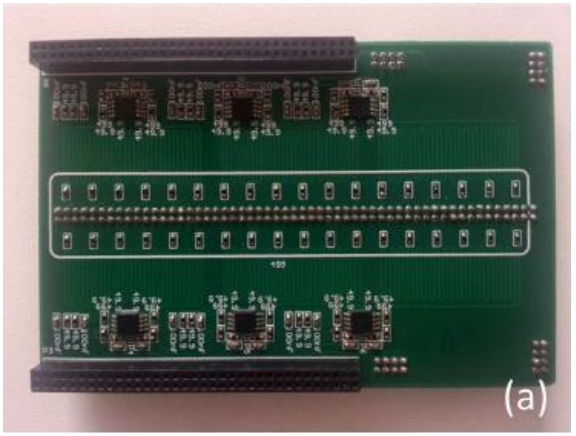
Multiplexing ratio 16:1

Examples

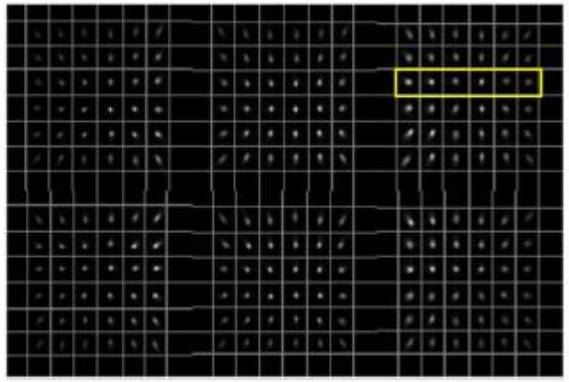
Modular PET unit

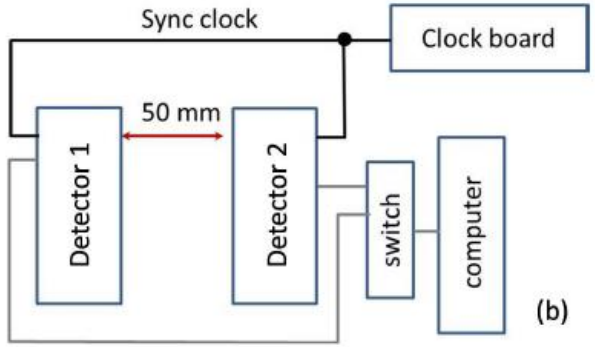






18x12 LYSO/SiPM

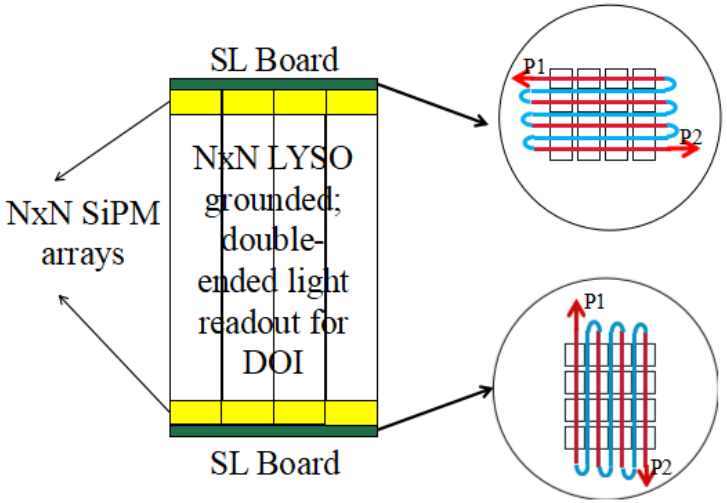


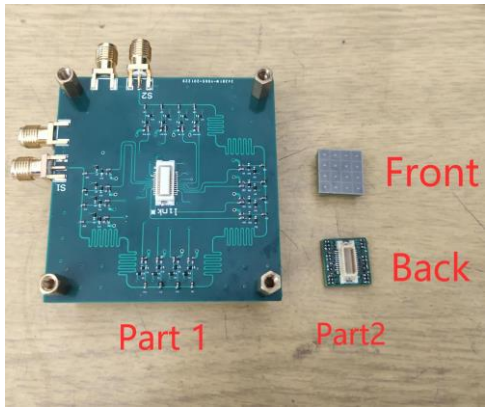


D. Xi et al, JMI, 2017

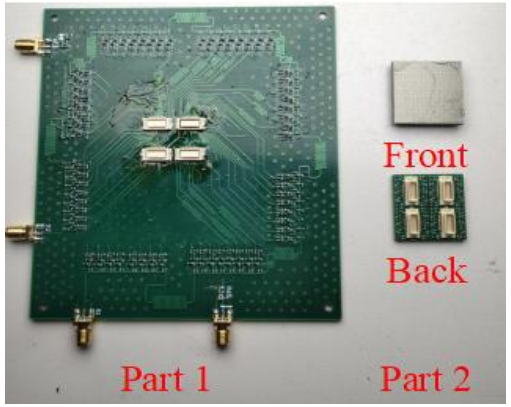
Examples

Compact DOI/TOF detector

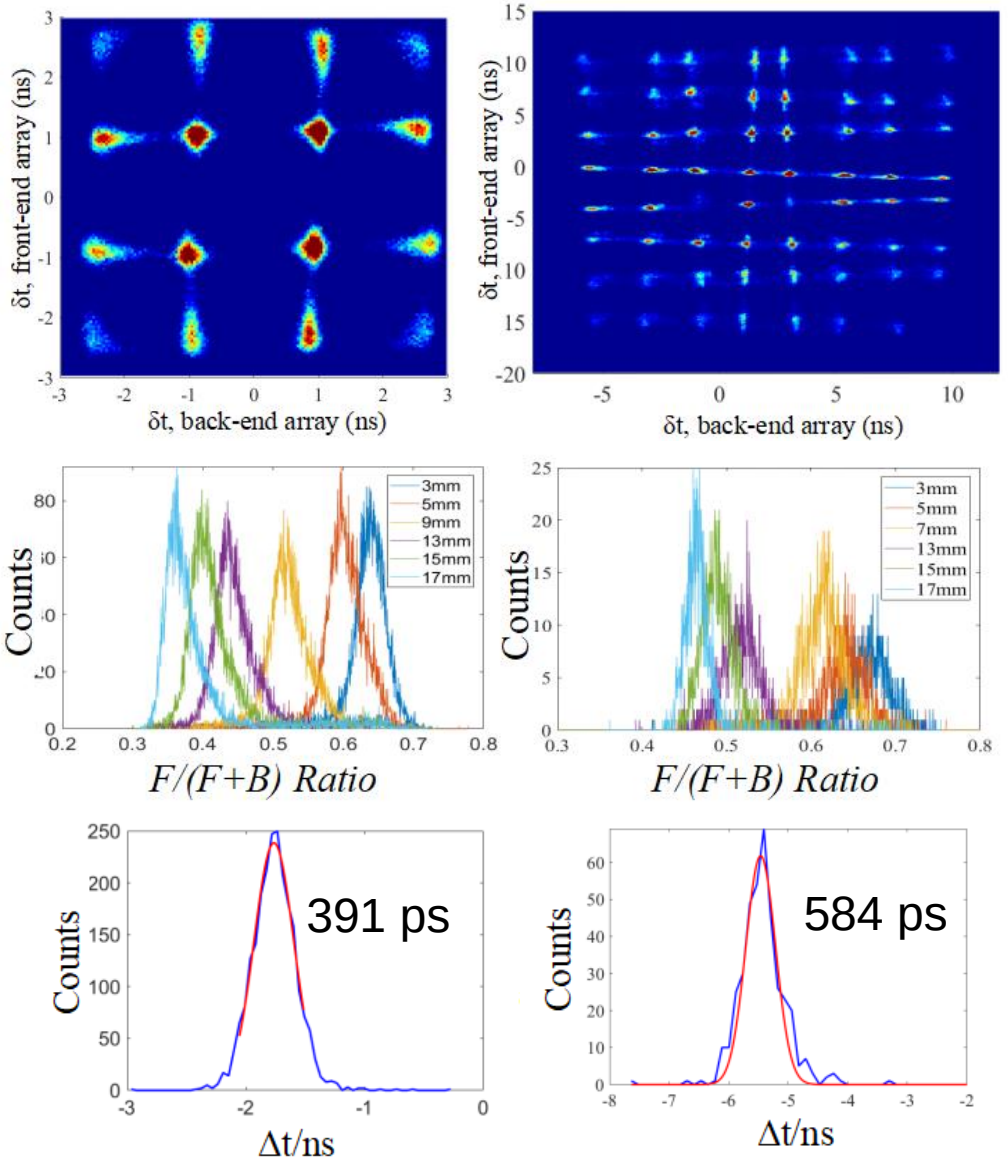




4x4

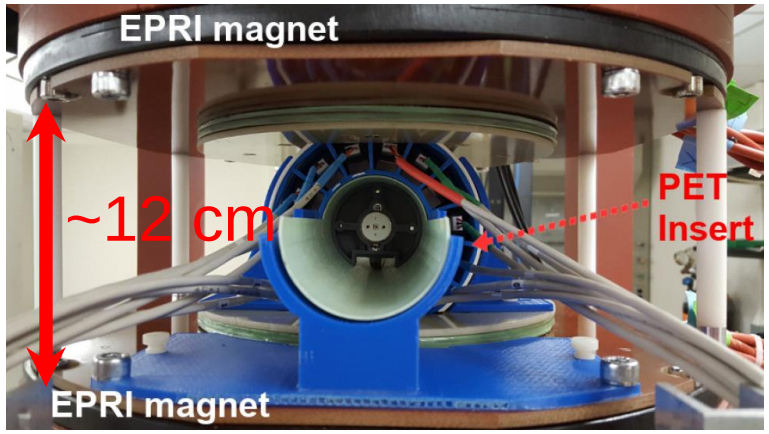


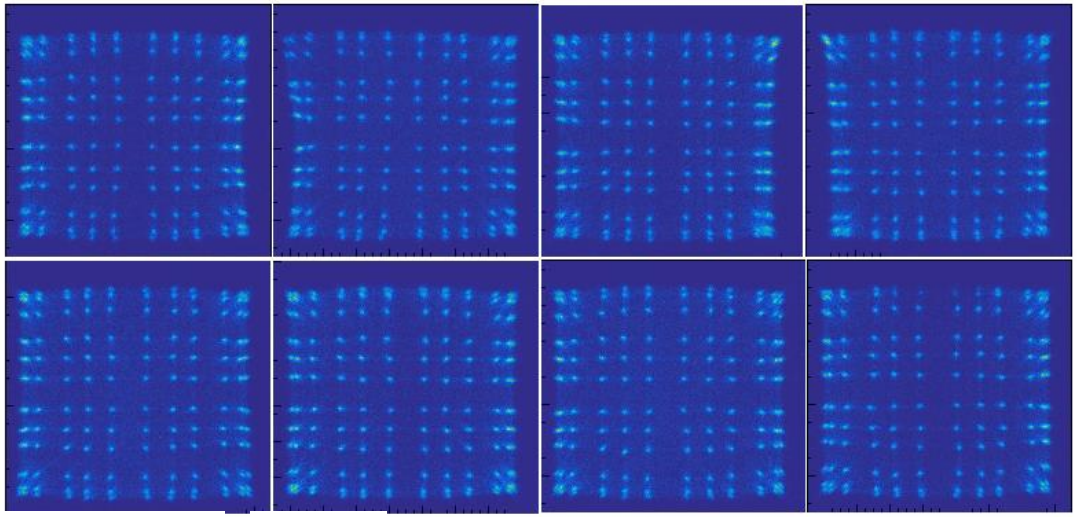
8x8

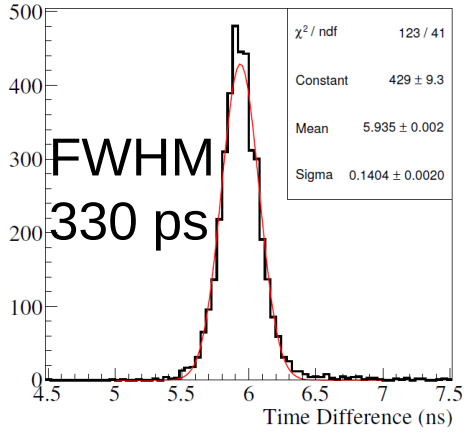


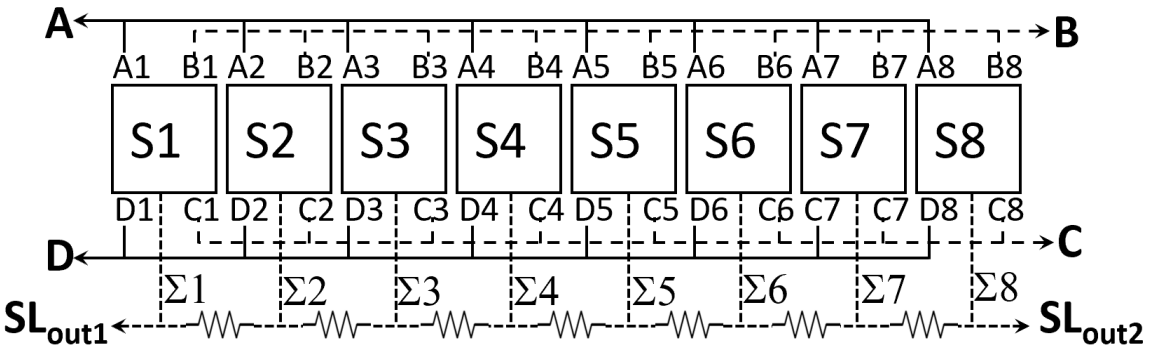
Examples

Detector for hybrid PET/EPRI

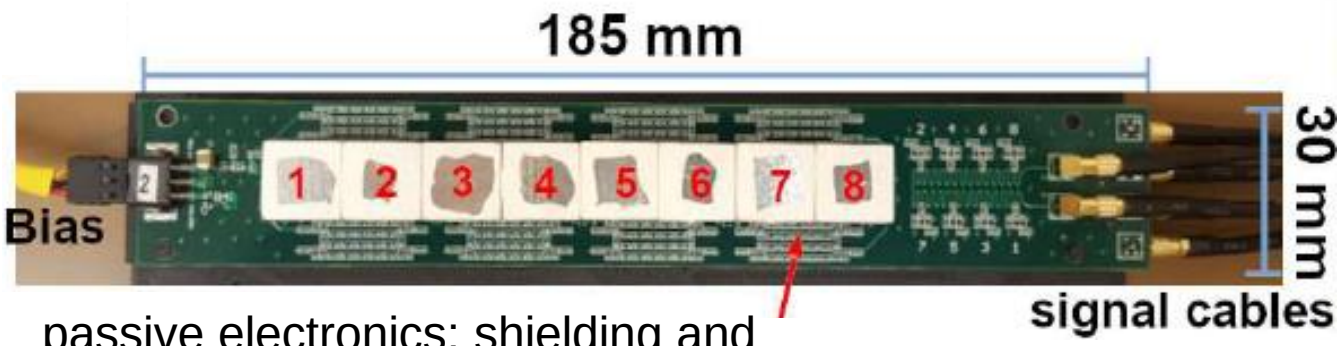








1,152 LYSOs ➔ 128 SiPMs ➔6 outputs



passive electronics: shielding and heat problem are reduced

Pulsar Board R&D Goals

The Pulsar is a custom **ATCA full mesh** enabled **FPGA-based** processor board which has been **designed with the goal of creating a scalable architecture abundant in flexible, non-blocking, high bandwidth interconnections**. Initially motivated by silicon-based tracking trigger R&D needs for LHC experiments, the Pulsar is uniquely positioned as a **flexible general-purpose platform ideally suited to situations where multiple processing engines need to be tightly coupled.**

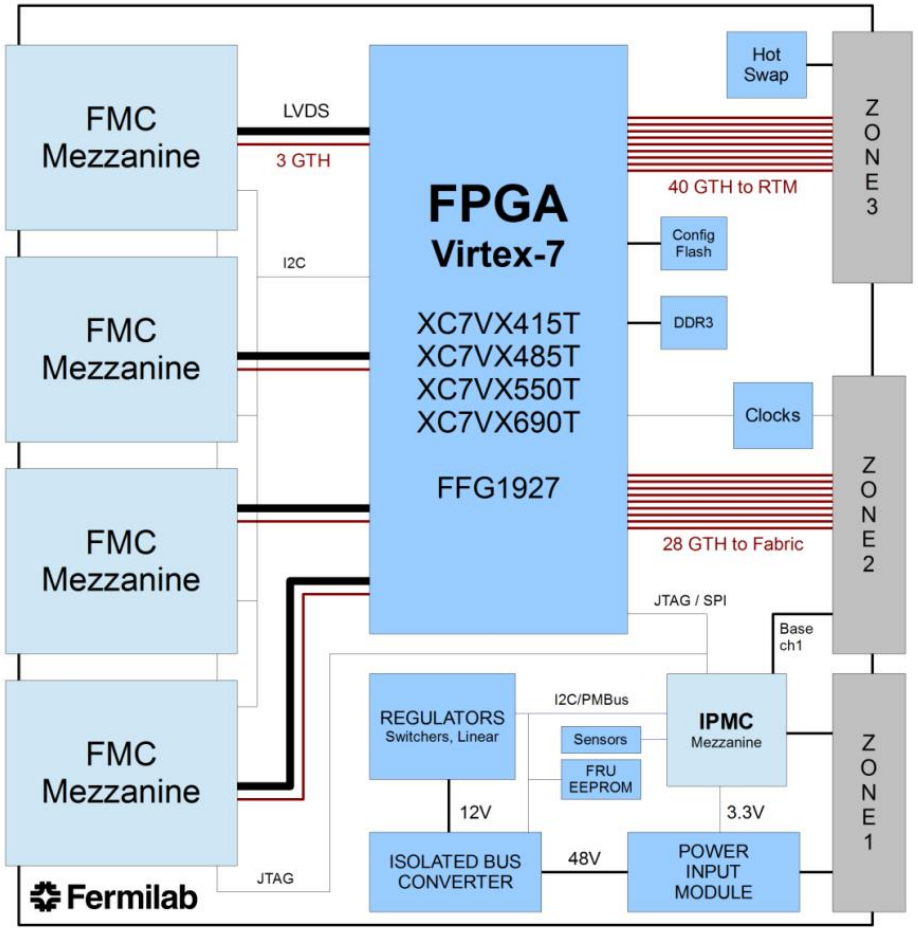
- ATCA platform, full mesh backplane
- Scalable, flexible, interconnected
- High bandwidth interconnects
- FPGA based, general purpose
- Multiple processors, tightly coupled
- Blur the distinction between FPGAs

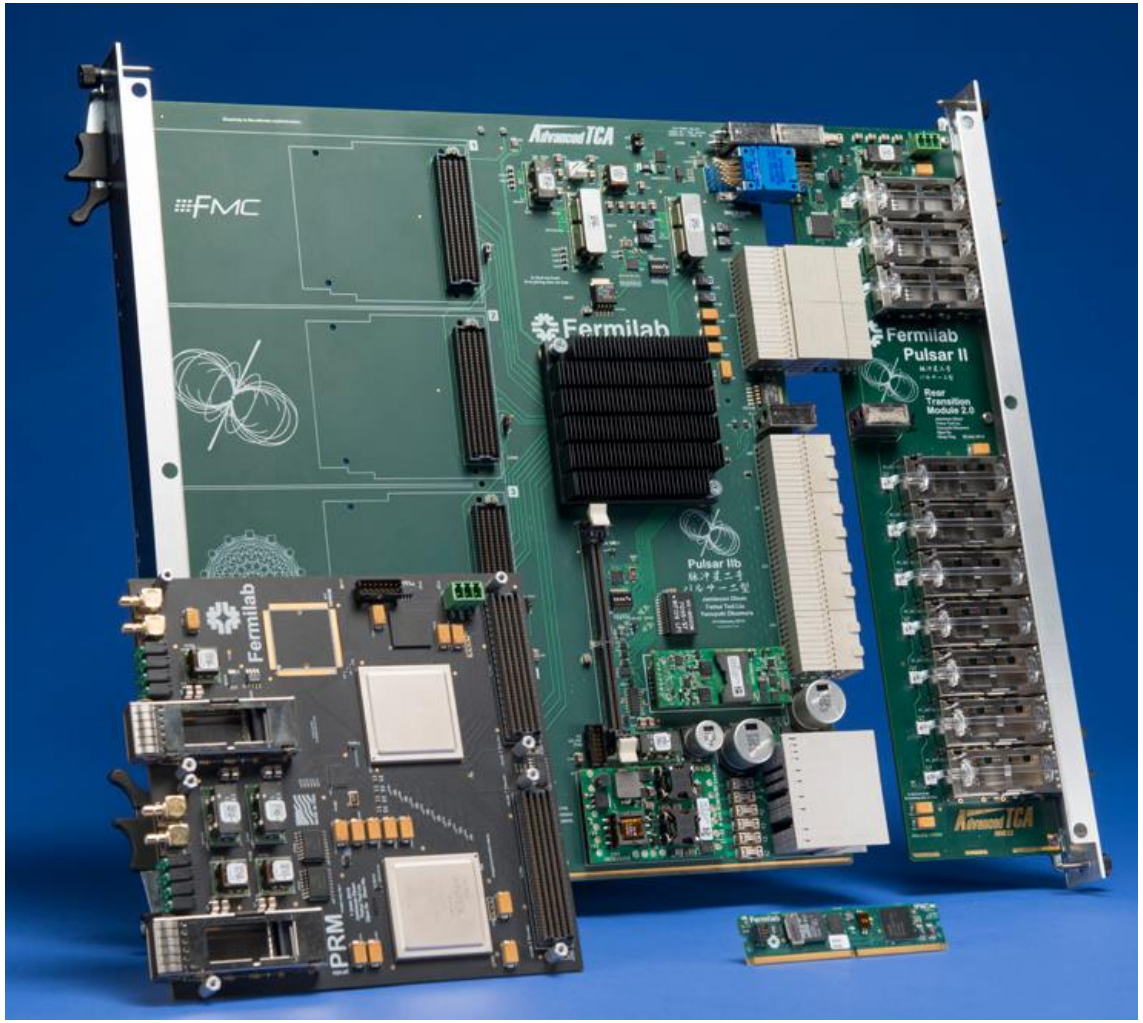
ATCA Background

- Advanced **Telecommunications** Computing Architecture
  - » High availability
  - » Redundant 48V power
  - » Redundant control
  - » Hot swap everything
- Unique full mesh backplane
  - » 4 lanes between all slots
  - » 10G – 40G – 100G
- Large 8U x 280mm form factor
- High power 300W+ per slot
- IPMI management of intelligent field replaceable units

Courtesy of Dr. T. Liu (FNAL)

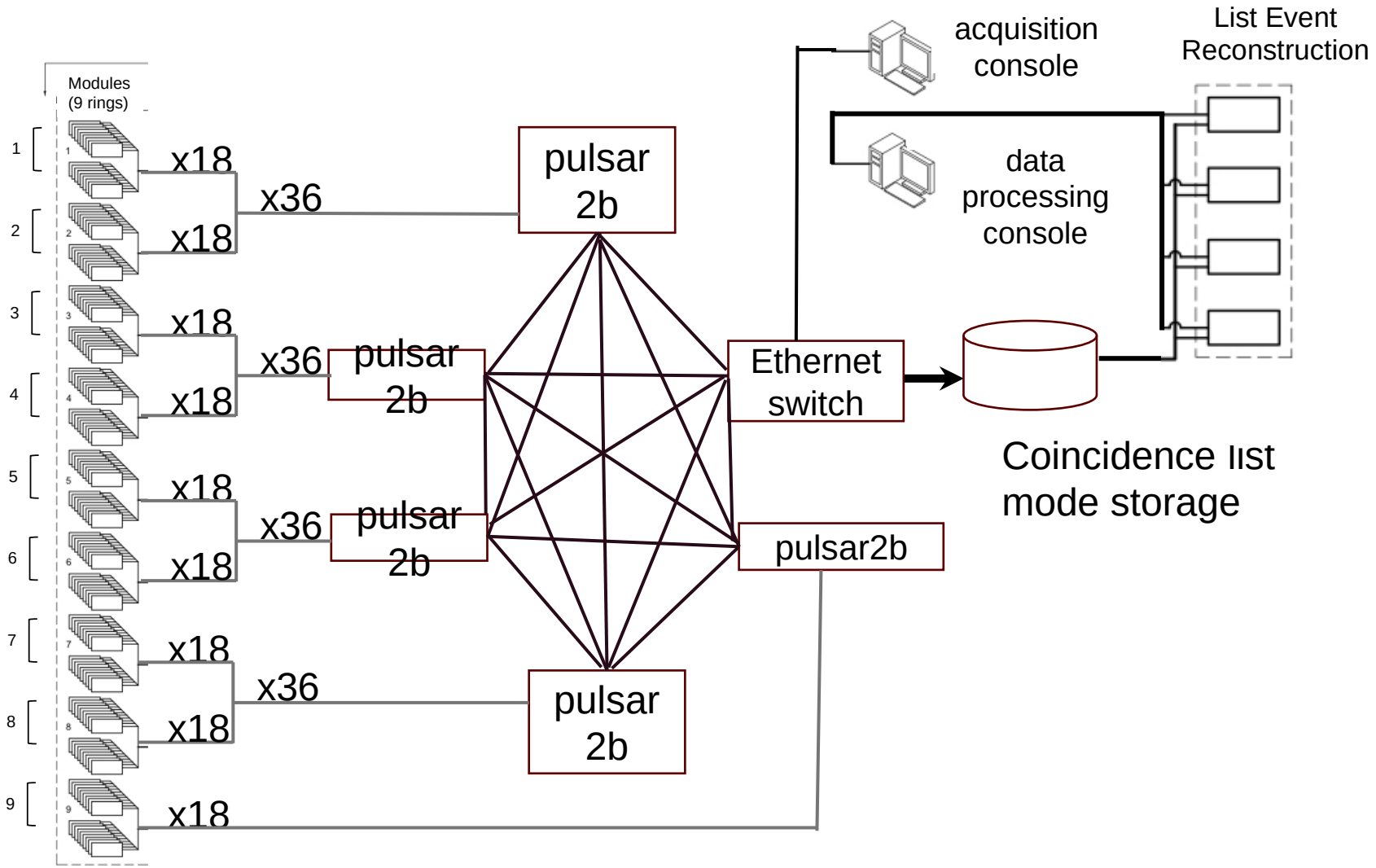
Pulsar2b Results





Pulsar2a/2b Expansion: Mezzanine Cards

- Single and Double wide FMC mezzanine cards
- Test high speed interfaces (LVDS, MGT) to Pulsar boards
- Expand processing power (2 x KU060 FPGAs)
- Standalone test platform for Pattern Recognition Associative Memory Devices
  - » ASIC
  - » FPGA
- Track finder board in the demonstration system

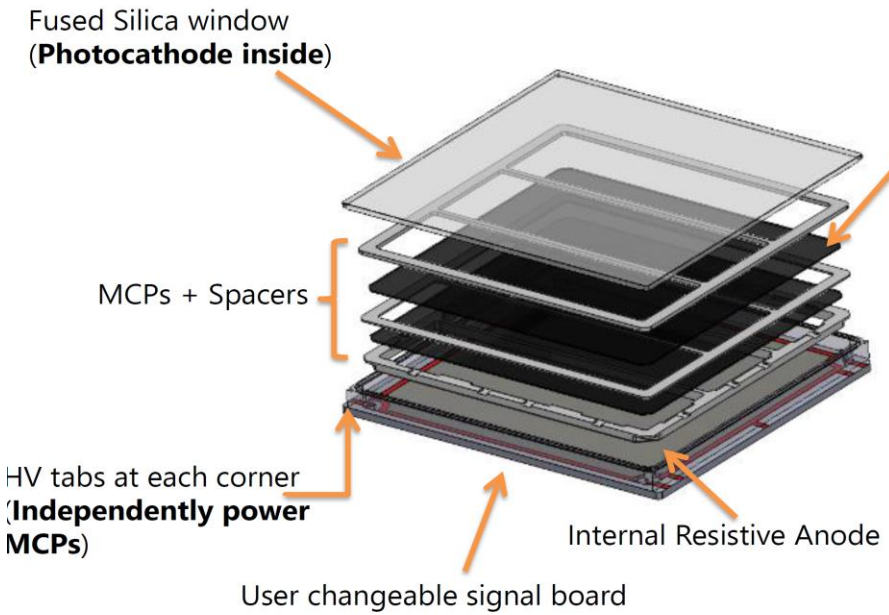

Modules
(9 rings)
1
2
3
4
5
6
7
8
9
x18
x18
x18
x18
x18
x18
x18
x18
x18
x36
x36
x36
pulsar
2b
pulsar
2b
pulsar
2b
pulsar
2b
Ethernet
switch
pulsar2b
acquisition
console
data
processing
console
List Event
Reconstruction
Coincidence list
mode storage

Observation

- time of flight ➔ need high bandwidth-gain product, power consumption
- Insert, OS systems ➔ limited space, heat
- long-bore system ➔ extremely larege number of channels
  - » Multiplexing, helps but TOF? count rate?
- Scalable backend electronics? For digital waveform processing?

DAQ Electronics

LAPPD Design



- **No wall or anode penetrations**
- **Active area: 195 mm x 195 mm**
  - **Grid Spacer leaves active area of 373 cm² (97%)**

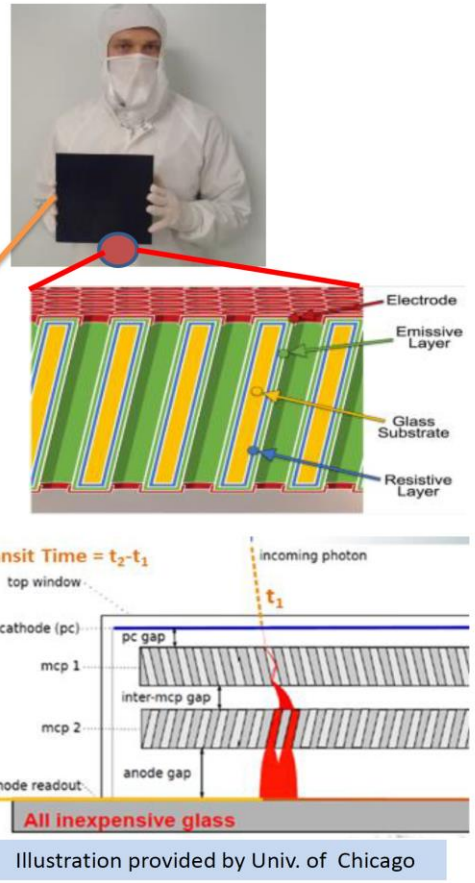
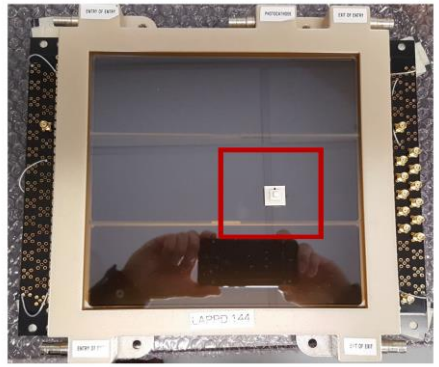
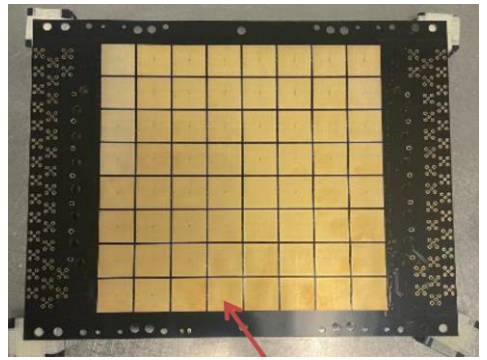
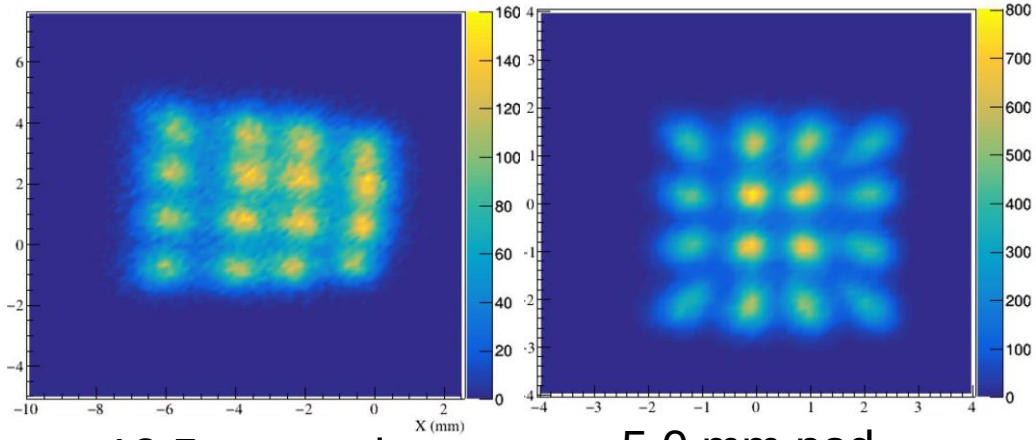


Illustration provided by Univ. of Chicago





4x4 array of 3x3x10 mm³ LYSO



12.5 mm pad
25.9 mm pitch

5.0 mm pad
6.0 mm pitch

DAQ Electronics