Capabilities from the Physical Sciences

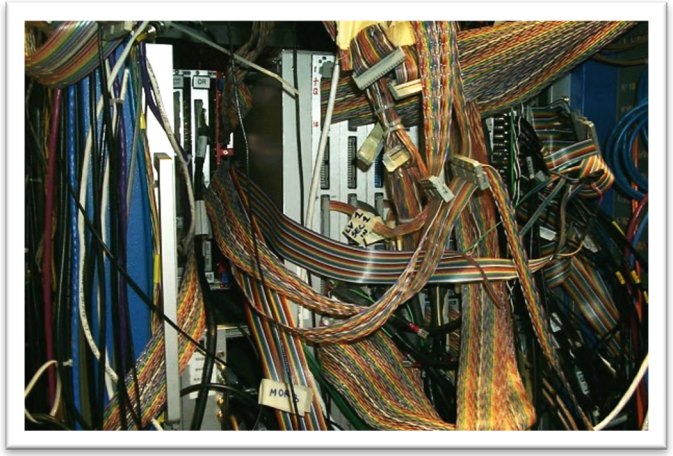
Electronics and Data Acquisition

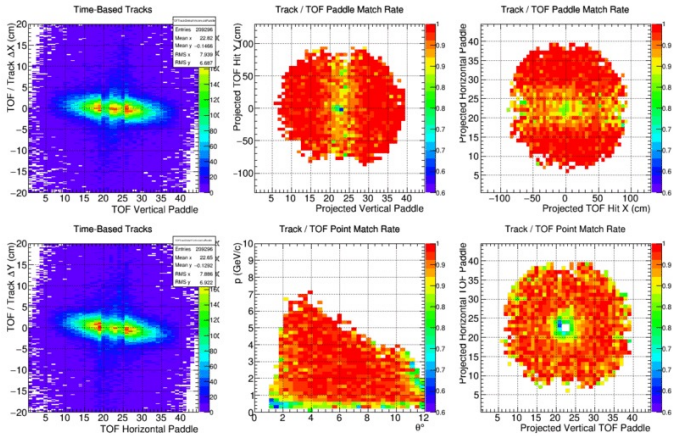
Joint DOE/NIH Workshop

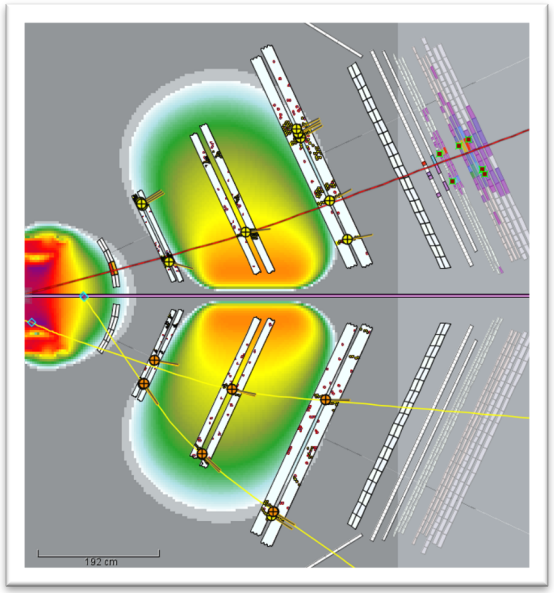
March 16-17, 2023

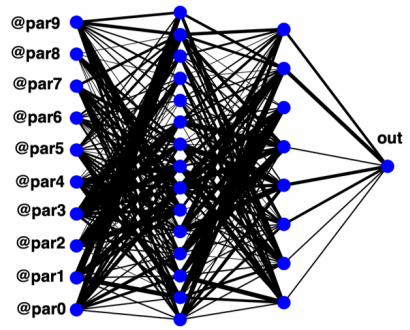
David Abbott - FEDAQ Group

Jefferson Lab – Physics Division









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U.S. DEPARTMENT OF ENERGY | Office of Science

JSA

Introduction

- Staff scientist - first arrived at the Lab as a post-doc in 1990.
  - Lab was still under construction.
  - I got involved in DAQ development in Experimental Hall C (first beam in 1994)

- Much has changed over the last 33 years.
  - How did we stay in front of the technology wave?

- Talk Outline
  - A brief history of electronics and DAQ in nuclear physics
  - Current capabilities and plans
  - What are the new challenges?

A Brief History of Data Acquisition in Nuclear Physics

- First nuclear physics “DAQ” (early 1900s) in Manchester, UK by Earnest Rutherford, Hans Geiger and a student, Ernst Marsden.
  - **Gold foil experiments** – confirmed that atoms were made up of a small positively charged nucleus and orbiting electrons.
  - Recorded the positions of light flashes on a fluorescent screen generated by alpha particles passing through and scattering from the foil.

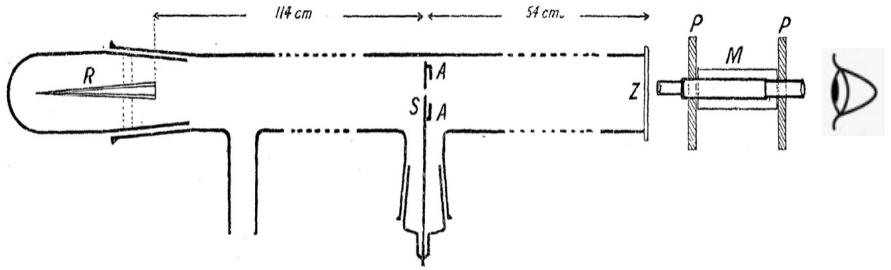
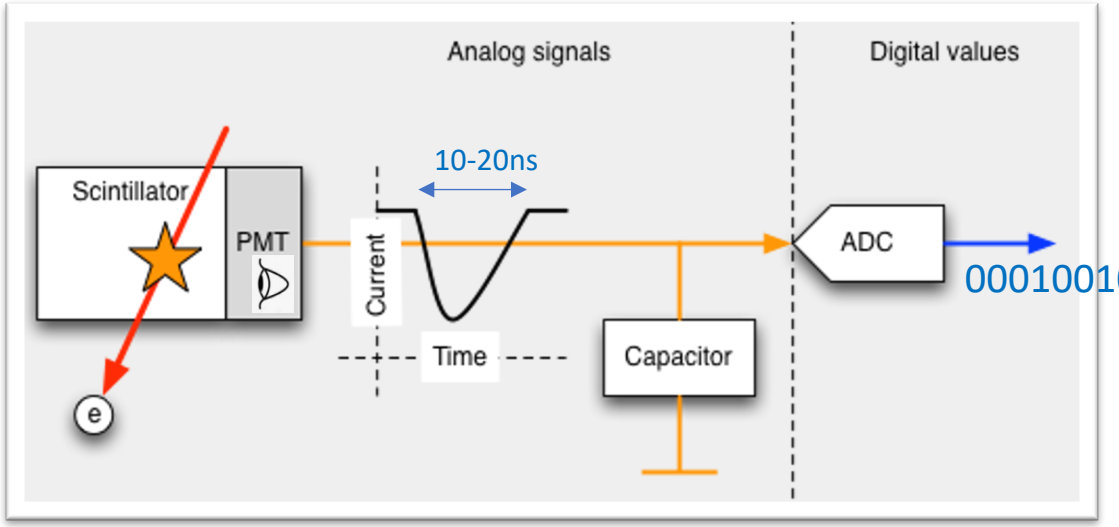
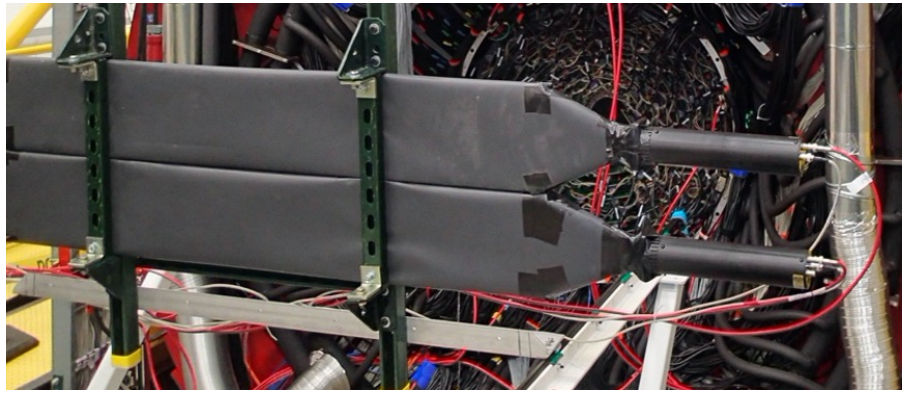


Fig. 1.

- Fast forward ~70 years
  - As a young college student on a semester “abroad” at Oak Ridge National Lab I did detector testing using **phototubes and scintillator paddles**.




scintillator paddles in Hall D

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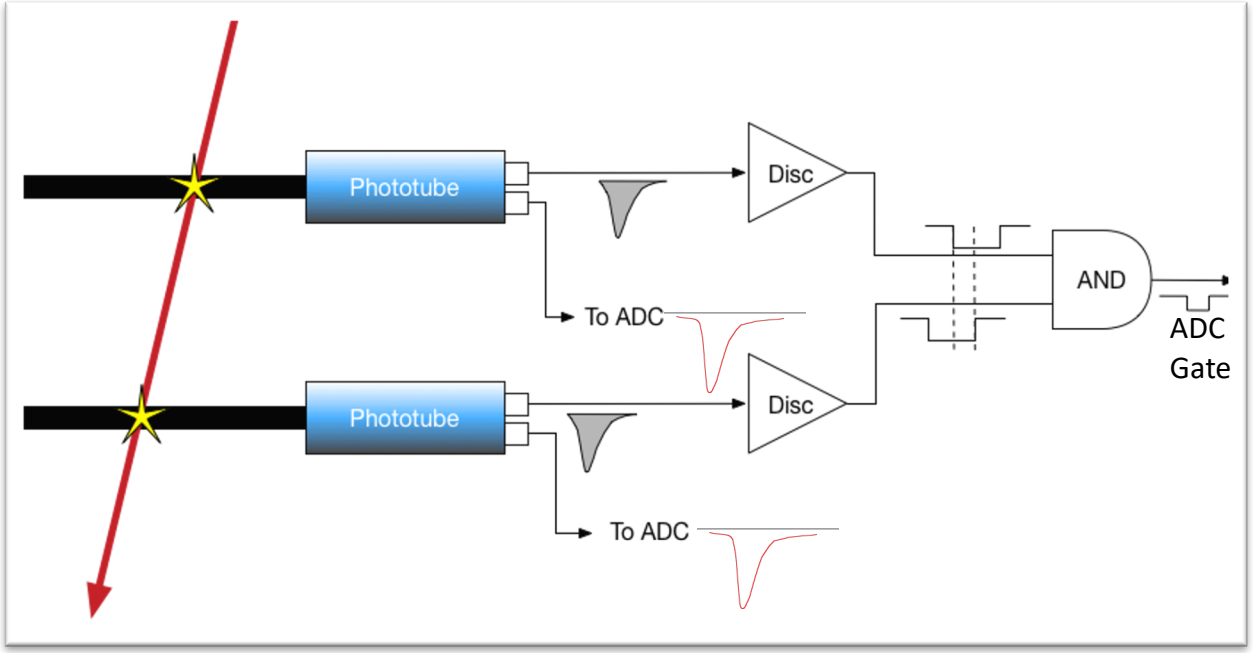
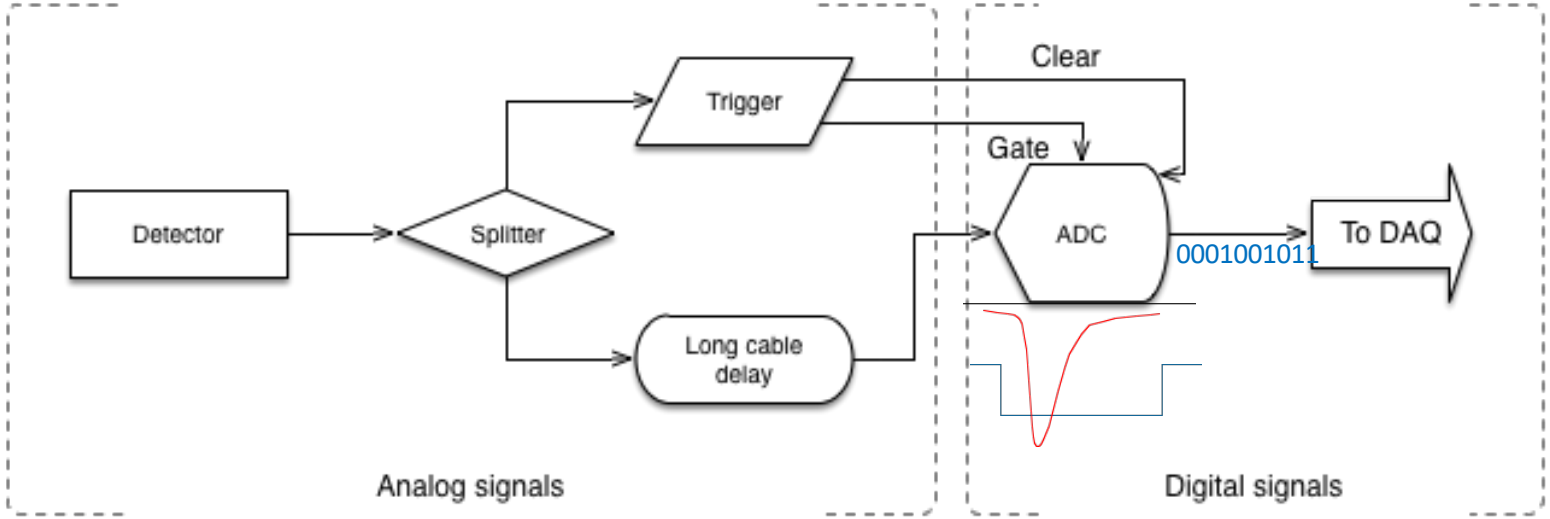
A Simple Trigger



- How do we determine which signals from our detector are from “interesting” physics?
- Combine signals from multiple detectors – e.g. coincidence.
- This “trigger” then tells the ADCs to digitize the detector signals.
- Digitization used to take a long time. This would significantly limit the accepted triggers by the DAQ.



For large experiments with many detector systems the experiment gets complex relatively quickly…

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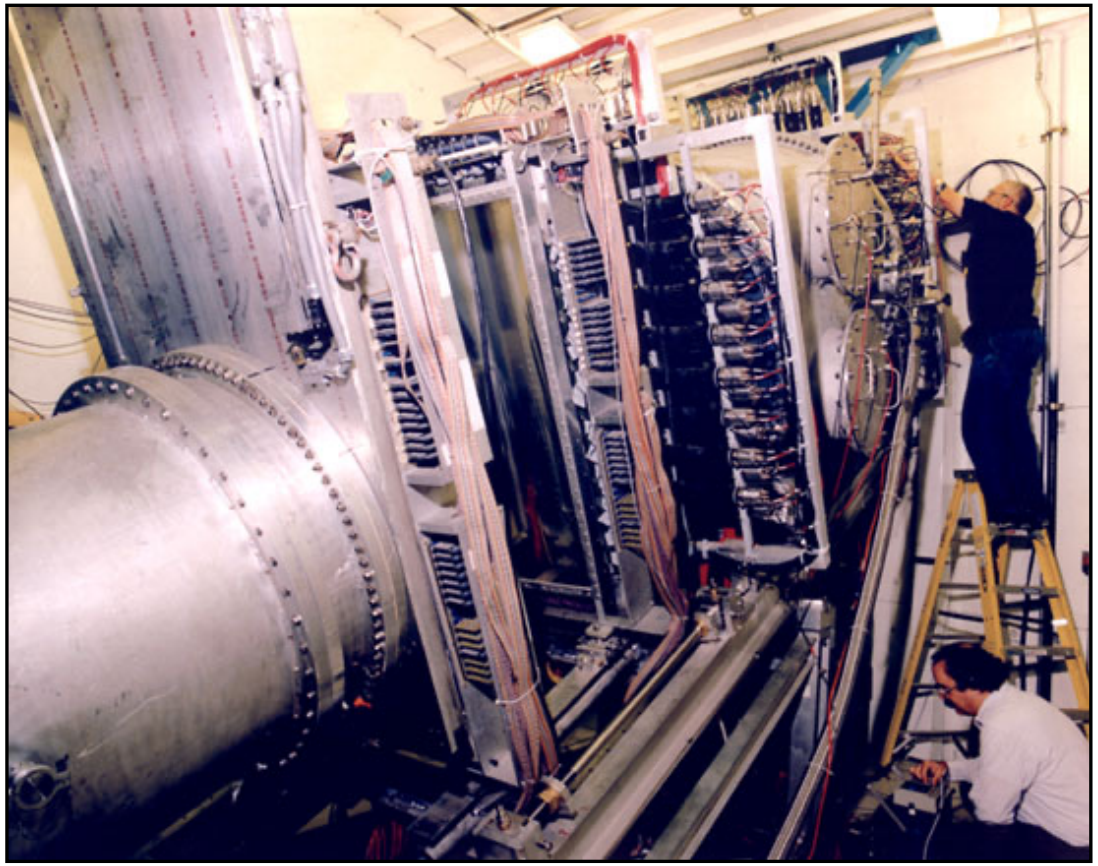
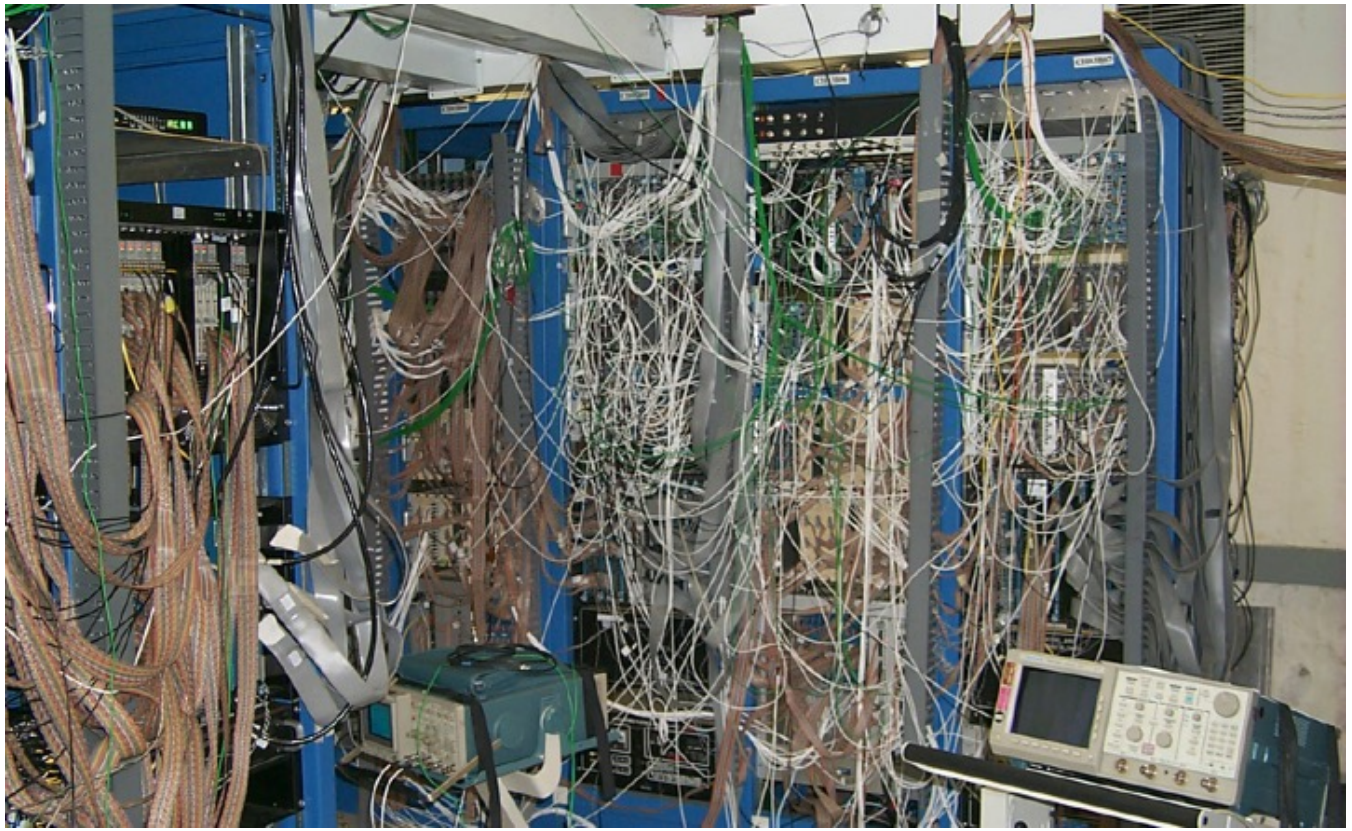
Early Experiments at JLab (Hall C, circa 1994)

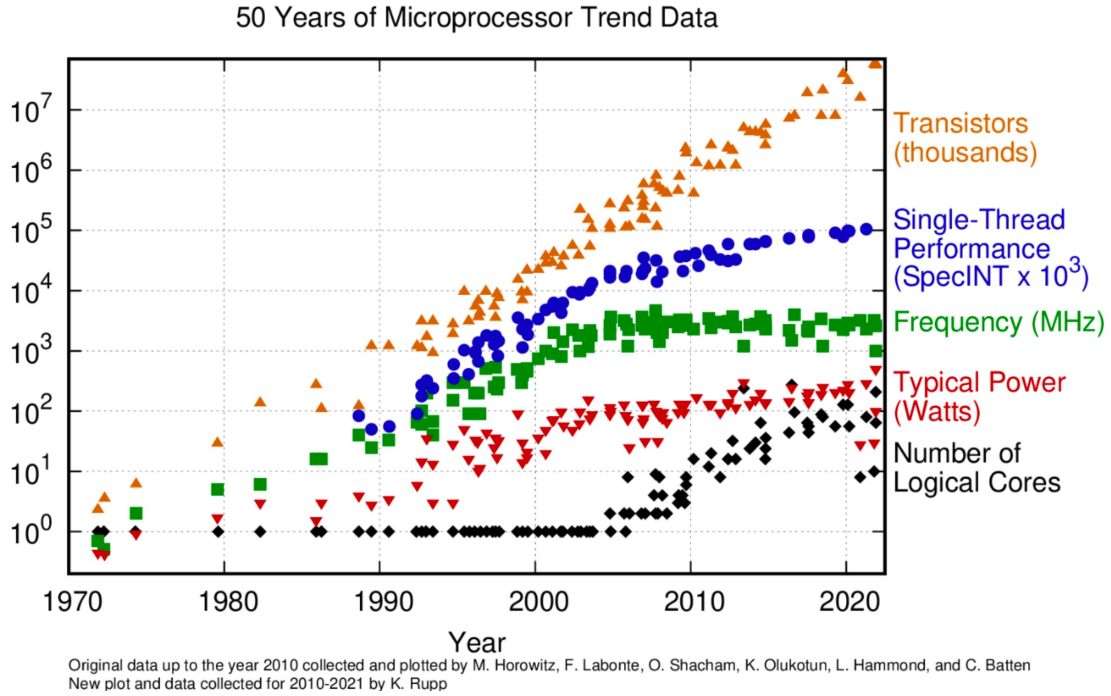


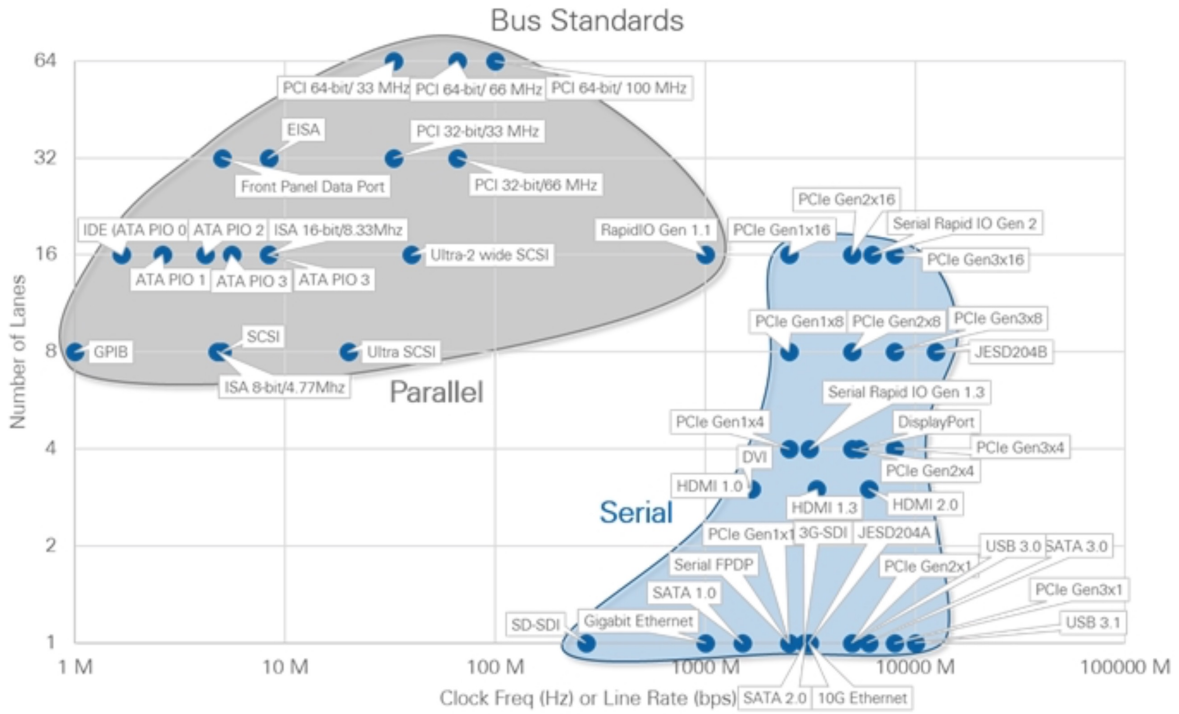
- HMS Spectrometer detector stack
  - Drift Chambers
  - Scintillator arrays
  - Cherenkov detector
  - Lead glass calorimeter



- Counting house
  - All analog signals brought up from the Hall
  - “Spaghetti” NIM trigger logic
  - Fastbus/VME based digitizers
  - DAQ: Network-based, ~1kHz, 600-700 kB/s

Evolution of technology





- Symmetric multiprocessing (SMP) –> multi-core CPUs
  - Development of “threaded” programming
- High speed serialized buses
  - Standardized data transport with an embedded clock
- Rise of the Field Programmable Gate Array (FPGA)
  - Customizable electronics in the palm of your hand

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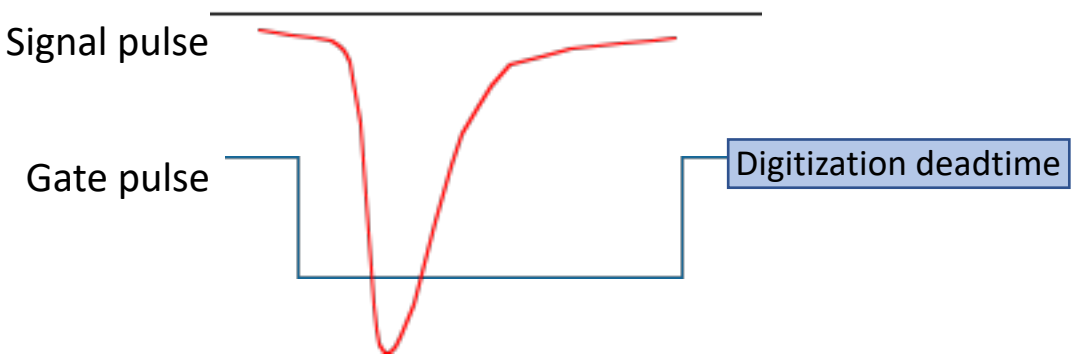
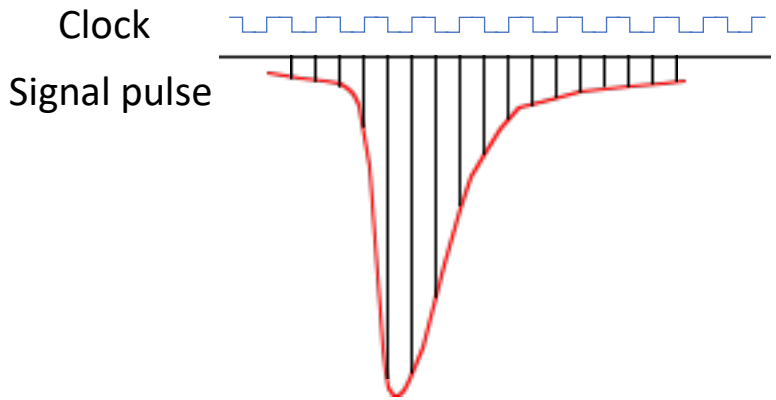
Digitization Evolution – Sampling vs Integrating ADCs

- A traditional “integrating” ADC can take many microseconds to digitize a pulse.
- This type of ADC generates a single measurement representing the **charge sum** during the gate.
- During the digitization period after the gate any later pulses from the detector signal are lost (readout dead time).



- A **Flash ADC** samples continuously at a fixed rate based on an input clock (using a reference voltage and comparator chain).
- For example, a 250 MHz FADC samples every 4 ns and generates ~5-15 measurements (12bit) during a typical phototube signal pulse.
- These samples describe the pulse shape as well as total charge.
  - Identify pile-up, particle type and a hit time (based on the FADC clock)
- There is no dead time!
  - Important for implementing a **Streaming** (triggerless) DAQ.



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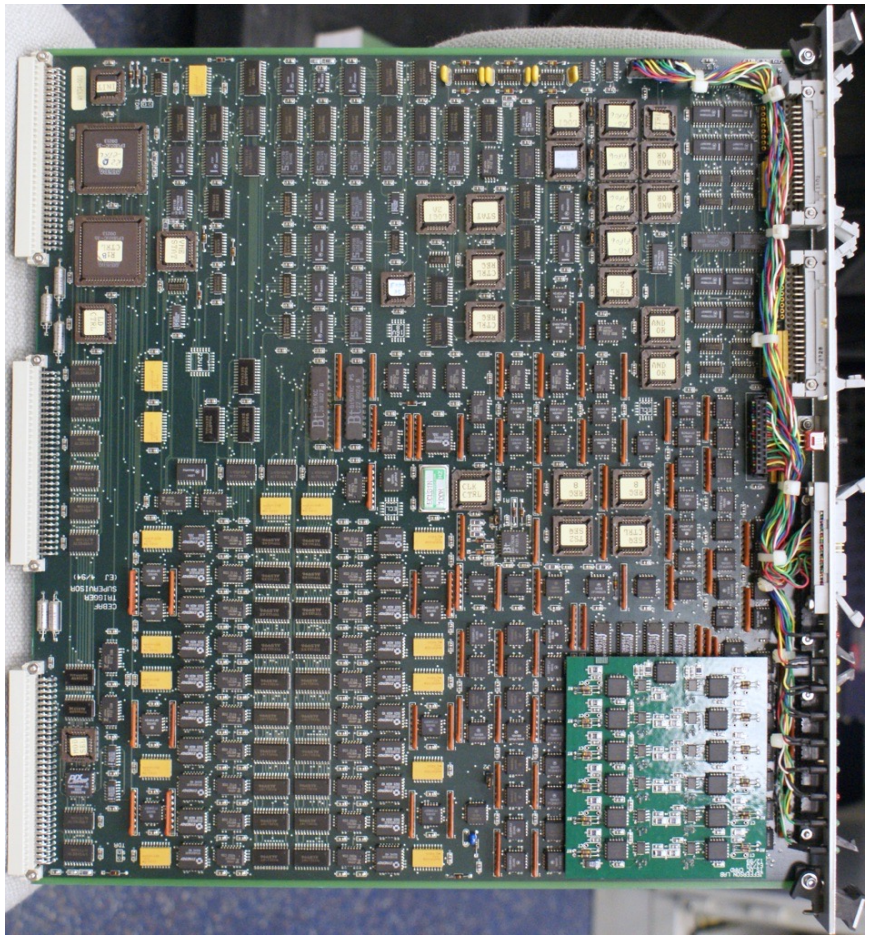
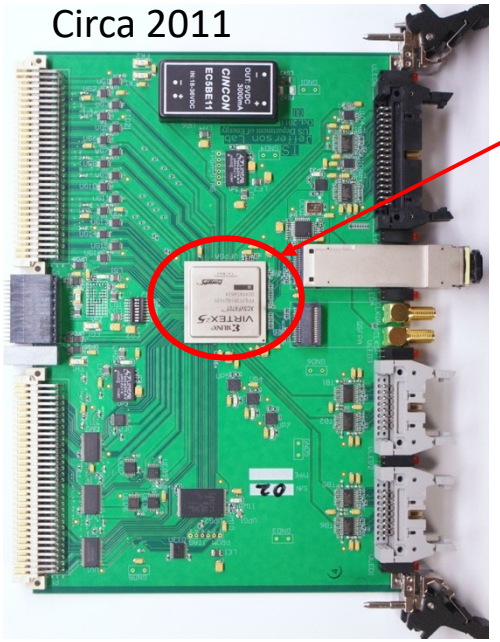
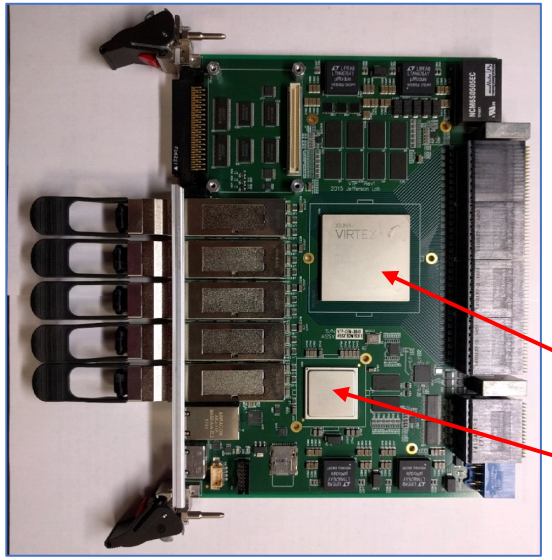
Electronics Evolution

Trigger Supervisor – Circa 1994



Circa 2011





Circa 2022
JLab VXS Trigger Processor (**VTP**)

FPGA – Field Programmable Gate Array

- We can now buy re-programmable logic chips that allow us to implement deterministic, complex algorithms in firmware on a single chip.
- Virtually all the hardware digital signal processing can be done in these very powerful chips. We just have to get all the relevant detector signals to them (the "spaghetti" goes away).
- FPGAs are becoming increasingly versatile including: System on Chip (SoC) microprocessors; Many high speed serial links supporting both proprietary (chip to chip) or standard (Ethernet) protocols; Significant DSP resources to support AI/ML, neural-net inference.

Xilinx Virtex FPGA

Zync (ARM) SoC

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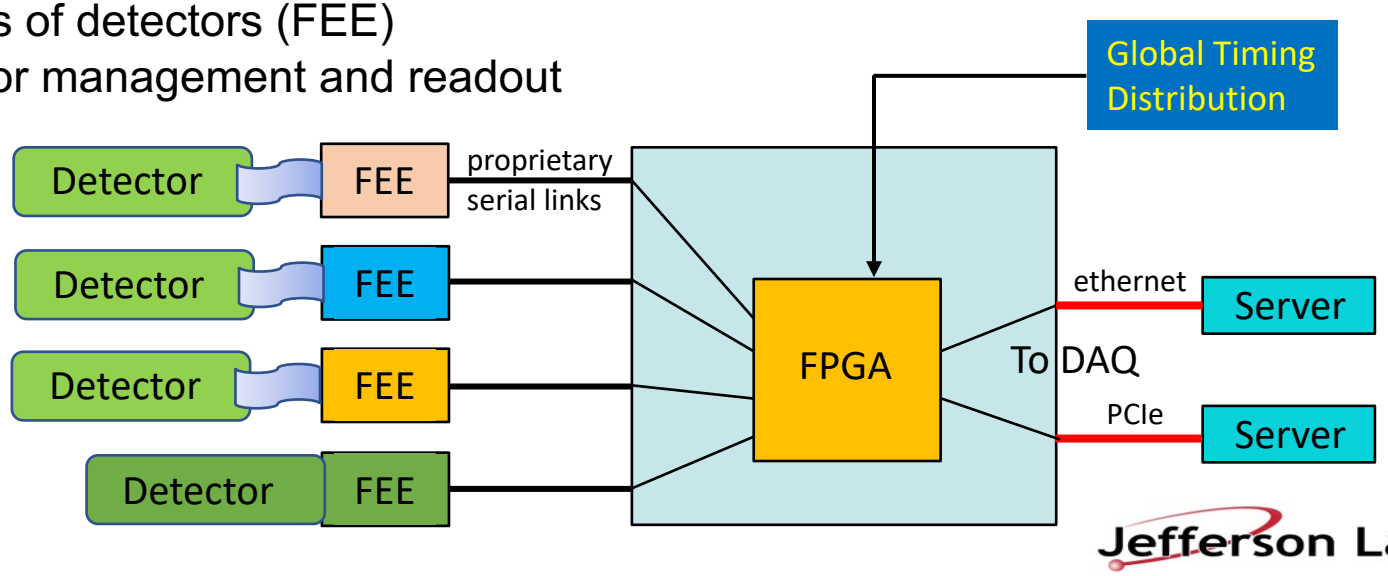
Interface to detectors

- The classical PMT + plastic scintillator is going the way of the Dodo.
  - The Silicon Photomulitplier (SiPM) has become the new workhorse
- Experiments are getting larger. Channel counts (and densities) are going up.
- Newer detector technologies are abundant (just check out this workshop's agenda)
  - Both gaseous and solid-state (semiconductor based)

- How do we implement the front-end analog and digitizing electronics in an efficient, low-cost, low-power and high density way?

- Application Specific Integrated Circuits (**ASICs**) are high density electronics chips tailored to the general features of a detector's output.
  - Many designs exist for the different types of detectors (FEE)
  - They are typically interfaced to FPGAs for management and readout

- A common clock can be distributed by an FPGA on proprietary serial links.



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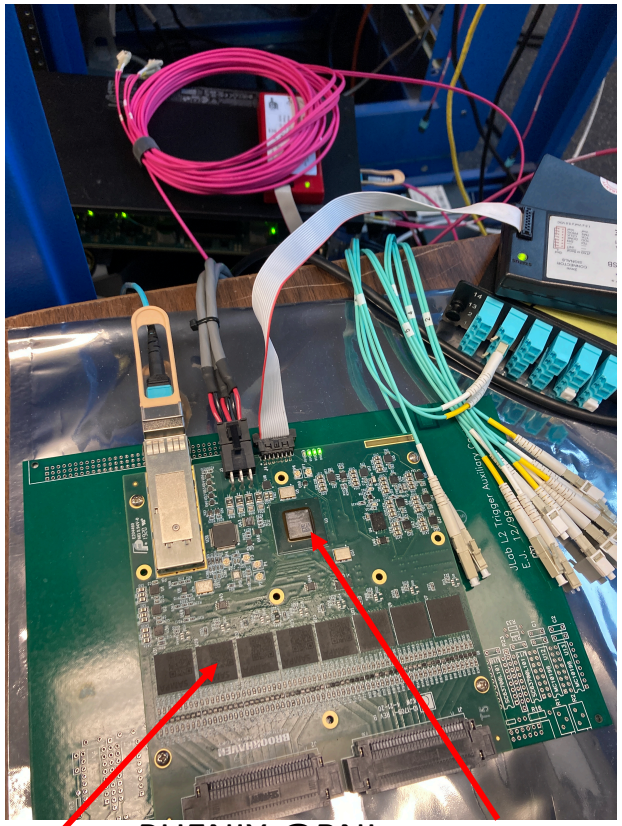
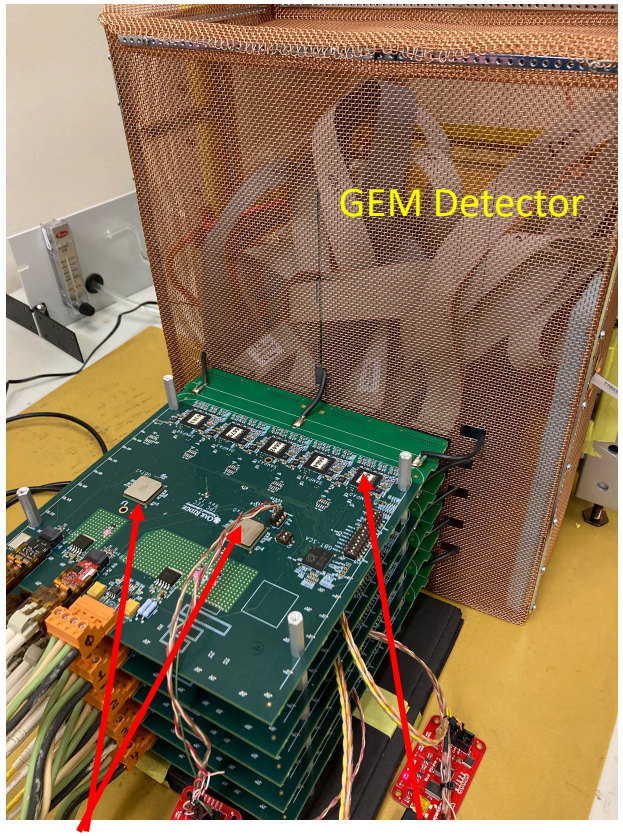
ASIC Front-End Electronics - Examples



sPHENIX @BNL

FPGA

SAMPA ASICs
32 channel
10 bit (10Mhz) ADC
Optional DSP



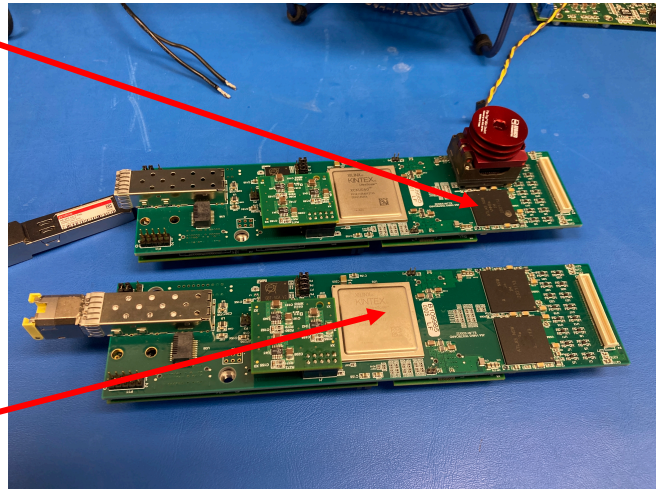
GBT ASICs

SAMPA ASICs

This FEE card was originally
designed for the ALICE TPC
(High radiation environment)

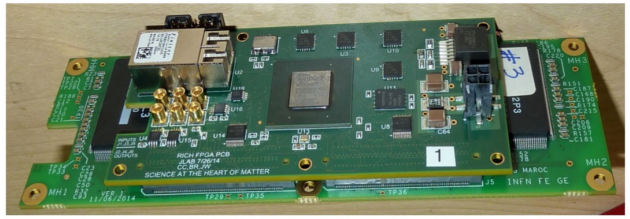
VMM3 ASICs
64 Channel
10bit/6bit ADC
GEM readout

FPGA



MAROC3 ASICs
64 channel
Fast ”trigger” bits
MAPMT/SiPM readout
Optional 8/10/12bit ADC

ASIC board produced for the RICH detector for CLAS12 with MAROC chips installed



FPGA Daughter card
with 1Gb Ethernet port

FPGA b Screenshot for the RICH detector for CLAS12 with ASIC board attached

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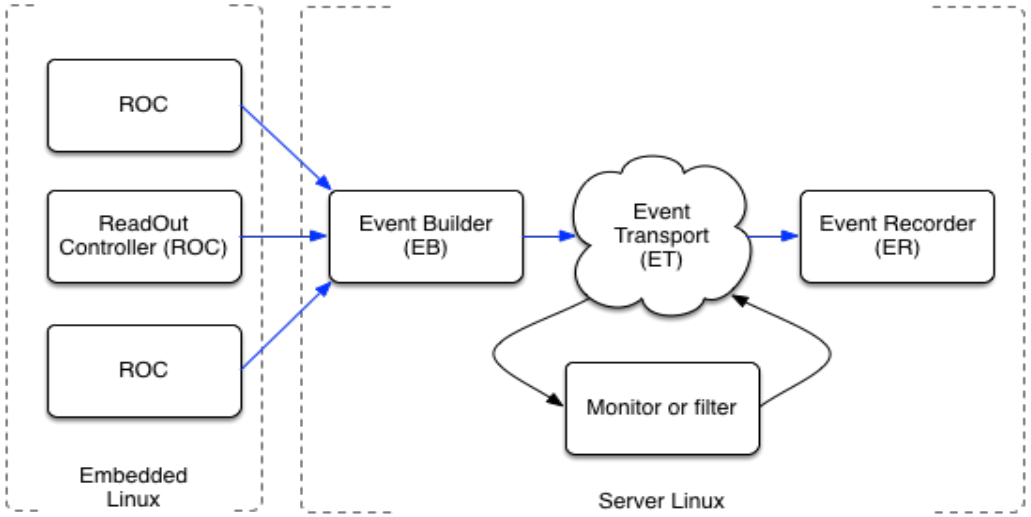
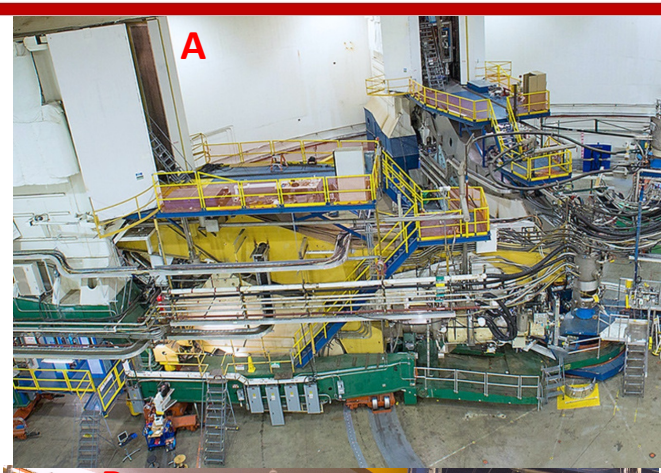
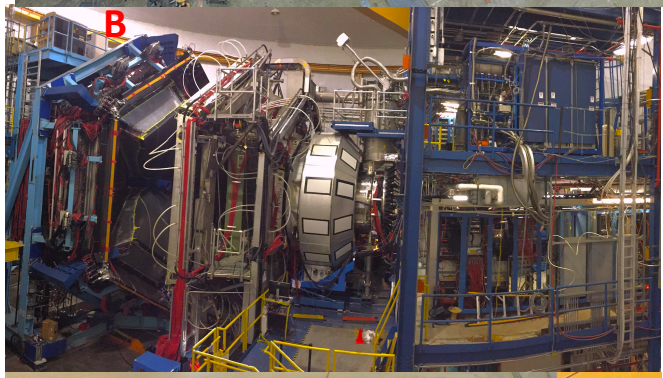
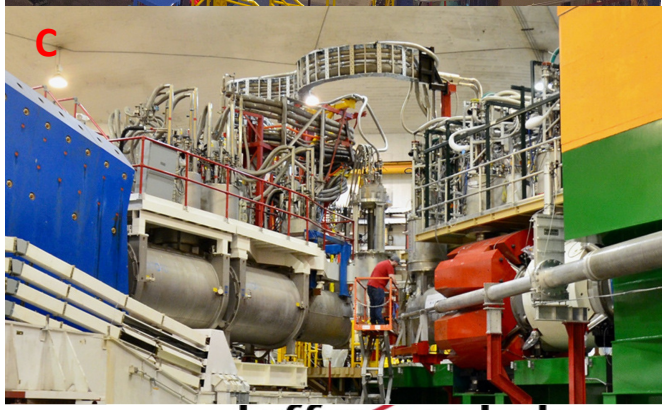
Data Acquisition at JLab

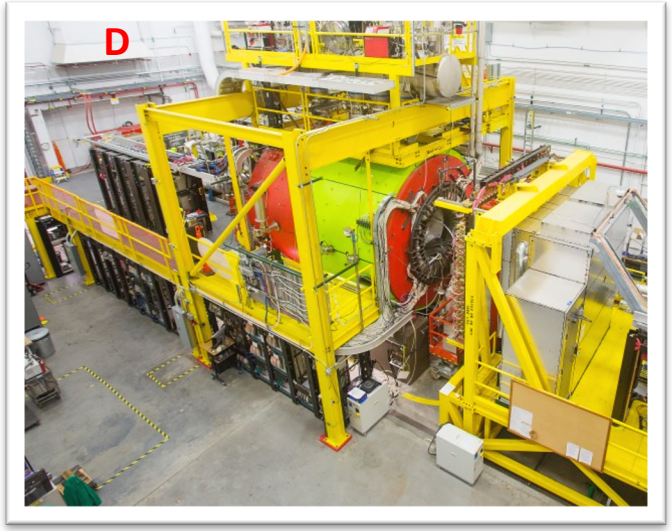
- At JLab we have 4 Experimental Halls, all running with different detectors - and physics focus.
  - Of course all are having increased demands for the DAQ.
- Experiments are increasingly reliant custom electronics to interface detectors and digitize signals.
  - ASICs and FPGAs are becoming the norm (and the future) for the front-end.
  - But older hardware is still relevant and useful (particularly for starving budgets)
- Our current goal is to support both the traditional **Triggered model** along with the **Streaming model** within one integrated DAQ framework.
  - Leverage existing hardware to implement streaming
  - Add support for new electronics
  - Try to keep it as seamless and user friendly as possible









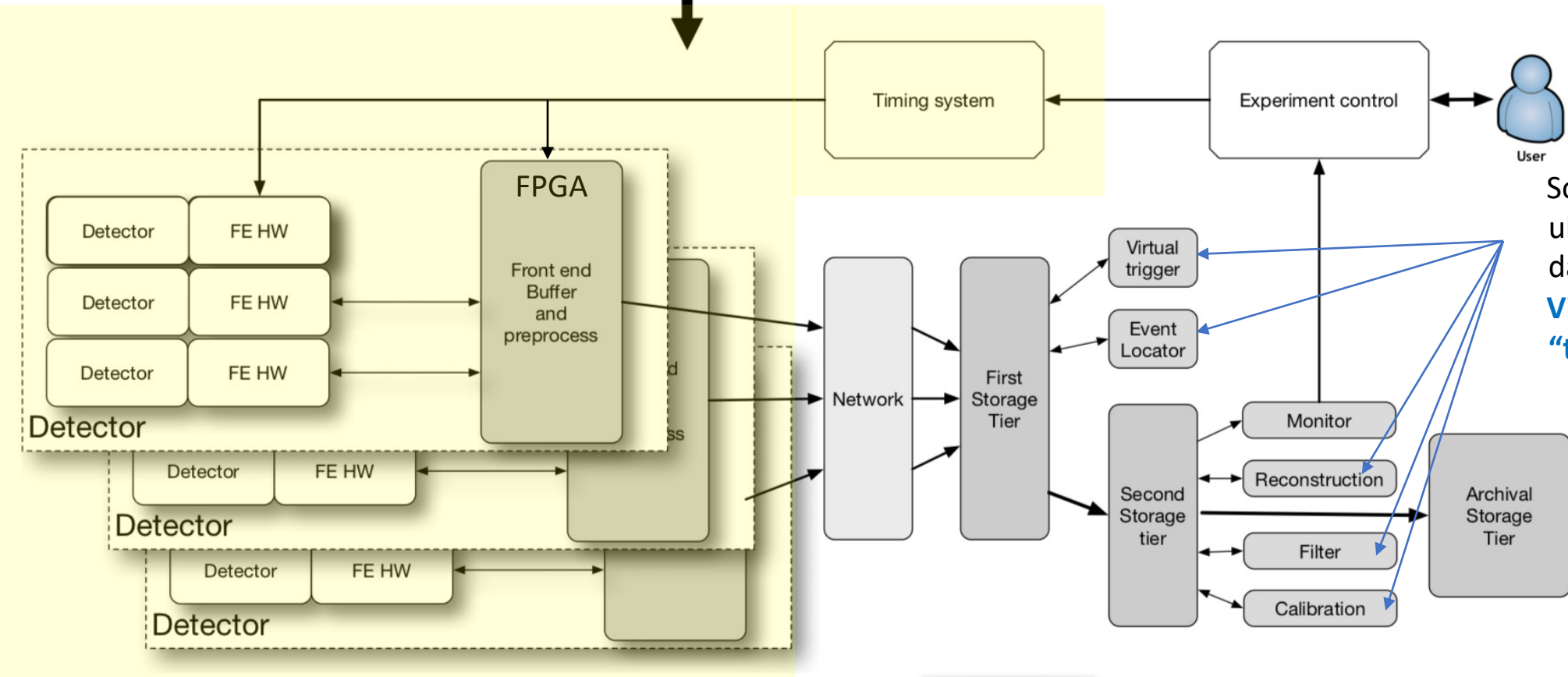


Streaming vs Triggered Readout

- In traditional Triggered readout the goal of the DAQ is to collect all data from the front-end that occurs within a narrow timeframe that has been tagged as “interesting”.
  - Data fragments from all detectors are built into what we call an Event.
  - At each stage congestion is managed by backpressure to the front-end where a global busy can disable the trigger.
- What if we just open the floodgates?
- In a Streaming system
  - All front-ends are free running (or self-triggered).
  - Data are continuously readout (with some validation to remove empty channels or noise via thresholds) and passed to the DAQ.
  - Data flow is controlled at the individual sources.
  - Data are characterized by channel and time-stamp.
- Streaming requires a robust and accurate clock to be distributed and synchronized to all the front-ends.

In practical terms, what does Streaming look like?

- A timing system synchronizes streams at source.
- Front-end outputs data in streaming format on a net.
- DAQ consists of tiers processing separated by tiers of temporary storage



Software processing ultimately reduces the final data storage requirements **Via a high level (software) "trigger"**

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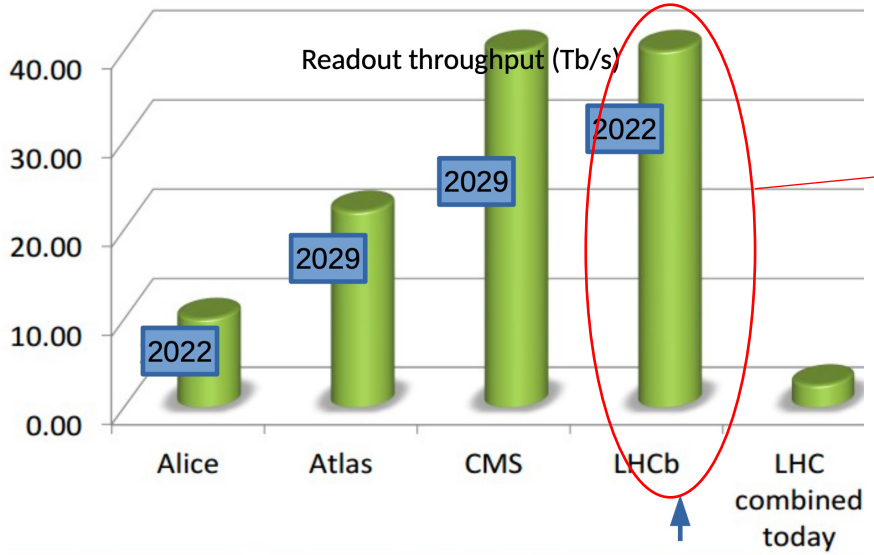
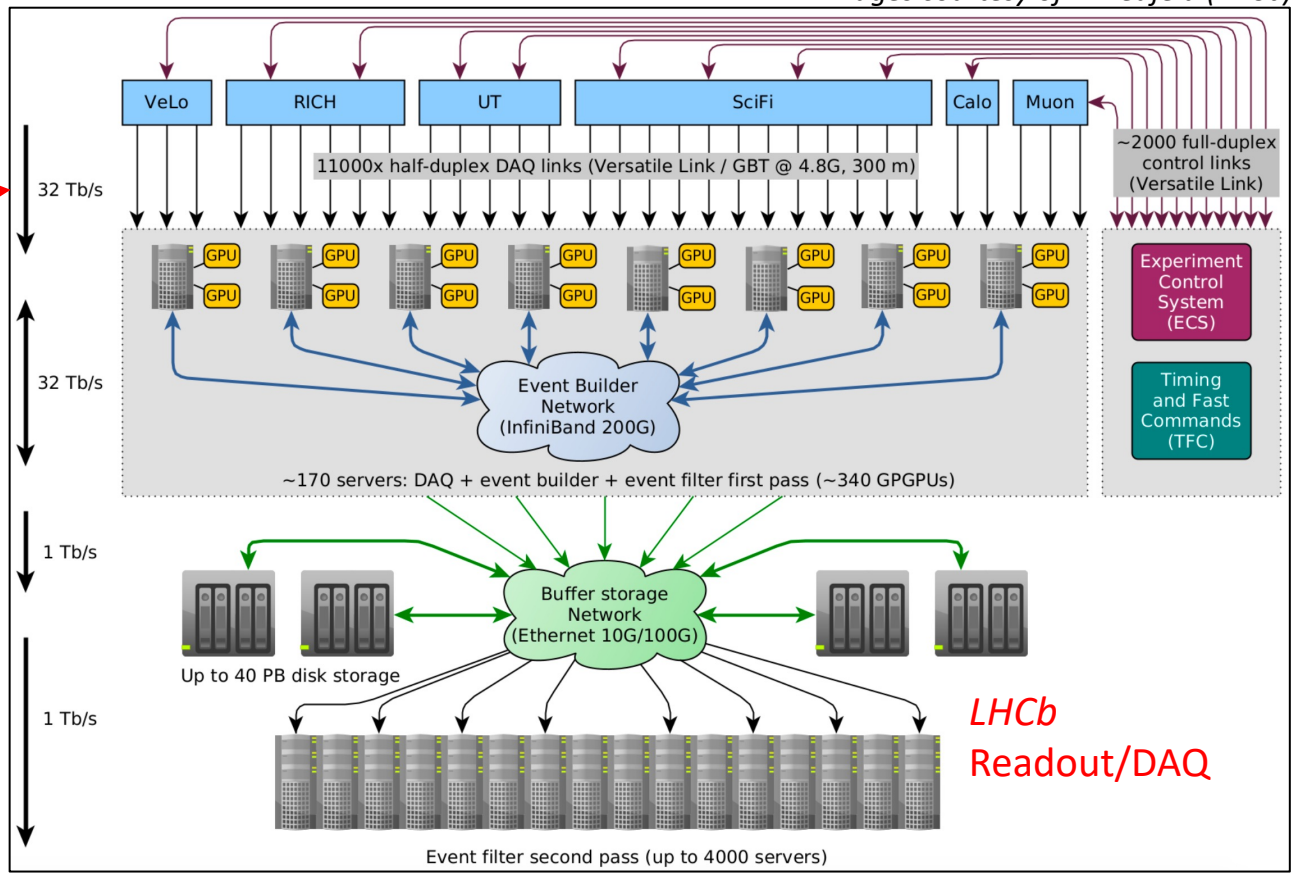
Some Cues from Particle Physics(LHC)

- LHC is already going triggerless (at least at the front-end)



Images courtesy of N Neufeld (LHCb)

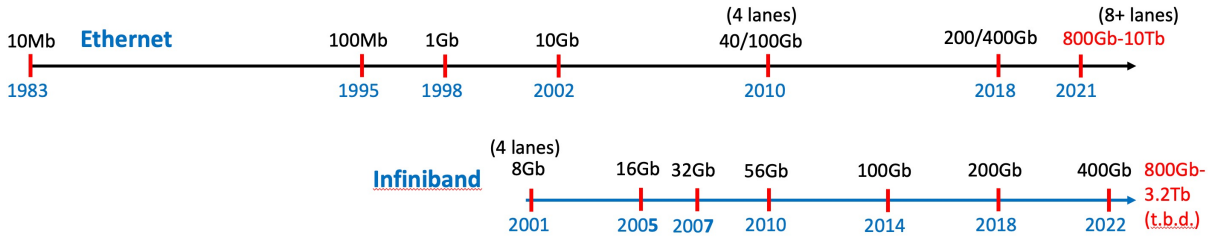


LHCb Readout/DAQ

Why?

- Higher luminosity does not necessarily mean more interesting physics events.
  - Trigger efficiency and bias are even more of a concern.

- Network bandwidths support it now and will only improve.



Push data filtering concerns to the back-end where one can put the full processing and analysis capabilities of the HPC computing infrastructure to good use.

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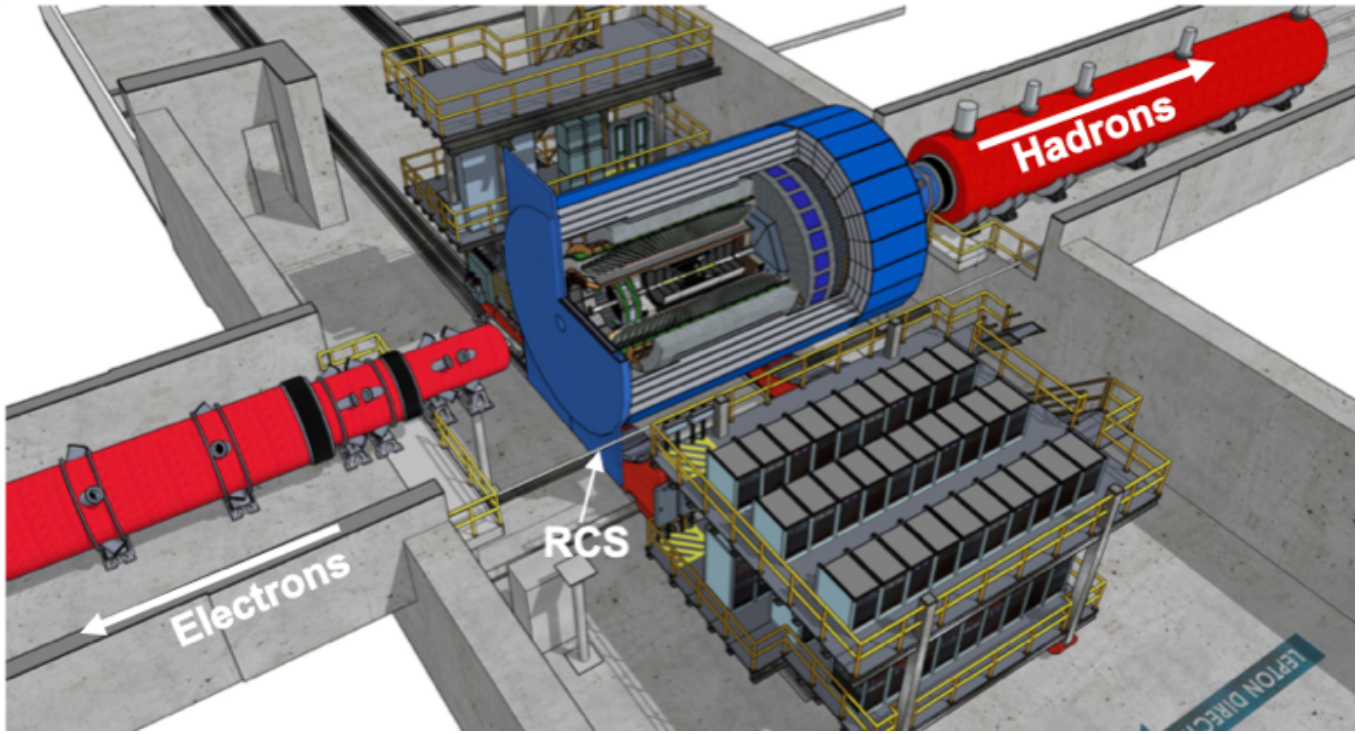
Electron Ion Collider (EIC)

- The next major project in NP is the Electron-Ion Collider (EIC) to be constructed at Brookhaven National Lab.
- BNL and JLab are partnering to build it (completion Circa 2034)
- The detector (ePIC) electronics and DAQ are being developed with Streaming as the default.



hadronic calorimeters

Solenoidal Magnet

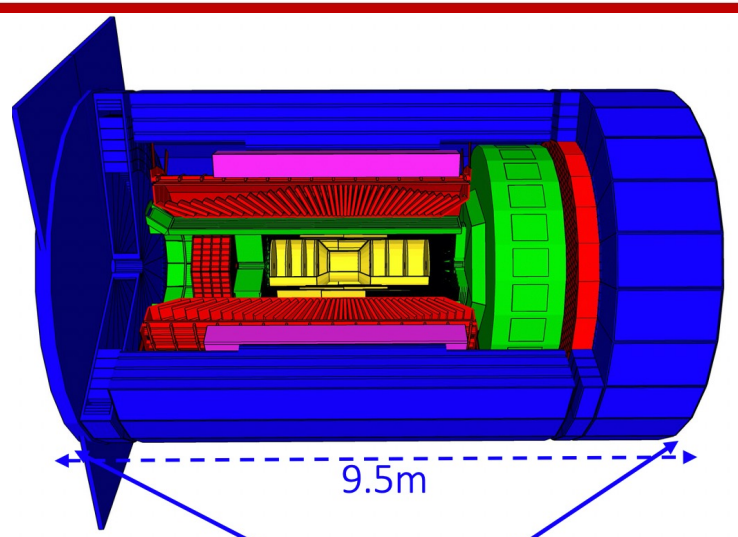
e/m calorimeters

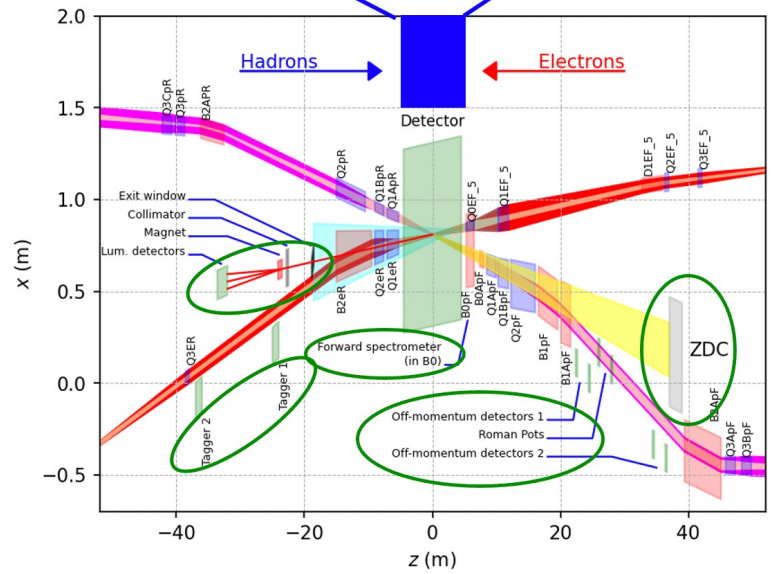
ToF, DIRC, RICH detectors

MPG trackers

MAPS tracker

25 Subdetectors incl. Polarimeters





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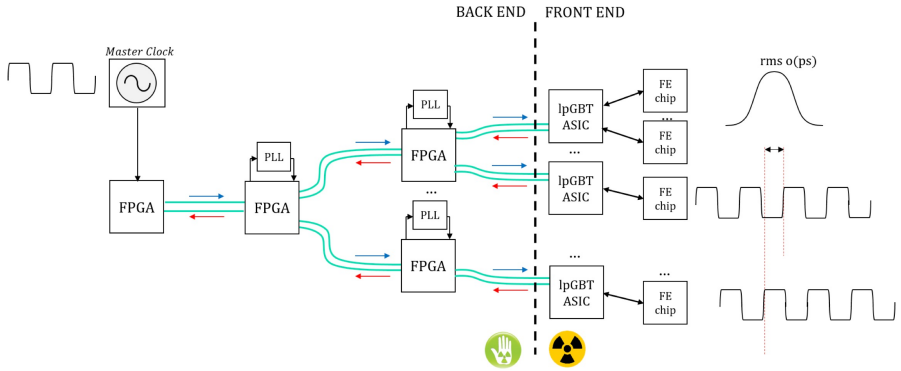
New Challenges

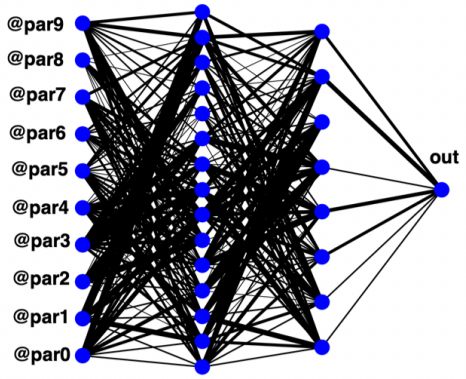
- Making the computing infrastructure (both Online and Offline) location agnostic is an appealing idea. Can we connect a BNL counting house based DAQ to a “online” processing farm at JLab?
  - A joint project with JLab and ESNET is looking at this idea.

EJFAT
ESnet-Jefferson Lab FPGA Accelerated Transport

- Providing a VERY low jitter (< 5ps) common clock to the front-end hardware is a necessary first step to supporting high resolution timing measurements (~20ps) from ePIC subsystems.
  - CERN-based working groups are currently exploring FPGA distributed reconstructed LHC clock (TCLink – timing compensated links https://pos.sissa.it/370/057/pdf).



- Implementation of real-time AI/ML inference in FPGAs as part of the front-end streaming readout has potential applications for monitoring, calibration and reconstruction.
  - Modern FPGAs are offering significant resources (DSP slices) to facilitate AI implementations.
  - Open source development tools are well supported hls4ml



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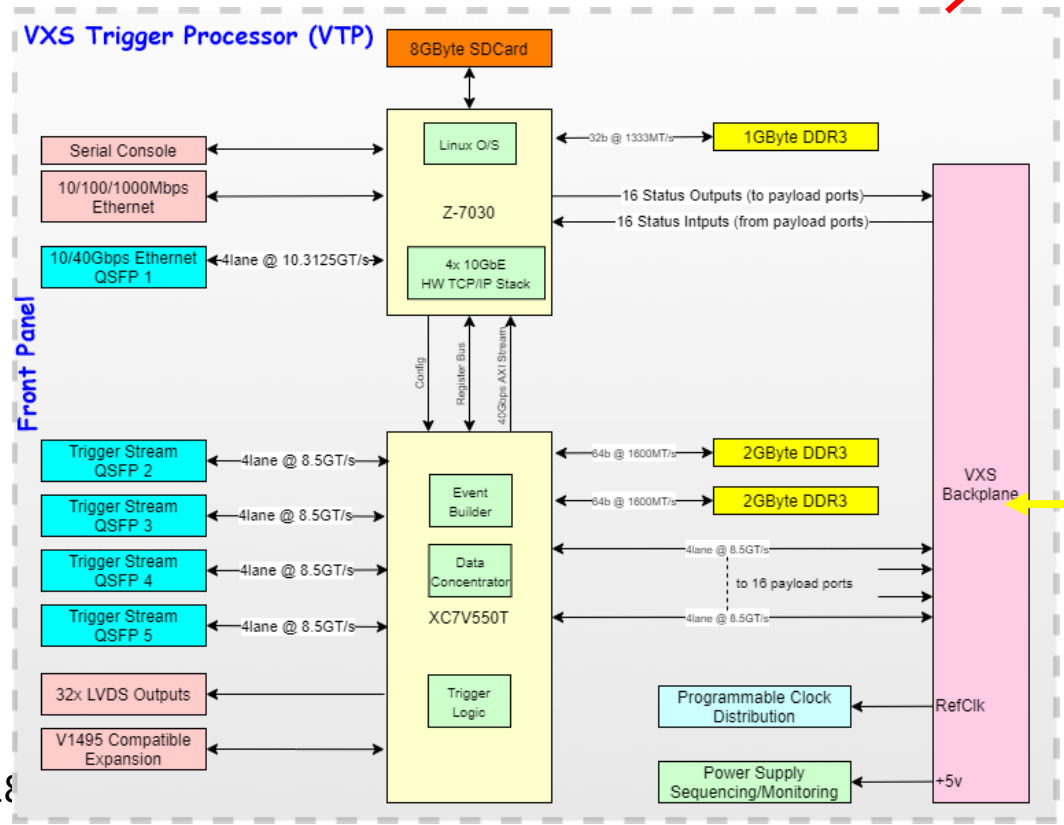
Thank you

Questions?

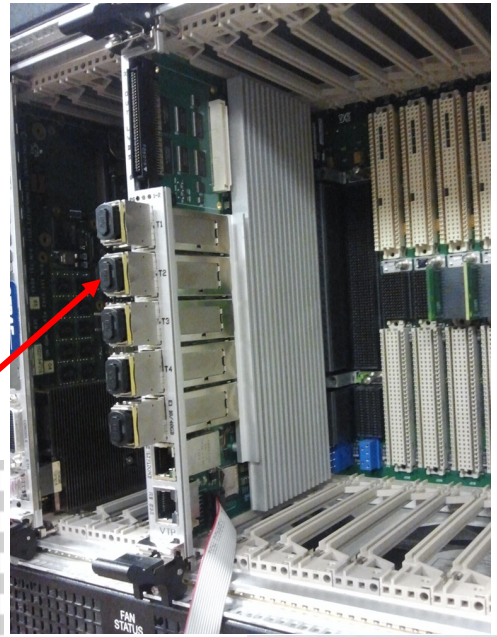
JLab VXS Platform

Linux OS on the Zync-7030 SoC
(2-core ARM 7L , 1GB DDR3)
10/40Gbps Ethernet output

Xilinx Virtex 7 FPGA
20x4 serial lanes from both the VXS backplane and the Front panel. 4GB DDR3 RAM

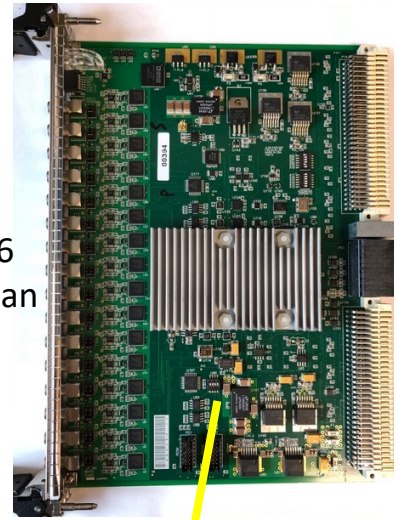


JLAB VTP Board



FEE

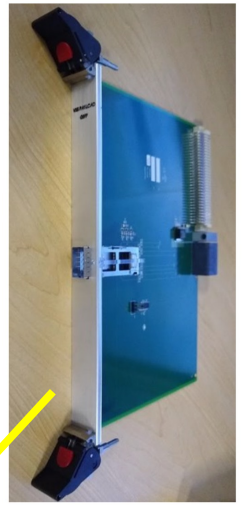
Local



16 Chan

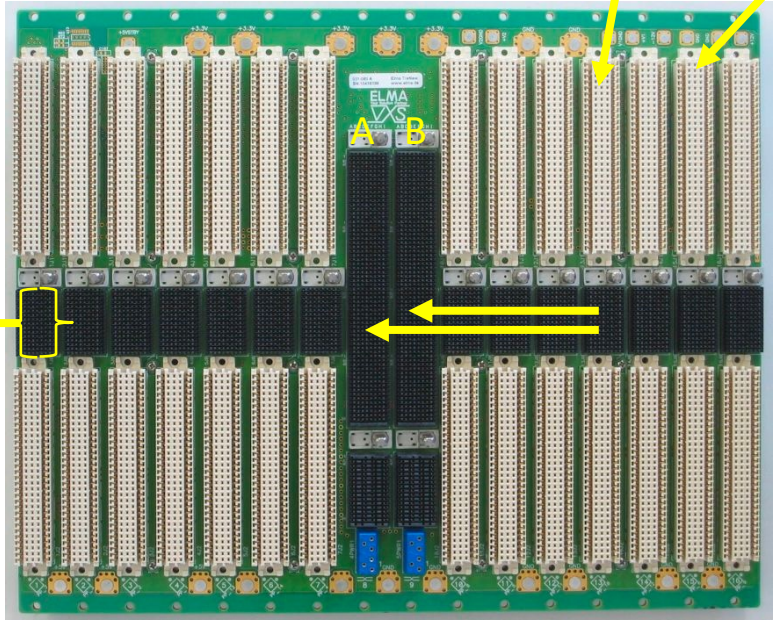
JLAB 250MHz FADC

Remote



QSFP Extender

16 payload ports supported

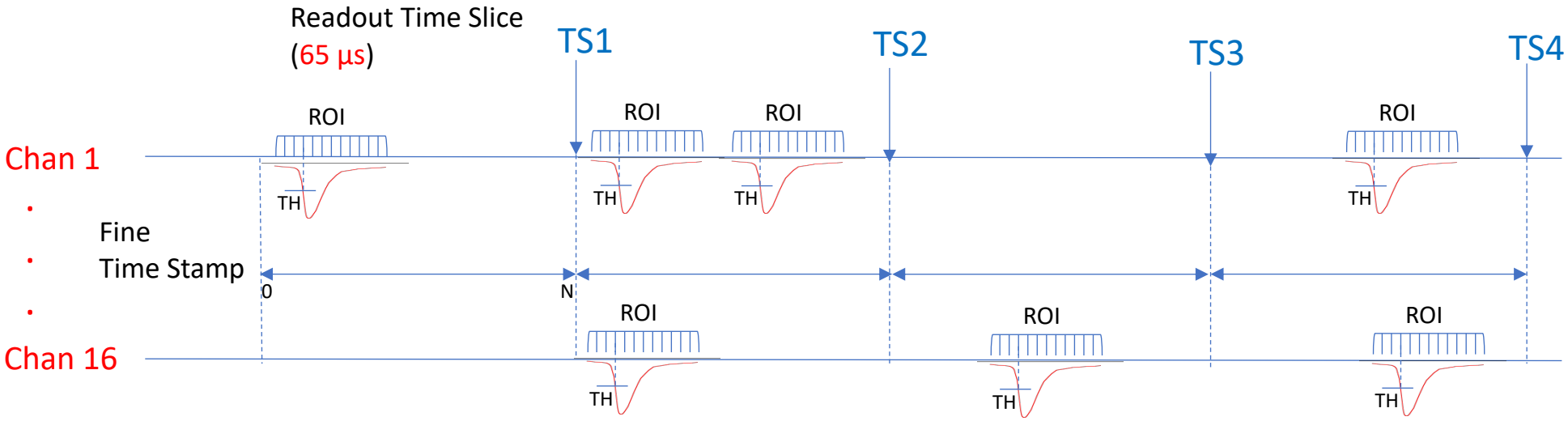


VXS Backplane
4 serial lanes to each switch slot – **20 Gbps**

JLAB FADC – Streaming mode

A 250 MHz FADC generates a 12 bit sample every 4ns. That's 3 Gb/s for one channel. 16 channels is 48 Gb/s. Currently, we identify a threshold crossing (hit) and integrate charge over a ROI and send only a sum and timestamp for each hit.

Available bandwidth will allow for 1 hit every 32ns from all channels.
A data frame (Time Slice) for all available hits is generated in the VTP every 65µs



The next revision to the firmware will have an option for full ROI wave forms to be streamed, but this will allow possible dropped hits due to bandwidth limitations

The FADC can still simultaneously operate in triggered mode with an 8µs pipeline and 2µs readout window.