Hpernuclear DAQ

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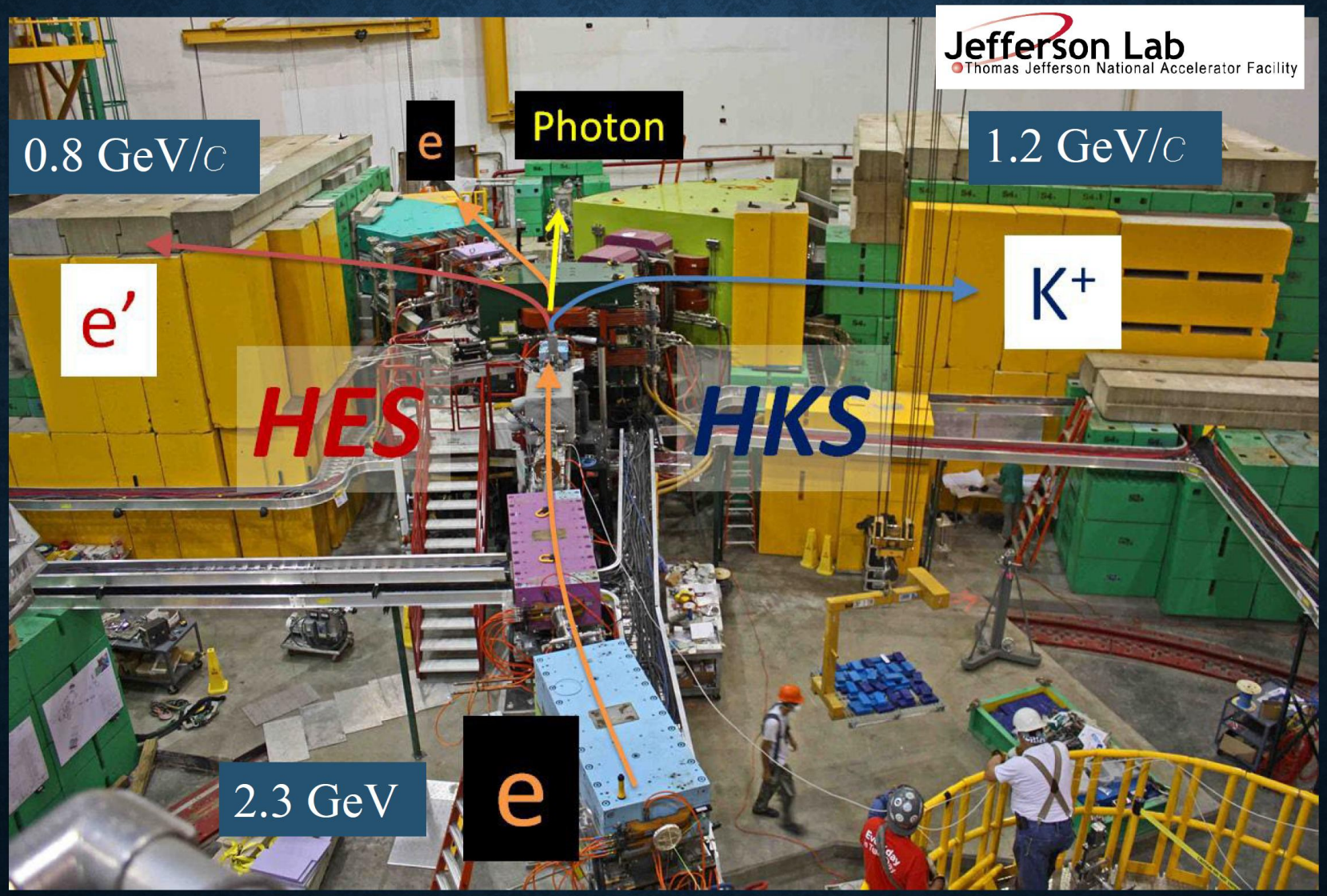
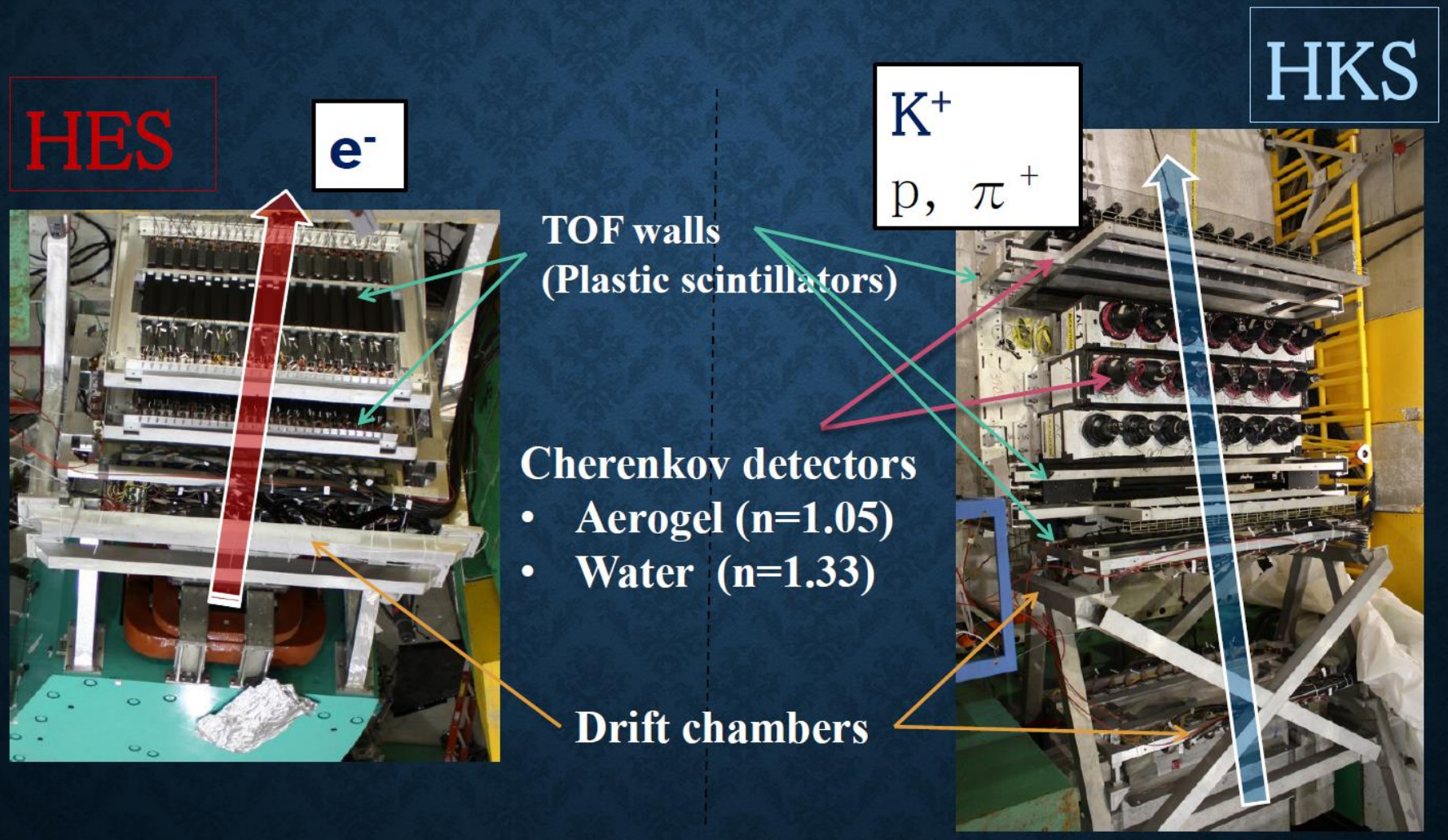
Outline

- Experiment overview
- Channel count
- Overview pipelined electronics
- Trigger overview
- To do
- Conclusion

Experimental setup for E05-115 (2009) at JLab Hall C



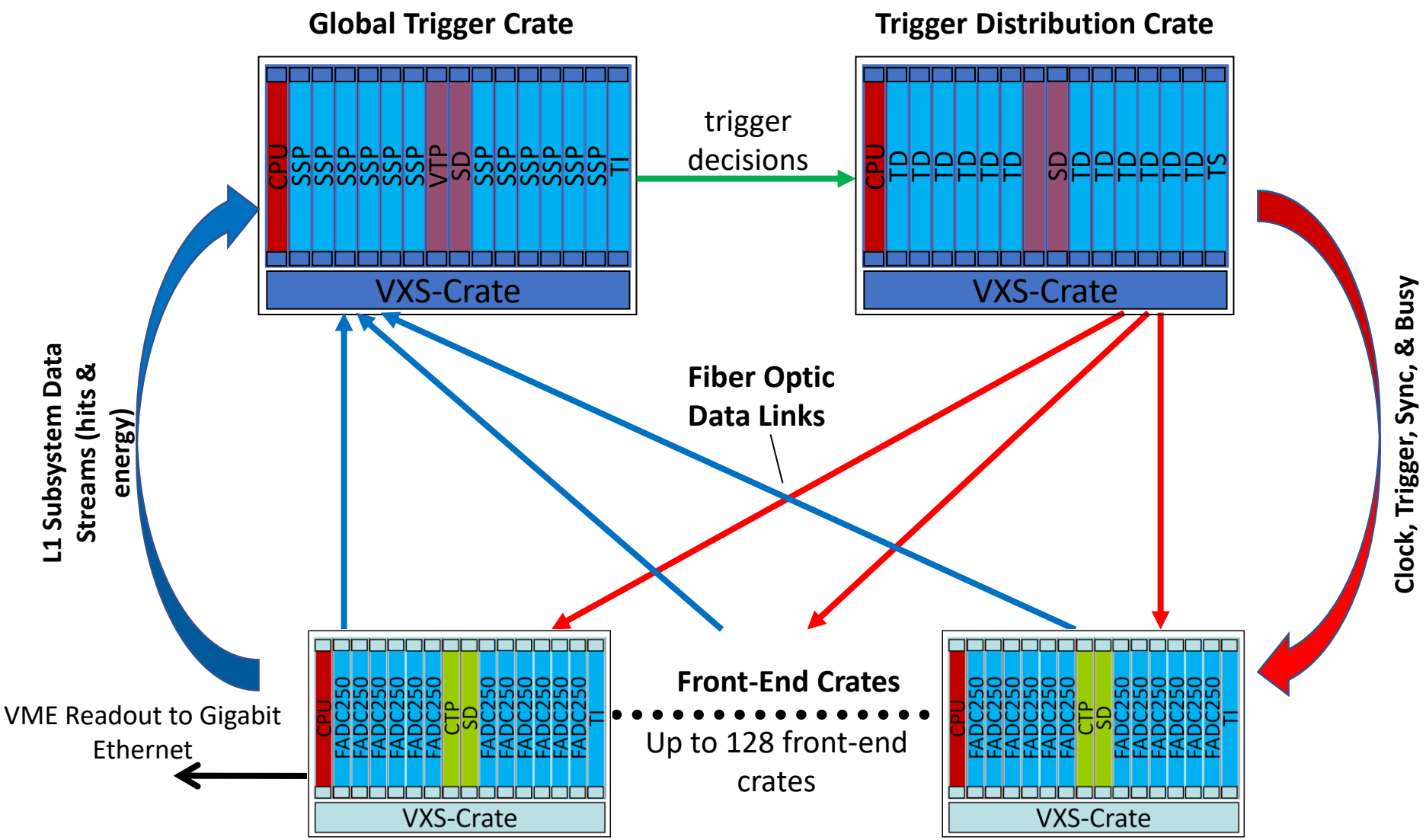
PARTICLE DETECTORS



Channel count

	Detector	Current status	No. of channels		Ready?
			ADC	TDC	
HKS	Drift Chambers	To be tested	N/A	360 + 360	Yes
	TOF counters	All PMTs were checked	88	88	
	Aerogel Cherenkov	Test done	42	42	
	Water Cherenkov	New boxes under construction	48	48	
HES	Drift Chambers	To be tested	N/A	1098+360	
	TOF counters	To be tested	116	116	

Level 1 & Trigger Distribution



Crate Level – Signal Distribution

- VXS Based, 20 Slot Redundant Star Backplane

- VME64x backplane w/VXS (VITA 41 Standard) provides standard with high speed serial extension (new J0 connector)

- 18 Payload slots w/VME64x, 2 Switch slots

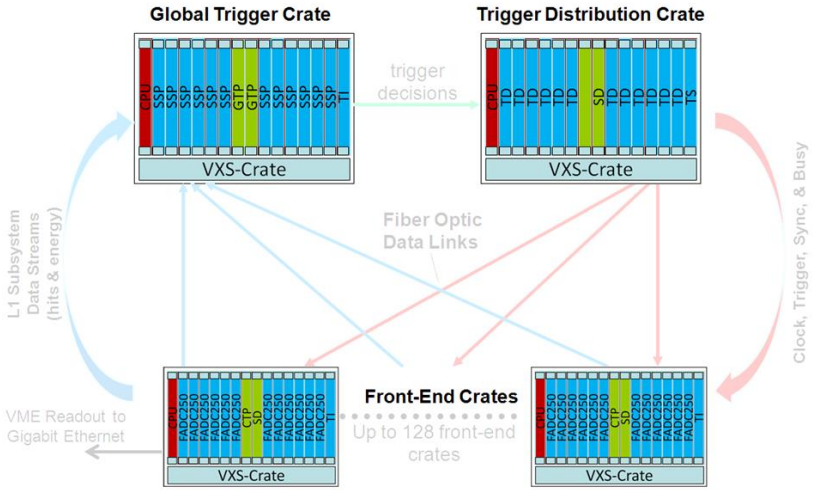
- Each payload slot has 8 high speed capable links (10Gbps each) to both switch slots

Crate Level Use:

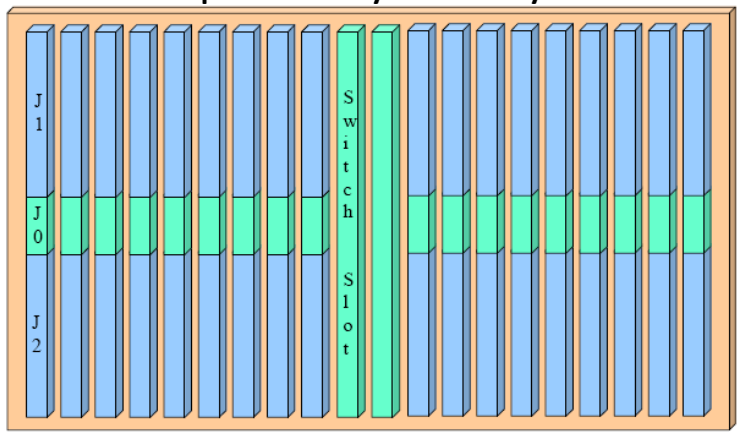
- VME64x used for event readout

- VXS: Low jitter clock & trigger distribution

- VXS: Gigabit serial transmission for L1 data streams to switch slot for processing



VXS Backplane Physical Layout:



VXS (VITA 41 standard)
VME64x + high speed serial fabric on J0

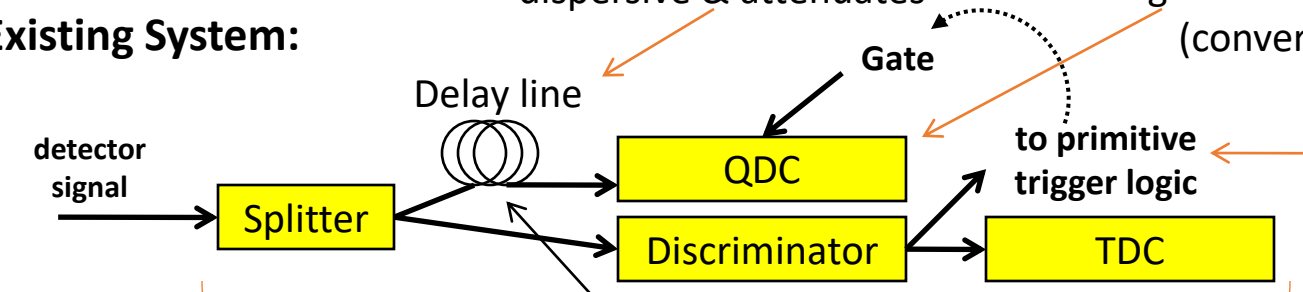
Capturing the Pulses…

Existing System:

Expensive, bulky delay cable dispersive & attenuates

Non-pipelined electronics guarantee dead-time (conversion time)

Very limited channel resolution used in trigger

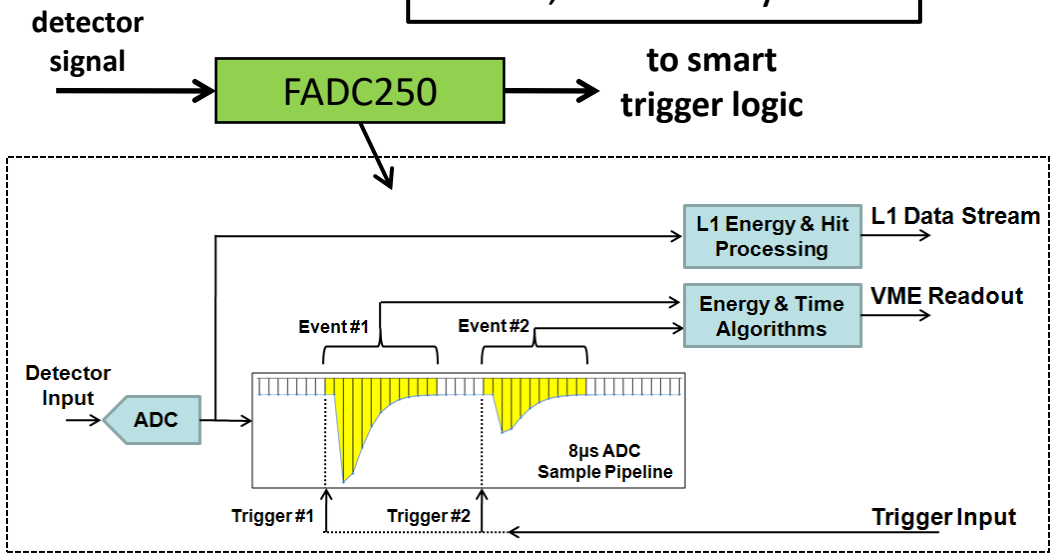


multiple modules for time & energy

New System:

(for timing >500ps)

CLAS TOF has >150,000ft delay line!



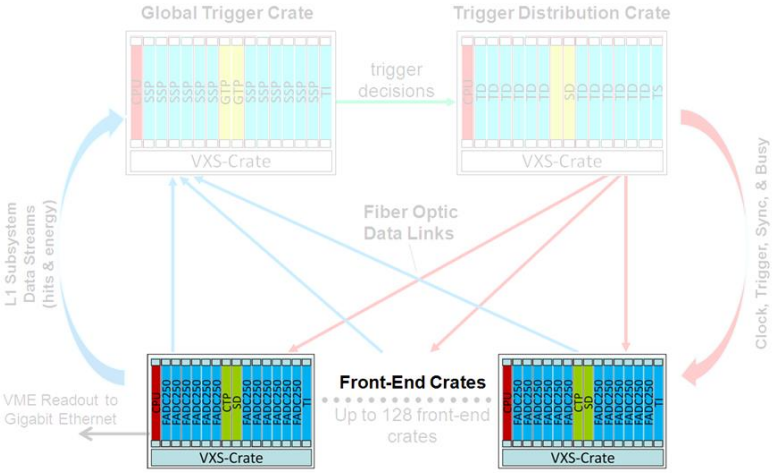
Time, energy, trigger output in 1 module

- **Pipelined sampling, readout, & trigger -> no dead-time**
- **Digitization retains original signal integrity**
- **Long pipeline allow more time for complex triggers**

Front-End Electronics: fADC250

- 16 Channel 12bit, 250Msps Flash ADC
- 8µs raw sample pipeline, >300kHz sustained trigger rate (bursts @ ~15MHz)
- Post-processing in customizable firmware to extract time, charge, and other parameters minimizing event size
- Module supports 2eSST VME transfers at 200MB/s transfer rate
- Large event block sizes (>100) to minimize CPU interrupt handling
- VXS P0/J0 outputs 5Gbps L1 data stream (hit patterns & board sum)

- Used in existing 6GeV program:
  - Hall A BigBite
  - Upgraded Hall A Moller Polarimeter



JLab-FADC250:

Channel count

	Detector	Current status	No. of channels		Ready?
			ADC	TDC	
HKS	Drift Chambers	To be tested	N/A	360 + 360	Yes
	TOF counters	All PMTs were checked	88	88	
	Aerogel Cherenkov	Test done	42	42	
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HES	Drift Chambers	To be tested	N/A	1098+360	
	TOF counters	To be tested	116	116	

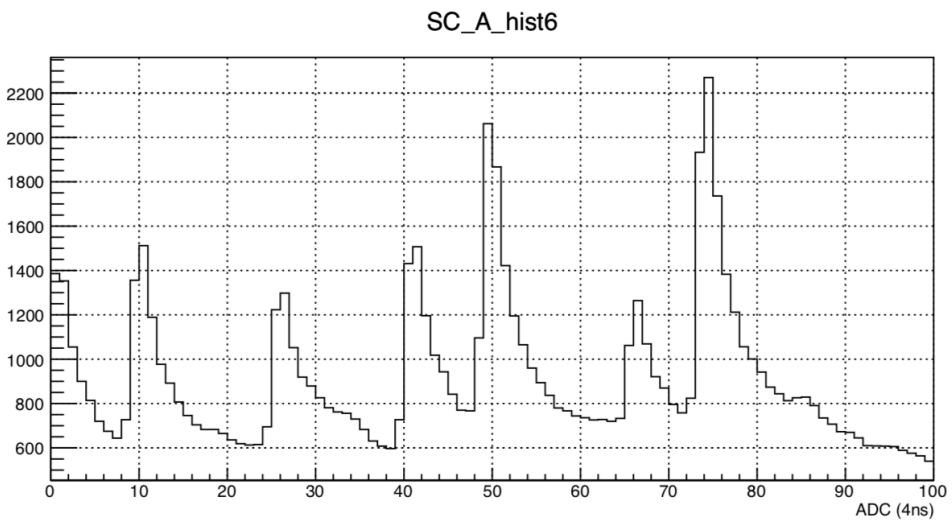
FADC = 88 + 42 +48 +116 = 294 channels = 19 FADCs = 2 VXS crates
V1190 = 2268 channels = 18 V1190 = 1 VME64X crate
TOF = 204 channels = 7 V1290 = 8 F1 = 3 VETROC

If not running with SBS or NPS most likely enough FADCs
Can use HMS electronics
BPM rasters : 2 FADC

Data rates

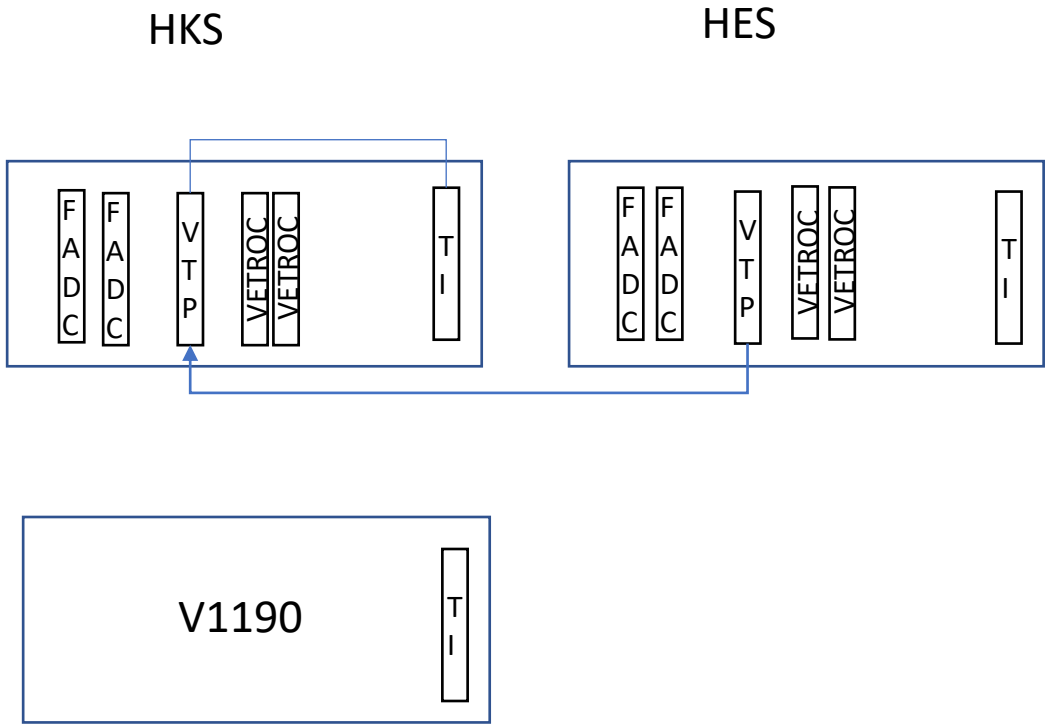
- Rough estimates
  - HKS = 1 MHz
  - HES = 1 MHz
  - Coincidence = 1MHz x 1 MHz x 20 ns = 2 KHz

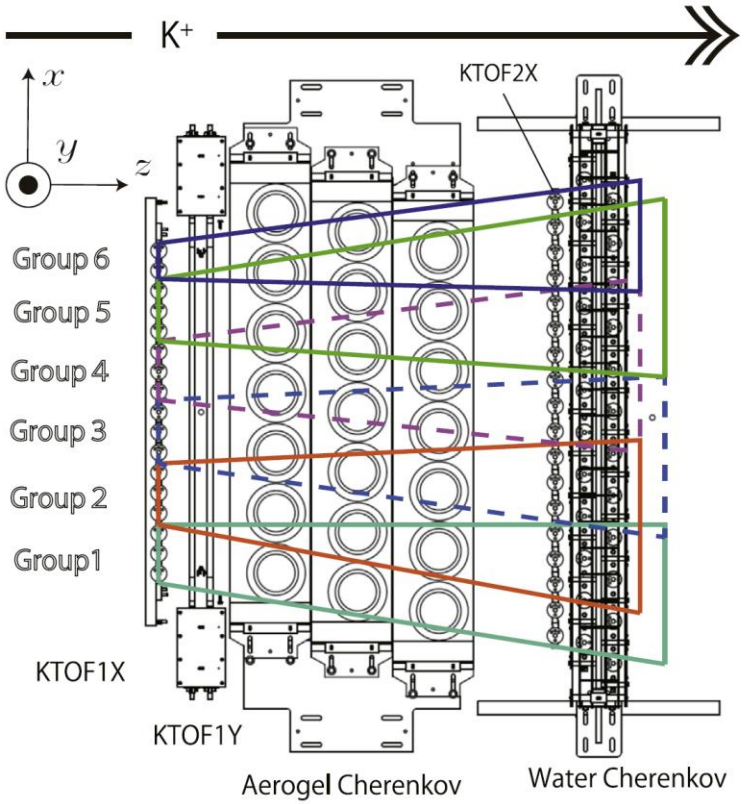
- Plan for up to 20 KHz desirable
- Using CODA3 and event blocking should be doable (similar to CLAS12) will be tested during NPS
- Need to evaluate detector occupancies
- If useful can record full FADC waveforms



Example scintillator SoLID beam test

Trigger





Can program VTP for coincidences between scintillators
If use VETROC instead of V1190 could add Drift Chamber to trigger

Additionnal electronics

- Beamline info
  - Target BPM
  - Raster
  - 1C12 BPM cabling

To do / Testing

- Bench testing and testing with detector VETROC
- Setup FADC trigger with VTP
- Setup testing in ESB

Additionnal detectors

- MCP PMTs
- MRPC
- Would need dedicated new electronics

Conclusion

- HKS and HES
  - FADC = 88 + 42 +48 +116 = 294 channels = 19 FADCs = 2 VXS crates
  - V1190 = 2268 channels = 18 V1190 = 1 VME64X crate
  - TOF = 204 channels = 7 V1290 = 8 F1 = 3 VETROC
  - Could use HMS/NPS/SBS hardware
- CODA3 with event blocking should allow 20 kHz trigger rate
- Digital trigger using FADC and VTP
- If use VETROC instead of V1190 can include in L1 trigger (High res TOF and Drift Chamber)

Backup

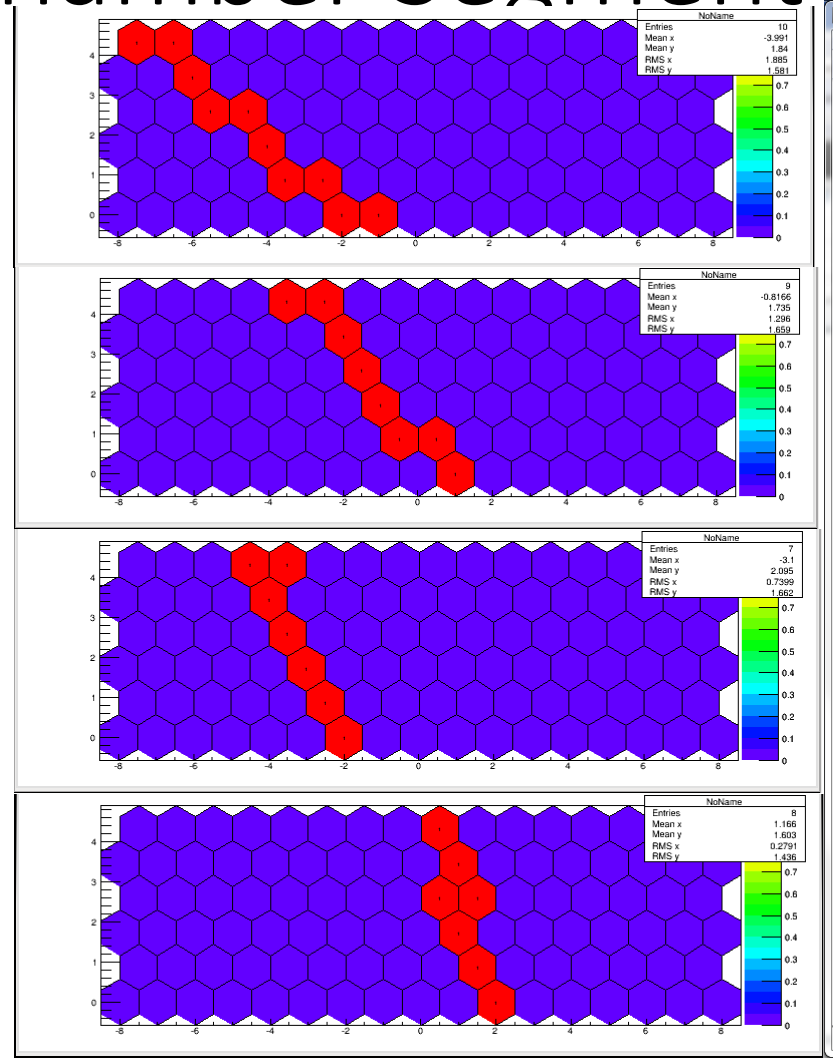
CLAS12

Detector	Can be in trigger?	Will be in trigger?	Trigger Algorithm
ECAL/PCAL	Yes	Yes	U/V/W Clustering
DC	Yes	Yes	Segment Position/Angle Finding
CTOF/FTOF	Yes	Yes	Hit based
HTCC/LTCC	Yes	Yes	Hit based
FT	Yes	Yes	3x3 Clustering
CND	Yes	No	N/A
SVT	Yes	No	N/A
RICH	Yes	No	N/A
MicroMegas	No	No	N/A

- CLAS12 triggering will support geometric matching (e.g. drift chamber segment points to clusters, etc…)

Drift Chamber Segment Finder Example

sweeps angle and wire offset:



valid segments are binned into common angle, VHDL file w/ equations autogenerated:

C:\Users\braydo.JLAB\Desktop\dcsegfinder.vhd - Notepad++

File Edit Search View Encoding Language Settings Macro Run Plugins Window ?

dcsegfinder.vhd

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

use work.utils_pkg.all;

-- Note: This source is auto generated by dctrackbin.C
--       This VHDL file should be modified/regenerated by changing the .C source.

entity dcsegfinder is
    generic(
        DC_ARRAY_START  : integer := -7;
        DC_ARRAY_STOP   : integer := 6
    );
    port(
        CLK             : in std_logic;

        SEGMENT_THR     : in std_logic_vector(2 downto 0);
        DC_ARRAY            : in slv6a(DC_ARRAY_START to DC_ARRAY_STOP);

        SEG_HIT_A       : out std_logic_vector(15 downto 0)
    );
end dcsegfinder;

architecture synthesis of dcsegfinder is
    function seghitsum(hits : std_logic_vector) return std_logic_vector is
        variable result : std_logic_vector(2 downto 0);
    begin
        result := (others=>'0');
        for I in hits'range loop
            if hits(I) = '1' then
                result := result + 1;
            end if;
        end loop;
        return result;
    end seghitsum;
begin
    SEG_HIT_A(0) <=
        '1' when SEGMENT_THR <= seghitsum((DC_ARRAY(-1)(0) or DC_ARRAY(0)(0))&(DC_A
        '0';

    SEG_HIT_A(1) <=
        '1' when SEGMENT_THR <= seghitsum((DC_ARRAY(-1)(0) or DC_ARRAY(0)(0))&(DC_A
        '1' when SEGMENT_THR <= seghitsum((DC_ARRAY(-1)(0) or DC_ARRAY(0)(0))&(DC_A
        '1' when SEGMENT_THR <= seghitsum((DC_ARRAY(0)(0) or DC_ARRAY(1)(0))&(DC_AR
        '0';

    SEG_HIT_A(2) <=
```

VHSIC H length : 20797 lines : 178 Ln : 1 Col : 1 Sel : 0 UNIX ANSI INS

Dri egn ndi ger

x14 DCRB

70Gbps
(DC Hits)

GTP:
prototype VXS concentrator card

- Receives all DC hits from DCRB
- Searches for track segments and reports position/angle to next trigger stage
- VTP (mentioned later in talk) with be used in CLAS12

- Scope like interface on GTP allows real-time display of found segments by trigger logic
  - Cosmic event shown where only 1 segment was the trigger condition