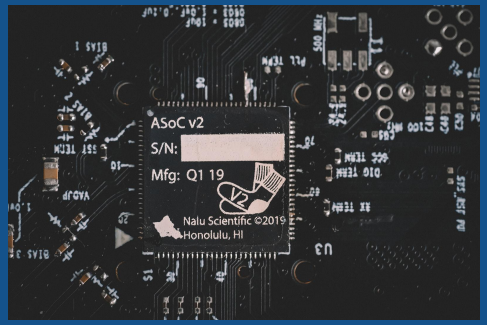
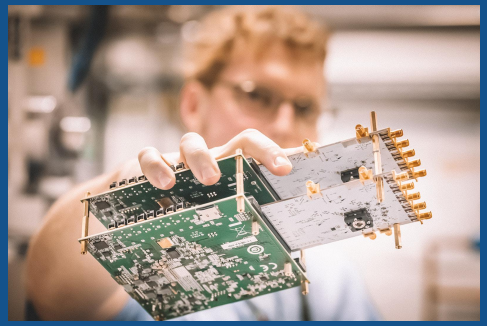
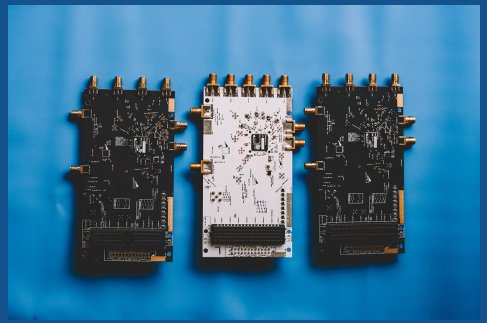
EIC-HPSoC - Project summary and response to reviewers

Luca Macchiarulo
11/16/2022







ABOUT NALU SCIENTIFIC

Fast Growing Startup in Honolulu, Hawai'i

- Located at the Manoa Innovation Center near U. of Hawaii
- 20 staff members-diverse background
- Access to advanced design tools
- Rapid prototyping and testing lab

Technical Expertise

IC design:	Analog + digital System-on-Chip (SoC)
Hardware design:	Complex multi-layer PCBs
Firmware design:	FPGAs, CPUs
Software design:	GUI, analysis, documentation

Scientific Expertise - NP/HEP subject matter experts

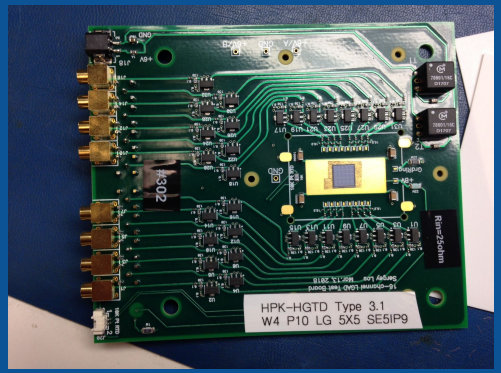
- Physicists (3x)
- Electronics for large scientific instruments

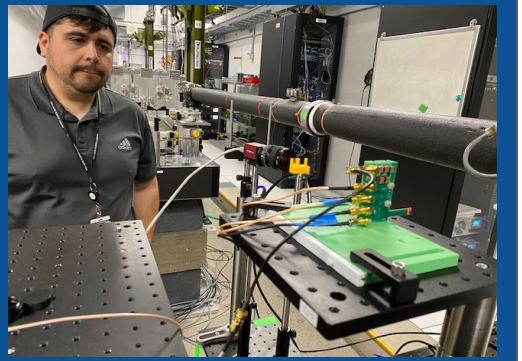
Exclusive Distributor Agreement for North America

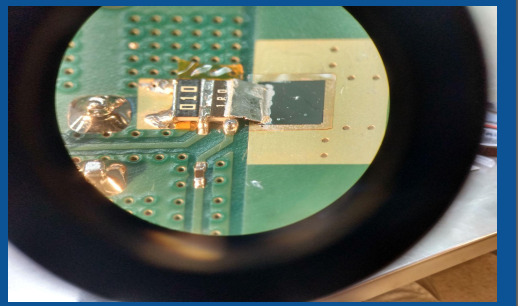
- Sales of ASICs, eval boards
- Enhanced OEM opportunities

CAEN Technologies Inc.

Nalu = 'wave' in native Hawaiian language







ABOUT SCIPP

SCIPP
SANTA CRUZ INSTITUTE FOR PARTICLE PHYSICS
UC SANTA CRUZ

The Santa Cruz Institute for Particle Physics (SCIPP) is

- A California state-supported research unit on the UC Santa Cruz campus
- Embedded within an AAU that is also minority-serving (one of only 5)
- Hosts research in Physics, Astrophysics, Life Science and Engineering
- Emphasis on Instrumentation

SCIPP Infrastructure

- Automated precision interconnect systems
- High-bandwidth (10+ GHz) test and measurement
- Benchtop characterization (Beta, alpha, fast-pulsed laser)
- Metrology and precision mechanics

SCIPP Capabilities

- TCAD simulation and sensor design
- High-speed detection systems
- Rapid prototyping
- Bench-test and test-beam based detector characterization
- Electronics design and characterization

SCIPP is internationally renowned as a driver of innovation in the field of nuclear instrumentation and its associated readout

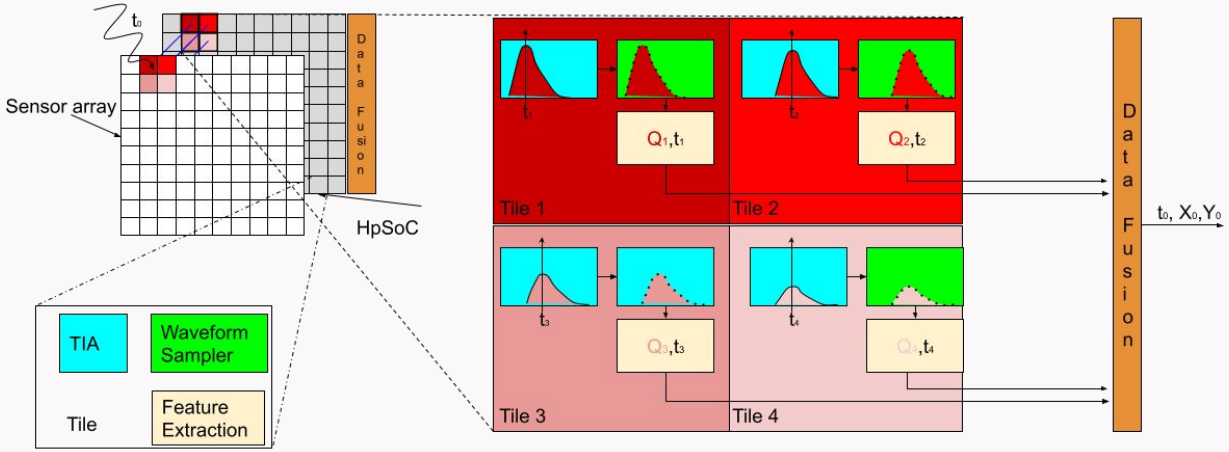
HPSoC - concept and target specs

- State of the art photodetectors (e.g. LGADs) -> excellent spatial and timing precision.
- Limited by existing readout electronics.
- Time-to-Digital Converter (TDC) and time-over- threshold (TOT) readout limitations:
  - Indirect estimate of integrated charge,
  - Limited sub-pixel spatial resolution
  - No correction for pile-up,
  - Sensitivity to sensor aging (radiation)
  - Time errors (timewalk, baseline wander, and waveform shape variations).
- Use full waveform information would solve all issues, but:
  - Expensive in area/power
  - Too large data BW required
- Proposed solution: HPSoC:
  - Full WaveForm Digitization **(WFD)** per pixel,
  - On-chip feature extraction
  - On chip data fusion (sub-pixel spatial resolution)

Parameter	Specification	Comment
Channel no.	100+	(pitch 300-500 µm)
Sample rate	10 GSa/s	
Bandwidth	2 GHz	
No. bits	10	
Supply Voltage	1.0V	2.5V for digital I/O
Timing accuracy	5ps	With calibration
Front-End stage	Embedded TIA	Optimized for AC-LGADs and other fast sensors
Analog buffer length/channel	256	Effectively operating with a 2 banking system to allow for bursty signals
Power/channel	2mW	Trade-off with integration
Integration	System-on-Chip	Digitizer. Feature Extraction, data fusion

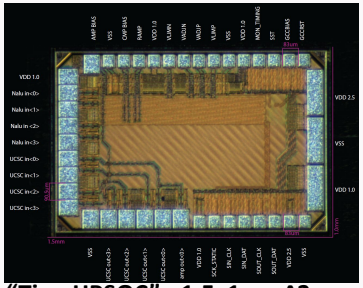
Target Structure

1. Dense sensor array readout (target of ~300um pitch)
2. Modular, independent (“tiles”), per pixel
3. On chip signal amplification (TIA+gain)
4. Continuous waveform sampling and triggered digitization - “ping-pong” operation to avoid deadtime.
5. On the fly timing and amplitude (charge) extraction
6. “Data fusion” and export.

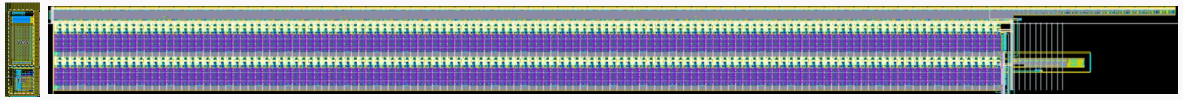


Existing channel-level layout

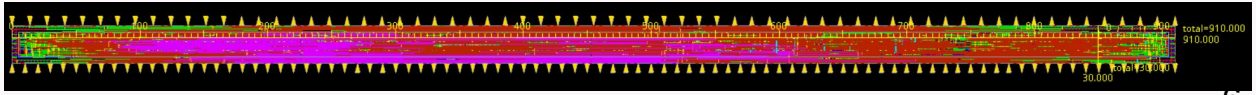
- Front End amplifier - composed of a TIA and gain stage - fabricated and extensively tested by SCIPP
- Sampling array and conversion logic: 3 different versions incorporated in fabricated chip - ready for testing (some supply issues need to be addressed before full evaluation possible)
- Digital control: fully placed and routed design to permit area/power estimation (NOT in fabricated chip):
  - control for channel,
  - readout of digitized data
  - preliminary logic for feature extraction
    - Thresholding (on digitized data) -> for time of arrival estimation
    - Integral over threshold -> for charge estimation



“Tiny-HPSOC” - 1.5x1mm^2 for part prototyping



Front end amplifier and channel layout - approximate size: 900um x 80um for 256 samples.



Fully placed and routed channel control - dimensions are 900x30um^2, including power rails.

Proposed work and work structure

WBS 1. <u>Design of the second iteration of the prototype chip (Nalu lead)</u>:

1. New *front-end* optimized for use with EIC-specific sensor(s);
2. *full channel* design (integrate ramp generation, sampling switching).
3. Add on-chip capability for *self-triggering* based on modification of existing Nalu designs;

WBS 2: <u>Integration of test chip, verification and foundry submission (Nalu lead):</u>

1. Fine tune with full-channel simulation *digital control* and integrate in single channel.
2. *Validation:* Full functional verification, physical verification (LVS/DRC)
3. *Fabricate the second prototype* chip iteration;

WBS 3: **<u>Evaluation PCB test board design, fabrication and chip testing (SCIPP lead)</u>:**

1. Packaging, (Nalu and SCIPP)
2. Testing board design for pre-amp stage, sampling and digitization quality
3. *Loading and verification* of the modified evaluation test board;
4. *Characterization* of new prototype chip using calibration and sensor data collected through both bench and beam testing, including
    a. Confirmation of basic *functionality*,
    b. Analog *gain and noise* performance,
    c. Analog *dynamic range* studies,
    d. Assessment of the *performance of the initial on-chip digitization feature,*
    e. Analysis of *characterization* data as it relates to *physics performance*.

WBS 4: **<u>Firmware Design</u> (Nalu led):** configure the chip, start/stop sampling, start digitization, export data,

Q1: Coupling to experiment

“Historically, electronics work which is not strongly and directly coupled to an experiment has been of limited value given the specificity of needs for the experiment (geometry, power consumption, etc). Can you detail the steps your collaboration is taking to ensure that the ASIC you are developing will stay relevant?”

1. Nalu participated in the ePIC LGADs group starting in 2022 while SCIPP has been a part of that effort since before the Yellow Report, presented results and intention to develop WFD electronics to them.
2. WFD advantages w.r.t TOT-TDC:
    a. Robust method of time and spatial reconstruction
    b. Better timing precision and subpixel spatial resolution (charge sharing among neighboring pixels)
    c. Relax requirements on pixel size and number
    d. More robust against systemic effects such as e.g. time walk, long-term degradation in harsh and inaccessible environment.
3. If funded, continue coordination for a robust alternative readout to the baselined TOT-TDC readout.
4. Nalu’s partnership with SCIPP will allow us to systematically and organically develop this readout capability while actively collaborating with the EIC LGADs group in designing for physics performance and power, thermal, streaming readout and mechanics targets.
5. WFD LGADs readout for the second detector effort - in contact with developers

Q2: Readout and Sync electronics

“In addition to the input stage, a full FEE system also requires configuration, calibration, data transport, and synchronization. Do these other stages of the FEE already exist, or are they currently in development, or will they require initiating an additional R&D effort? What is the strategy to implement a synchronization across a whole system on the level of 10ps, which is smaller than the transition jitter of many clock distribution systems?”

A:

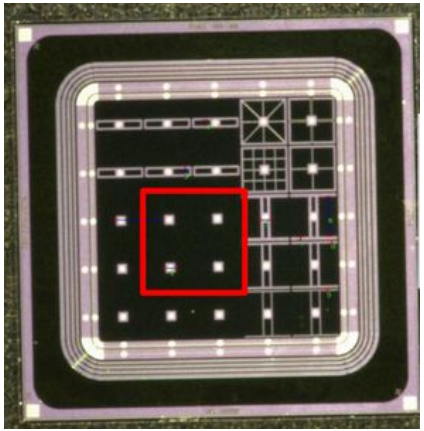
1. FEE:
    a. No FEE system is part of this development (no budget in this proposal).
    b. However, the interface with the chip will be studied to be compatible with and able to support EIC reqs;
        i. A different project (HDSoC, aimed at SiPM readout) is prior Nalu art that can live within EIC;
    c. Interface with the rest of the system very minimal:
        i. input reference clock,
        ii. slow serial interface for configuration
        iii. fast serial interface for data.
    d. Data packetized made compatible with the requirements of any chosen FEE.
2. Synchronization depends only on a proper low-jitter input reference clock,
    a. Distributed to the chips via high-quality differential clock trees using low jitter LVDS drivers and used as differential pairs to the chip input ,
    b. chip to chip relative skews calibration features (i.e. switchable calibration inputs) to recalibrate channels on the field
    c. We have experience with other similar system in which chips needed to be synchronized with careful board design practices should allow the target.
    d. Incidentally, the problem of tight timing synchronization is common to any design that is aiming at the accuracy that is required in the EIC design, and it is not limited to our approach.

Q3: Smaller pitches

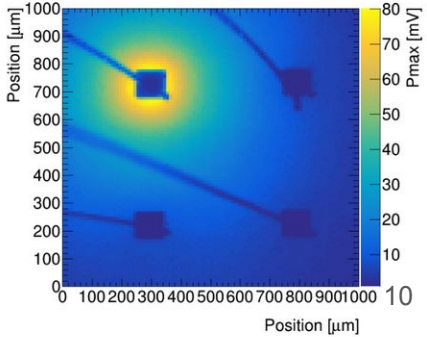
“On a longer time scale, what is the possibility to include interconnections for potentially smaller pitches in view of issues observed with first version of the chip? Ie, is less than 300 um feasible?”

A: Given the chosen process node and requirement for deadtime free operation at reasonable rates, the present envelope is already quite aggressive, -> no further pitch reduction in the immediate future. However:

1. Use of finely calibrated charge information from waveform readout can outperform other mechanism for subpixel identification, mitigating the need for finer pixelation.
   a. AC-LGADs will be the reference approach -> show position determination at the 10 um level for 500 um pitch
2. Larger contribution to the area: sampling array (128+128 samples in ping-pong configuration) Very fast sensors (i.e. 10 um thick AC-GADs)-> reduction of sample requirements (i.e. as low as 32). With such improvements we could reduce the pitch to (at most) a factor of less than 2 (due to other overheads)



500um pitch pad



Q4: Outsourcing

“The chip and board design seems to be fully outsourced to a commercial company. What are the implications for collaborators in using the design/chips? Also for the longer term?”

A:

1. Nalu confirmed the feasibility of a commercial company applied for this type of funding
2. Nalu to keep ownership of IP developed but availability and support for the chips is affirmed throughout the entire EIC project period and EIC physics data-taking.
3. Work at Nalu has been funded via DOE SBIRs. As per US law, SBIR funded technology can be sole source selected for product and service procurement by US funded experiments. DOE highly encourages such collaborations to retain knowledge-base and workforce in commercial and academic sectors, and to commercialize DOE funded R&D.
4. US Gov has certain march-in rights on data and technology that is developed.

Q5: Timing accuracy goal

“Which version of the chip should achieve the 10 ps timing?”

A:

1. Timing accuracy independent on the scale -> channel feature,
2. Good timing be available from the next version of the chip
3. Other ROICs from Nalu (AARDVARC/UDC), in older technologies and operating at the same sampling rate -> accuracy (<10ps) for signal with sufficient SNR.
4. Well known that very good sub-sampling rate timing is possible- for example, DRS4 samples nominally at 5 GSPS, but can reach impressive values of 3-4 ps RMS with calibration (https://arxiv.org/ftp/arxiv/papers/1405/1405.4975.pdf).

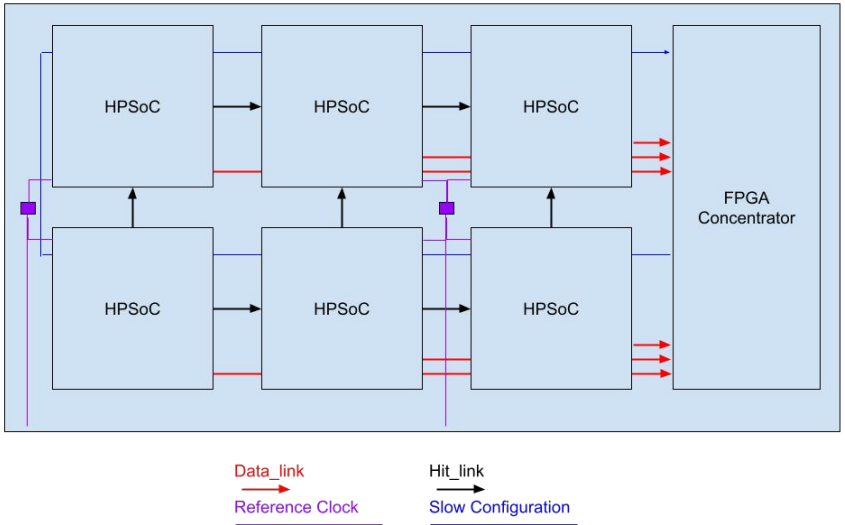
An important evaluation will be that of multi-channel to ensure that incomplete isolation between channel is not adding crosstalk and timing jitter, so a mini-module of 4 channel would effectively be able to probe that as well.

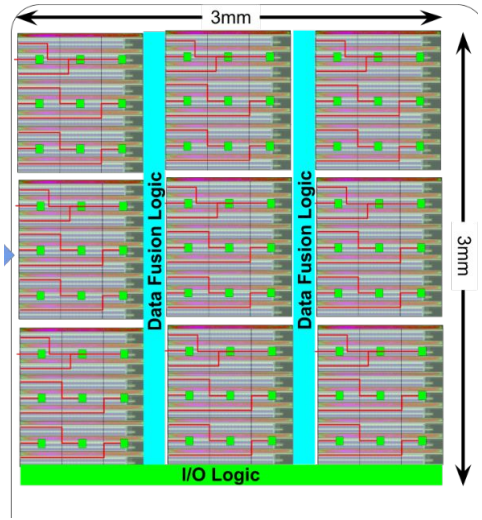
Q6: Interconnect and larger area detector

“It would be good to see a concept for interconnection and larger area detector.”

A:

1. Lean interfacing structure to the FEE electronics, modularly expandable
2. Sensor interfacing, dependent on type and form factor of the chosen sensor - SCIPP expertise in performing experiments with LGADs crucial in defining a proper concept. Use of a redistribution layer on the top will permit an area access to the chip that will be mounted directly behind the sensor using customizable interposers.





Q7: Feature extraction details

“The digital feature extraction is not yet well defined, some initial tests are envisaged for a FPGA implementation. What is the exact strategy to implement a feature extraction with lots of parameters inside the ASIC?”

A:

1. Some basic forms of FE designed and implemented in synthesizable digital code, to evaluate complexity of implementation.
    a. 2 different algorithms: a CFD (constant fraction discrimination) algorithm and a centroiding algorithm.
    b. It also performs charge estimation based on direct Riemann sum of samples over programmable threshold.
2. Preliminary software evaluations of least squares as well as more complex pattern matching algorithms.
3. A simplified version of laid out digital core for HPSoC (threshold crossing for time and sum over threshold for charge)
    a. Feasible in area within the minimum pitch design for individual channel.
4. FPGA-level exploration to selecting the most appropriate algorithm (i.e. lower cost in area and power for a given performance in timing and latency/rate) - but the existing implementation shows that a moderate complexity FE is possible within the specs (some trade-offs of accuracy/power might be necessary).
5. Algorithm parametrizability - introduce programmable registers to control:
    1. Threshold for pulse definition (possibly different for leading edge/tail)
    2. Programmable Fraction for CFD (limited selection to reduce division complexity)
    3. Coefficients for FIR/matched filters (probably shared among groups of channels)