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Development of a Generic, Low-power and Multi-channel Frontend Readout ASIC for Precision Timing Measurements at EIC

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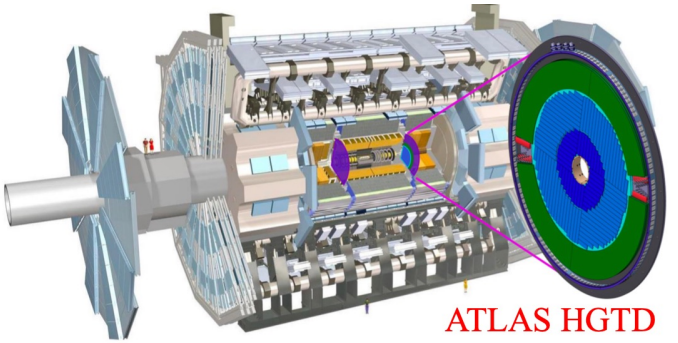
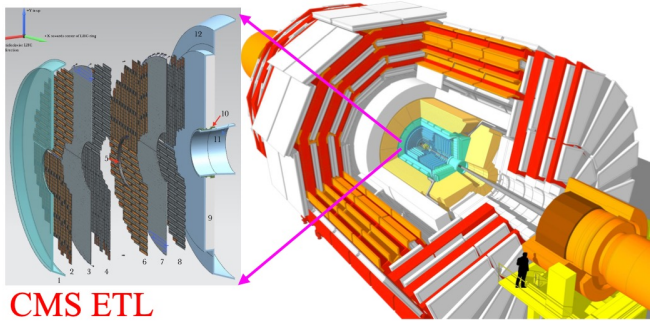
FCFD: Fermilab CFD chip

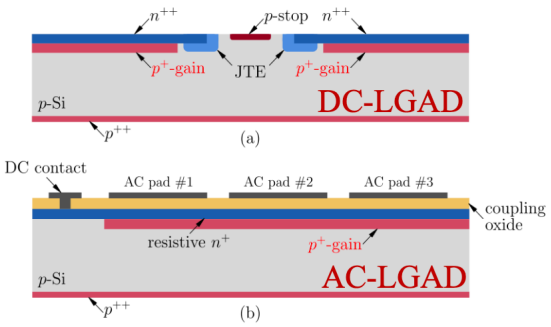
- Goals:
  - Develop a robust fast-timing measurement technique for fast detectors
  - 30 ps time resolution or better
  - Easy to use and stable: no corrections, or repeated calibrations and threshold adjustments
- Our approach:
  - **We propose to develop a multi-channel ASIC to measure both the arrival times and amplitudes of signals from such detectors.**
  - Our solution utilizes Constant Fraction Discriminator (CFD) that does not require offline corrections, calibrations or corrections, is simple in operation.
- General principle could be useful for other applications, e.g. AC-LGAD, or LAPPD
  - **The main deliverable of this project is a multi-channel chip that achieves time resolution of around 25 ps and position resolution around 5 μm.**

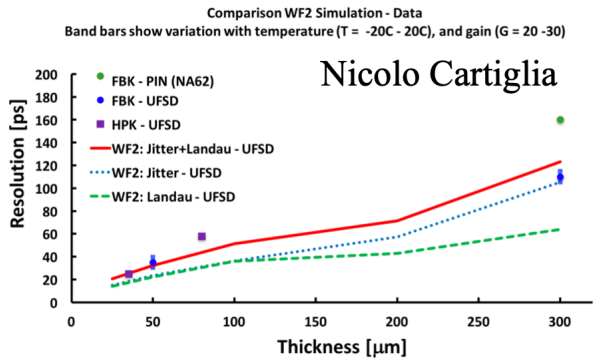
AC-LGAD Technology

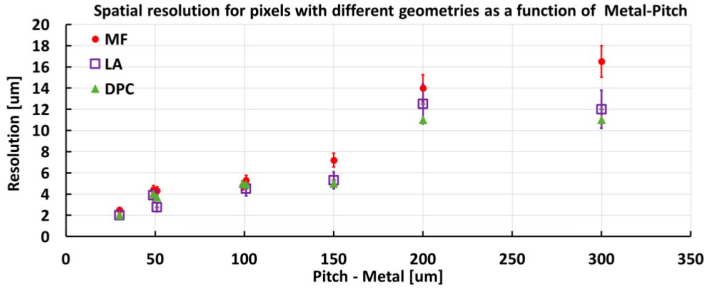
- Timing detectors based on DC-LGAD being built by ATLAS (6.4 m^2) and CMS (14 m^2) for data taking in 2028+.
- AC-LGAD not only provides precise timing resolution like DC-LGAD, but also 100% fill factor and much better spatial resolution with signal sharing.
- AC-LGAD proposed for EIC experiments
  - TOF PID and tracking for central detectors
  - Timing and tracking for forward detectors with common designs in sensor, ASIC etc. where











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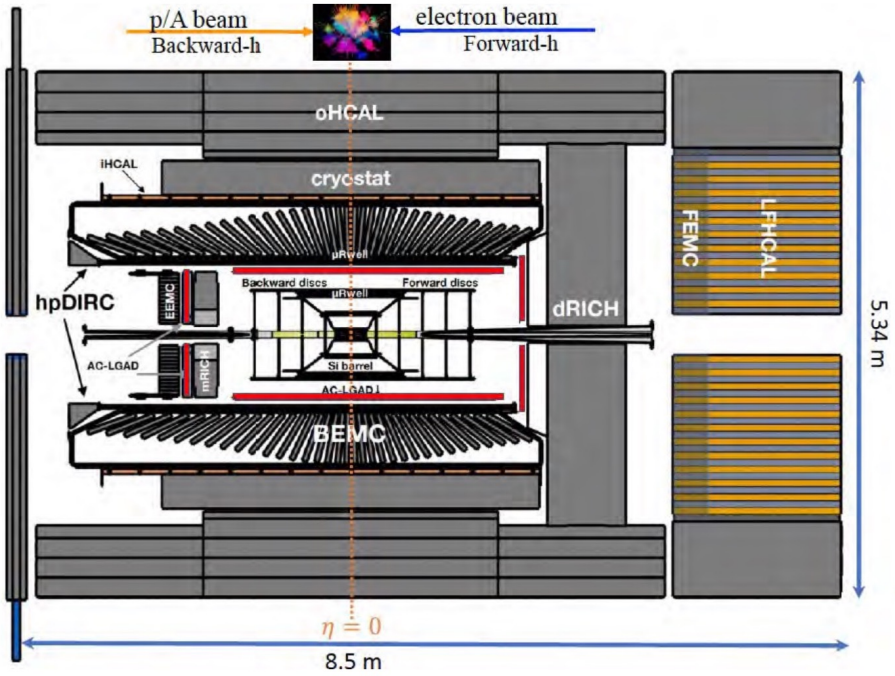
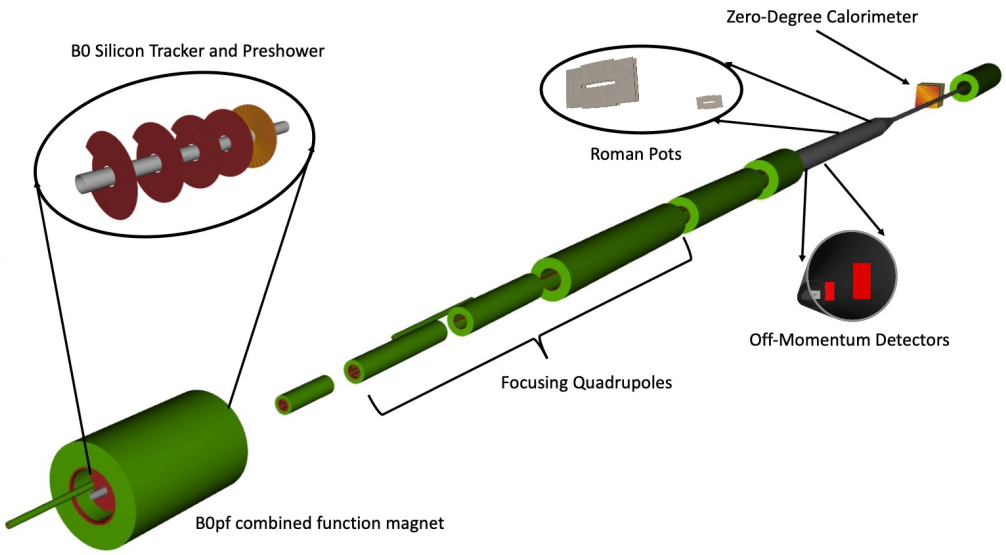
AC-LGAD Detectors for EPIC





Detector	Angular accept.	p_T coverage
ETTL	$-3.7 < \eta < -1.74$	0.15 < p <2.0 GeV
CTTL	$-1.4 < \eta < 1.4$	0.15 < p_T < 1.5 GeV
FTTL	$1.5 < \eta < 3.5$	0.15 < p <2.0 GeV

Detector	Angular accept.	p_T coverage
B0 Detector	$4.6 < \eta < 5.9$	Higher p_T
Roman Pots	$\eta > 6$	Low p_T cut-off from beam optics
Off-Momentum	$\eta > 6$	Low-rigidity from nucl. breakups

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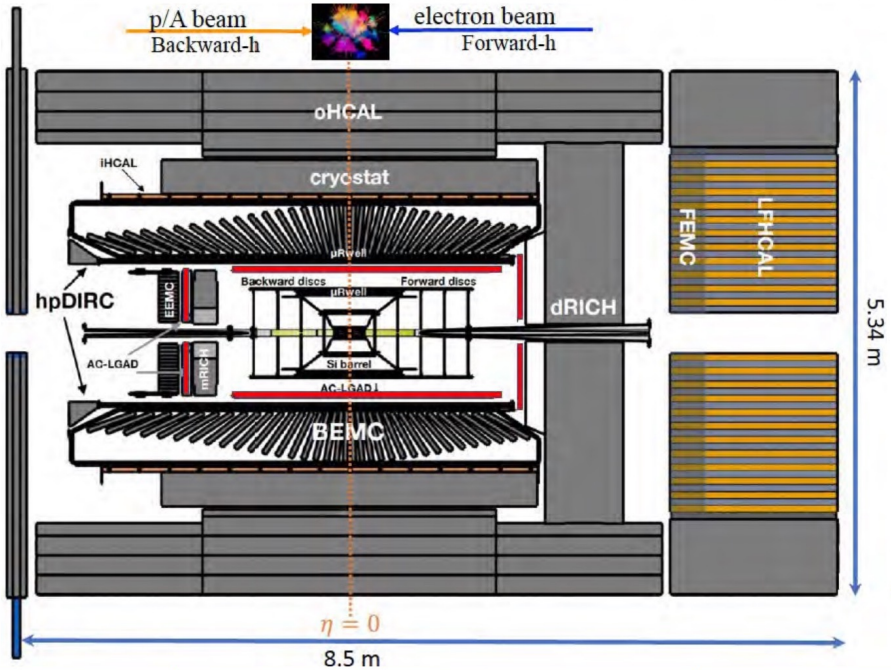
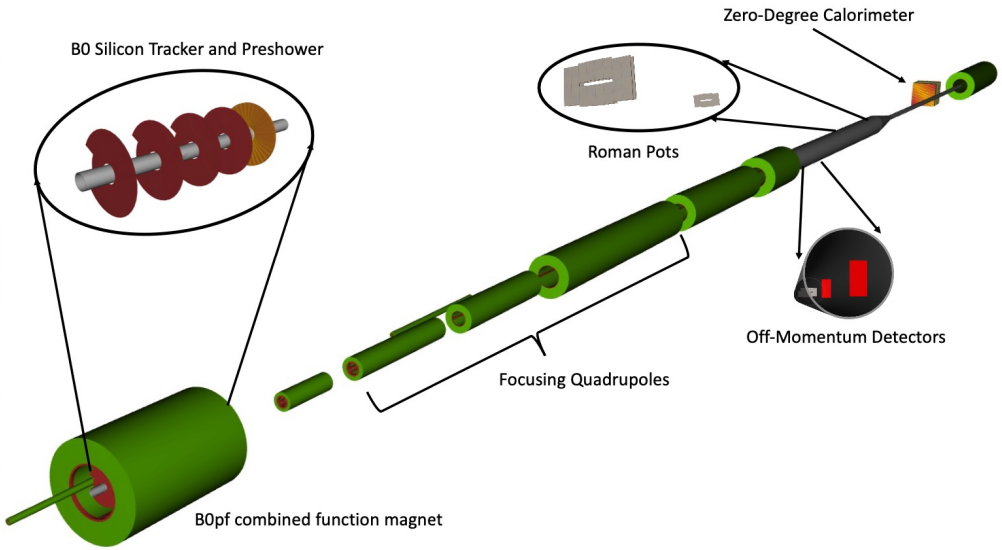
AC-LGAD Detectors for EPIC





	Area (m^2)	Channel size (mm^2)	# of Channels	Timing Resolution	Spatial resolution	Material budget
CTTL	10.9	0.5*10	2.4M	30 ps	30 μm in $r \cdot \varphi$	0.01 X0
E/FTTL	1.20/2.22	0.5*0.5	4.8M/8.8M	25 ps	30 μm in x and y	0.08 X0
B0 tracker	0.07	0.5*0.5	0.28M	30 ps	20 μm in x and y	0.01 X0
RPs/OMD	0.14/0.08	0.5*0.5	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.

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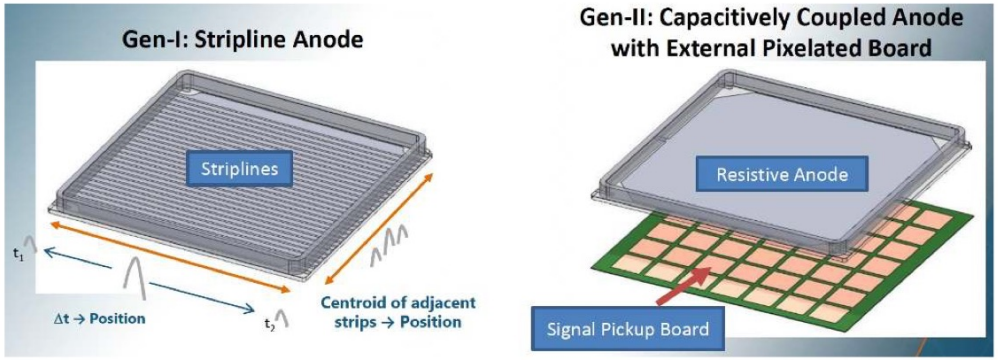
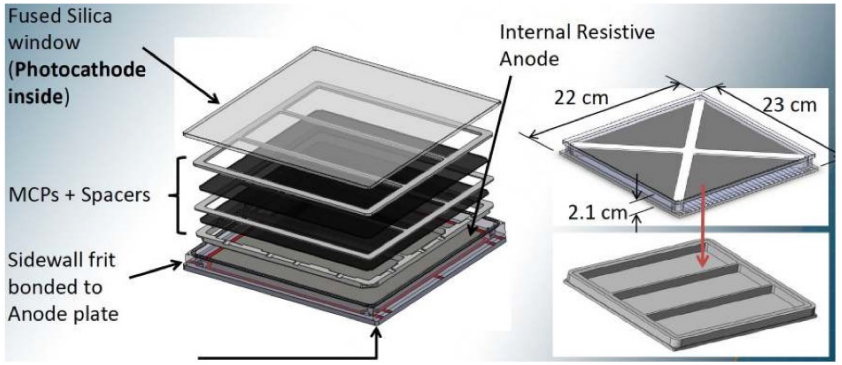
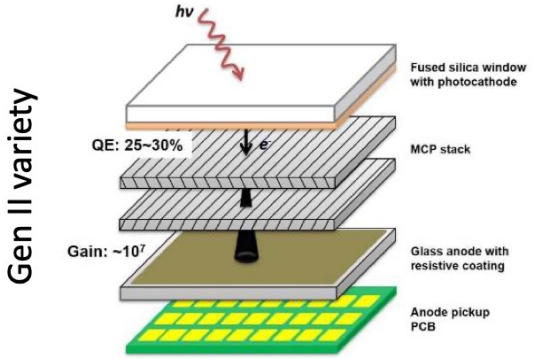
Incom LAPPDs





- An affordable large area (finely pixelated) vacuum photosensor
- Originally developed by LAPPD collaboration; now commercialized and produced by Incom Inc.
  - 10x10 cm^2 or 20x20 cm^2 active area
  - DC- (Gen I) or capacitively (Gen II) coupled species
  - DC-coupled strips or 2D pixellation
  - Expected to be (very) cost efficient in mass production
  - High enough quantum efficiency and uniform high gain up to ~10^7
  - Sub-mm spatial resolution for finely pixelated tiles
  - Single-photon timing resolution on a ~50ps level or higher



From A. Kiselev talk:
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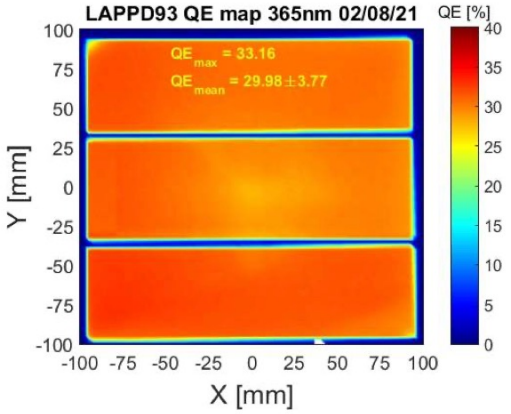
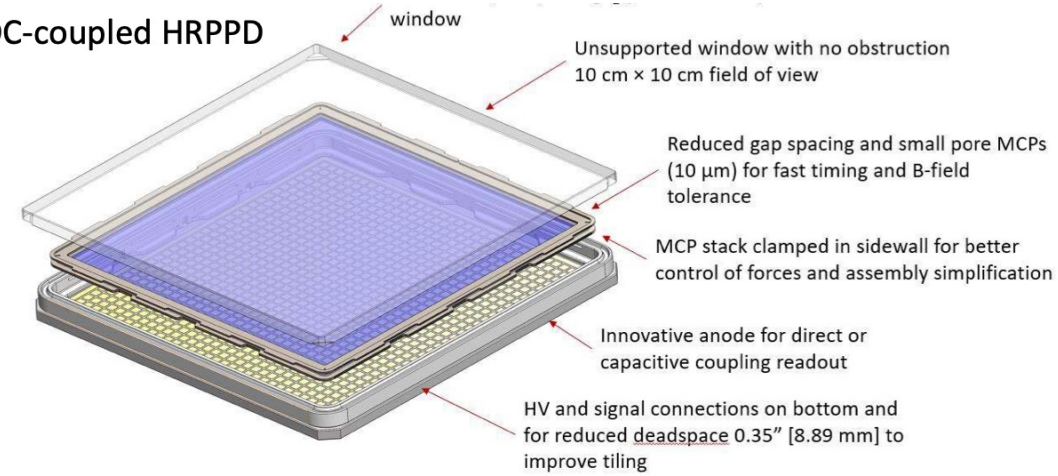
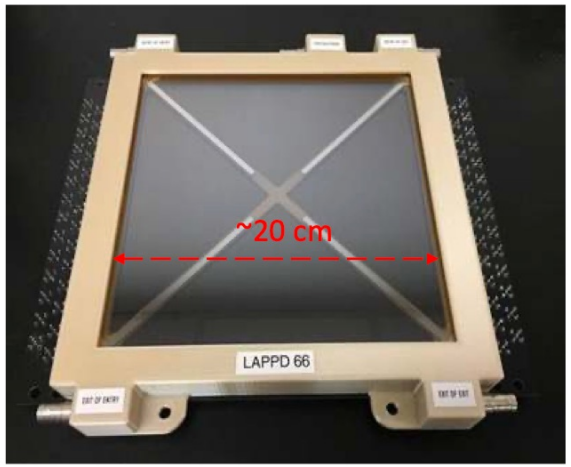
Incom LAPPDs







- ePIC PID detector applications:
  - mRICH / pfRICH: low dark noise, Time of Flight capability (vs SiPMs)
  - DIRC: expected to be more cost-efficient (vs other MCP-PMTs)
  - dRICH: problematic, because of the magnetic field orientation
- Preferred variety:

mRICH	either DC-coupled or Gen II, 10cm formfactor
pfRICH	Gen II, either 10cm or 20cm
DIRC	DC-coupled, 10cm

From A. Kiselev talk:
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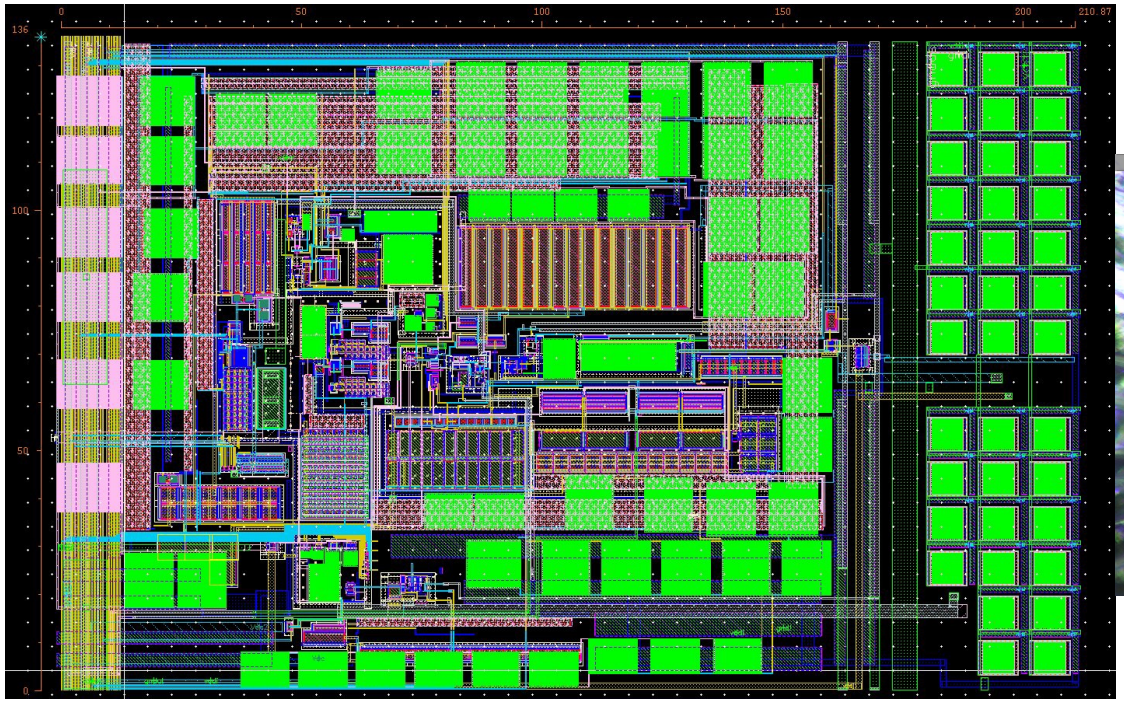
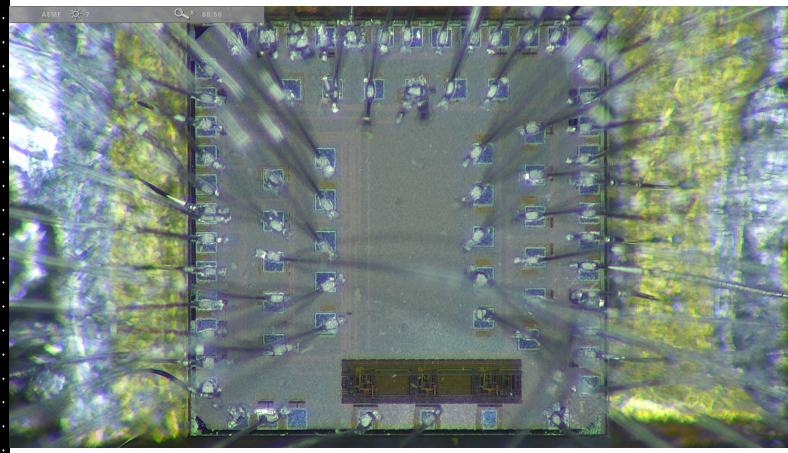
Fermilab CFD ASIC v0 (FCFDv0)

- First version of the chip to test and study the approach
  - Only analog output to measure the performance of the CFD approach
  - Performance measured using internal charge injection, laser, and beta source signals



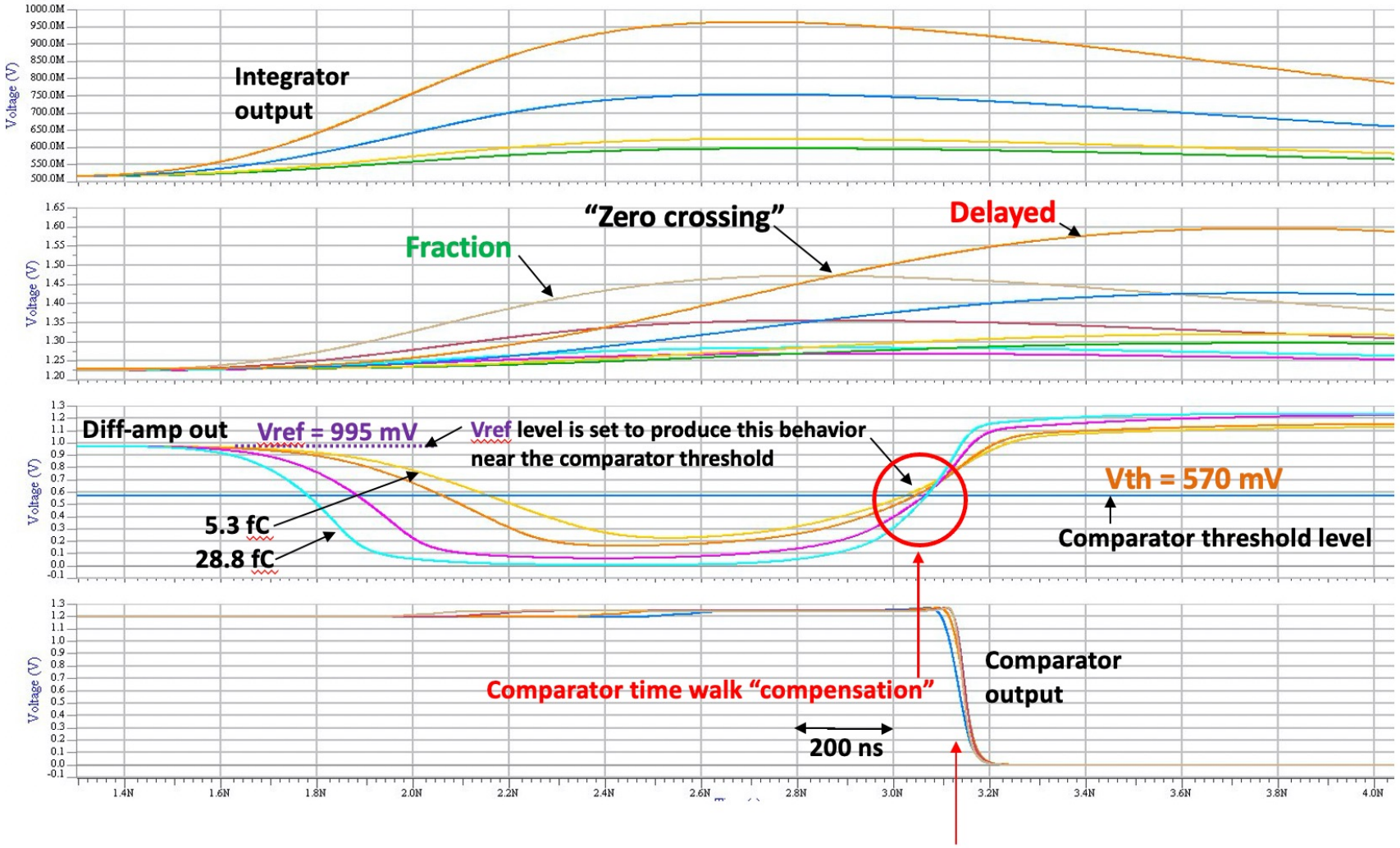
FCFDv0 layout



FCFDv0 wirebonded

Simulation

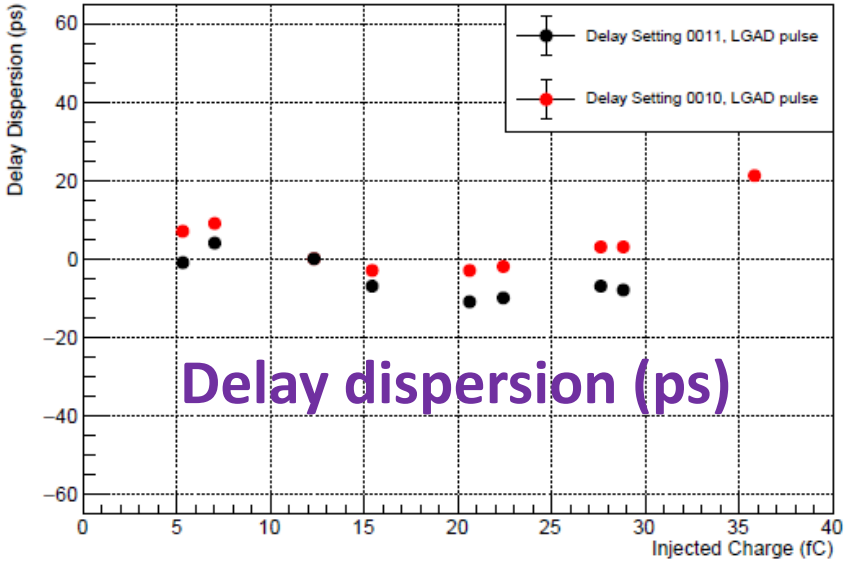
Apply LGAD-like charge pulse to FCFD0 input.
Inject 4 different amplitudes: Qin = 5.3 fC, 7.0 fC, 15.3 fC, 28.8 fC

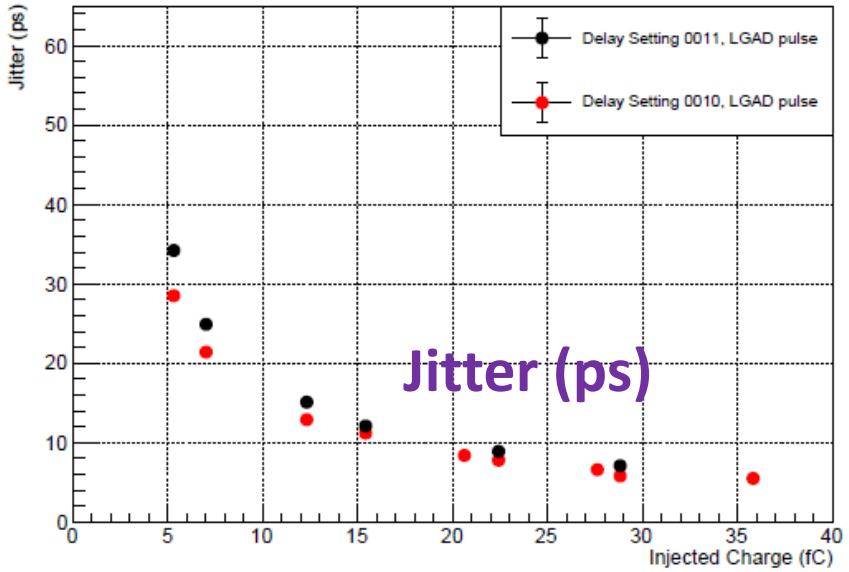


Comparator output has same delay for a range of input amplitudes

Testing with internal charge injection

- Measured delay dispersion and jitter vs. input charge for two different power modes
  - https://indico.cern.ch/event/1019078/contributions/4443948/attachments/2277824/3938152/FCFD0_TWEPP_talk.pdf

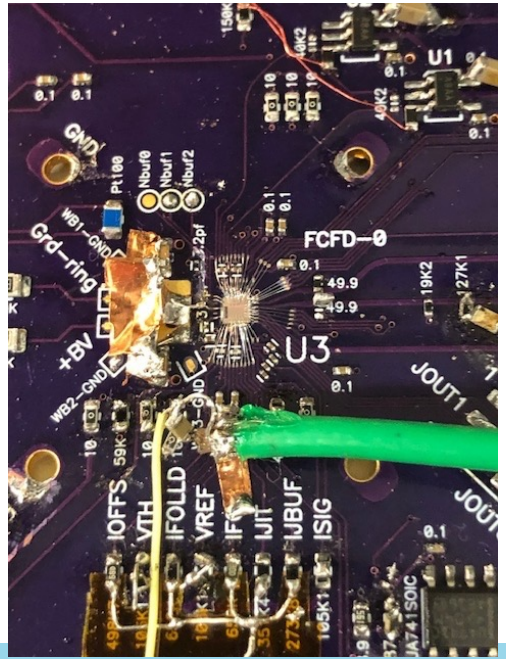


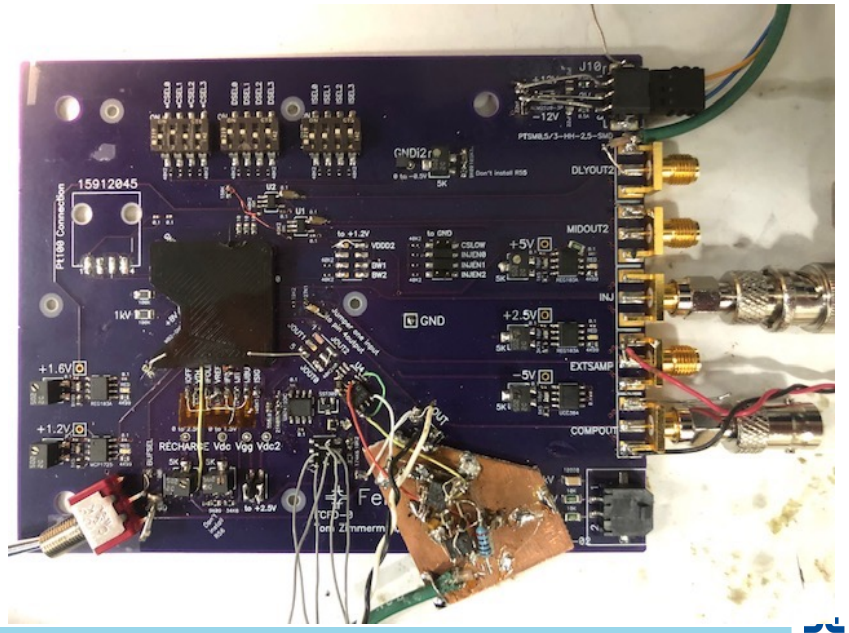


Negligible time-walk, intrinsic jitter around 8 ps at 30 fC

Testing with LGAD signals

- Characterization of FCFDv0 with beta source and test beam
  - Designed dedicated board for measurements with LGADs
  - On-board regulators for charge injection, switch ON/OFF analog buffers
  - SMA-output of the comparator and analog buffer
- Wirebond LGAD sensor of CMS-size pixels (1.3x1.3 mm^2)





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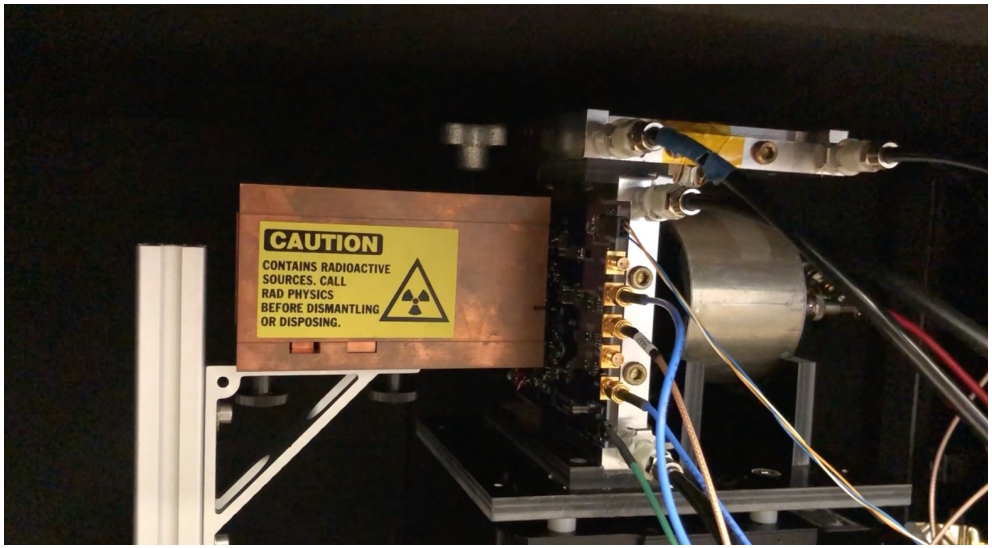
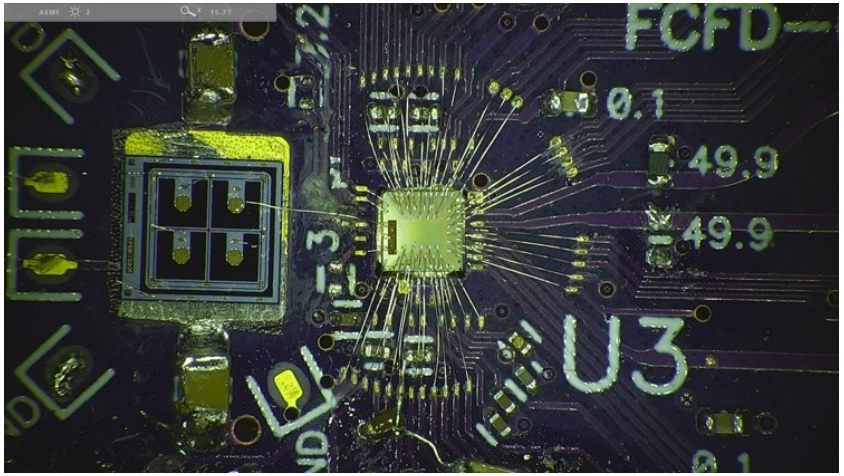
Beta-testing setup

- Board with sensor mounted inside environmental chamber in SiDet
- Test with IR laser and β-source,
  - Test beams to follow when beam returns this Winter



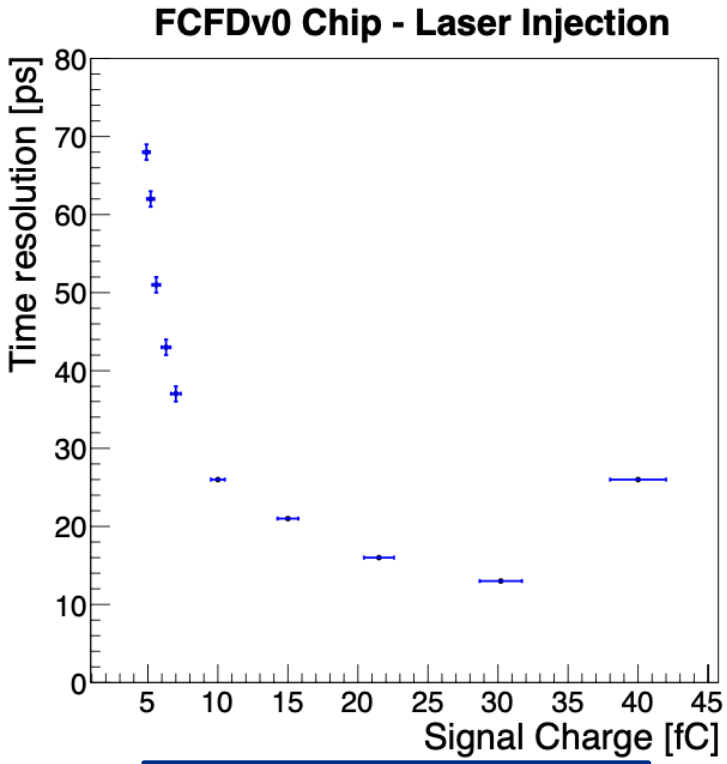
Board mounted with β-source



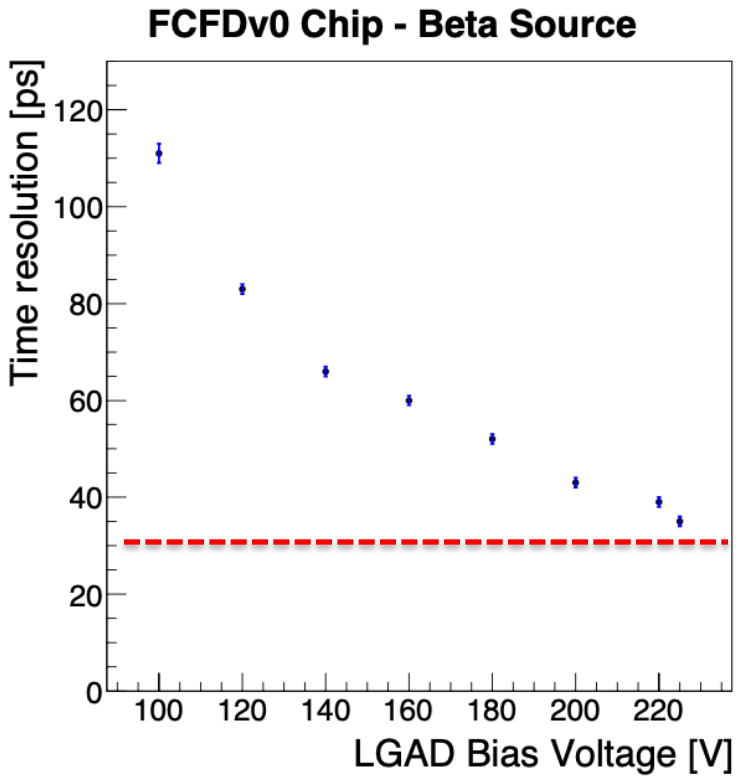
FCFD0 chip mounted to LGAD

Timing ASIC with CFD

- Measurements with laser and beta-source confirm the excellent expected time resolution



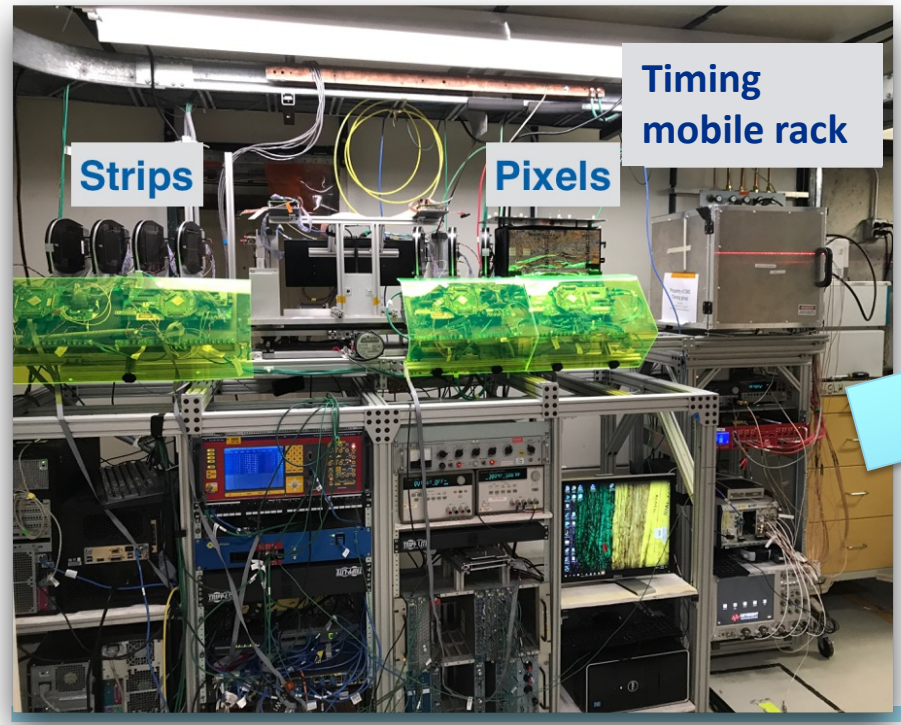
Time resolution with 1.3x1.3 mm^2 LGAD sensor

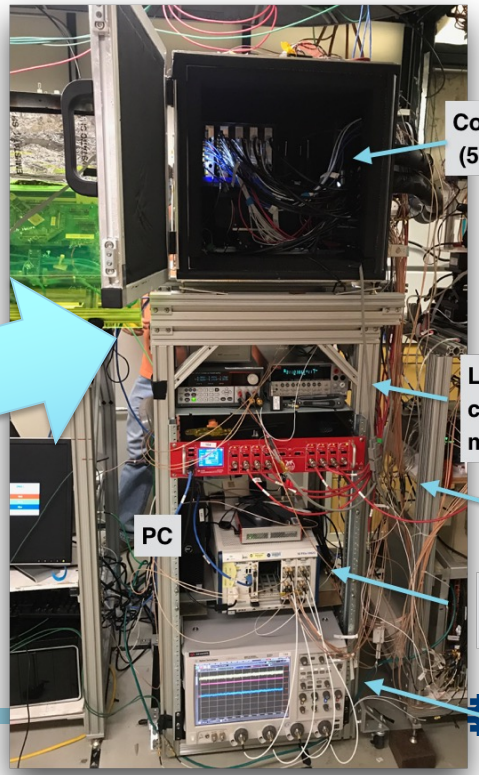


Time resolution with 1.3x1.3 mm^2 LGAD sensor

Fermilab 4D-trackers test beam infrastructure

- Permanent setup in FNAL test beam facility (FTBF)
  - Movable: slide in and out of beamline as needed, parasitic use of beam
  - Environmental controls: sensor temperature (-25 C to 20 C), and humidity, monitoring
  - Remote control (stages, HV, LV), logging & reconstruction; $\sigma_T \sim 10$ ps time reference (MCP)
  - Cold operation of up to 10 prototypes at the same time
  - DAQ: high bandwidth, high ADC resolution scope 4- or 8-channel scope
  - Record 100k events per minute, tracker with ~10 µm resolution





Next steps for FY23

- Develop the next version targeting EIC sensors
  - Option for AC-LGAD readout needs amplitude measurement, in addition to timing, to reconstruct position with high precision
  - Option for LAPPD with larger signals, adapt the readout board with attenuators
  - Intensive work on defining specifications for FCFDv1 is ongoing, leveraging expertise on FCFDv0 design, precision timing sensor characterizations (AC-LGAD and MCP-PMT studies)

Table 1: Year-by-year timeline of the project

Activity	BY1	BY2	BY3
Development of FCFDv1, production, and start testing			
Characterization of FCFDv1 in beams, design of FCFDv2			
Production of FCFDv2 and testing in beams			

Question #1:

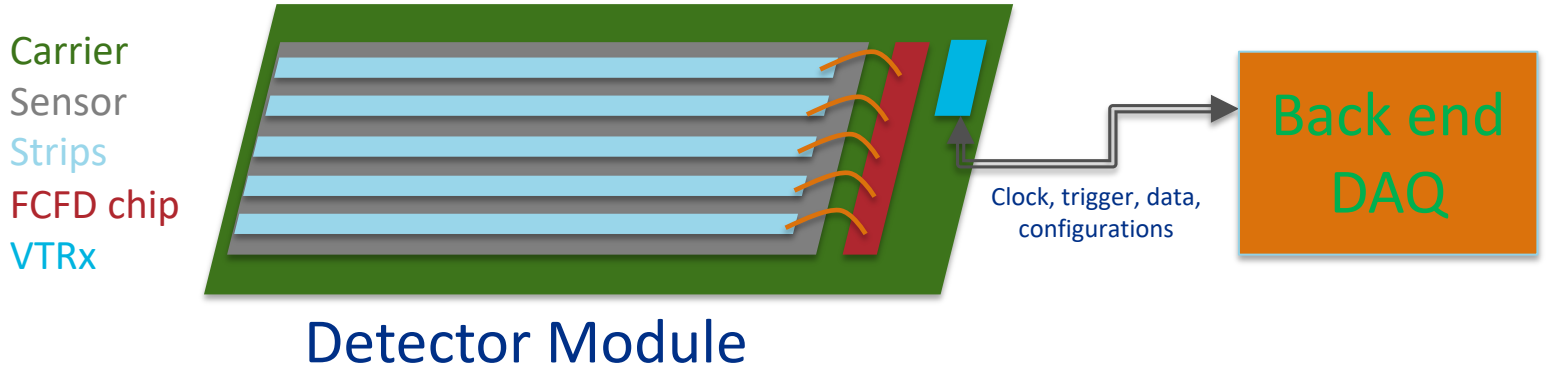
- Historically, electronics work which is not strongly and directly coupled to an experiment has been of limited value given the specificity of needs for the experiment (geometry, power consumption, etc). Can you detail the steps your collaboration is taking to ensure that the ASIC you are developing will stay relevant?
  - The first version of was designed, produced and tested with DC-LGAD sensors
    - FCFDv0+LGAD has been extensively tested with charge injection, laser and beta source and we know how it behaves
  - The next version (FCFDv1) is being optimized with EIC sensor specifications
    - In close collaboration with the EIC detector experts
    - For AC-LGAD or LAPPD: signals in LAPPD are larger by x10-20, and we can implement an attenuation either internally to ASIC, or externally before ASIC
    - The parameters will be presented to EIC community to discuss and agree prior to finalization with engineers

Question #2:

- In addition to the input stage, a full FEE system also requires configuration, calibration, data transport, and synchronization. Do these other stages of the FEE already exist, or are they currently in development, or will they require initiating an additional R&D effort?
  - The FCFDv1 will focus on the optimization of the analog front-end suited for EIC needs, and demonstration of its performance.
  - FCFDv2 will add the remaining missing digital blocks to implement the rest of components required for a full experimental chip.
  - Extensive experience, and existing ASICs in the same technology (65 nm TSMC) have been developed for the CMS timing layer (ETROC) and will be implemented in this chip for the next version, FCFDv2
  - The rest of the FEE system (transceivers, configuration, synchronization chips) will adopt to the EIC common systems. No additional R&D effort required.

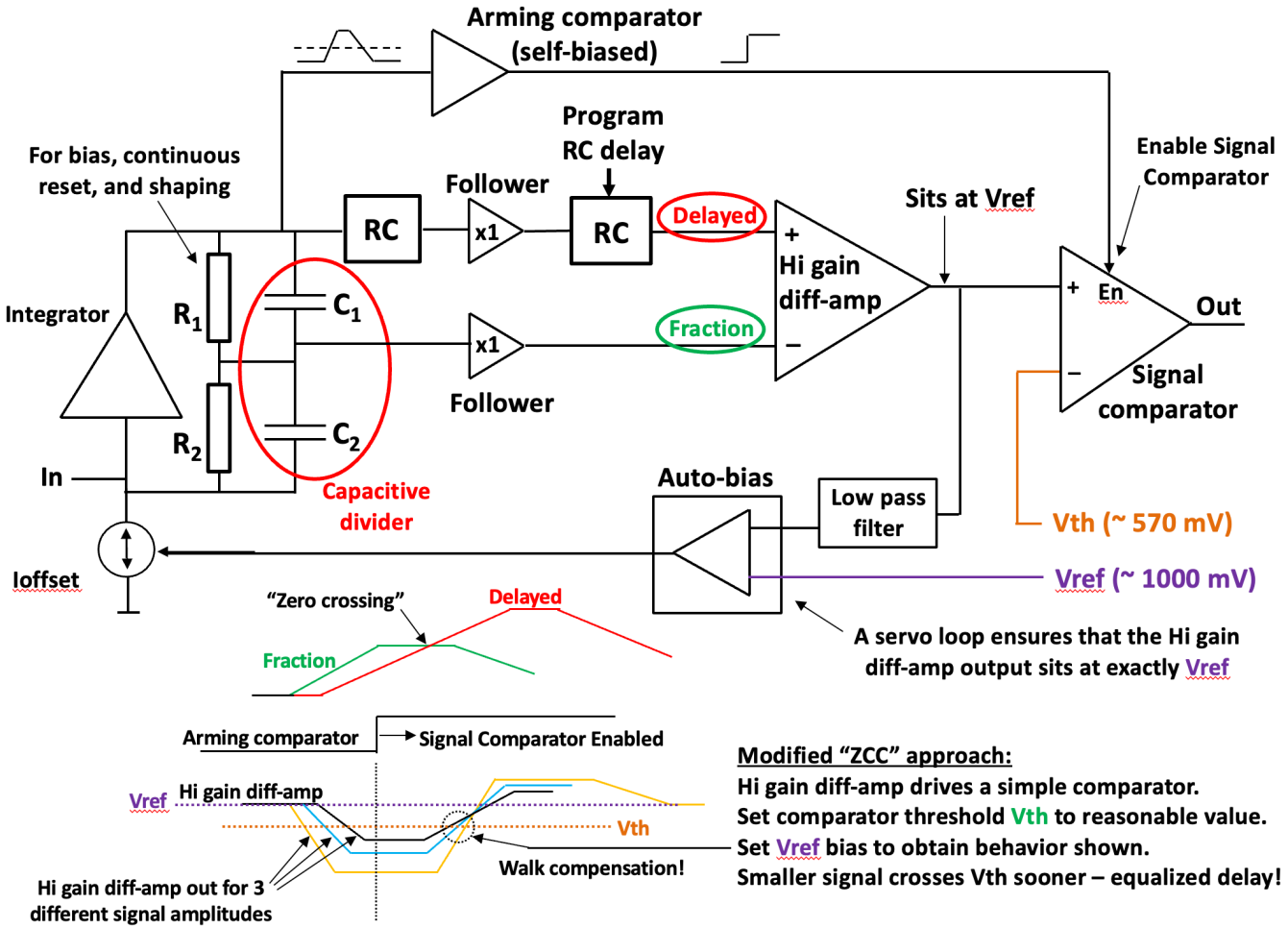
Question #3:

- It would be good to see a concept for interconnection and larger area detector.
  - The conceptual schematics of a detector module is shown below, representing a sensor mounted on a carrier plate, wirebonded to an ASIC
  - Signals from the readout ASIC are then transmitted to the backend through fiber optics
  - LAPPD application will function following the same conceptual design, with the difference being the presence of an attenuation between strip and ROCs



Question #4:

- Can you show a schematics of the chip and the overall system with TDC and global synchronization?



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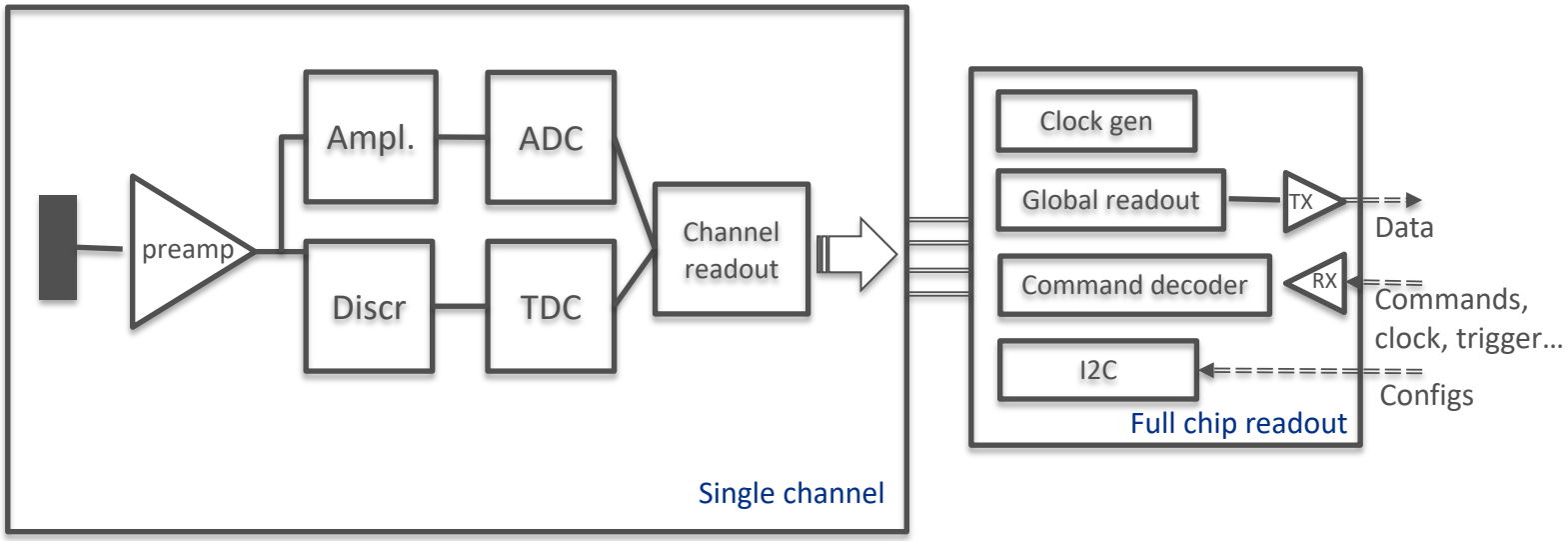
Question #4:

- Can you show a schematics of the chip and the overall system with TDC and global synchronization?
  - For FCFDv1 the analog part will largely be the same, and will include additional blocks for digital components, as shown in diagram below
  - Will closely follow the developments in the timing chip developed for the CMS timing detector readout, adapted for EIC



Question #5:

- What is the schedule and milestones to reach a full readout system?
  - BY1:
    - Specifications for the FCFDv1, and selection of the sensors for demonstrator
    - Design, submission and initial testing of 10-channel FCFDv1
  - BY2:
    - Testing of the FCFDv1 with prototype sensors
    - Design of the complete (full readout) final FCFDv2 ASIC
  - BY3:
    - Completed technology demonstrator fabrication, detailed studies of its performance

Question #6:

- What is the difference in performance, power consumption, and cost between a CFD and LED solution?
  - The difference in performance was studied in detail in NIM 940 (2019) 119-124
  - At low signal amplitudes, CFD algorithm outperforms LE
  - CFD algorithm offers significant reduction in noise, as demonstrated in TOFHIR ASIC for CMS barrel timing detector
  - CFD-based readout is much simpler in operation and maintenance, no need for continuous monitoring and calibration
  - Power consumption for analog front-end LE and CFD comparable (wrt ETROC)
    - Consumption for the digital parts is expected to be low, completed blocks exist
  - Cost for ASIC is defined by the technology node, regardless of algorithm

Question #7:

- The costing for the ASIC development is quite vague. What does the cost entail?
  - In this proposal we request funding for
    - ASIC design engineer time ($150k) for approximately 0.5 FTE
      - Based on the experience with FCFDv0 on design and commissioning time spent by the ASIC designer of the chip
    - TSMC 65 nm MPW production cost ($25k). This is an estimate, and the final cost depends on the ASIC area
    - Test-board design and manufacturing ($30k) to test the chips with connected prototype AC-LGAD and/or LAPPD sensors