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Radiation tolerant low power PLL IP block in 65nm technnology for precision clocking at EIC

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Generic R&D for EIC review

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Motivations

Specifications and state of the art

Research program

Budget

MOTIVATIONS FOR THE PLL IP BLOCK

Clock signals crucial in frontend electronics

- Used for several functionalities
  - Time and amplitude measurements
  - Gigabit serial communications
  - Embedded signal processing
- Fine tuning of phases of the different clocks to optimize signal samplings
- Reduction of jitter of external clock signals to optimize ADC, time measurements and signal over noise ratio
- Radiation hardness

A phase-locked loop (PLL) device could meet all the above requirements

MOTIVATIONS FOR THE PLL IP BLOCK

Objectives of the project

- Study and design of a PLL IP block in TSMC 65nm technology
- Wide range of input reference clock
- Several clock outputs derived from external clock signal, with configurable frequencies and phase shifts
- Low jitter < 10ps
- Small size
- Low power consumption
- Radiation hard
- To be integrated in new ASICs designed in same technology, like the SALSA chip
- To be the base of a possible standalone jitter cleaner PLL or clock fan-out ASIC to be used in electronics boards
- Freely available for all EIC projects

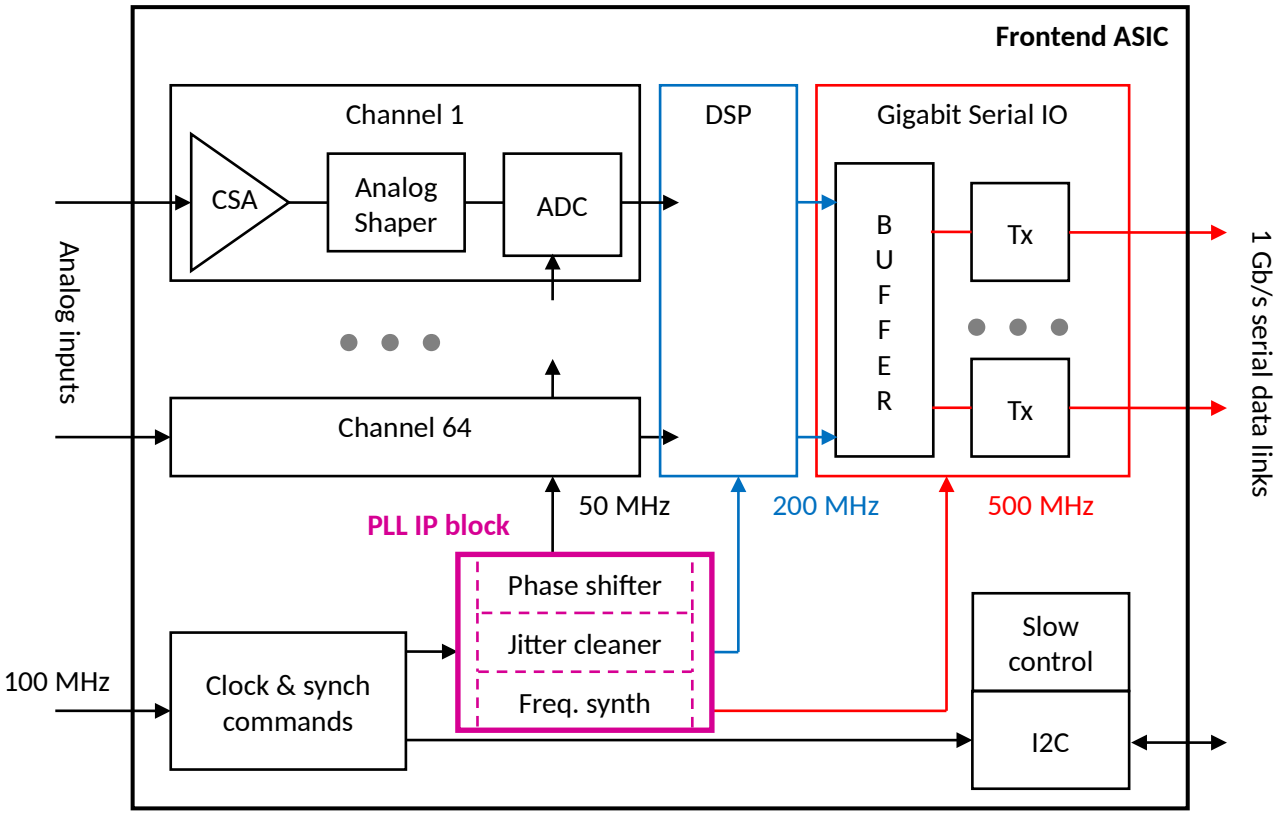
SPECIFICATIONS OF THE PLL IP BLOCK

Technology	CMOS TSMC 65nm
Power voltage	1.2 V
Internal VCO oscillator frequency	2.4-4 GHz, nominal value 3.2 GHz
Input clock frequency	Optimally 100 MHz, large range at least 40-125 MHz
Number of output clocks	4
Output frequencies	Programmable fractions of VCO up to 1.6 GHz
Phase shifter steps	300 ps
Internal jitter, analog PLL case	< 10 ps RMS up to 1 GHz
Internal jitter, hybrid PLL case	~ 3 ps RMS up to 1 GHz
Power consumption	< 3 mW, < 6 mW for hybrid PLL case
Size of the block	~0.1 mm^2
Radiation hardness aspects	Triple redundancy (TMR) including clock divider, minimized SEE, total ionization dose up to 4 MGy

EXAMPLES OF USAGE OF PLL BLOCK

Possible usage in a front-end ASIC

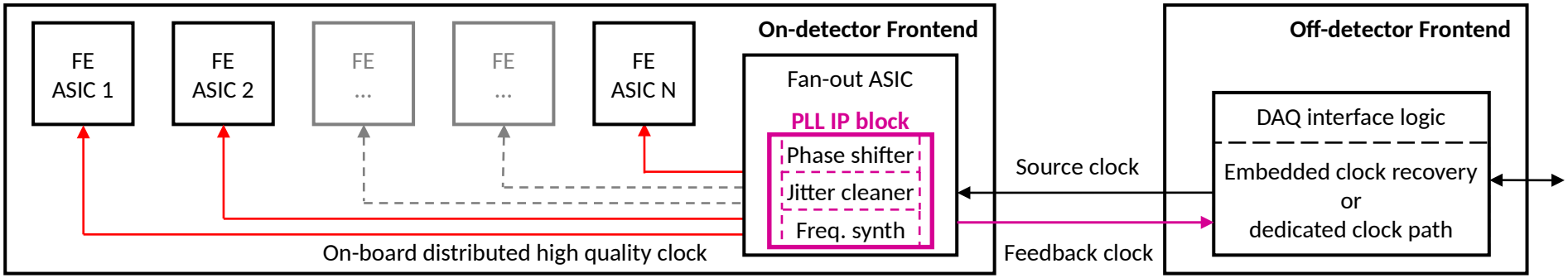
- Frequency upscaling from reference clock
- Delivery of signals with different frequencies
- Reduction of jitter
- Tuning of phase shifts for ADC clock



EXAMPLES OF USAGE OF PLL BLOCK

Possible usage as a clock fan-out ASIC in a front-end card

- Fan-out of low-jitter clock signals to front-end ASICs with configurable phase shifts
- Possible clock feedback to DAQ
- Configuration through I2C bus
- Minimizes the number of signals exchanged between the common and the specific parts of the front-end electronics
- Facilitates card designs
- Improves signal integrity



STATE OF THE ART

Existing PLL chips

- Several commercial chips exist with large input frequency range and excellent output clock purity
- Phase can be tuned but not with thin enough granularity
- Often large power consumption, too small number of outputs, or no radiation hardness

Existing IP blocks

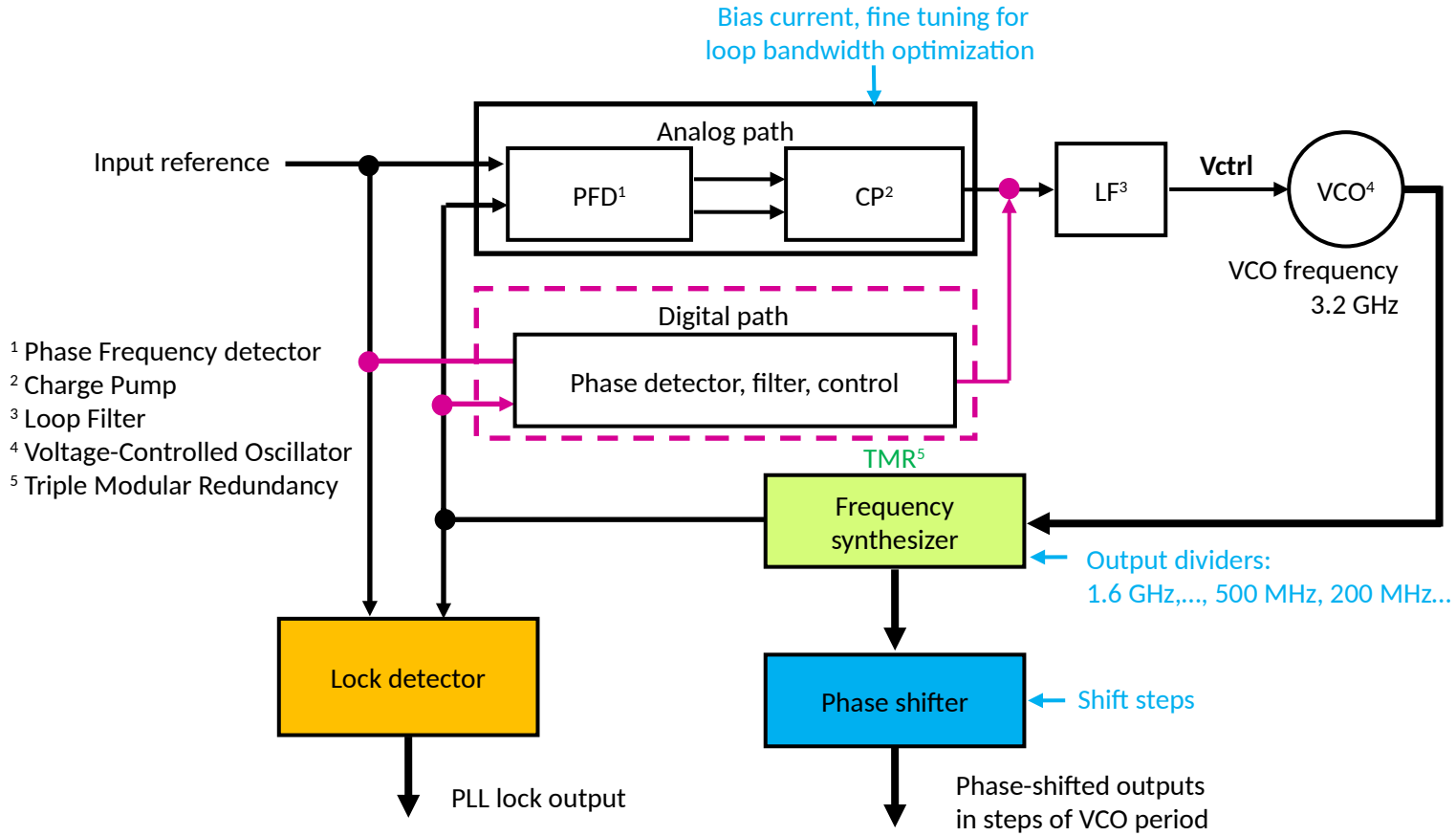
- IP block for lpGBT ASIC developed in 65nm technology: radiation hard, large output frequency range, very low jitter (< 5ps), phase adjustable; but designed for input frequency of 40MHz only (+-1MHz); impossible to adapt without support from CERN lpGBT team
- Block from HGCROC chip for CMS: large input clock frequency range, radiation hard, but 130nm technology. Developed at IRFU, would be used as a base for the development of the future IP block

Digital PLL

- Based on digital loops instead of analog ones → smaller passive elements, easier to filter noise
- Superior jitter performances with larger input frequency range
- Best performance obtained by combining analog and digital loops (hybrid PLL)

PRELIMINARY ARCHITECTURE OF THE BLOCK

Analog PLL based on a voltage controlled oscillator at 3.2 GHz nominal
Optional combined analog+digital control of the oscillator
Tuning of different parameters with slow-control: CP biasing, filter bandwidth, divider settings for the different outputs, phase shifters



RESEARCH PROGRAM

R&D on PLL block

- TSMC 65nm ASIC for larger density, speed and radiation tolerance, already used in some recent ASICs in HEP
- But based on know-how acquired with 130nm PLL developed for HGCROC chip
- R&D based on TSMC PDK simulation tools in order to estimate and optimize performance of the block, + measurements on real prototypes
- Study foreseen on possibility to add digital regulation in loop control, in order to improve jitter performance over a large frequency range with minimal increase of area and power consumption

Development program and schedule

- Development of the low jitter PLL, associated to the study on additional digital regulation of the PLL loop; development of the phase adjustment feature; design of a standalone prototype chip based on the developed IP block, associated with required support circuitry (slow-control, biasing) → 4 months
- Production of the prototypes through the TSMC mini@sic program, suitable for die surfaces up to 2x2mm² → 3-4 months
- Packaging in standard packages (QFN) → ~1 month
- Production of test cards → 4 months (in parallel with chip production)
- Performance measurement with test-bench at IRFU, environmental tests at University of Sao Paulo, at IRFU, and in irradiation facilities → 4-6 months

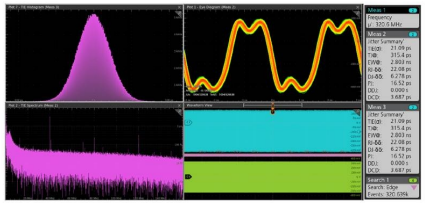
TESTS AND PERFORMANCE MEASUREMENTS

Tests to be done on prototypes

- Determination of lock ranges of PLL; measurements of absolute output frequencies vs expected values
- Measurements of jitter over both short (between two consecutive ticks) and long periods of time; Noise frequency spectra; Measurements of phase noise levels
- With different configurations of the PLL loop
- In different conditions: variation of supply voltage values, noisy supply voltages, various chip temperatures, impact of irradiation, etc...

Test-bench equipment

- ASIC evaluation test-bench already existing at IRFU
- Also existing at IRFU
  - Variable frequency clock generators, with possibility to degrade clock quality
  - 80GS/s oscilloscope
  - phase noise spectrum analyzer
  - Variable temperature chamber (-30 to 60°C)
- Irradiation facilities at Sao Paulo, at CERN and in Slovenia



INTEGRATION OF THE BLOCK IN AN ASIC DESIGN

IP block to be integrated to the SALSA frontend chip design

- Provides clock signals to different elements: integrated ADCs, DSP, Gigabit link
- Same 65nm technology for the block and the ASIC

Also open to be integrated to other ASIC designs for EIC

- If same TSMC 65nm technology
- If block input frequency range compatible with the ASIC specifications
- Full layout of the block directly provided, ready to be implemented in the design
- Slow-control registers to be connected to the block
- Freely available for EIC applications, details of the agreement to be discussed directly with interested groups, including documentation and reasonable support
- Public advertisement to be done to the EIC community and to the HEP community about this project

Standalone PLL and/or clock fan-out ASIC

- Possibility to produce a standalone PLL ASIC based on this block, with fan-out capability if needed
- ASIC design to be adapted if more output clock signals required
- Also public advertisement foreseen to EIC in order to get expressions of interest
- Future production to be discussed with interested groups

BUDGET OF THE PROJECT

Nature of expenses	Cost (k$)	Group
Mini@sic ASIC submission	18	IRFU
Packaging and test cards	10	IRFU
TID radiation tests	5	Univ. Sao Paulo
SEU radiation tests	10	IRFU
Intern student (4-6 months)	6	IRFU
Travels for radiation tests	5	IRFU
Total	54	

	ASIC production	Tests	Radiation tests	Travels	Total
IRFU CEA Saclay	18 k$	16 k$	10 k$	5 k$	49 k$
U. Sao Paulo			5 k$		5 k$
	18 k$	16 k$	15 k$	5 k$	

TEAM OF THE PROJECT

IRFU CEA Saclay

- Damien Neyret (contact person)
- Pascal Baron
- Florent Bouyjou
- Olivier Gevin
- Fabrice Guilloux
- Irakli Mandjavidze
- Additional intern student to perform test measurements

University of Sao Paulo

- Wilhelmus Van Noije (contact person)
- Marco Bregant
- Hugo Hernandez
- Bruno Sanches