EIC generic R&D

Aluminium Flexible PCB (cable)

Fast timing (<10ps, <10μm) MAPS layer

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Aluminium Flex PCB (cable)

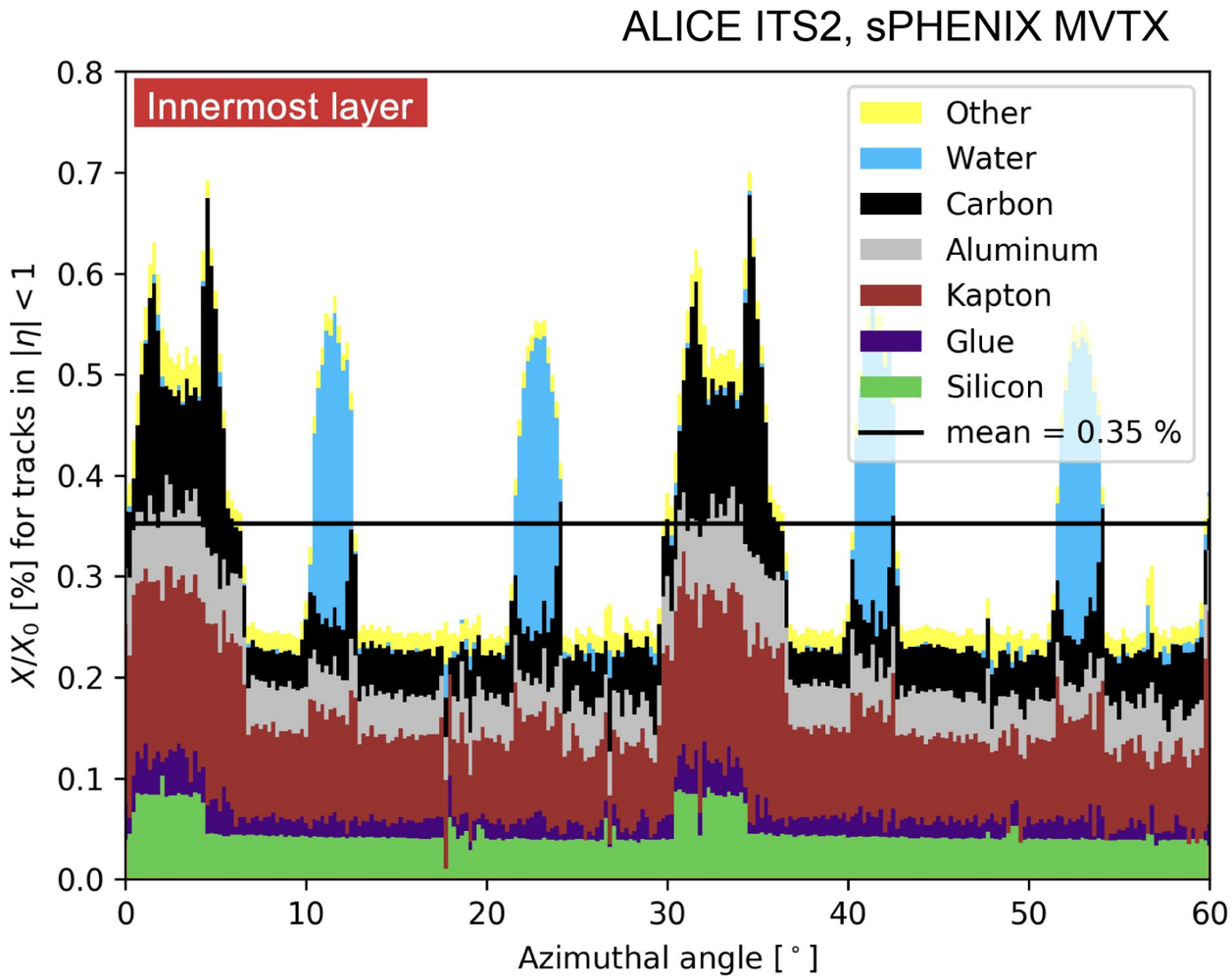
Radiation length:

$X_{0\ Cu} \sim 1.4cm$
$X_{0\ Al} \sim 8.9cm$ } factor 6

CERN
Kharkiv Institute

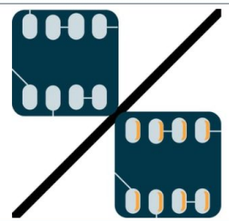
Explore companies:

- Hughes Circuit Inc. (CA)
- Qflex Inc. (CA)
- Omni Circuit Boards Ltd. (BC, Canada)



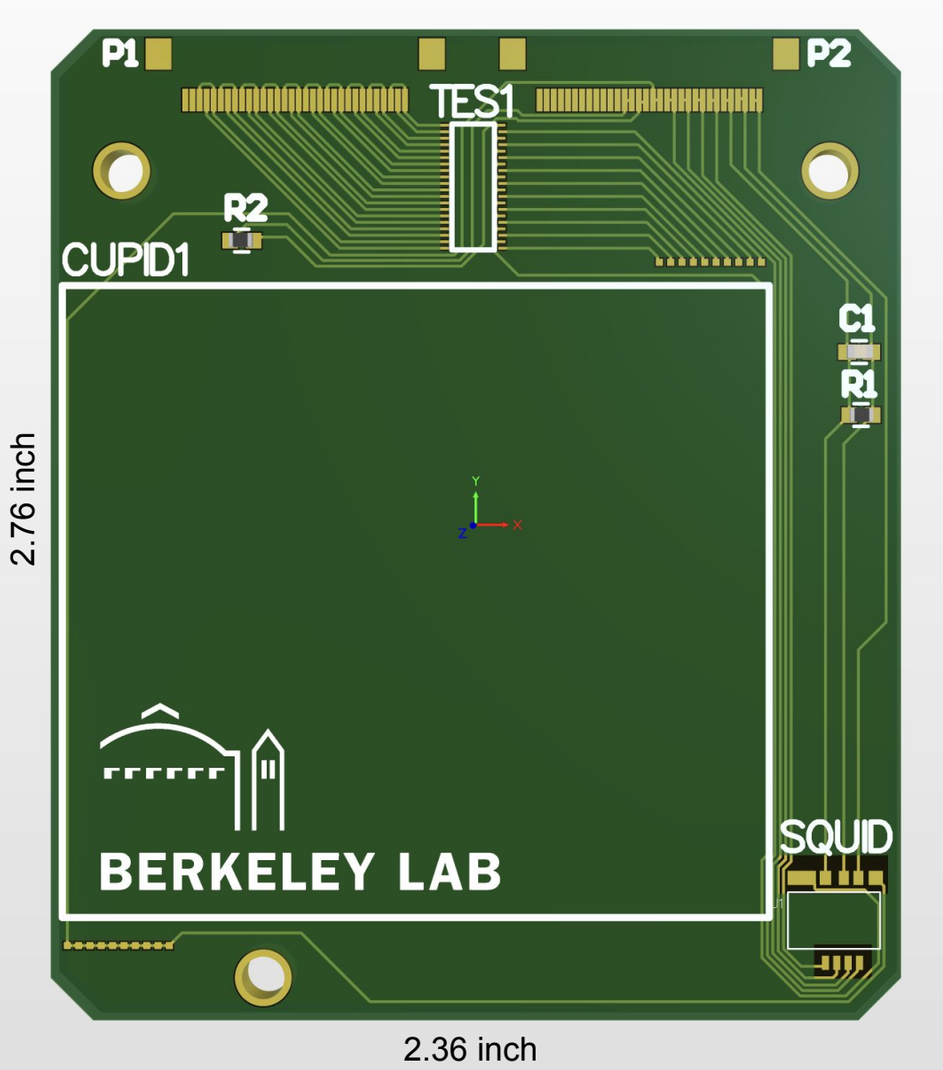
Aluminium Flex PCB (cable)

Characteristics - 2 Layer Boards

Specifications		Plated Through Hole Version	Non Plated Through Hole Version
Aluminum thickness		20µm, 22µm (lower or higher upon request)	30µm
Aluminum alloy		Pure aluminum	AL 3003 H18
Base material type		AD1000 - Rogers 4350B - Rogers P96/P26 - Isola	FR4
Base material thickness		As per base material type offerings from manufacturer	0.009"- 0.031"
PCB final surface finish		Bare Aluminum / Aluminum with selective copper	

https://www.omnicircuitboards.com/

Aluminium PCB example



2 layer

Finished PCB Thickness: .025"

Finish: Aluminium **Hard Gold:** No **Laminate:** FR4 **Ext Cu/Plated Cu:** Oz/Sq ft **Solder Mask:** Top Green

Silkscreen: Top White

Holes per Board: 3 **Plated Slots:** 0 **Unplated Slots:** 0 **Min Trace:** 0.008" **Min Space:** 0.007"

Min Hole: 0.118" **Max Plated Hole:** 0.118" **Route:** Single **Aluminium Plate:** No **Internal Build AI:** SK-LM-MT5305u40-6Xf2116MR-ccU9

NRC (tooling) cost: $210.00

10 boards @ $109.00 per board

Kapton (Polyimide) is available (P96/P26 from Isola)

https://www.omnicircuitboards.com/

Aluminium Flex PCB (cable)

Aluminum conductors for existing vertexing instruments came from:

- CERN
- Kharkiv Institute

Commercial sector is developing closely related capabilities driven by applications in Quantum Computing and other interests; explore possibility to commercially manufacture flex PCB for EIC tracking / vertexing subsystem and reduce risk(s),

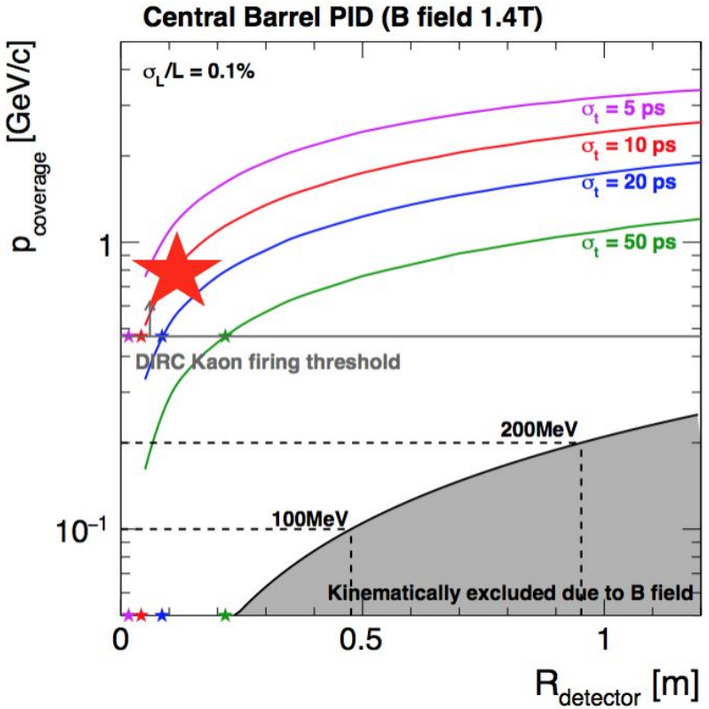
Request: 15 k$ in seed funds (12.5k$ material + 2.5k$ travel)

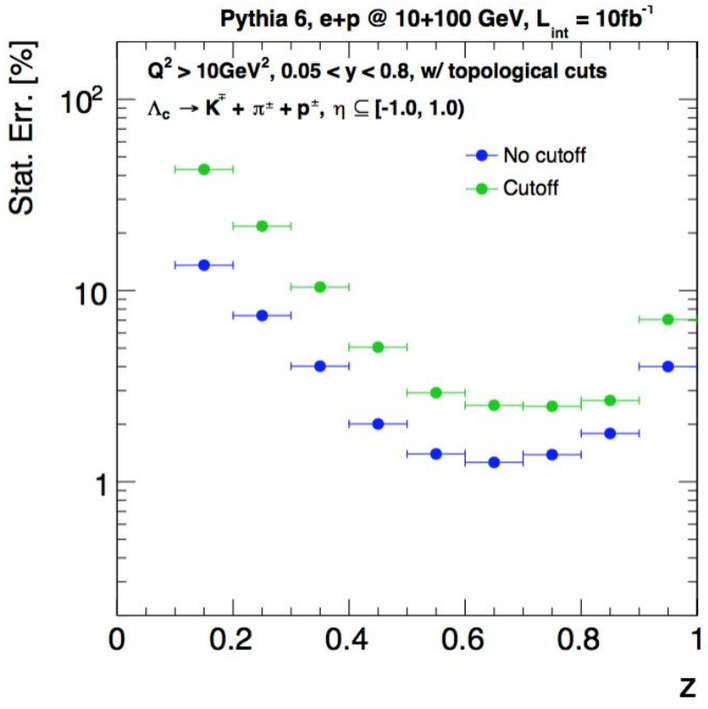
Deliverables: manufacturability & accurate cost estimate at scale

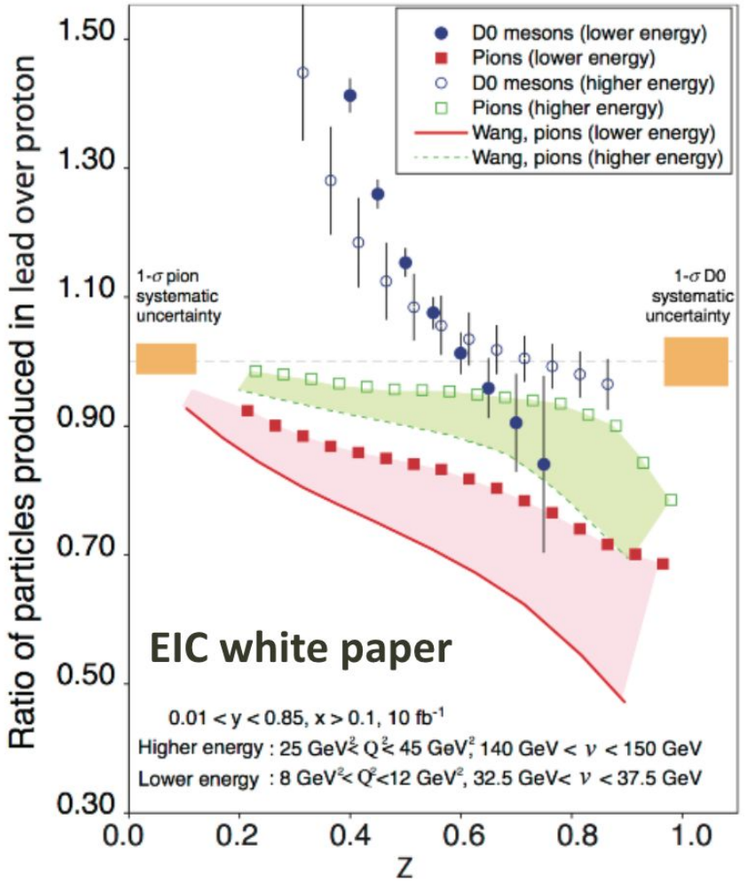
MAPS with 10ps timing, 10μm resolution

Hadronization of charm-quarks is a driving motivation for vertexing and time-of-flight (TOF) capabilities,

Integration of both capabilities in a single subsystem will reduce material, can improve performance, and will provide technological complementarity to the current EIC concepts.



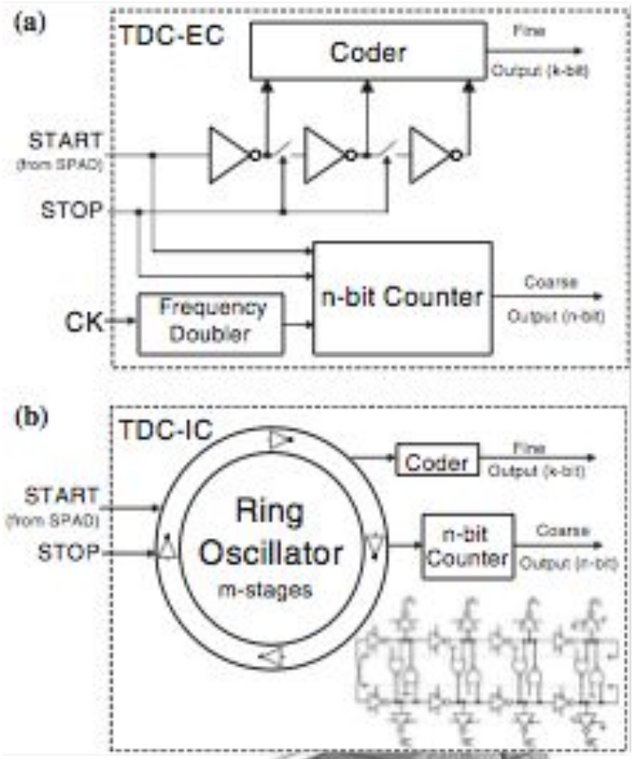


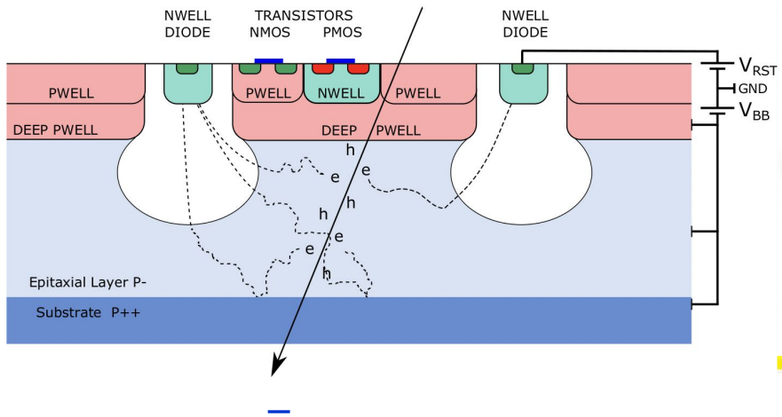


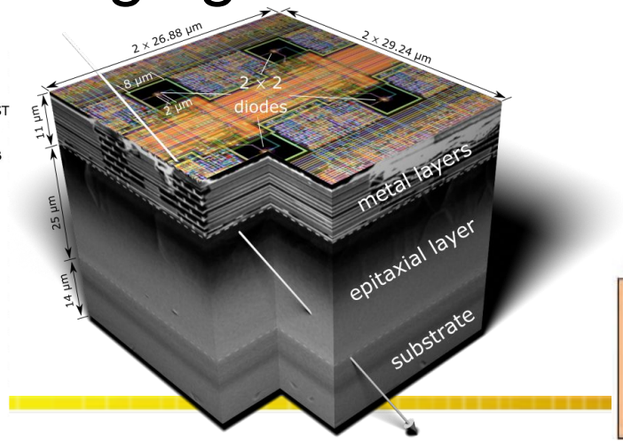
For example, 10ps TOF at 0.1m will improve the statistical significance of Λ_c baryon by factor 2-3; this is considerably more compact than the 25ps at 0.5m AC-LGAD reference with similar capability.

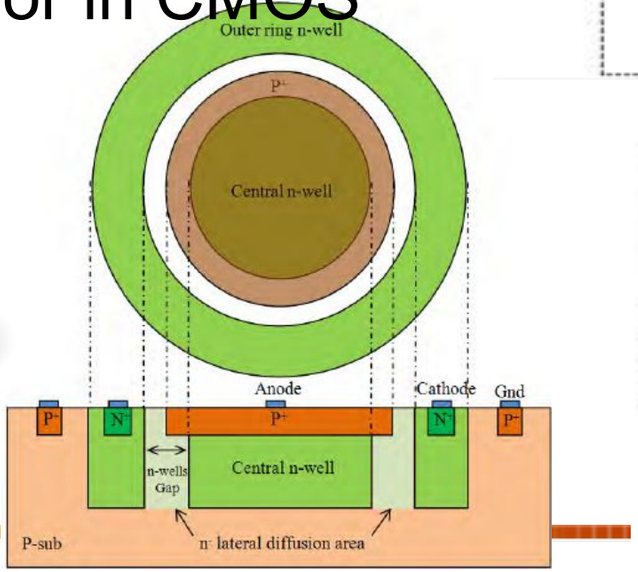
Add ~10ps timing resolution to pixel (2018 proposal)

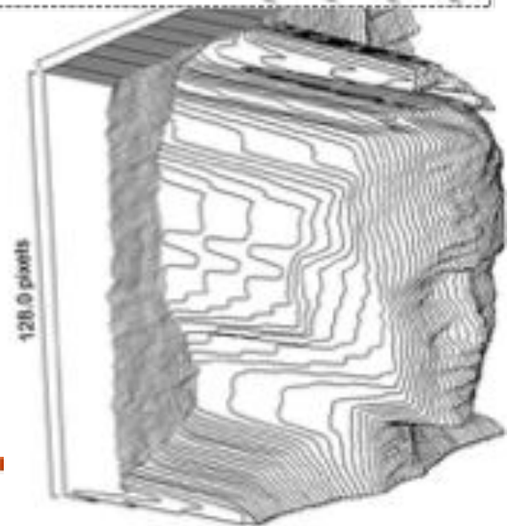
- Keep all nice features of MAPS (10μm spatial resolution)
  - Low radiation length, good radiation hardness
  - Commercial CMOS manufacturing process
- ~10ps timing: on the verge of possibility
  - Existing fast-timing circuitry implemented in CMOS
  - Existing fast-timing charge/light sensor in CMOS
- Ref: SPAD array 3D imaging sensor











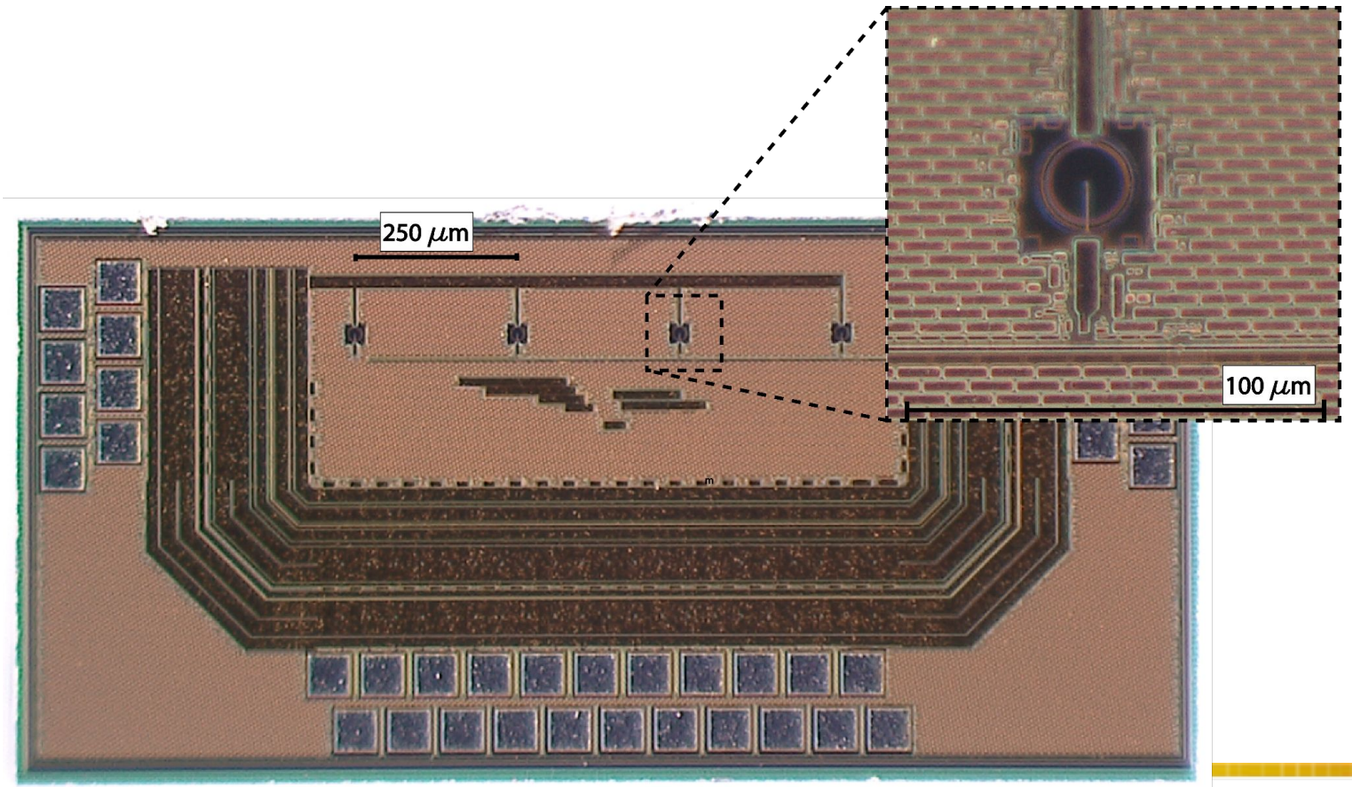
Recent advancement

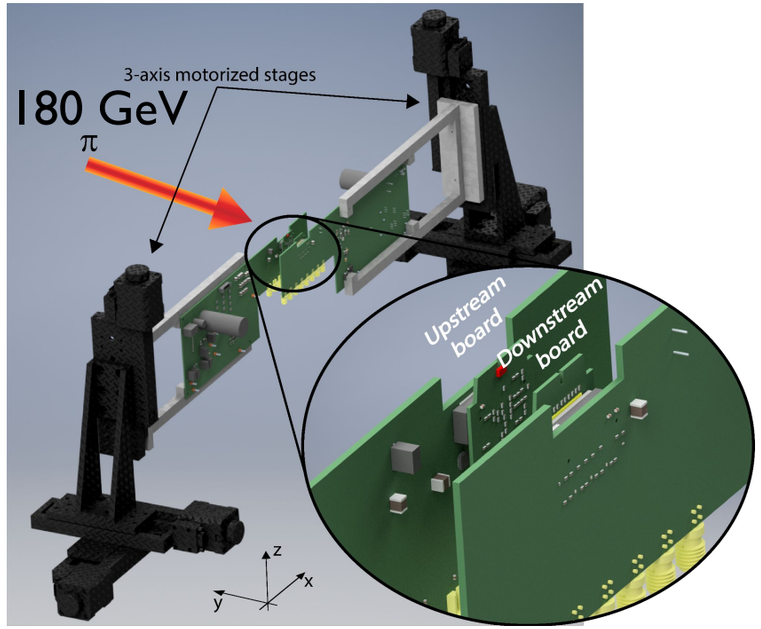
Sub-10 ps Minimum Ionizing Particle Detection with Geiger-Mode APDs

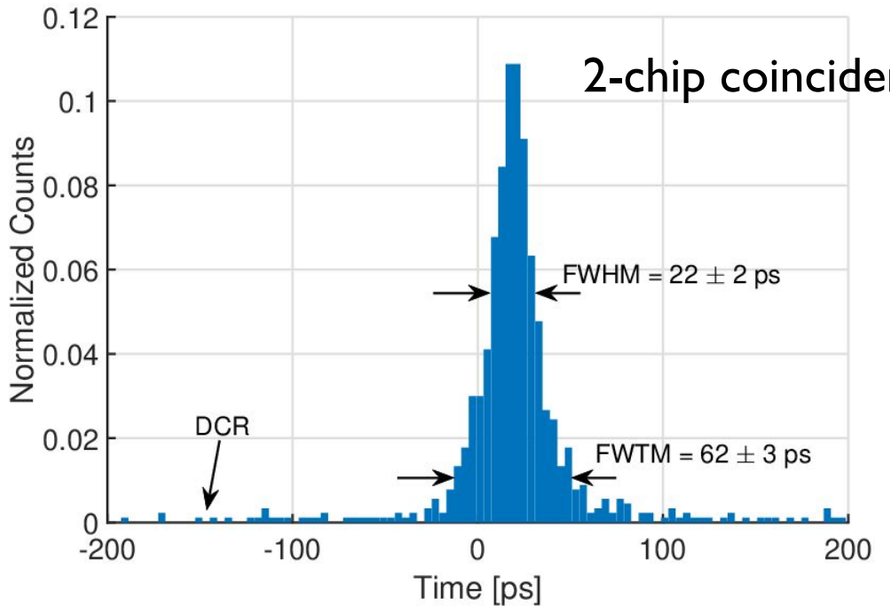
Francesco Gramuglia,[1,*] Emanuele Ripiccini,[1,*] Carlo Alberto Fenoglio,[1]
Ming-Lo Wu,[1] Lorenzo Paolozzi,[2,3] Claudio Bruschini,[1] and Edoardo Charbon[1]

[1] *École polytechnique fédérale de Lausanne (EPFL)*
[2] *University of Geneva*
[3] *CERN*

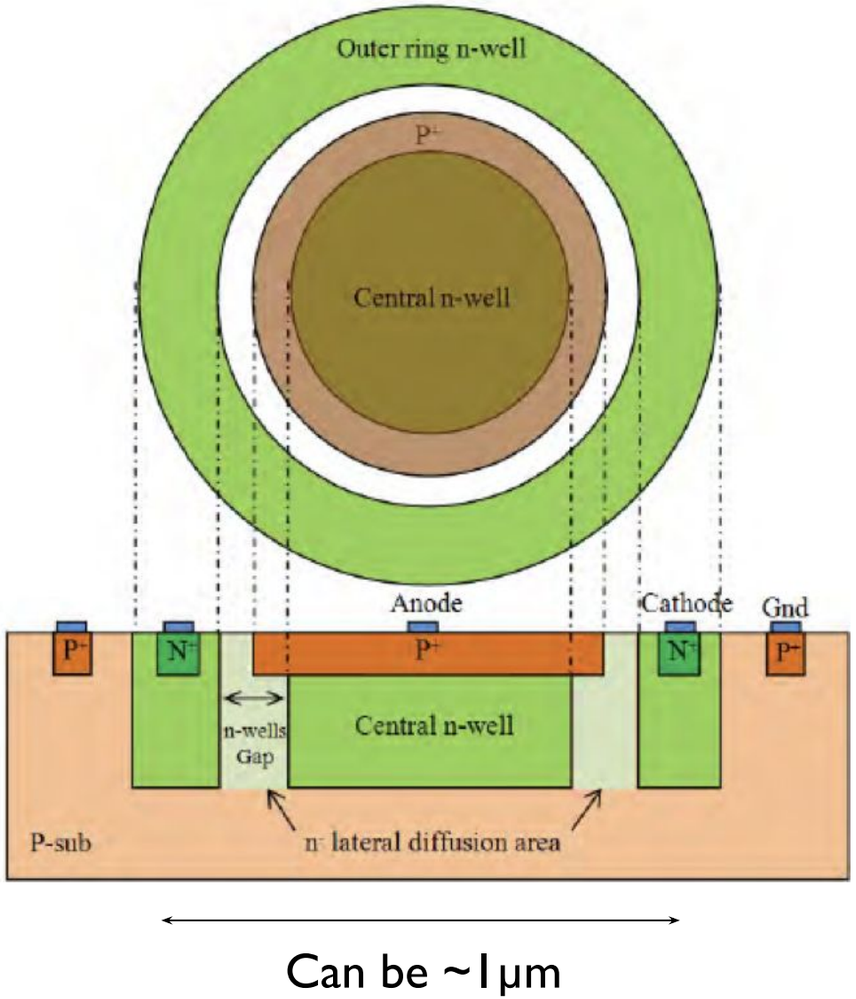
(Dated: November 22, 2021)



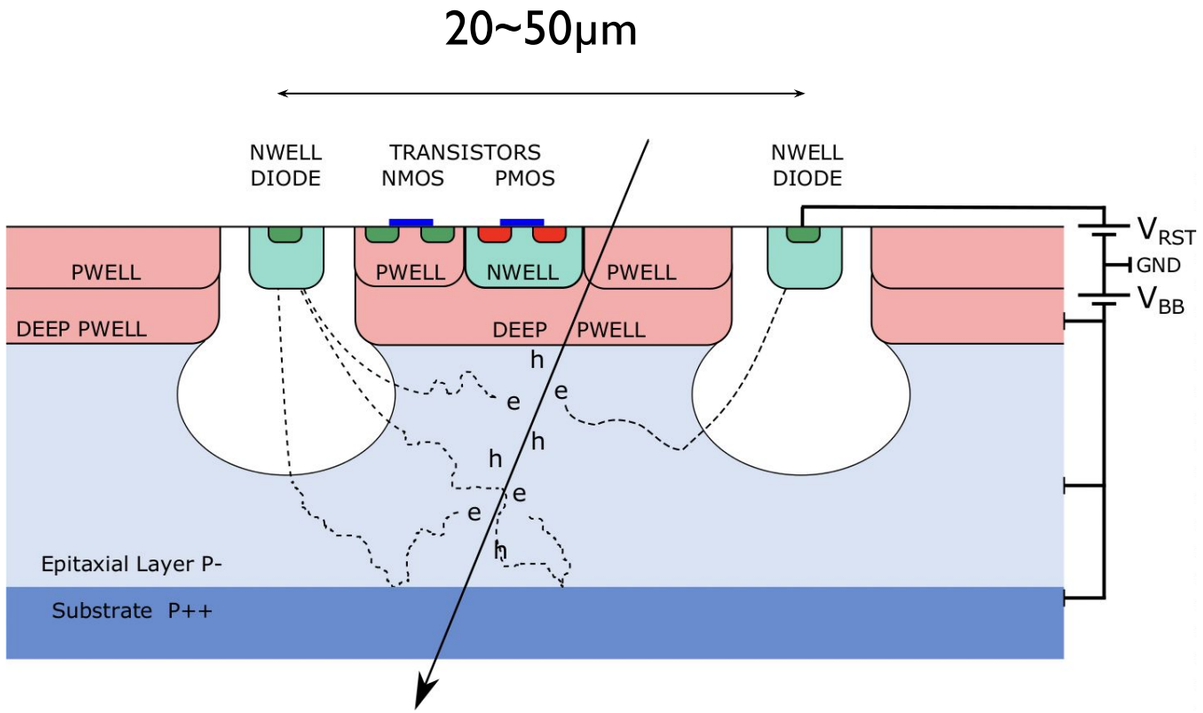




Avalanche Diode (distributed)

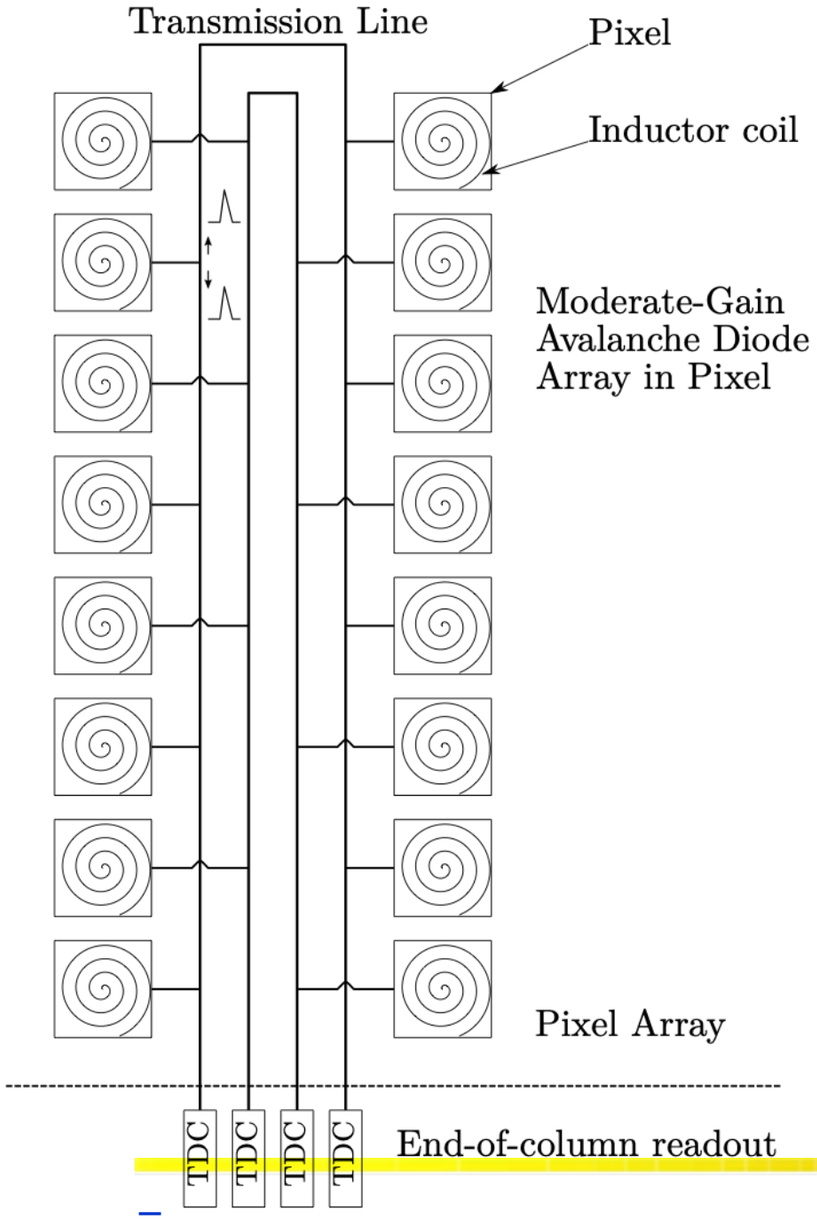


Array of tiny SPADs



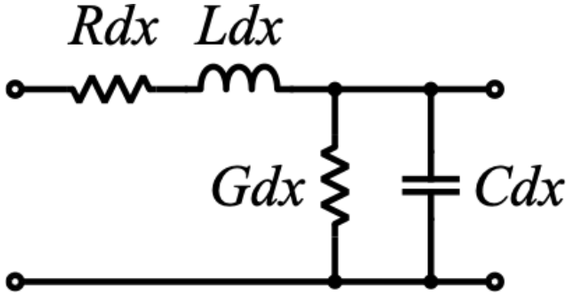
A Scaling Law for SPAD Pixel Miniaturization, Sensors 2021, 21(10), 3447

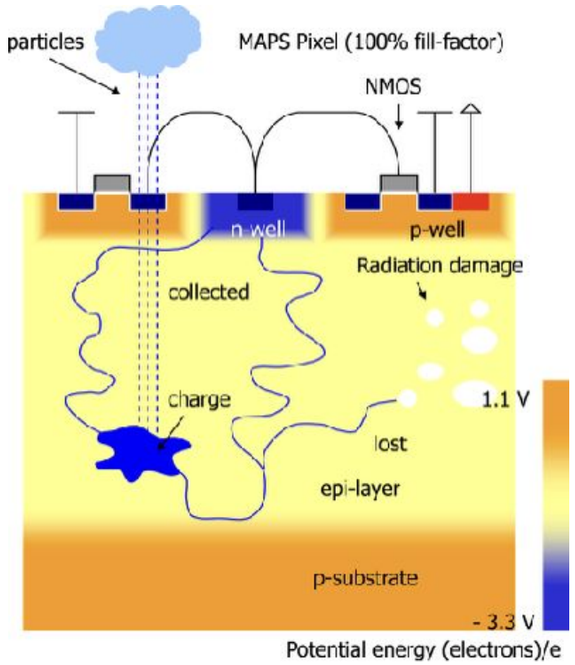
AD-TL pixel array and TDC readout

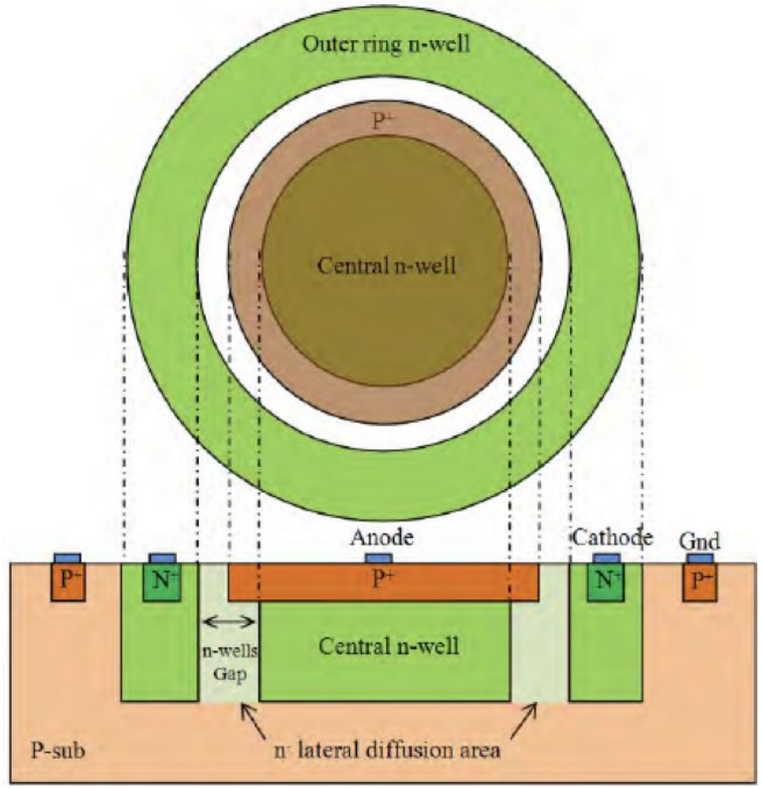


$$u = \frac{1}{\sqrt{LC}}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$







Avalanche Diode in CMOS

MAPS with 10ps timing, 10μm resolution

- What is the physics case for an ultra-fast MAPS beyond the existing RICH and LGAD technology?
- What is the effective fill factor of the SPAD array - how closely can they be packed?
  - A large array of tiny SPADs with sub-charge cloud size spacing. The first one gets charge fires.
- Dark noise control - do they have to be cooled? How much material and power would this use?
  - To be explored. Split SPADs onto many separate delay lines allow coincidence and dark count rejection.
- Charge sharing - how would multiply hit SPADs affect the transmission line scheme?
  - Split SPADs onto interleaved delay lines.
- Regarding the TDC: A low power, psec TDC is very difficult to design, hence will probably dominate the power. Will the power consumption become problematic when a realistic TDC is considered?
  - TDCs should dominate power. TDCs are placed at the edge of the chip, which allow concentrated cooling. Many good designs have been demonstrated.