Silicon Tracking Topic 1: Embedded MAPS R&D

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EIC generic R&D preliminary presentation meeting

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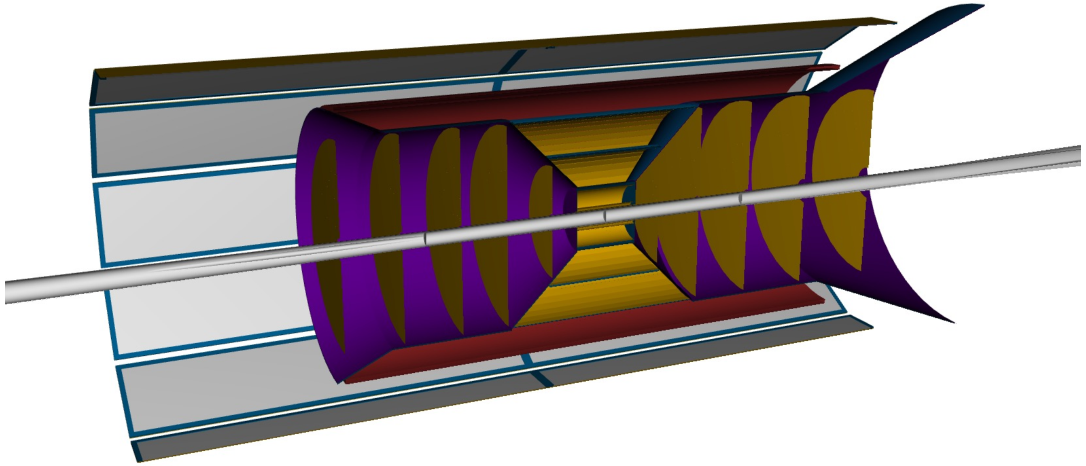
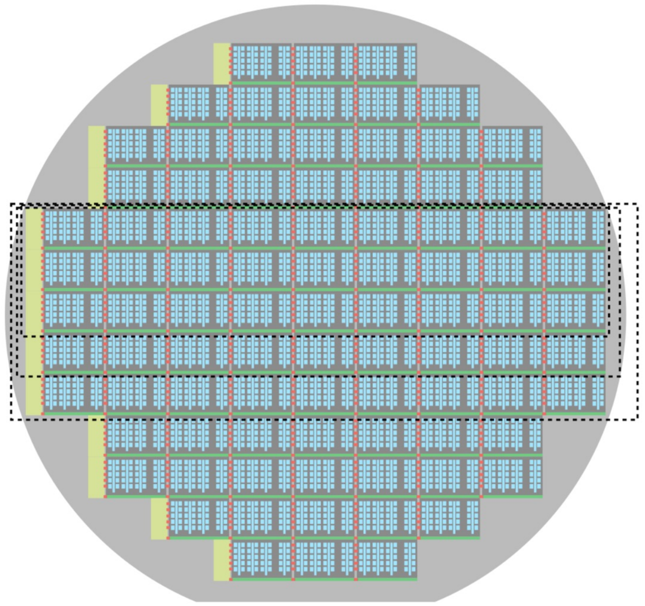
EPIC Silicon Vertex & Tracking Detector

- EIC science program requires a large acceptance vertex & tracking detector with high granularity & low material budget → MAPS
- EPIC detector based on 65 nm MAPS technology
  - Starting from ITS3 sensor design
- ITS3-like layers (0-2)
  - Re-use ITS3 sensor as is
  - Adapt to EIC radii
- EIC variant for staves & discs
  - EIC Large Area Sensor (LAS)



65 nm MAPS

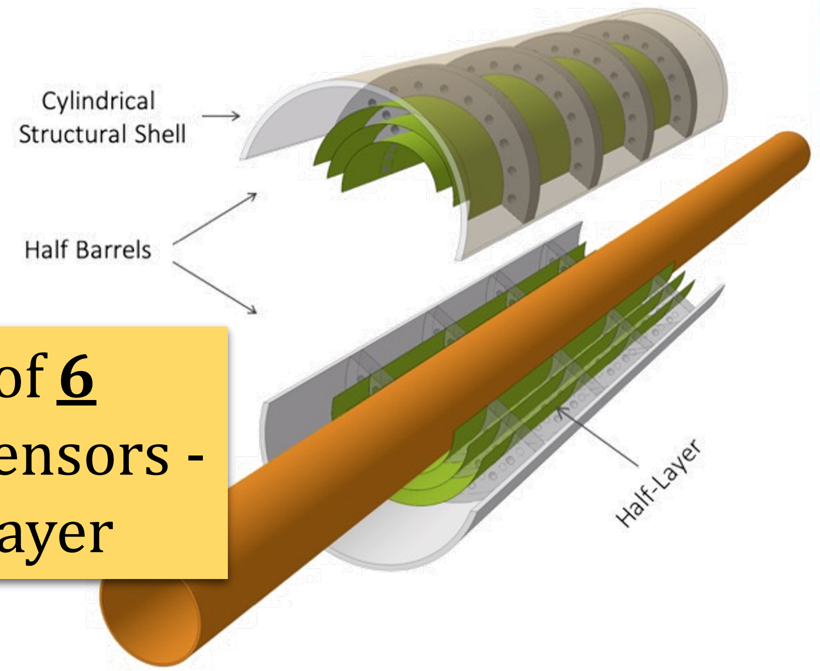


- ALICE ITS3 MLR1: 2021+
  - 65 nm process verified
- ALICE ITS3 ER1: submission end of 2022
  - Stitching verification & first yield information ← **Big unknown!**

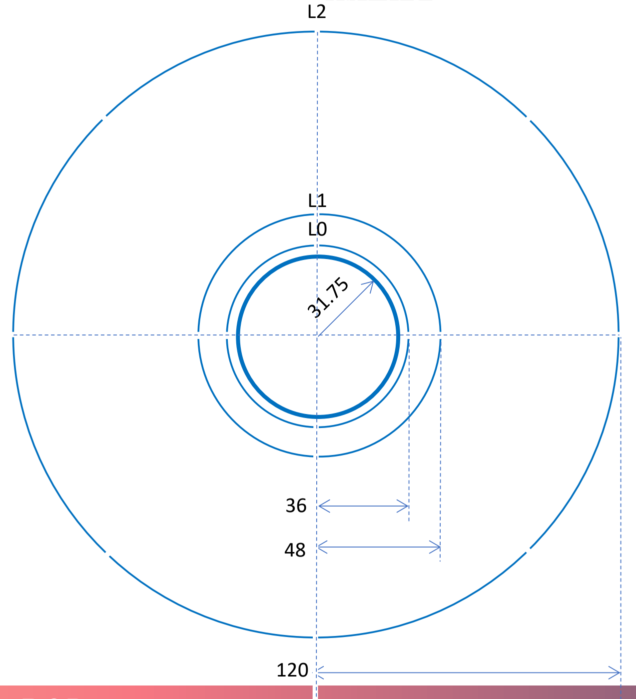
- Open questions:
  - What changes need to be made if yield is low?
  - Power distribution over the stitched sensor

From ALICE ITS3 to EIC

- ITS3 sensor reticle size will be optimized for ALICE radii
- EIC radii larger → geometry needs to be adapted
- Some mechanical challenges still to be thought out
  - Lose some of the structural support from curvature
  - What is the stress/strain on silicon?



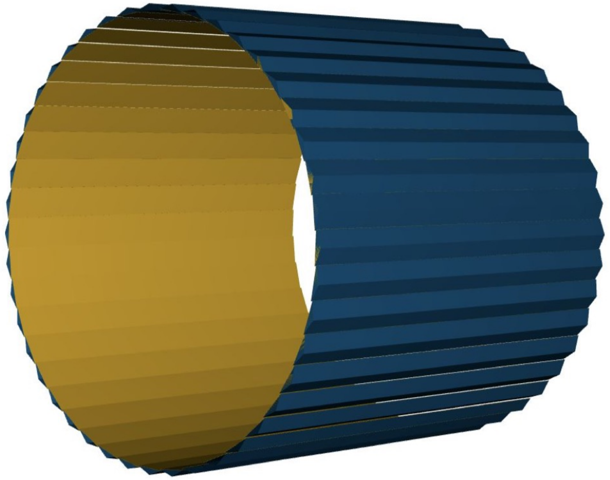
Total of **6** stitched sensors - 2 per layer

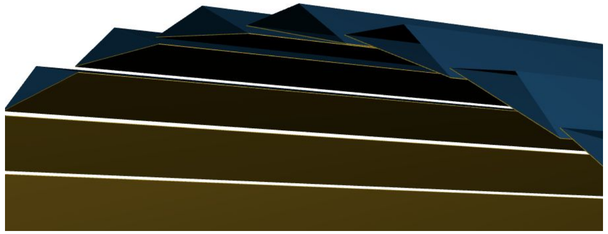


Option for EPIC layers 0-2

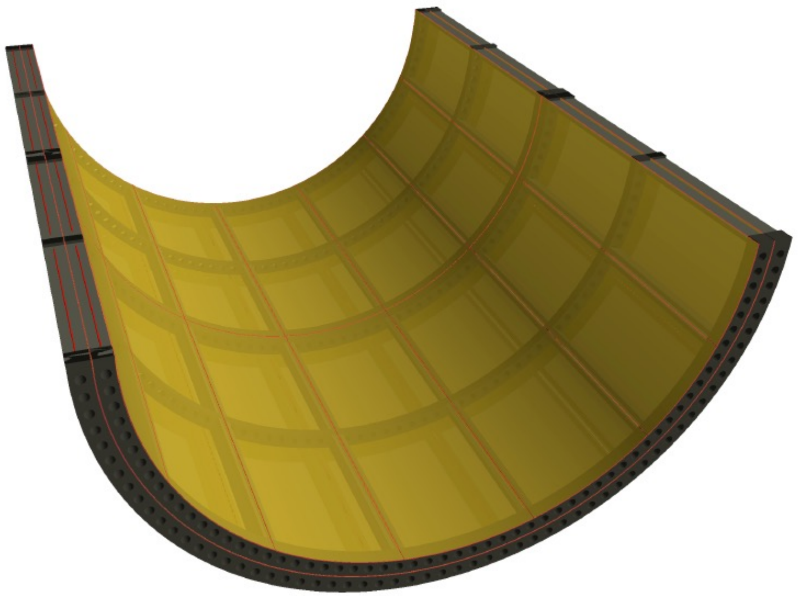
Total of **16** stitched sensors
Layers 0, 1: 4
Layer 2: 8

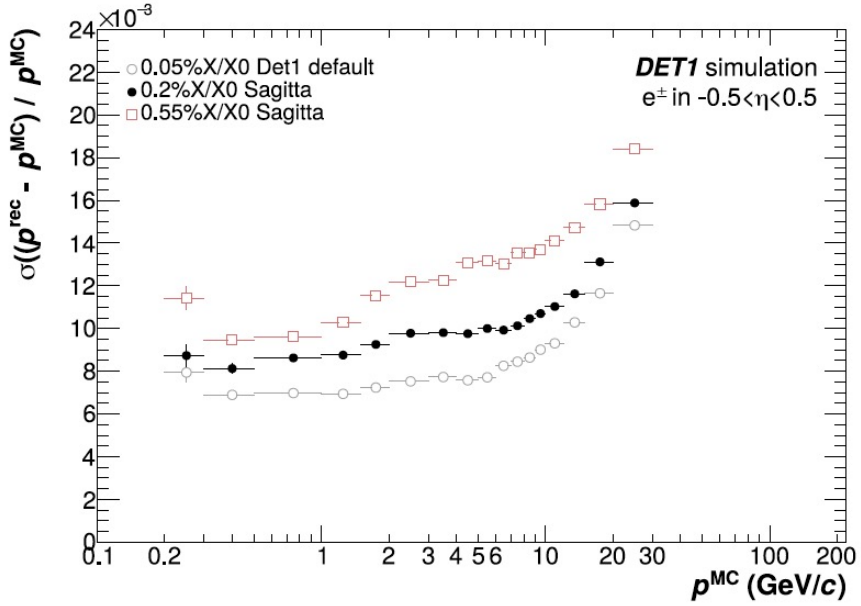
Staves & discs



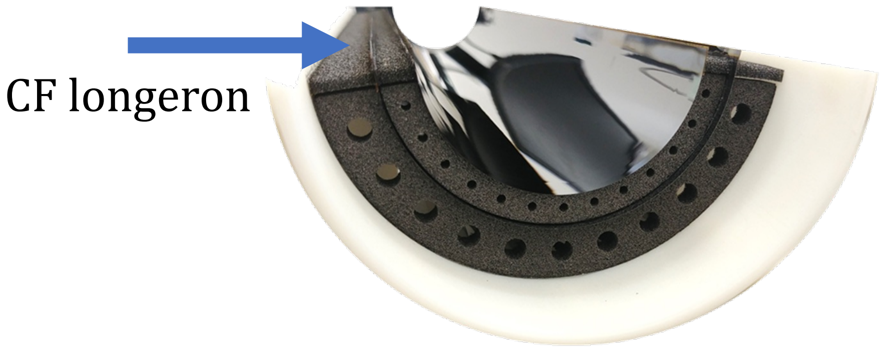


- Material budget an issue for tracking
  - Longer sensors mean more material (power, support)





R&D Motivation



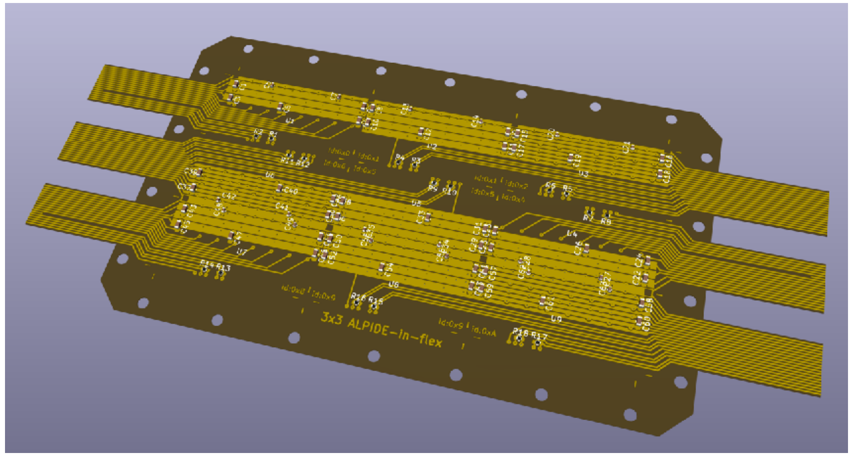
- Alleviate deformation expected from carbon foam longerons
- Reduce mechanical strain to the bare silicon
- Sagitta/Outer layers: Planar staves → larger, more cylindrical barrel structures
- Overcome possible weakness in power distribution network in 65 nm process

Risk reduction for detector 1, options for detector 2

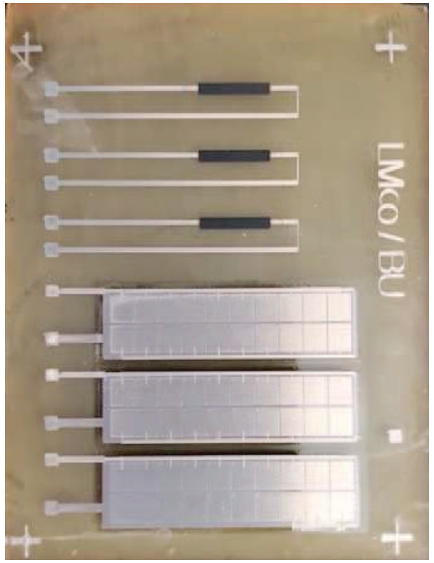
Additive manufacturing

- Power distribution from edge along entire stitched sensor not yet verified
- Printing of dielectric & metal patterns directly on the silicon
  - **Risk reduction for vertex layers**
- Would be a simpler, lighter, & more adaptable layout than separate power bus or FPC

Aerosol-Printed Highly Conductive Ag Transmission Lines for Flexible Electronic Devices



Example of ~ 10 x 5 cm sensor matrix connection trace layout



Fully Additive Manufacturing of Passive Circuit Elements using Aerosol Jet Printing

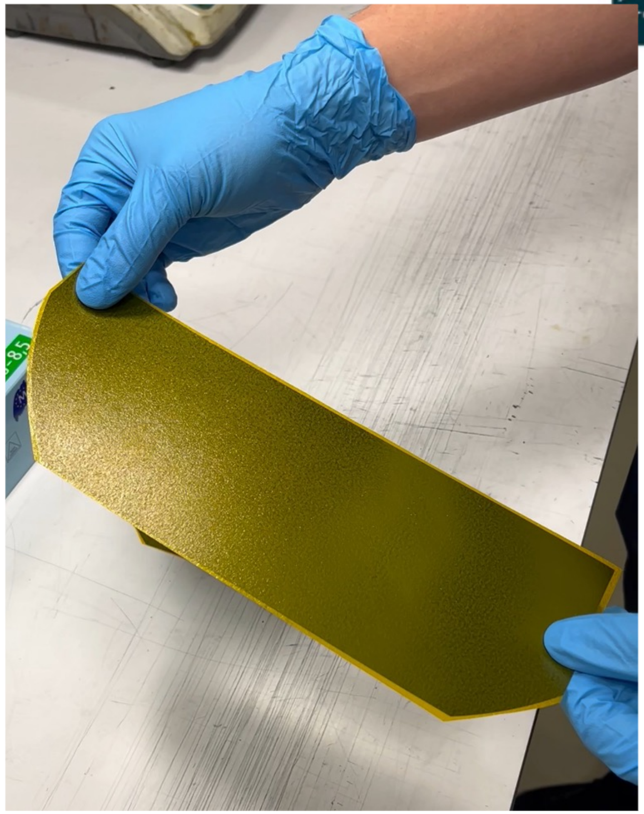
Additive manufacturing: vendors

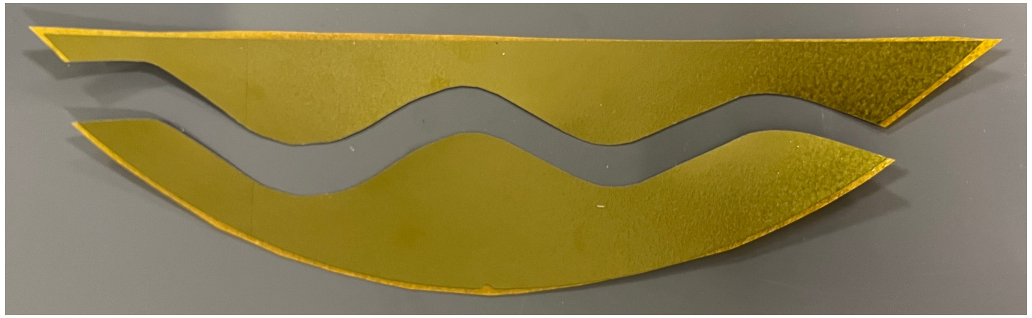
- CNR-IOR Nano- and Micro-fabrication Laboratory in Trieste
  - Active collaborators of the University of Trieste, INFN Trieste proponent institute on different R&D
  - Experienced in evaporation and deposition of conductive materials on different substrates
- Printed and Flexible Electronics lab at the Silicon Austria Labs (SAL) research center in Villach (Austria)
  - Established first exploration of capabilities
  - A series of printers based on ink-jet and aerosol-jet techniques are being commissioned for the development of deposited re-distribution layers on a wide variety of substrates
- Aerosol Printing & Photonic Curing Laboratory at the University of Brescia (Italy)
  - Established first contacts for possible collaboration
  - Offers similar capabilities in the field of 3D additive manufacturing based on aerosol-jet printing

Silicon lamination

- [ORNL Manufacturing Demonstration Facility]
    - ORNL on-site facility
        - Have been used by the ORNL group members previously
    - Conversations with staff are ongoing

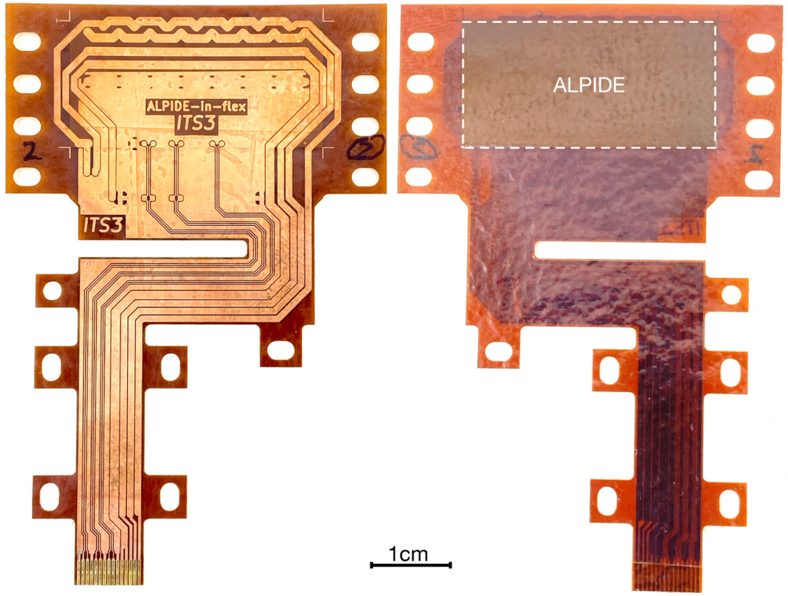
- Similar process ongoing at CERN

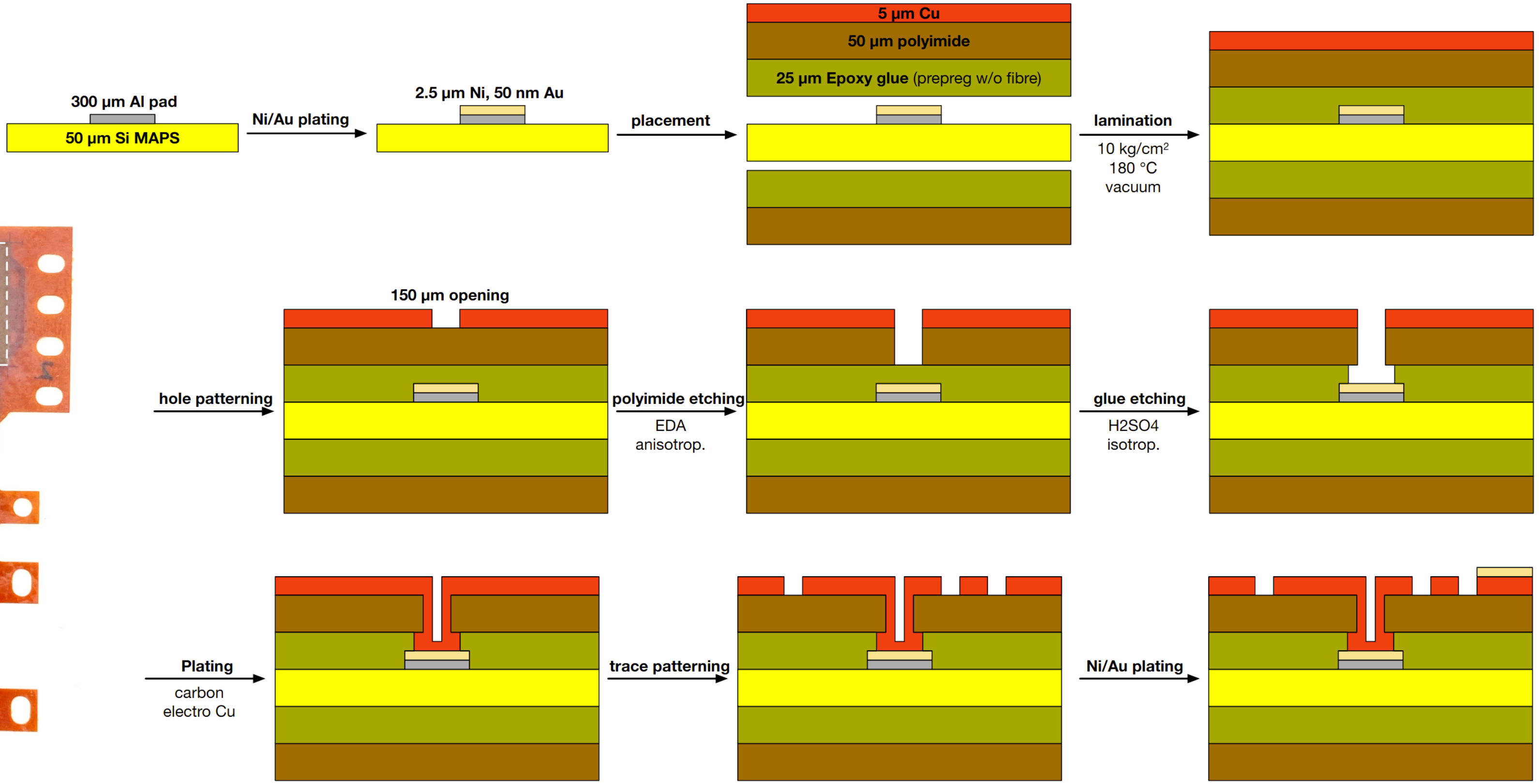




Improved mechanical resistance with low material: 0.1% X/X_0 silicon + kapton

“MAPS foil”

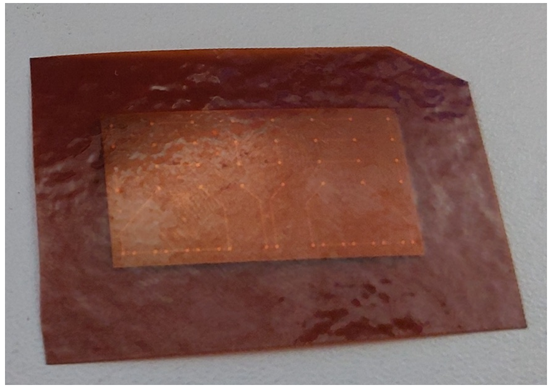




https://doi.org/10.1016/j.nima.2022.167673

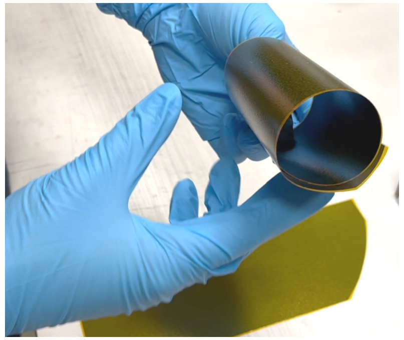
- Kapton foil lamination process developed for thinned MAPS
- Demonstrated successfully on single ALPIDE sensors (ITS2)

FY23: Single reticle size lamination



- Validation of the lamination process
- Glue variations
- Variations of thickness?
- **FY23 deliverables: Embedding small, ALIPDE-sized silicon mock-ups**
  - **Production of test pieces to be used in mechanical & cooling tests**
  - **Written report (in conjunction with large area mock-ups)**

FY23: Large scale lamination



- Thickness, glue, etc. based on validation from single reticle
- Large, stitched size sensors
- Staves made from multiple single or stitched sensors
  - How to align & place them
  - Additional mechanical stress?
- **FY23 deliverables: Embedding large scale silicon mock-ups**
  - **Production of large scale (stave size) test pieces to be used in mechanical & thermal tests**
  - **Written report (in conjunction with single reticle mock-ups)**

FY23: Laminated sensors: mech & thermal

- Thermal studies of the laminated sensor – with & without cooling
- How does the material deform under air flow?
- Laminate a sensor to hold a curved shape
- **FY23 deliverables: Mechanical and thermal properties of laminated sensors**
  - **Written report detailing the mechanical and thermal properties of the laminated sensor**

FY23: Additive manufacturing

- Evaluate dielectric & conductive aerosol/ink material properties & optimization of electrical characteristics
- Fabricate small size prototypes to study mechanical properties on curved silicon
- Extend to large-area prototypes to evaluate & improve process
- **FY23 deliverables: Additive manufacturing of power & data redistribution layers on thin large-area silicon**
  - **Written report detailing the electrical properties of the different additive manufacturing technologies**

Q1: Have initial thermal model studies already been done to explore feasibility & the need for thermal vias?

- No, to the best of our knowledge → Thermal tests are just beginning with the ALICE ITS3 collaboration on small size samples
- While Kapton (~0.1 – 0.8 W/m*K) foils transfer heat to a certain degree, it has not been investigated how well the sensors in this configuration can be cooled. We would perform a thermal evaluation of the sensors to determine the integrated cooling requirements of multi-sensor detector modules.
- The inclusion of thermal vias in the assembly, as well as different embedding options with larger thermal conductivity properties, like the printing of dielectric & metal patterns directly on the silicon, will be explored through ink-jet & aerosol-jet techniques

FY23 Request

- Laminated sensors
  - ORNL: labor & material for creating/validating lamination
  - LBNL: labor & material for mechanical & thermal testing
  - Staff & PD support will be provided in-kind
- Additive manufacturing
  - INFN: 0.5 FTE PD stationed at INFN Trieste & materials for AM evaluation, engineering & technical support will be provided in-kind

institute	cost in k$					total in k$
	mech. engineer	technician	postdoc	material	travel	
LBNL	32.4	57.6		5.0	2.5	97.5
ORNL	41.4	60.8		17.5	2.5	122.2
INFN			34.0	15.0		49.0
UTK						(in kind)
UCB						(in kind)
	73.8	118.4	34.0	37.5	5.0	**268.7**

Summary

- Laminated sensors have low material budget & provide added mechanical strength
- Additive manufacturing can provide industry tested ways to strengthen power and signal propagation
- **Want to mitigate risk to the project detector 1 and/or provide options for detector 2**