Simplified LGAD structure with fine pixelation

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Basic structure of LGADs

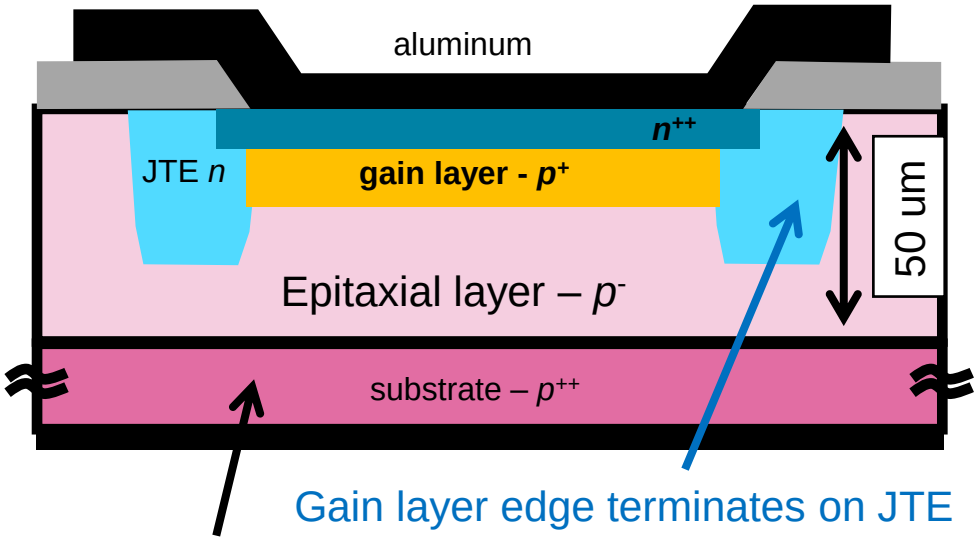
Low-gain Avalanche Diodes (LGADs) are Avalanche Diodes specifically tailored for the detection of mips in HEP

LGADs are 20-50um thick (only active volume!) as compared to hundreds of um of std strip/pixel sensors.
LGADs feature a p+-layer (gain layer) under the n+.
Depletion of the p+ gain layer creates intense Electric Field, high enough for electron impact ionization to occur.
Hole impact ionization ~ 0

→ LGADs operate before BreakDown (linear region)
→ gain ~ few 10s

Amplification is needed to have a good S/N when reading-out fast.

For mips: if the substrate is thin (~ 50 μm) and the gain is ~ 20 → signal is fast (~30 ps)



BNL, CNM, FBK, HPK, … do LGADs

Limits of LGADs

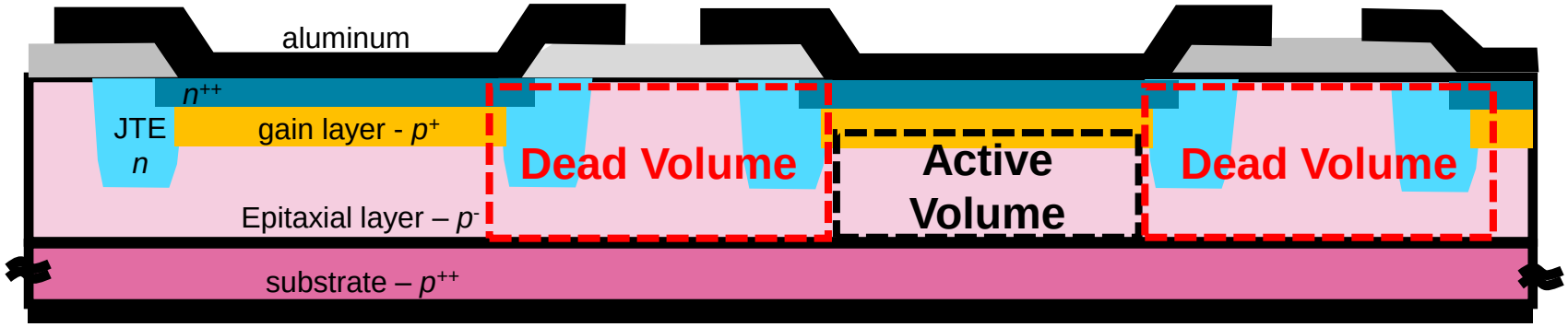
Lateral dimensions of Gain layer must be much larger than thickness of substrate, for a uniform multiplication.

Dead volume (gain~1) extends within the implanted region of the gain layer:

→ pixels/strips (pitch ~ 100 μm) with gain layer below the implant have a Fill Factor<<100% (Voltage dependent)

→ large pads are preferred (~ 1 mm); e.g., HGTD of ATLAS and MTD of CMS

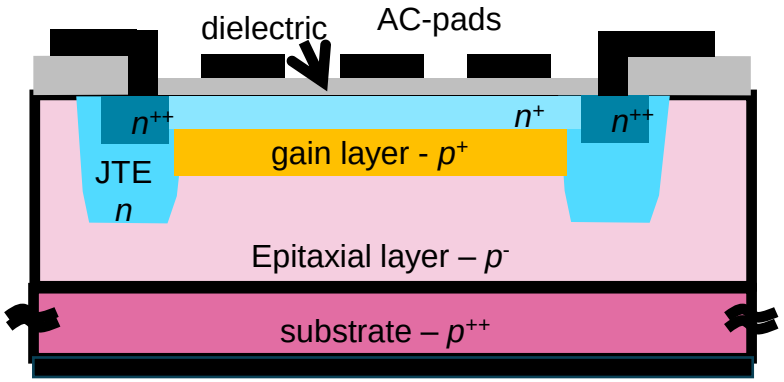
→ 4D detector not possible!!!

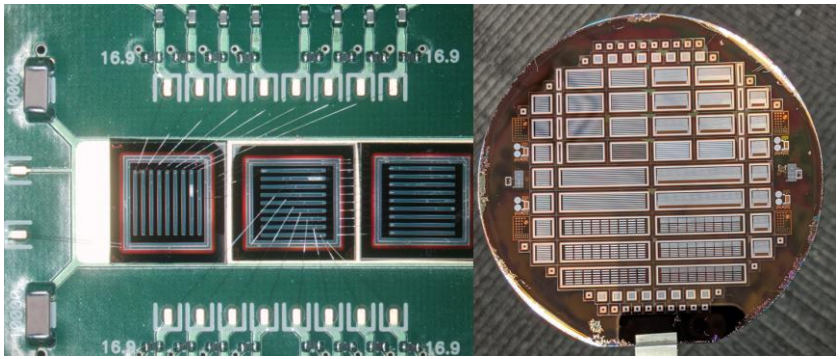


Towards a 4D detector

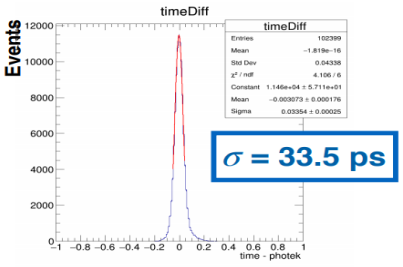
AC- LGAD

Modification of DC-LGAD
Fabricated @ BNL, FBK, HPK, CNM.

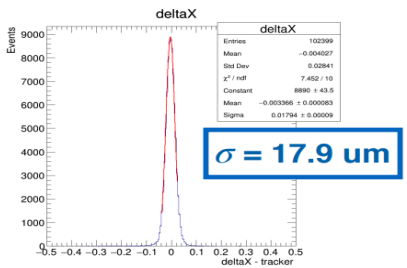




- Signal shared among several AC-pads, making occupancy high (only low event rate possible)
- Signal sharing can be used to fit hit position and hit time. Need also reconstruction algorithms.
- Optimization of several technology parameters (ρ_{n+} C_{AC}, …)
  → still ongoing
- Optimization of AC-metal needed, but pitch/resolution > 20
- High capacitance (long strips show slower signal) – difficult to measure at HF



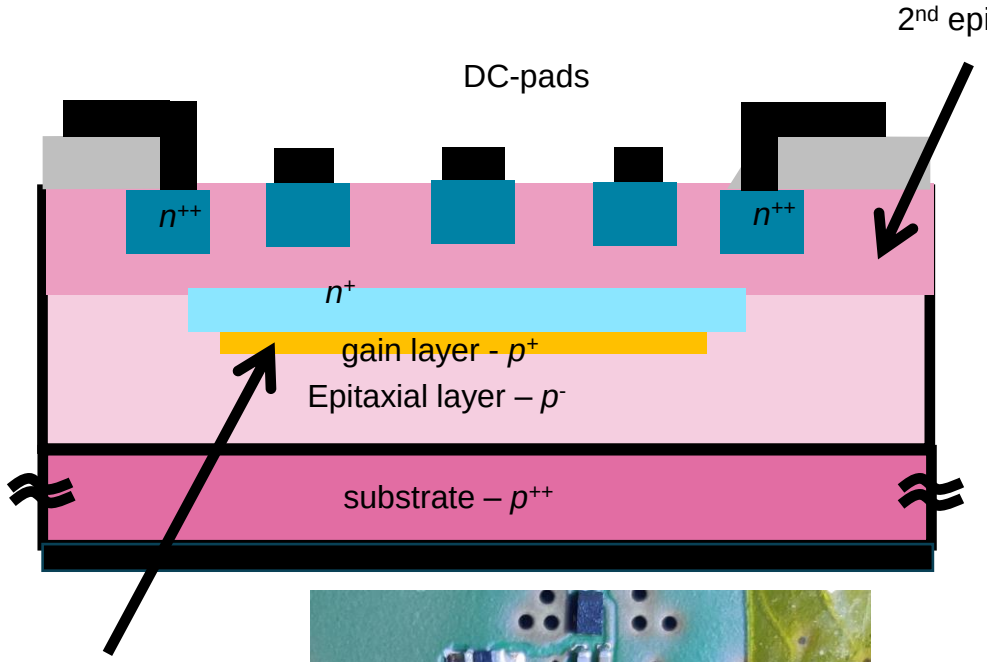
(σ_t can be lower if substrate is thinner – i.e. 20um – and gain larger)

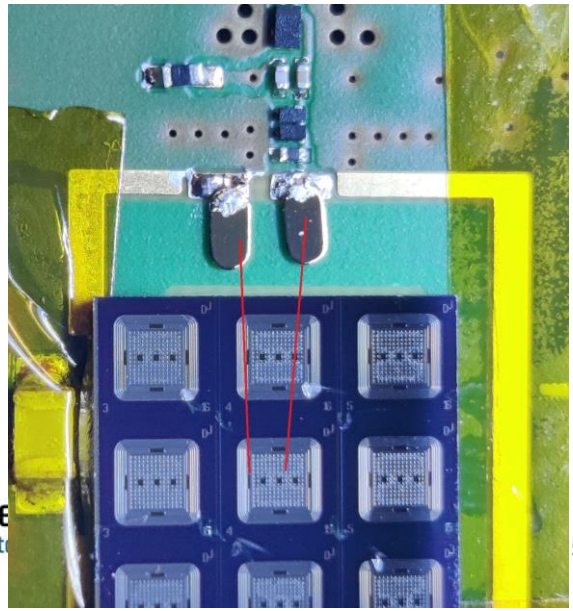


(σ_x includes the resolution of the tracker, ~ 10um)

Towards a 4D detector

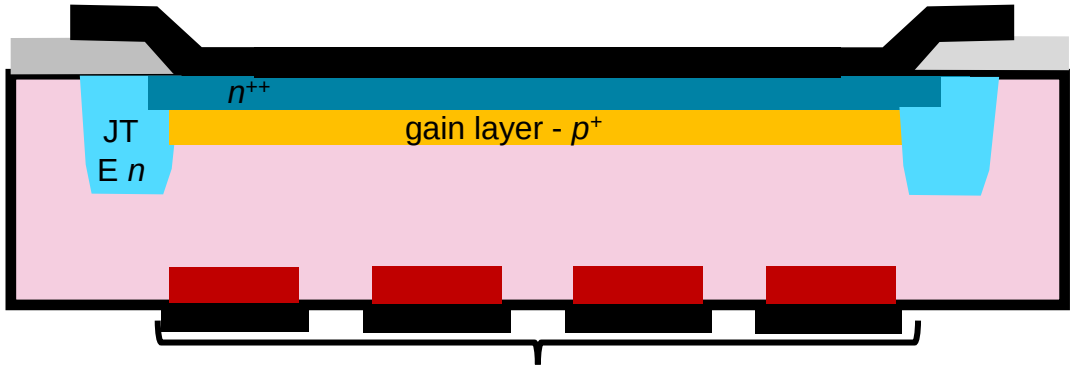
Deep-Junction LGAD



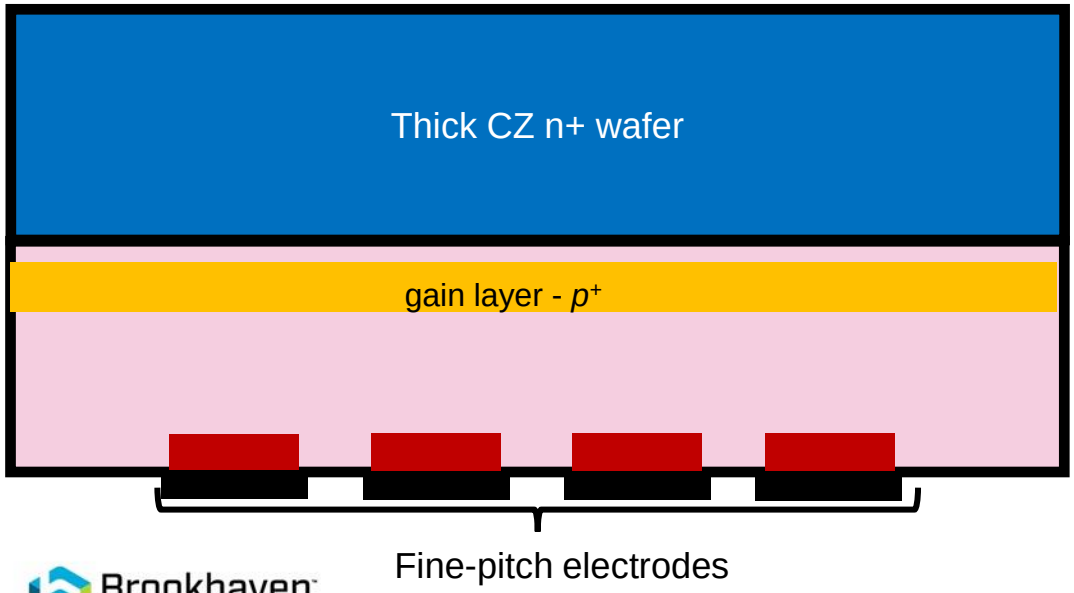


- Uniform junction is buried deep into the substrate
- Position resolution given by pitch, as in std pixel/strip detector
- Careful: slightly smaller electric field in the gain region in-between pads, but seems OK from TCAD simulations: to be verified
- Under development by UCSC, BNL and Cactus Materials: firs batch completed, under study.

A possible Solution:



Closely-spaced electrodes can be put on the opposite of the wafer (**i-LGADS**, CNM Barcelona),
but wafers must be thick to be processed.
→ not possible to associate fast-time information on a per-pixel level!

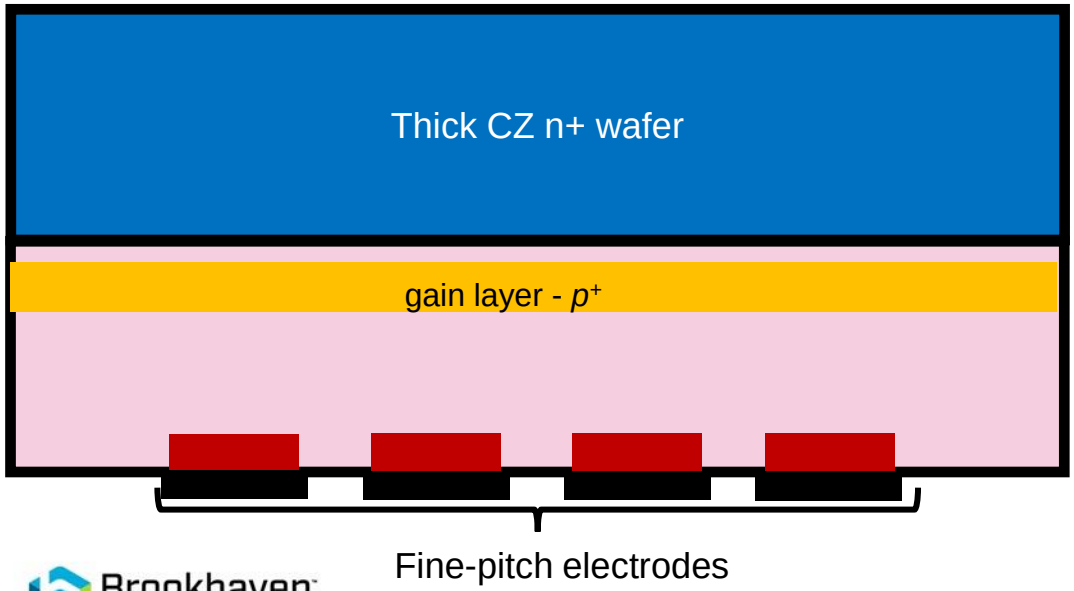


Or:
The n+ is replaced by a thick CZ wafers, acting as:
1. **mechanical support**
2. **ohmic contact**

Aim of the project

- Fabrication @ BNL (+ external vendors)
- Test @ UCSC + BNL

Requires wafer bonding + grinding/polishing
Not @ BNL, but still standard in industry (we are already collaborating with the vendor)



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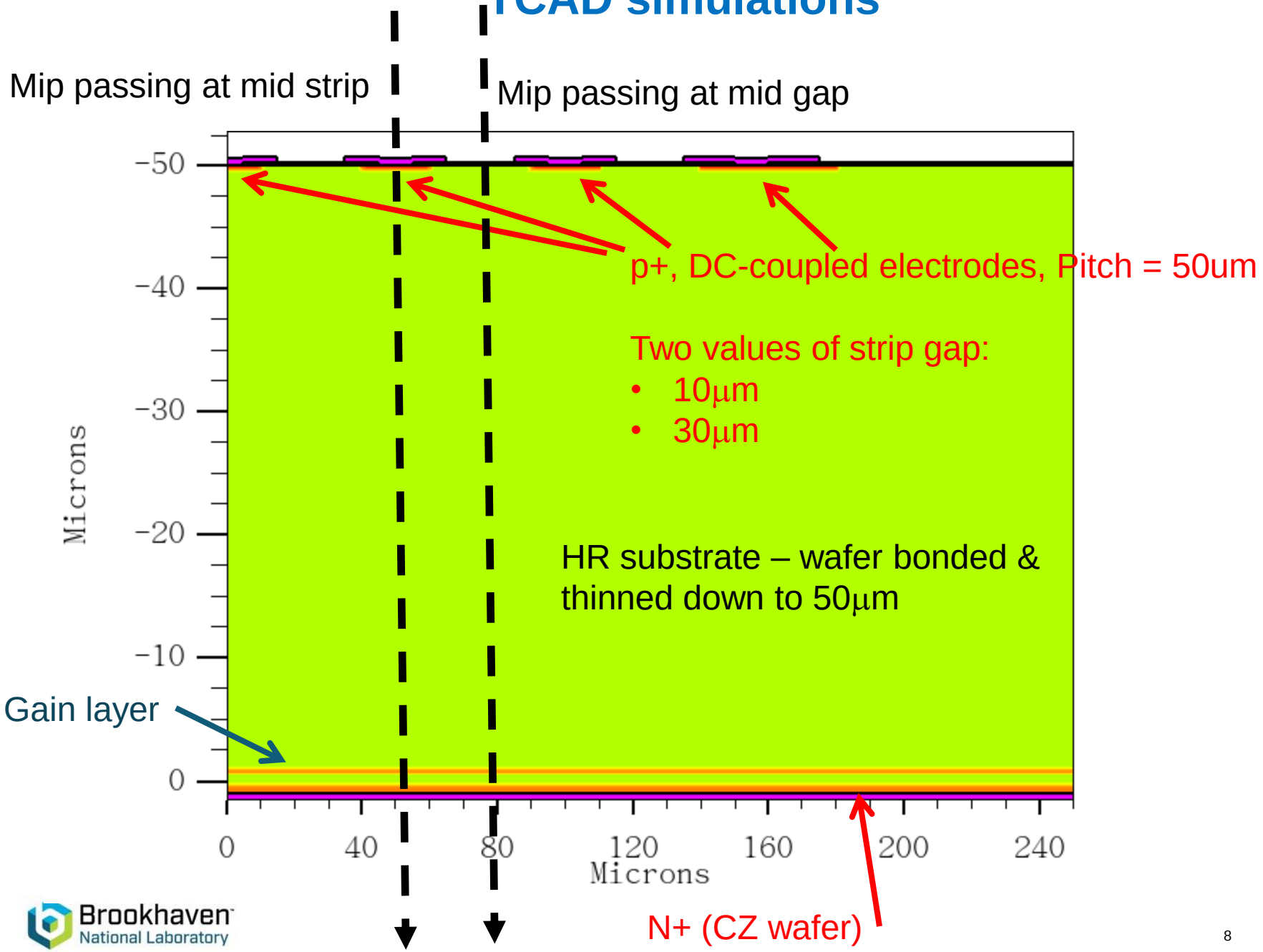
TCAD simulations



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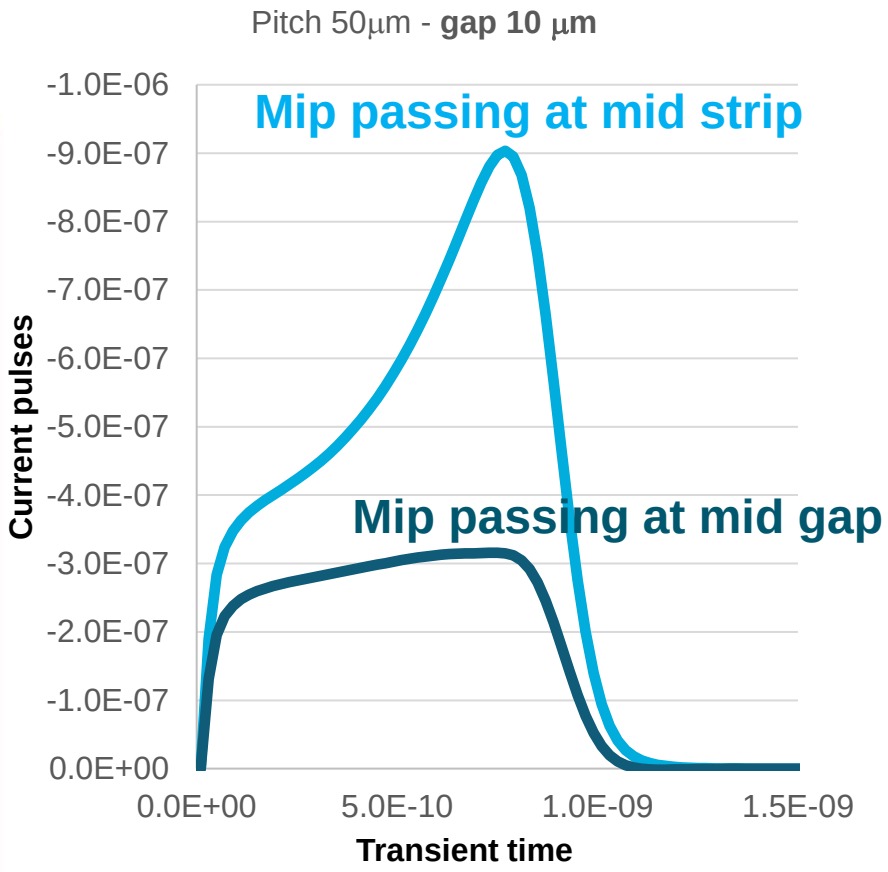
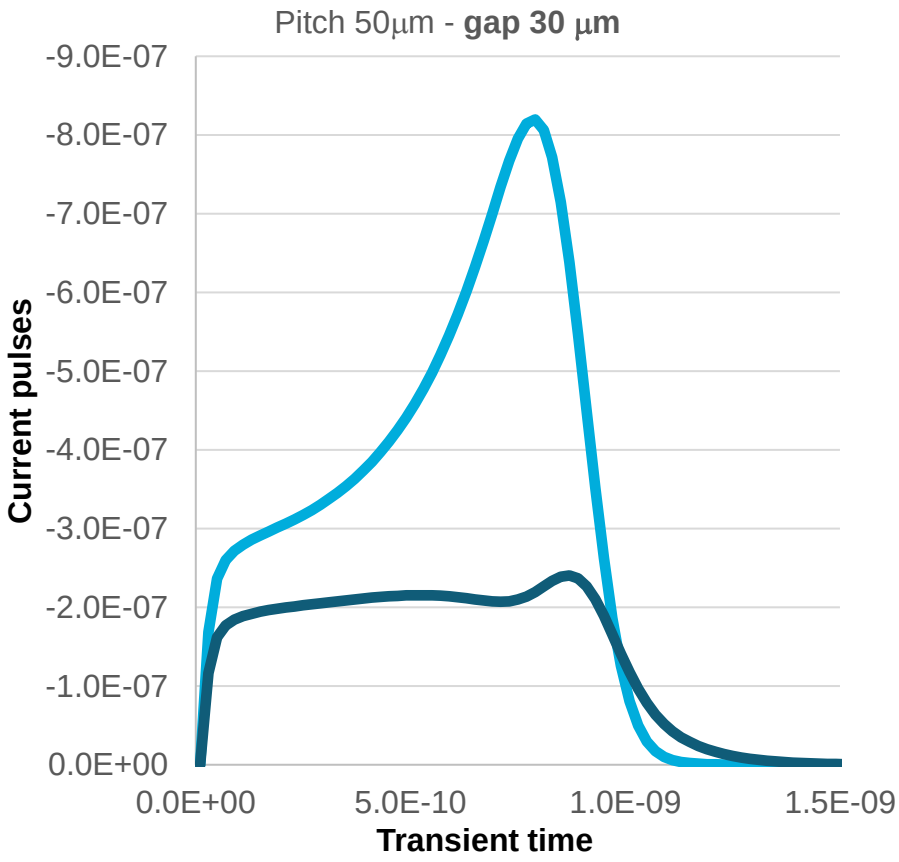
Current pulses at DC-coupled electrodes





Even in the case of pitch 50um when we expect max dis-uniformity, no major difference in pulses from devices with different gap value.

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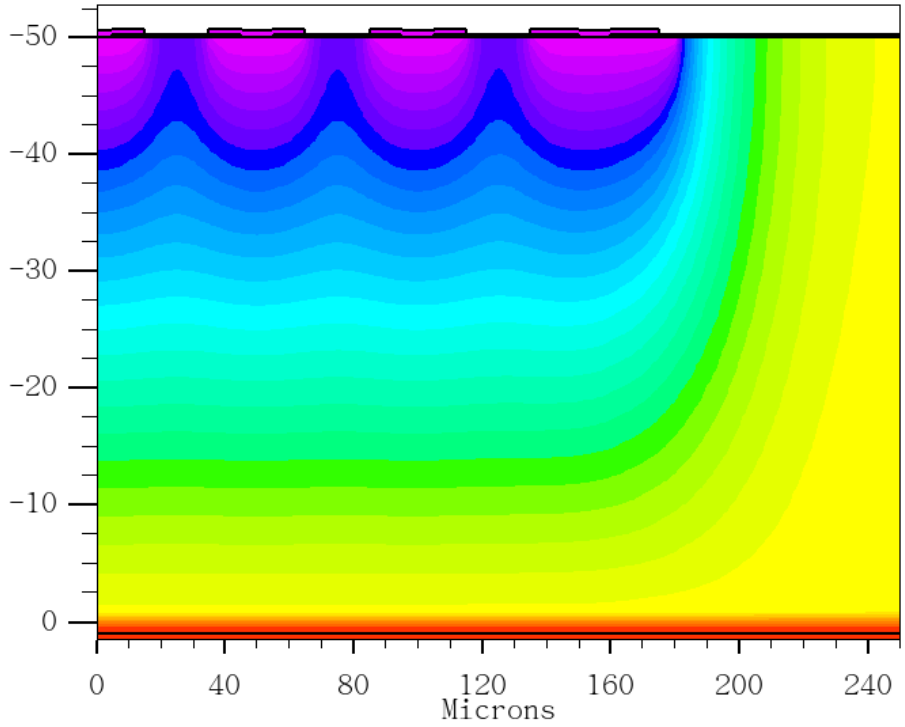
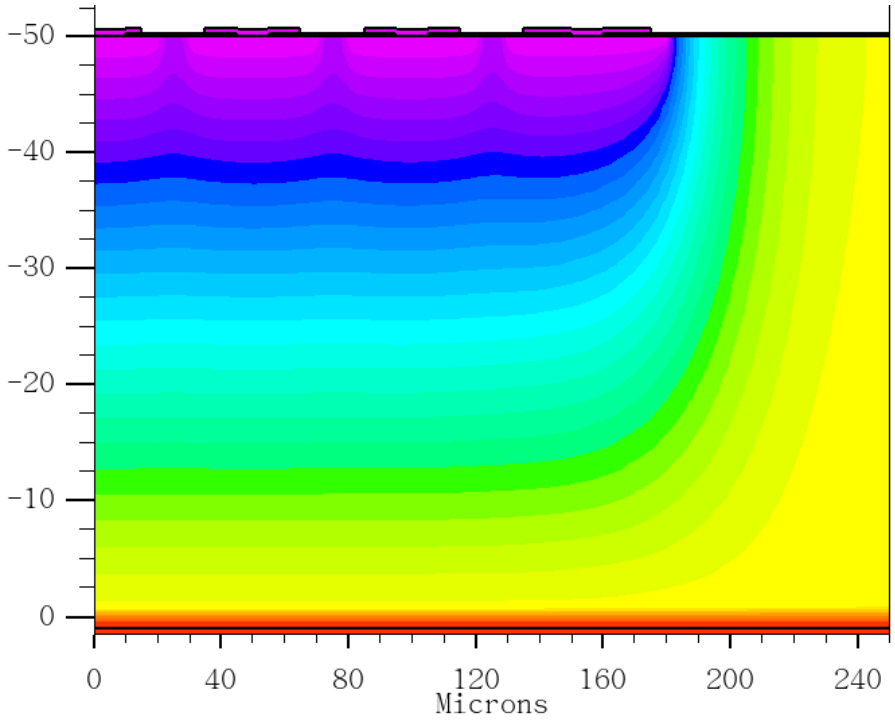
Electrostatic potential

Strip pitch = 50 μm

Gap = 30 μm



Gap = 10 μm



Along the gain layer, X-electric field show oscillations but:

- 1/5e3 in the case of gap 30μm
- 1/1e4 in the case of gap 10μm

Negligible!

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Good news:

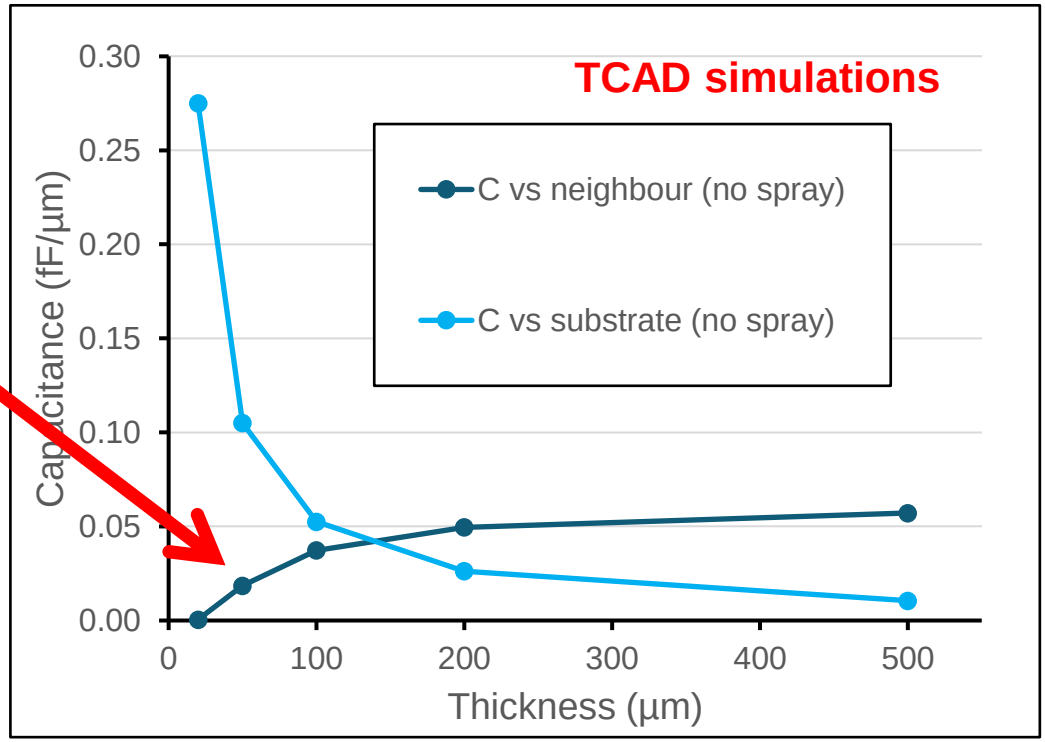
Interstrip Capacitance in thin layers

To make the weighting field as uniform as possible, small gaps between pixels are preferred.

How does the interpixel capacitance behave?

For thin substrates, Interpixel capacitance is not dominant

Observed and measured also on 50um thick LGADs for HEP



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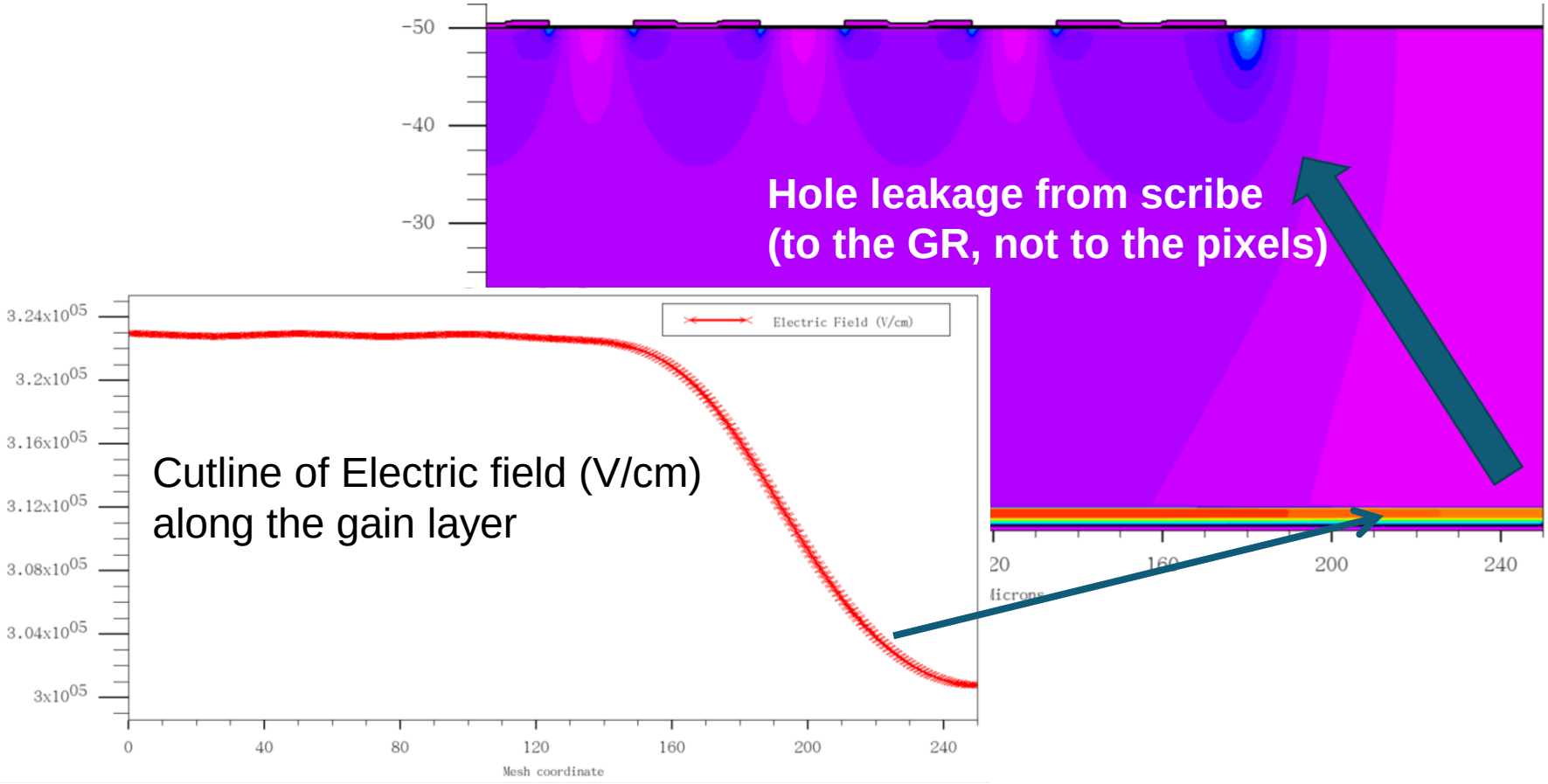
Challenge

As in any silicon device, a proper termination is the only option



The scribeline will introduce defects, acting as generation center (high leakage current).

May be hard to bias → **trench terminate the LGAD !!!!**

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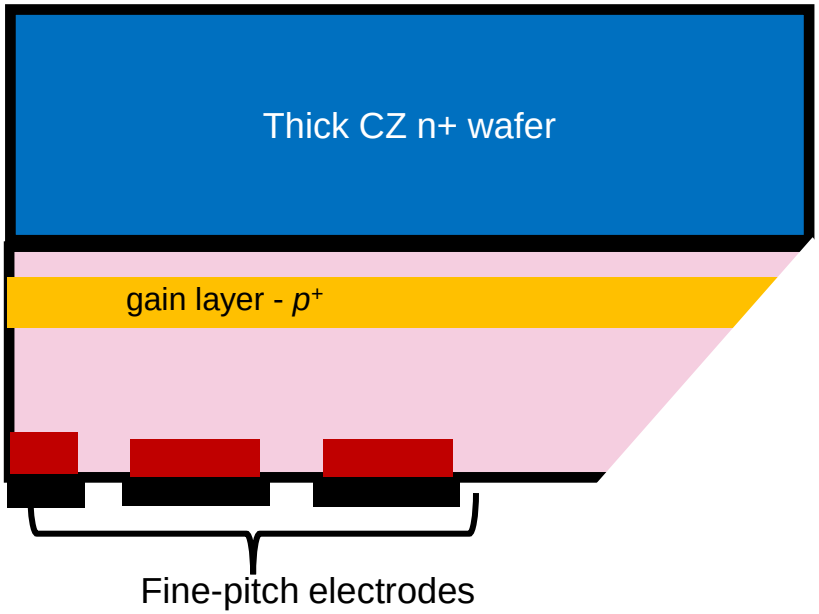
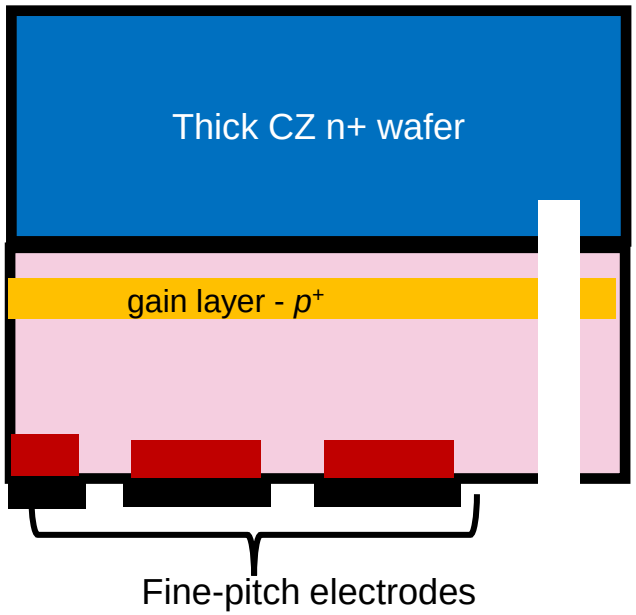
Trench termination

Wet process (KOH)



Dry process
(Reactive Ion Etching)



followed by oxidation for passivation of defects
Both trenching options will smooth the electric fields at the edge, preventing early breakdowns

Timetable

month 1-3:

refinement of TCAD simulations (students), production of the photolithographic masks and definition of the clean-room process.

Splittings in the process for the gain layer dose (start with ~ 8 wafers)

month 4: initial wafers (CZ and FZ) ready for wafer-bonding

month 5-7: CZ and FZ wafers bonded together

month 8-9: LGAD devices completed at BNL

month 10: results of static tests at BNL

month 11 -12: results of functional test at UCSC/BNL

month 13-14: with inputs from the characterization, study of the would-be issues and solutions. Publications.

Budget

	Sensor fabrication	Sensor testing	
BNL	$145k	$45k	**$190k**
University California at Santa Cruz	N/A	$25k	**$25k**
	$145k	**$70k**	**$215k**

Budget scenario (80% full funding) :

- **no test at BNL**

Budget scenario (60% full funding) :

- no test at BNL,
- delays in fabrication, which will not be prioritized

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