A superconducting nanowire binary shift register for SNSPD readout

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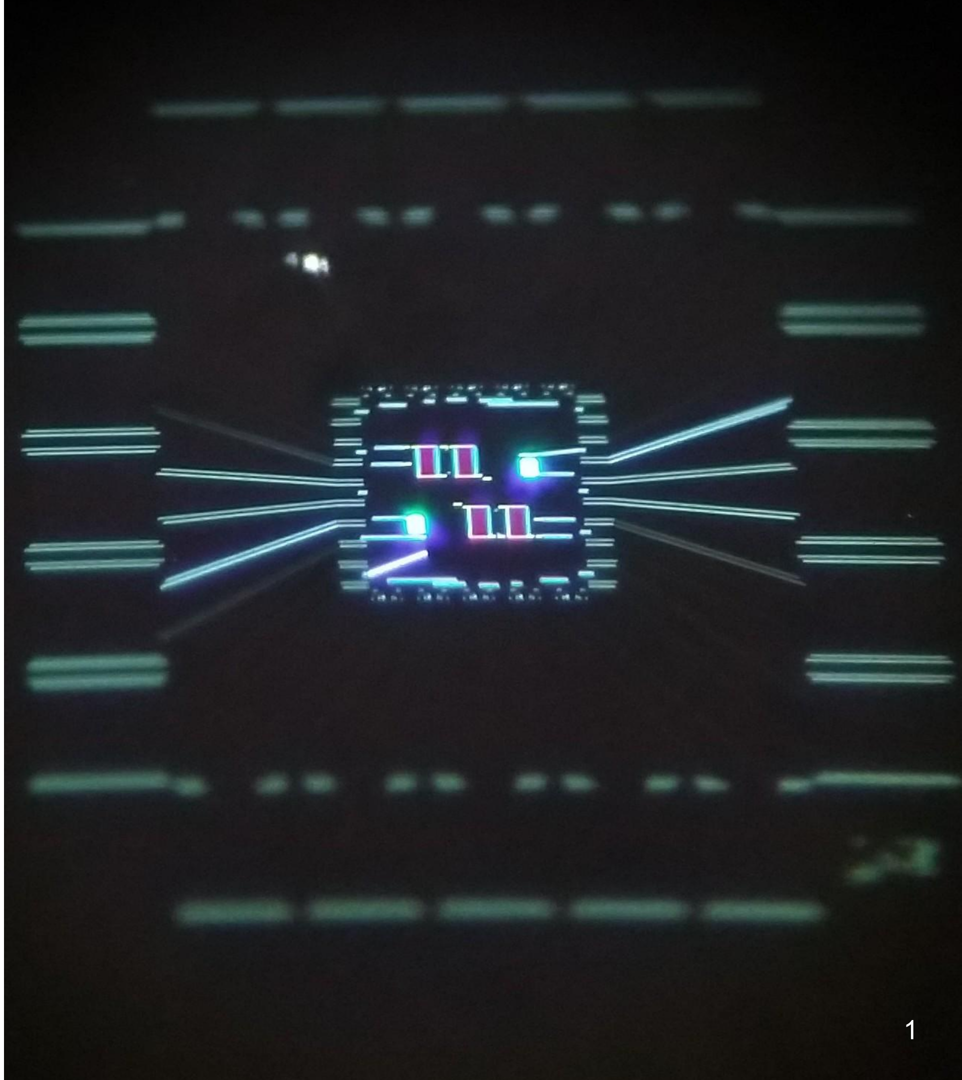
Quantum Nanostructures and Nanofabrication Group
Massachusetts Institute of Technology



Readout techniques for multi-pixel SNSPD imager arrays

One wire per pixel is not practical due to thermal load [1]

Microwave delay line [2], row-column multiplexing [3], frequency multiplexing [4] have been demonstrated

SFQ logic for array readout has also been demonstrated [5,6]

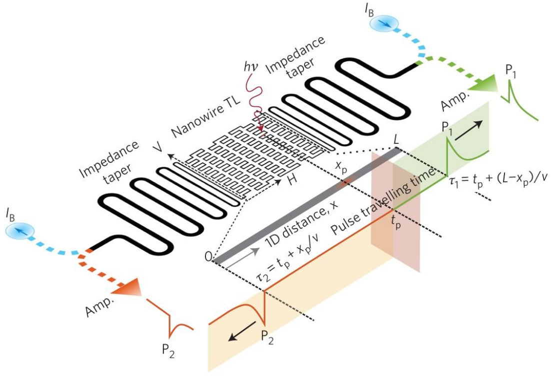


Fig 1a. from [2]

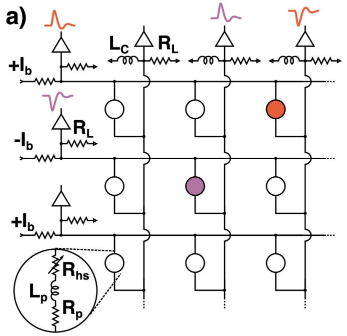


Fig 1a. from [3]

[1] Steinhauer, S., et. al., Appl. Phys. Lett. 118 (2021)
[2] Zhao, QY., et. al., Nature Photon 11 (2017)
[3] Wollman, E., et. al., Opt. Express 27 (2019)
[4] Doerner, S., et. al., Appl. Phys. Lett. 111 (2017)
[5] Yabuno, M., et. al., Opt. Express 28 (2020)
[6] Miki, S., et. al., Opt. Letters 46 (2021)

Digital readout of SNSPD arrays with superconducting nanowires and nanocryotrons

Simple fabrication: superconducting nanowires and nanocryotrons (nTrons) can be made on the same chip, with the same process as SNSPDs

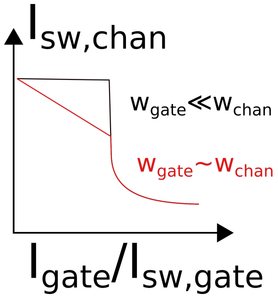
Large hotspot resistance R_n: ability to drive high impedance (e.g. 50Ω) loads to interface with room temperature electronics

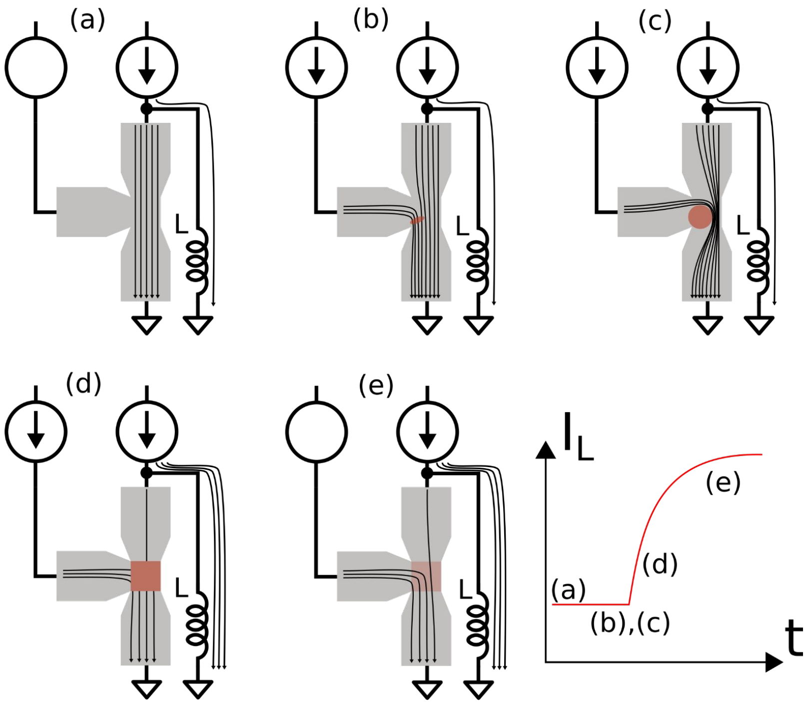
High kinetic inductance L_k: compact storage of high flux supercurrents, reducing sensitivity to magnetic field

Inductively-shunted wide-gate nanocryotron

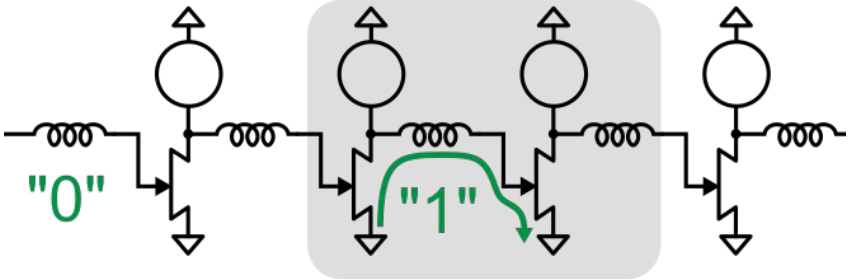
Three terminal nanocryotron can be used to store current in an inductor, conditional on the presence of a gate current

Using a wide gate allows the control current and inductor current to be comparable





Synchronous flux transfer between loops



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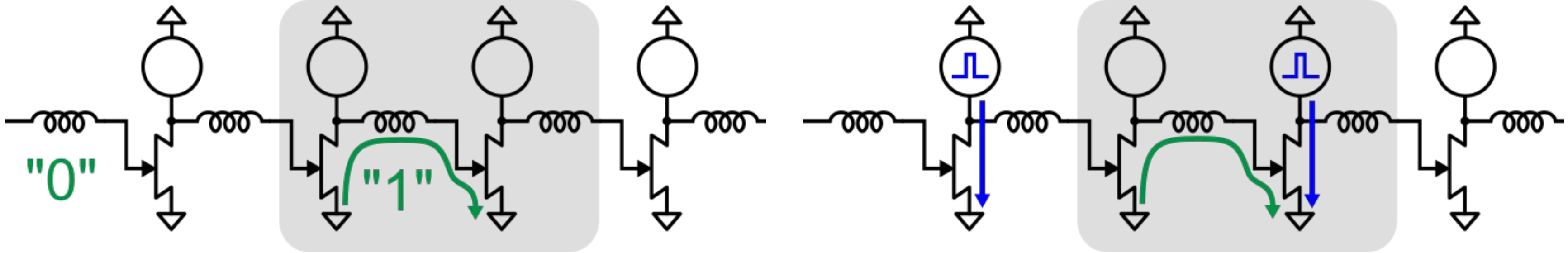

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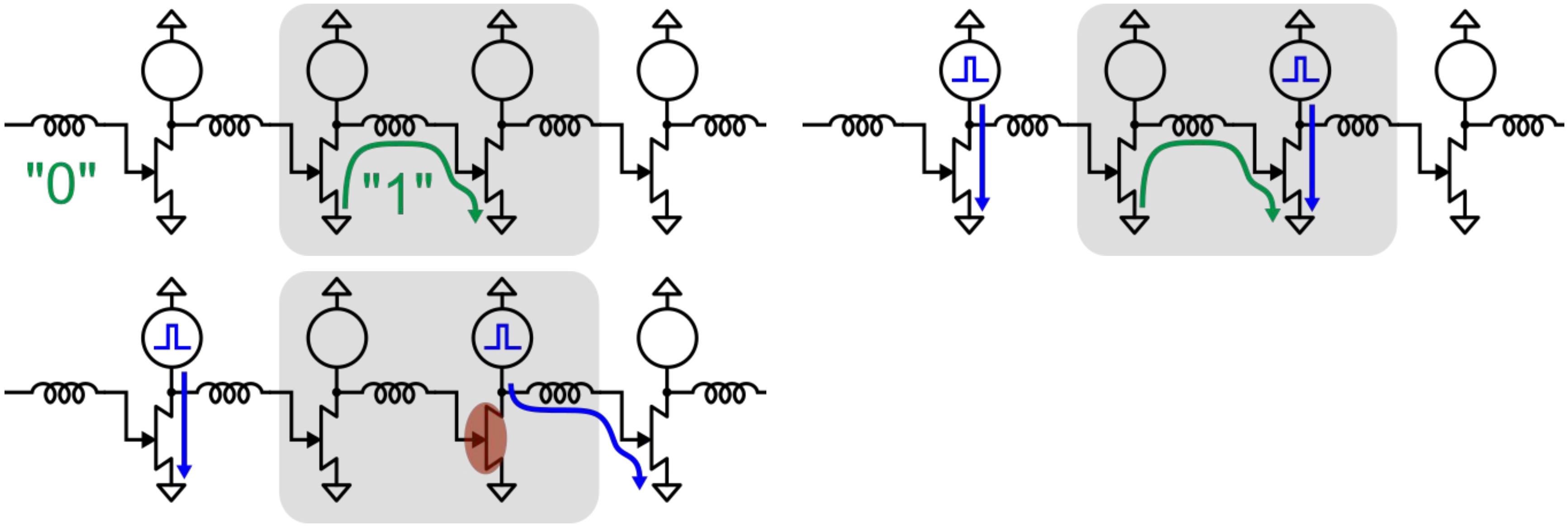

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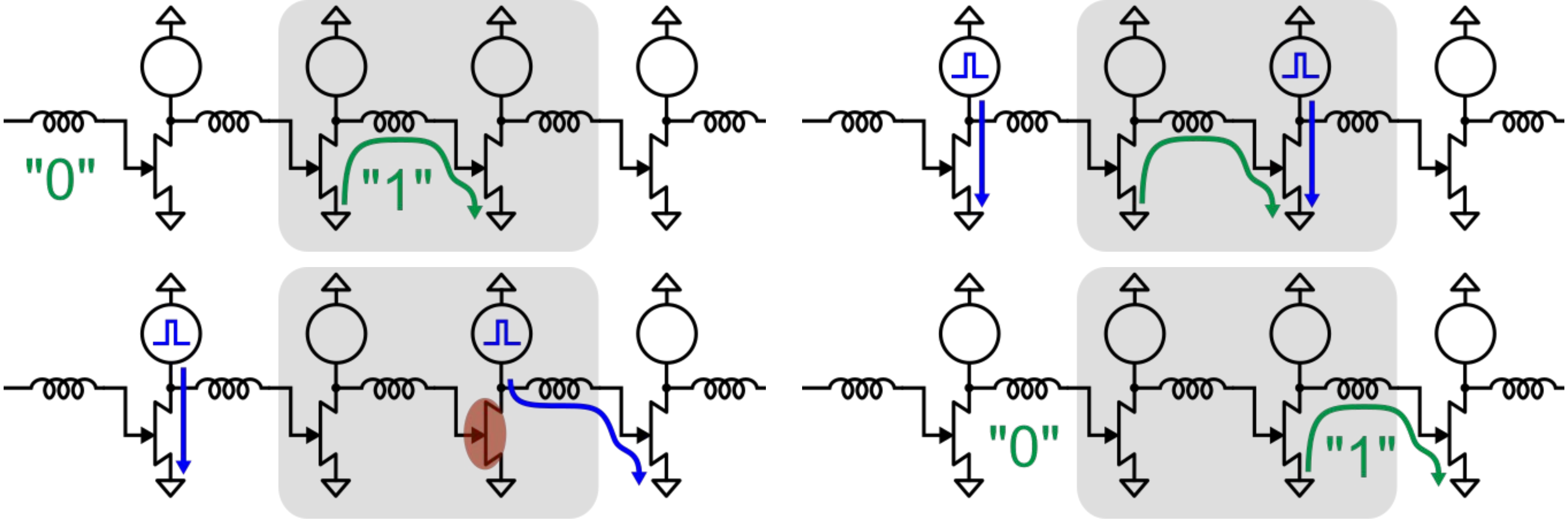
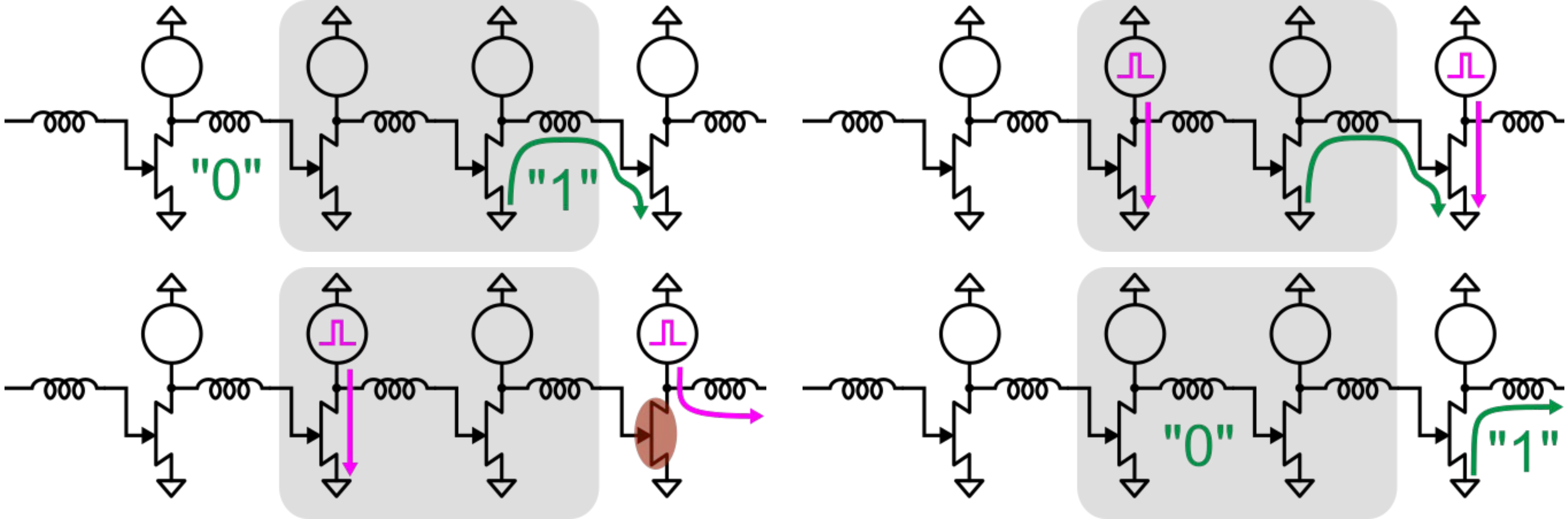
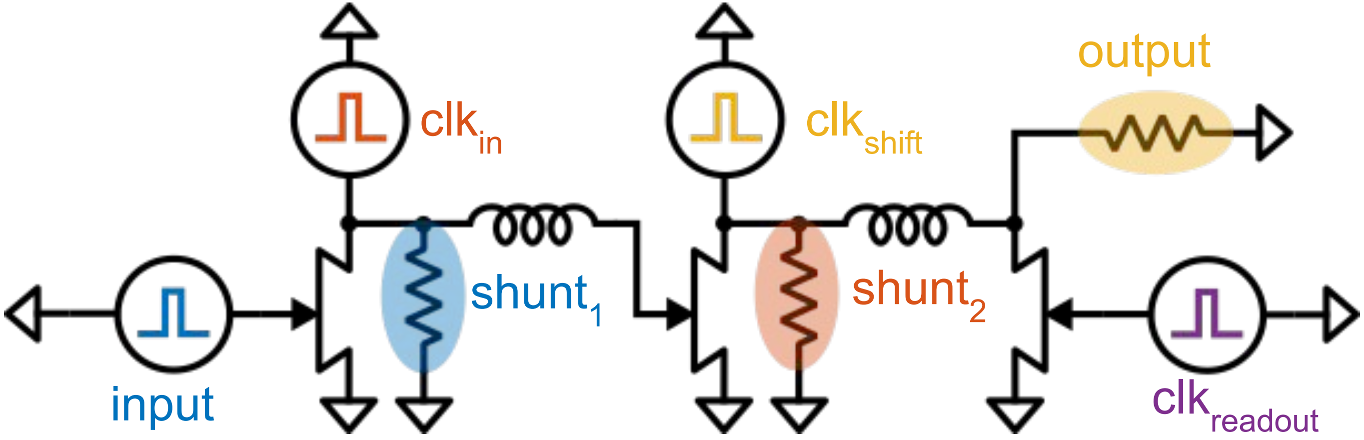


Synchronous flux transfer between loops

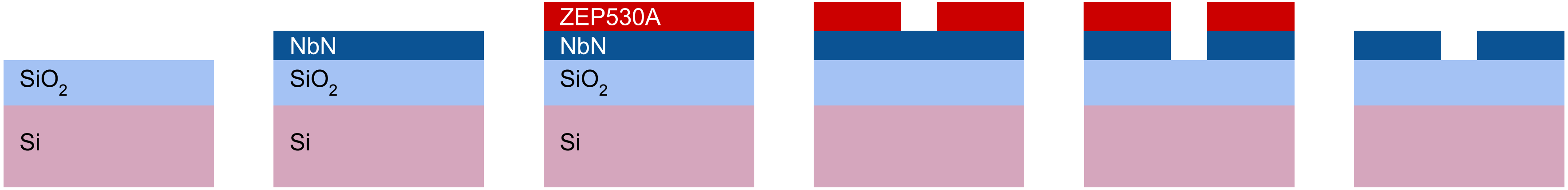


Two-loop experimental shift register circuit

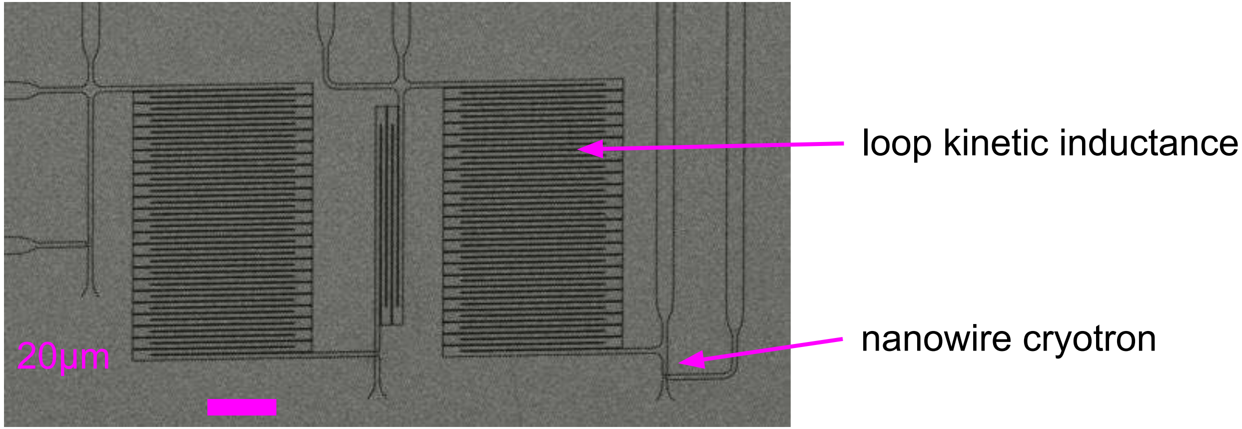
Goal of experiment: test if shifting operation is possible

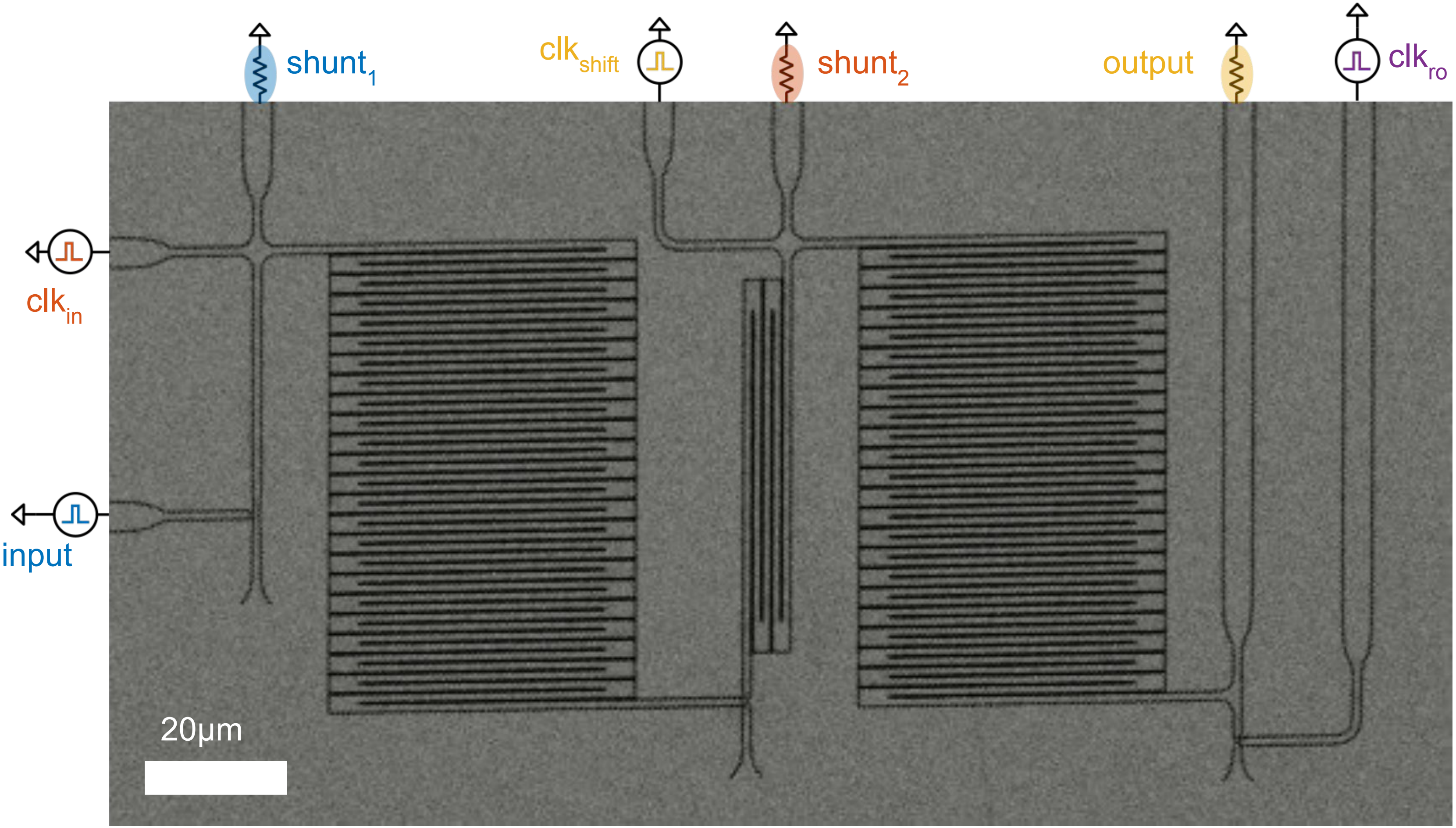


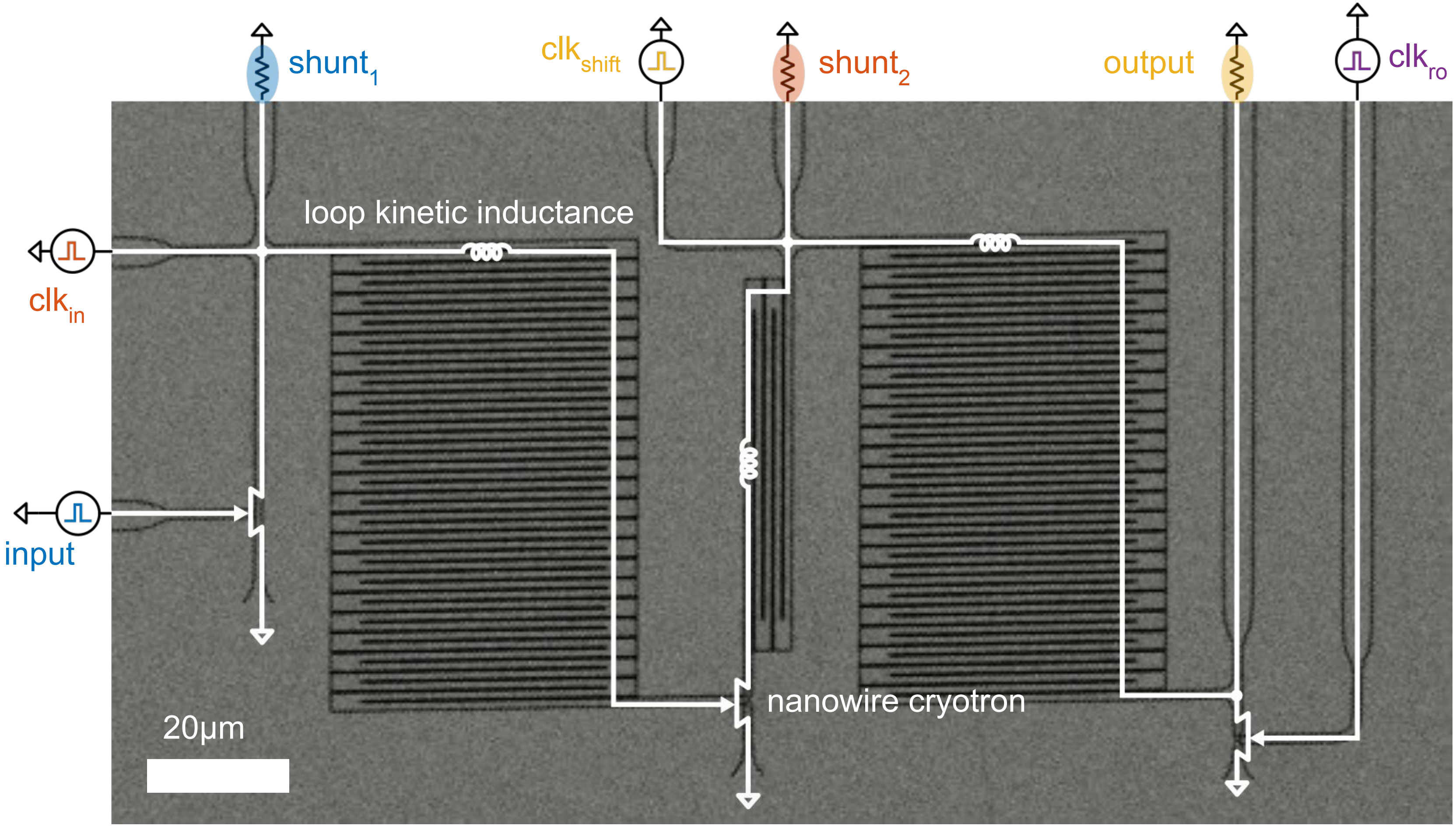
Nanocryotron single-mask fabrication process



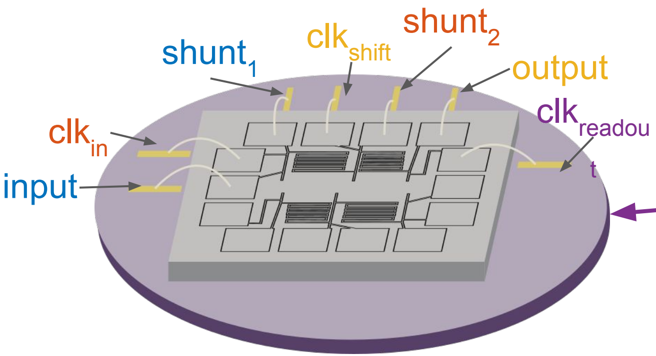
SiO_2 on Si wafer — sputter 15nm NbN — spincoat ZEP530A — e-beam lithography — CF_4 reactive ion etch — resist strip

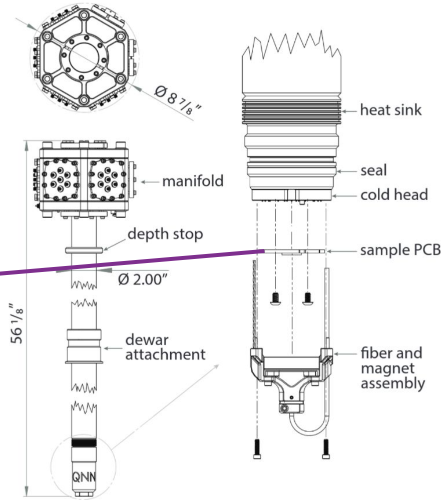


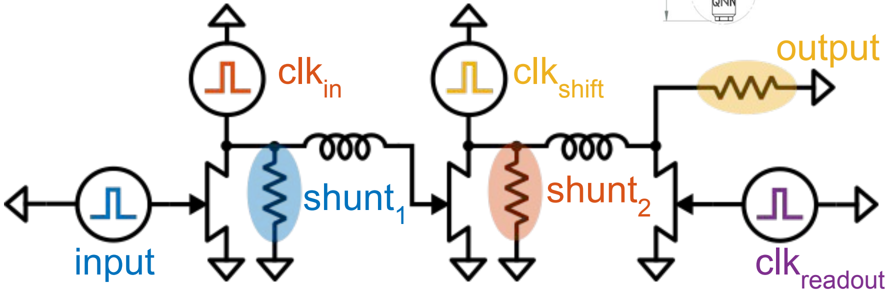

shunt1
clkshift
shunt2
output
clkro
clkin
input
20μm


shunt$_1$
clk$_{shift}$
shunt$_2$
output
clk$_{ro}$
loop kinetic inductance
clk$_{in}$
input
nanowire cryotron
20μm

Experimental setup







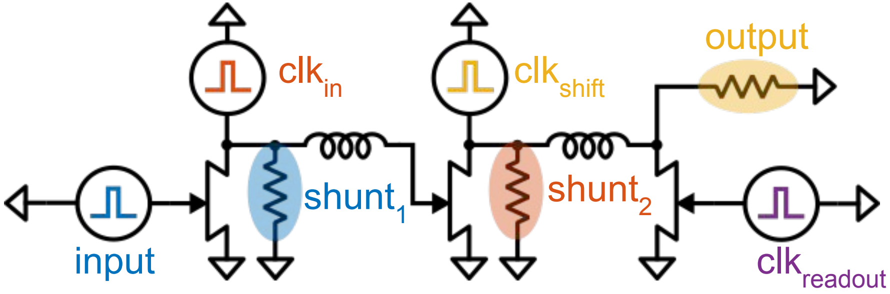
Wirebonded directly to NbN
cooled to 4.2K in LHe dewar with dipprobe
coax to interface with LNAs, bias tees, Keysight DAQ
11kΩ resistors used as current sources for clocks

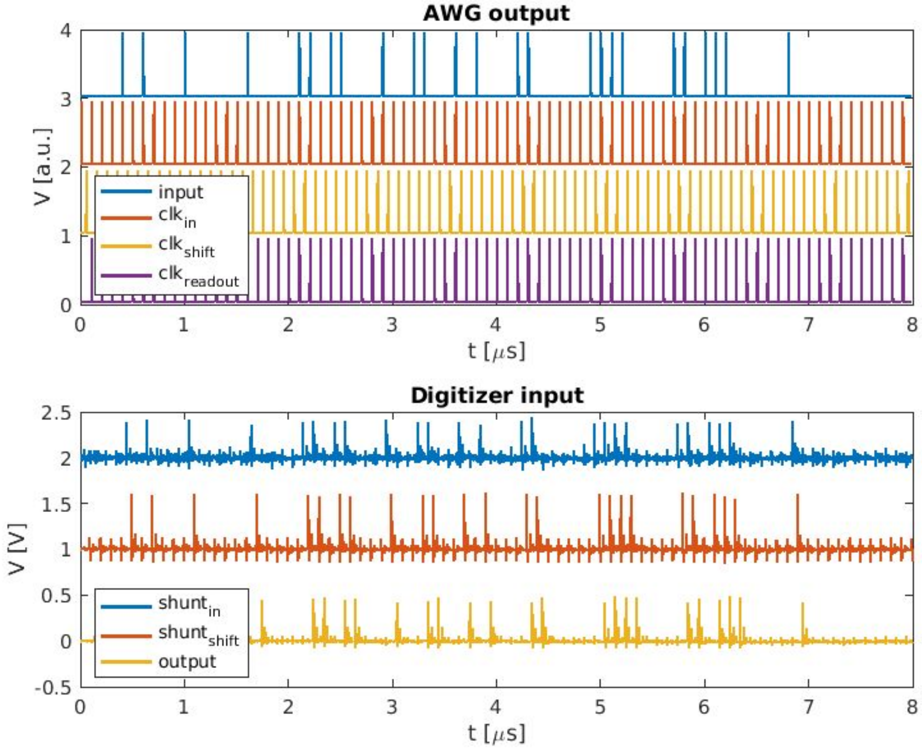
[7] Butters, B., PhD Thesis

Demonstration of synchronous flux transfer

Maximum operating frequency: 83MHz

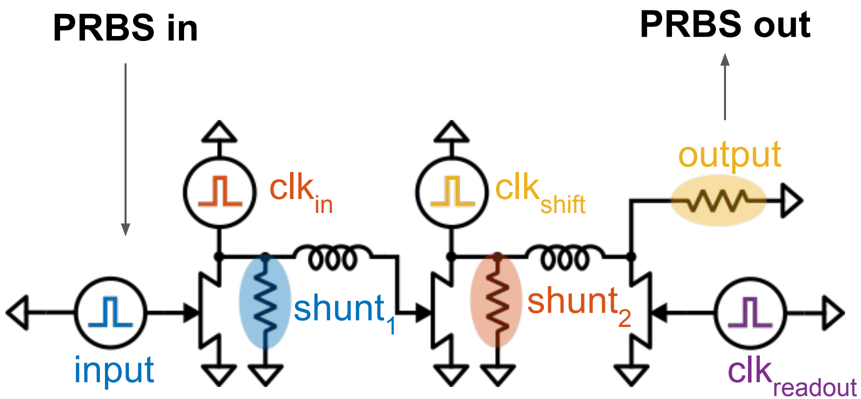
Thermal reset time of nanowire devices should allow for operation >200MHz if the loop inductance and operating current are reduced

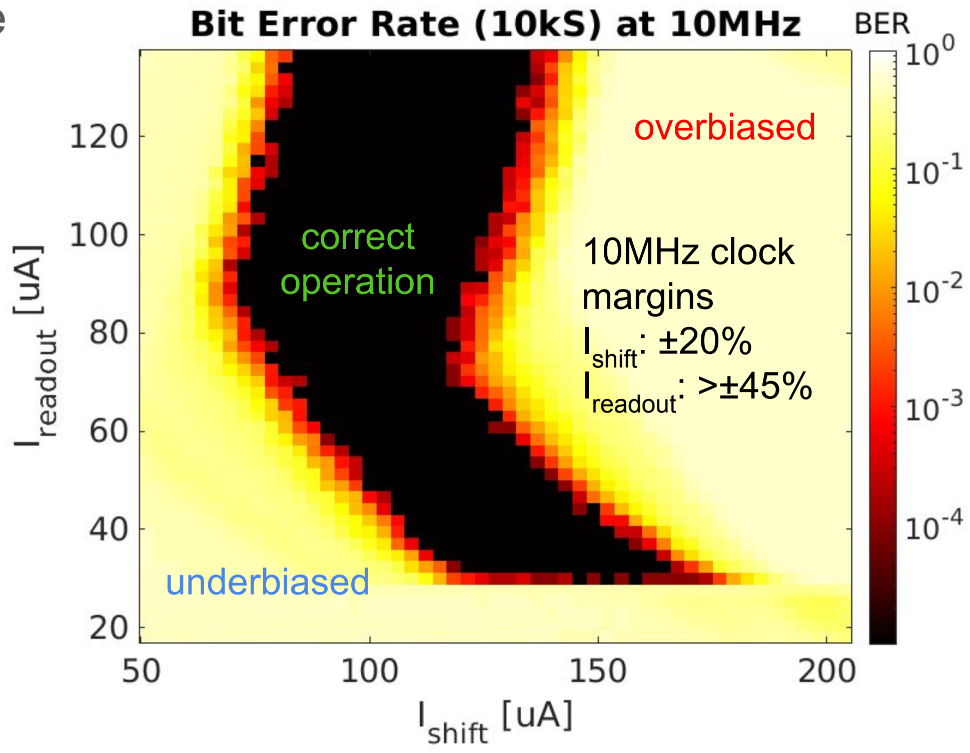




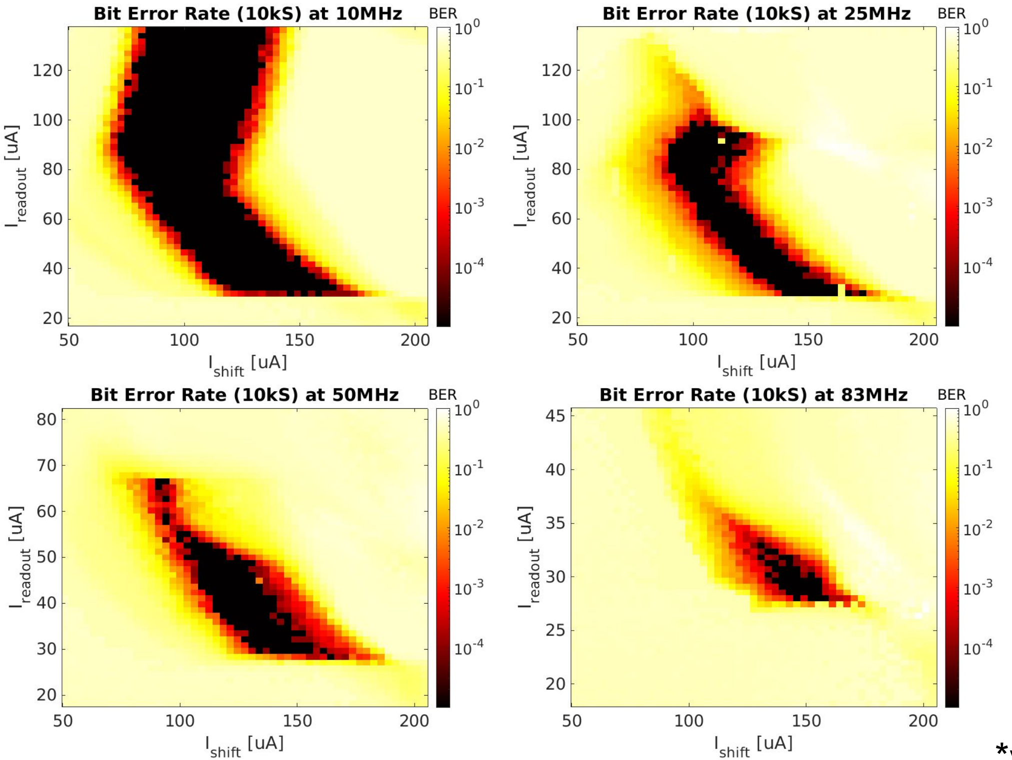
Bias margin analysis: bit error rate

Send a pseudorandom binary sequence of pulses, sweep shift and readout current amplitude for each sequence



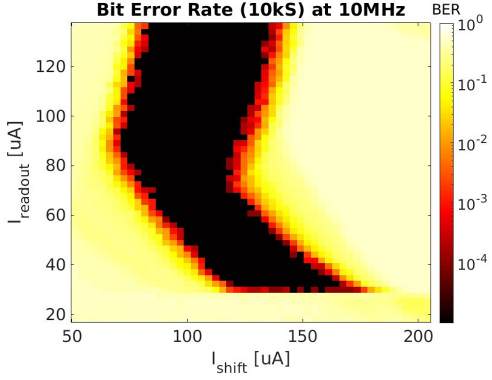


Bias margins as a function of frequency

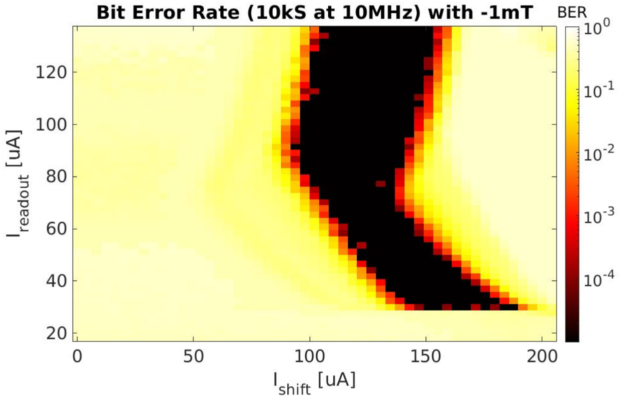


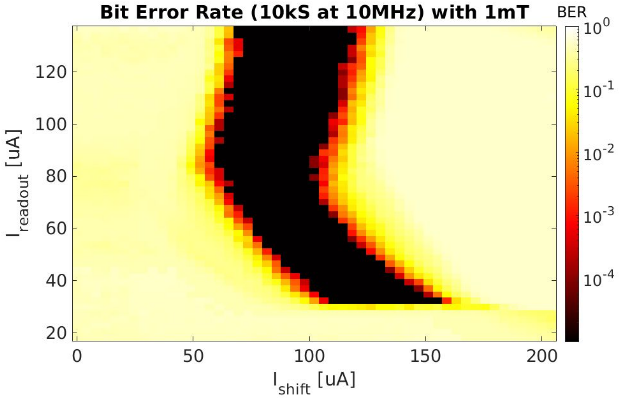
*yaxis changed for clarity

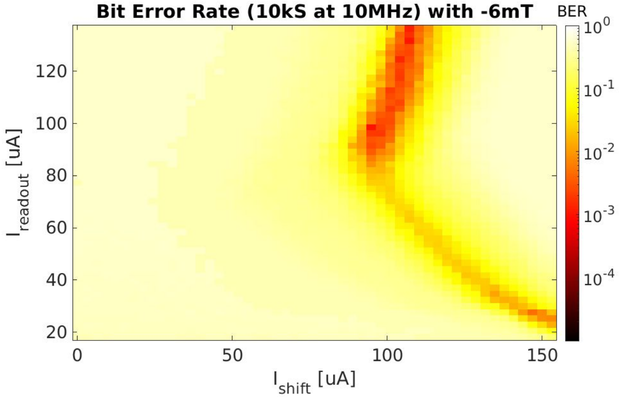
Bias margins as a function of magnetic field

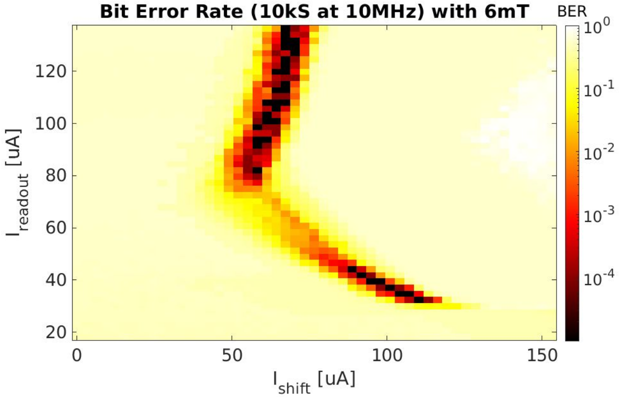


Bias landscape at 0mT









Lower limit on energy consumption

When switching, energy/bit ≈ $1/2*L*I^2$ ≈ 1 fJ as designed (~150nH, 120μA)

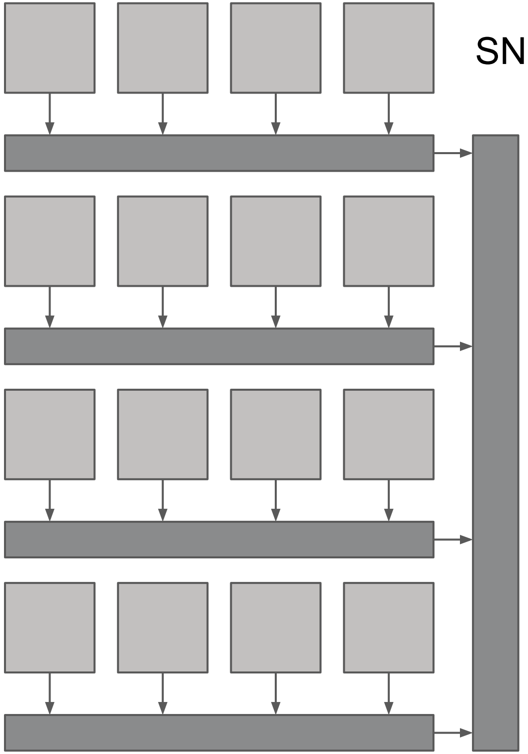
- 1Kpixel array clocked at 10MHz (9.8K fps) would dissipate 100nW-25μW
- Scaling allows for reduced energy consumption:
  - lower loop inductance: proportional reduction
  - lower critical current (and therefore loop current): square-law reduction
  - e.g. a 20nH loop with 30uA loop current would dissipate about 10aJ/bit

Energy of clock generation and distribution not taken into account

Serialization of SNSPD array readout

Analogous to bucket-brigade operation of CCD

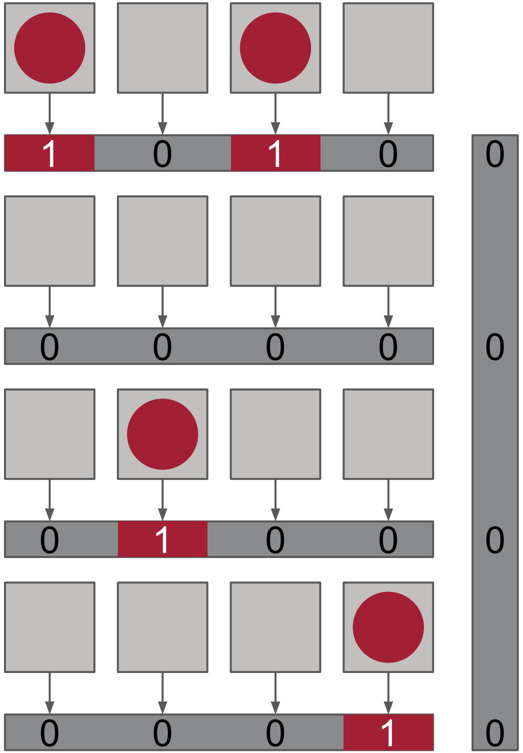
Shuttle flux (instead of charge) between neighboring cells



Serialization of SNSPD array readout

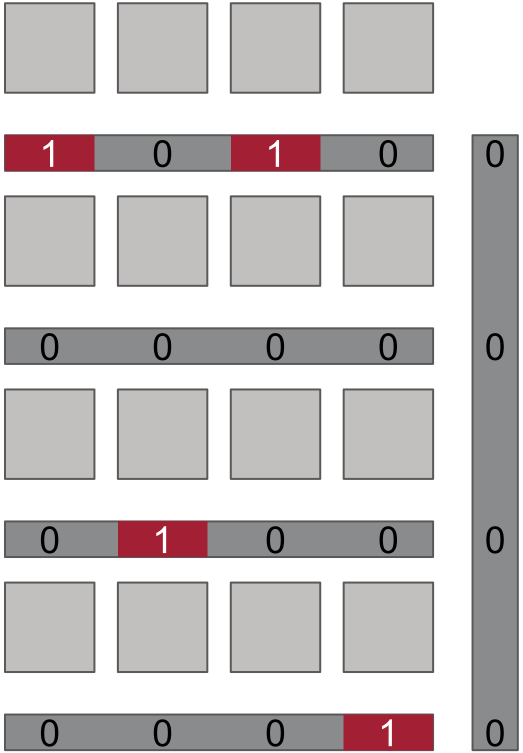
Bias SNSPDs near critical current

Detected photons store flux directly into shift register



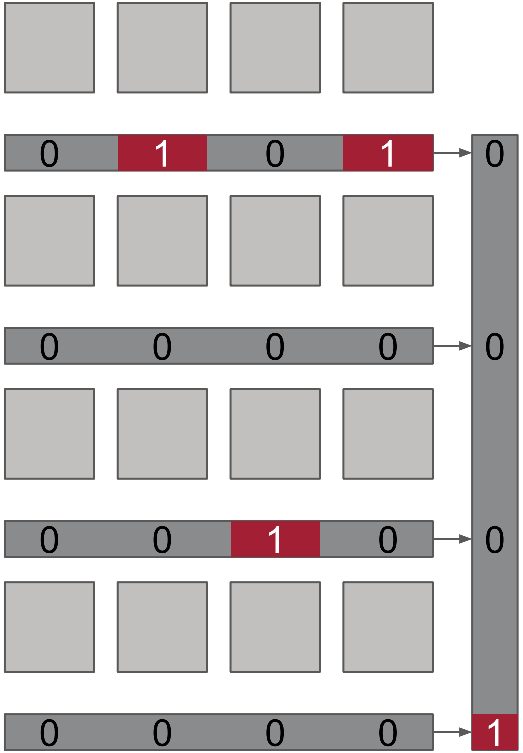
Serialization of SNSPD array readout

Disable SNSPD bias



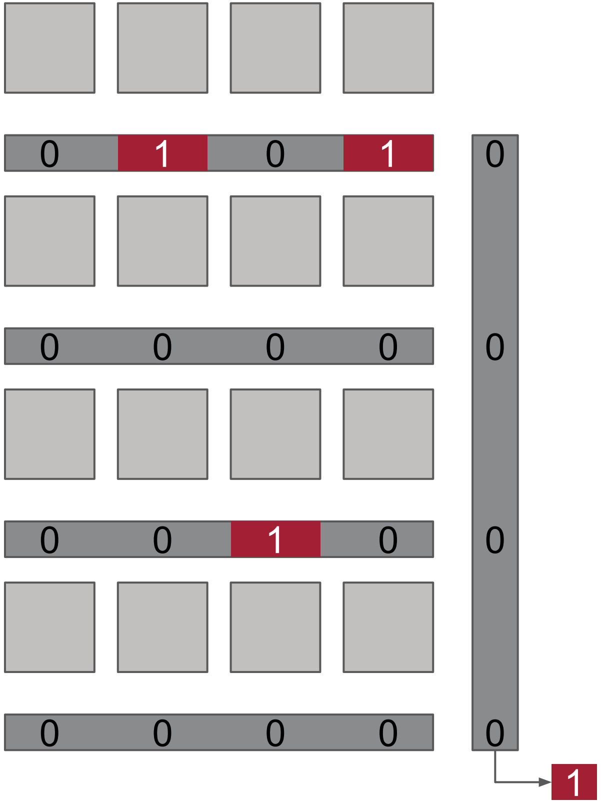
Serialization of SNSPD array readout

Shift first column of array into another shift register



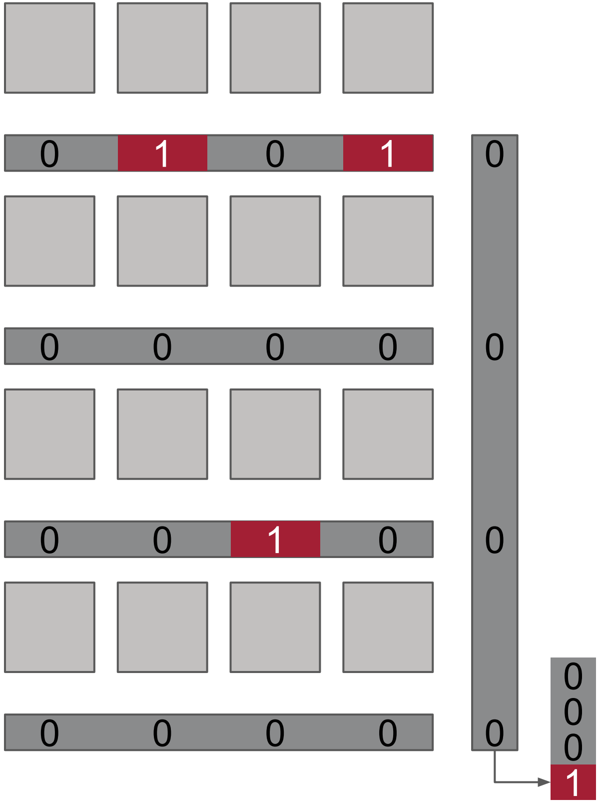
Serialization of SNSPD array readout

Shift out first column



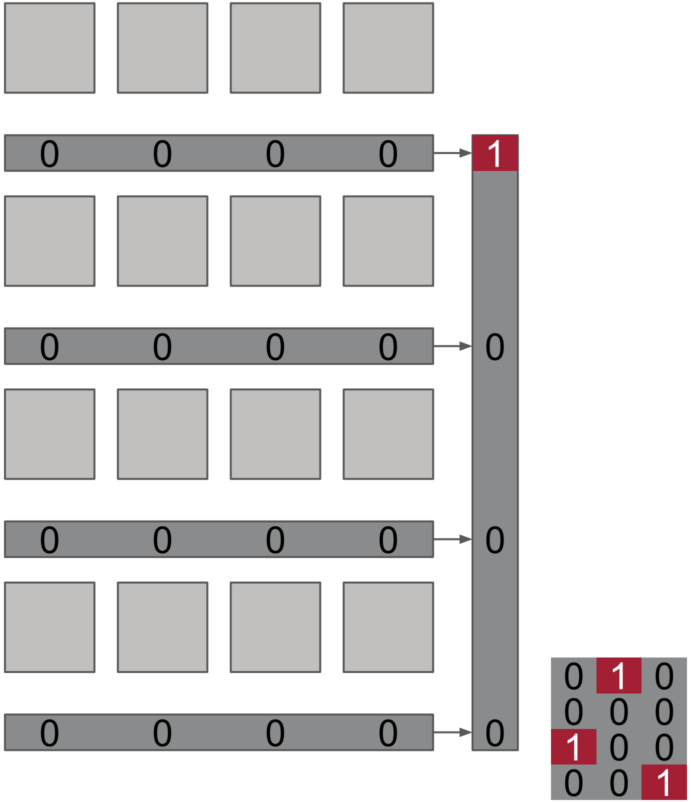
Serialization of SNSPD array readout

Shift out first column…



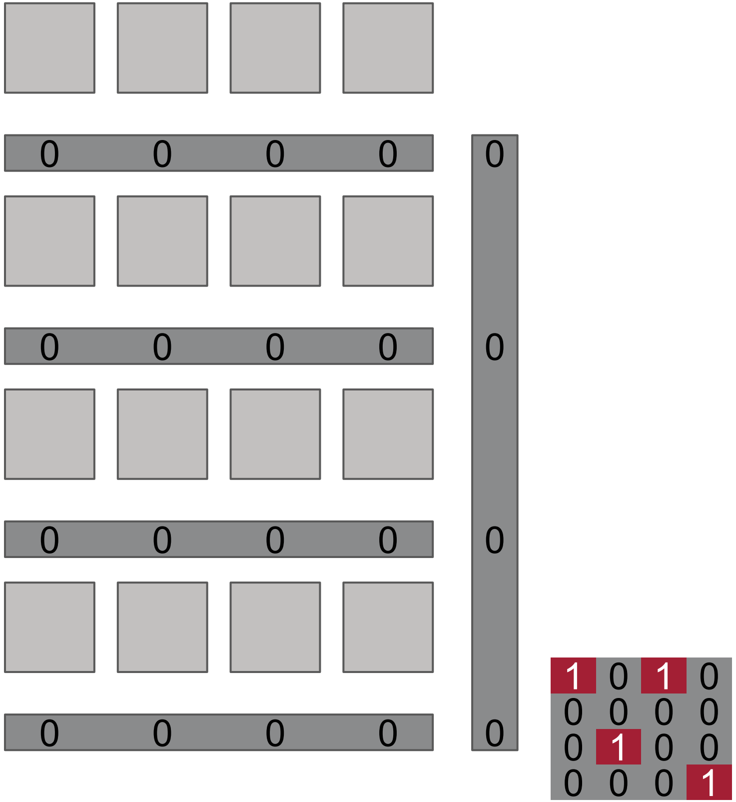
Serialization of SNSPD array readout

Repeat for remaining columns

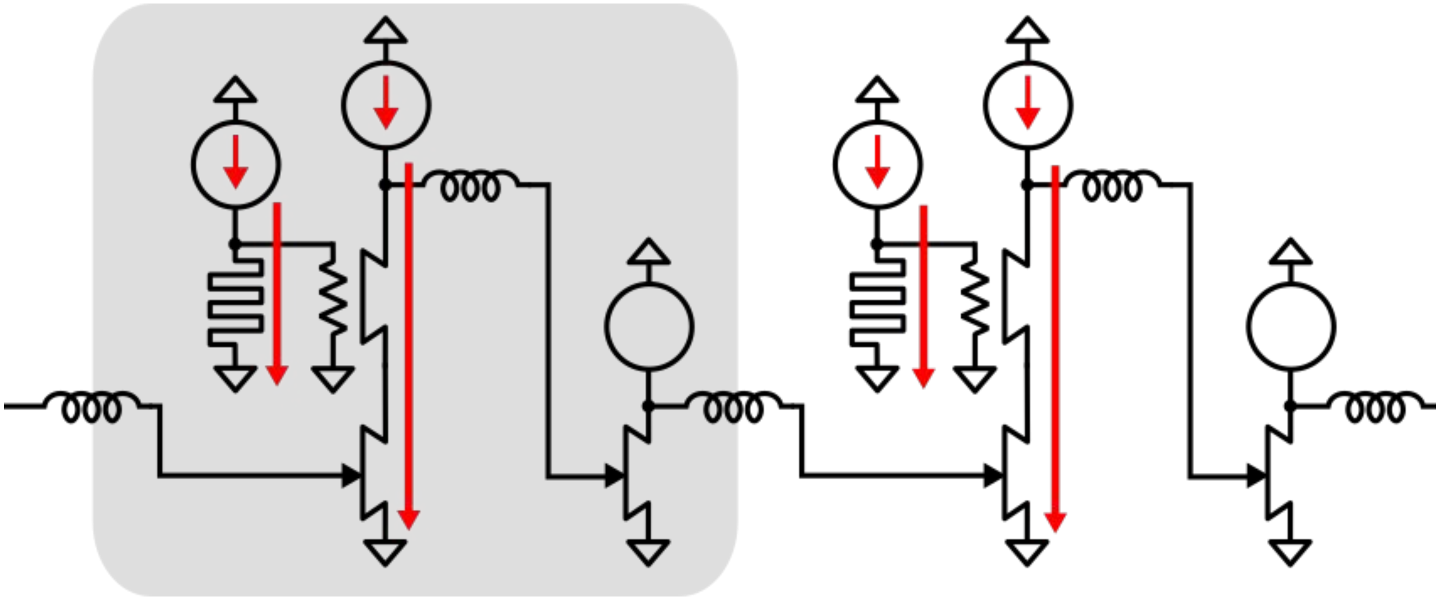


Serialization of SNSPD array readout

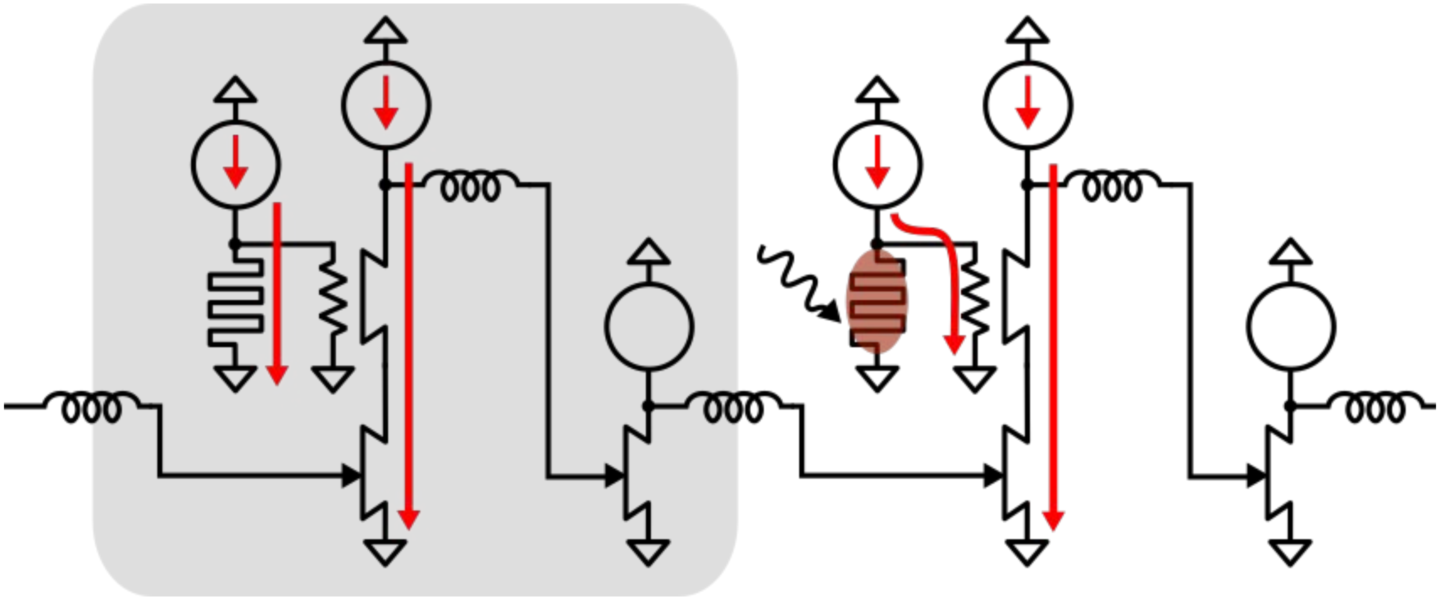
Repeat for remaining columns



Serial readout of a row of SNSPDs



Serial readout of a row of SNSPDs



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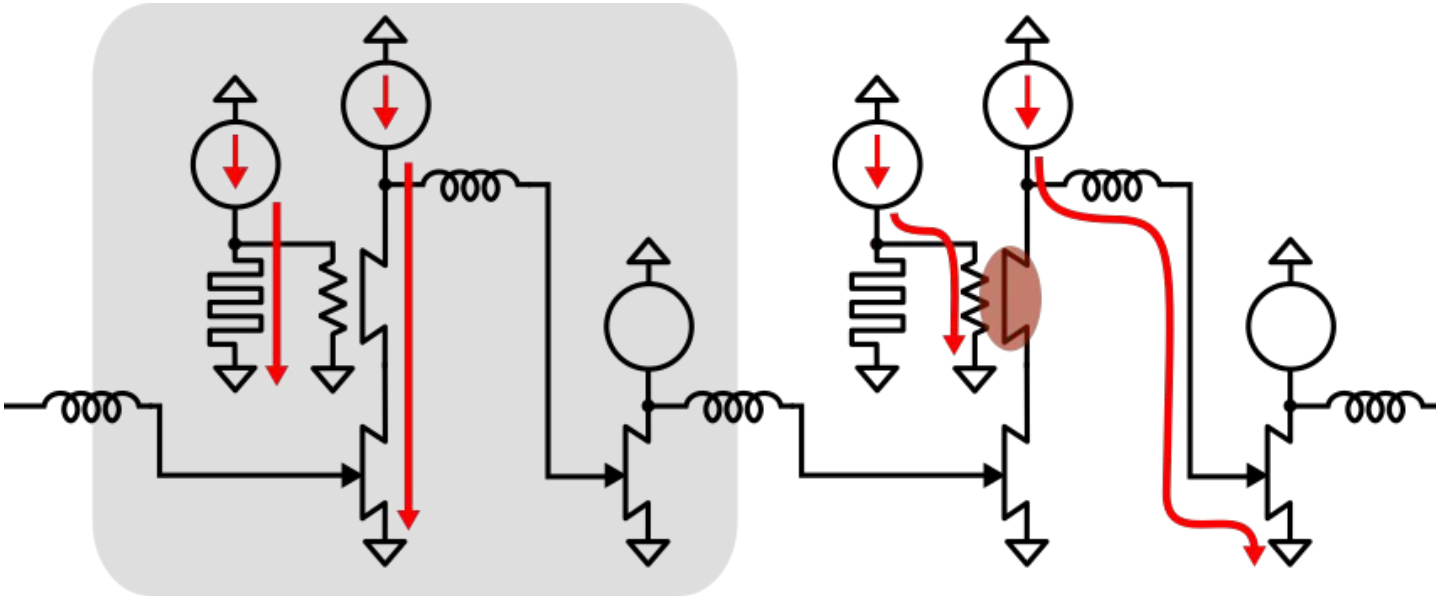

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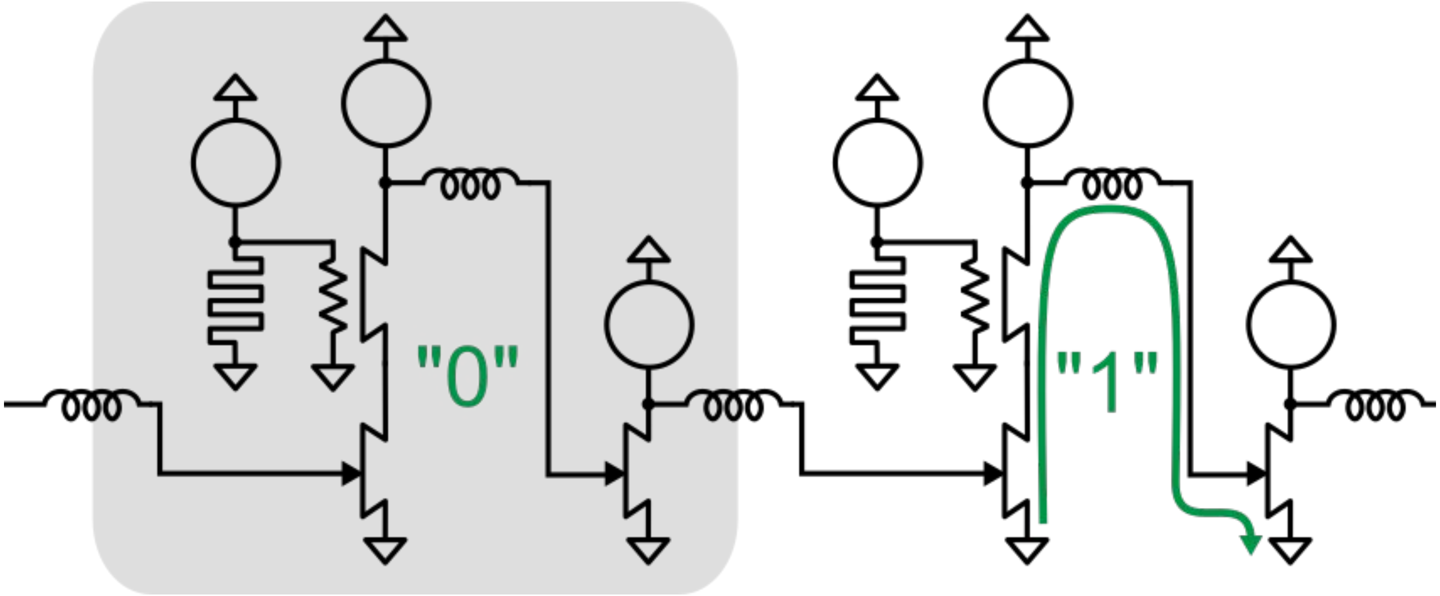
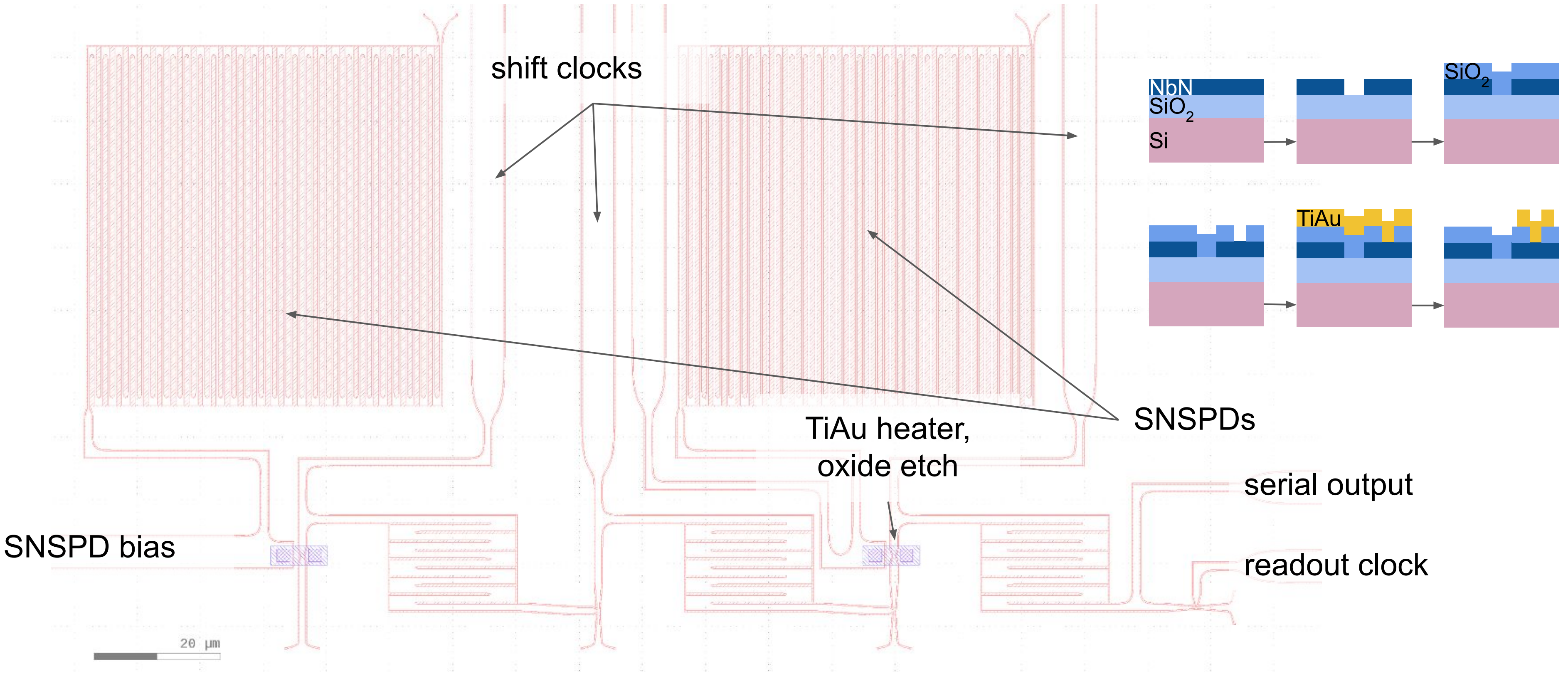


Serial readout of a row of SNSPDs

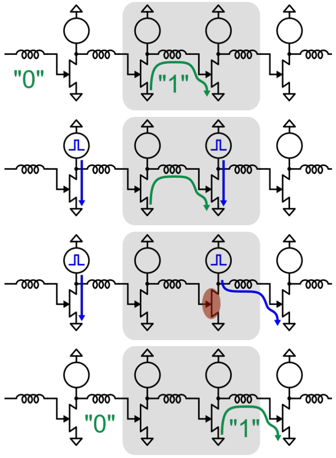


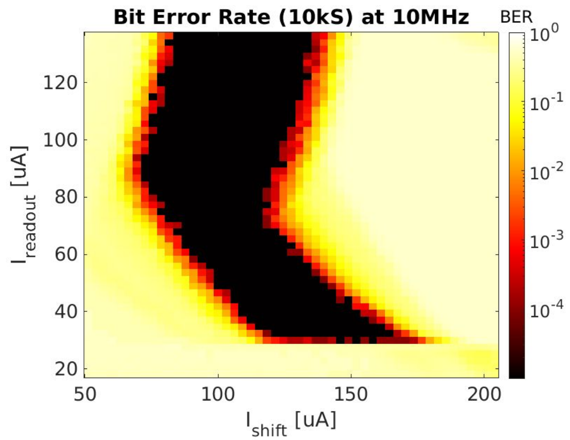
Summary and outlook

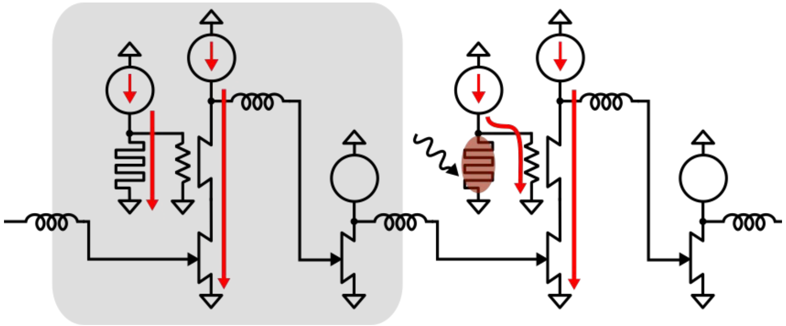
Method for **transferring flux between superconducting loops** has been experimentally demonstrated

A circuit for **serial readout of a row of SNSPDs** has been proposed and simulated

Serialization and deserialization is a **generalizable strategy for reducing wire count** for readout and control of multiple superconducting devices







Acknowledgements

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RESEARCH LABORATORY OF ELECTRONICS AT MIT

Quantum Nanostructures and Nanofabrication Group

References

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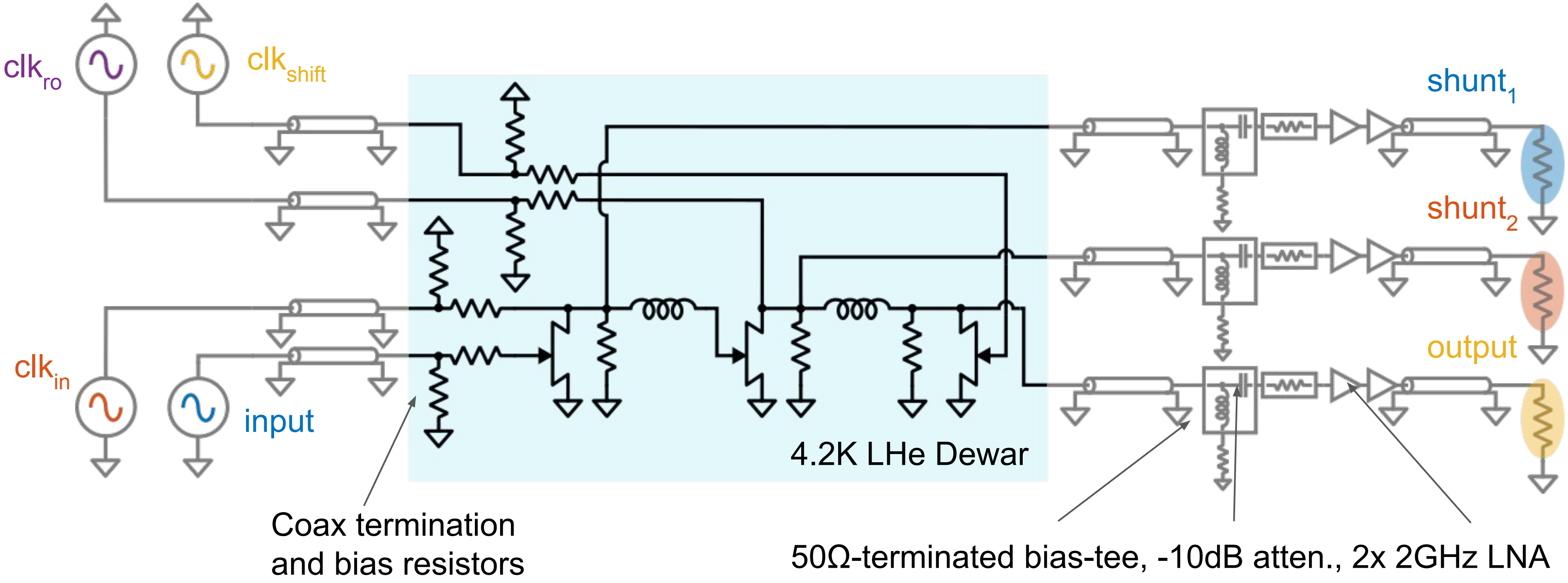
[7] Butters, B., “Digital and microwave superconducting electronics and experimental apparatus,” Ph.D. dissertation, Massachusetts Institute of Technology, Feb. 2022

Experimental setup



Serial row readout simulation results

SNSPD events captured as loop current

clocks

shunt voltages (a pulse is generated when an ntron switches)

SNSPD photon arrivals and sample bias

loop currents