Fabrication Challenges for Superconductor Electronics

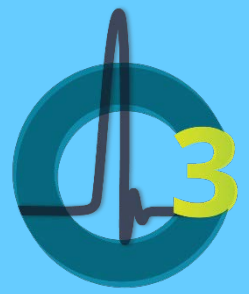
D. Scott Holmes
DARPA MTO Program Manager

Seminar at

2019-

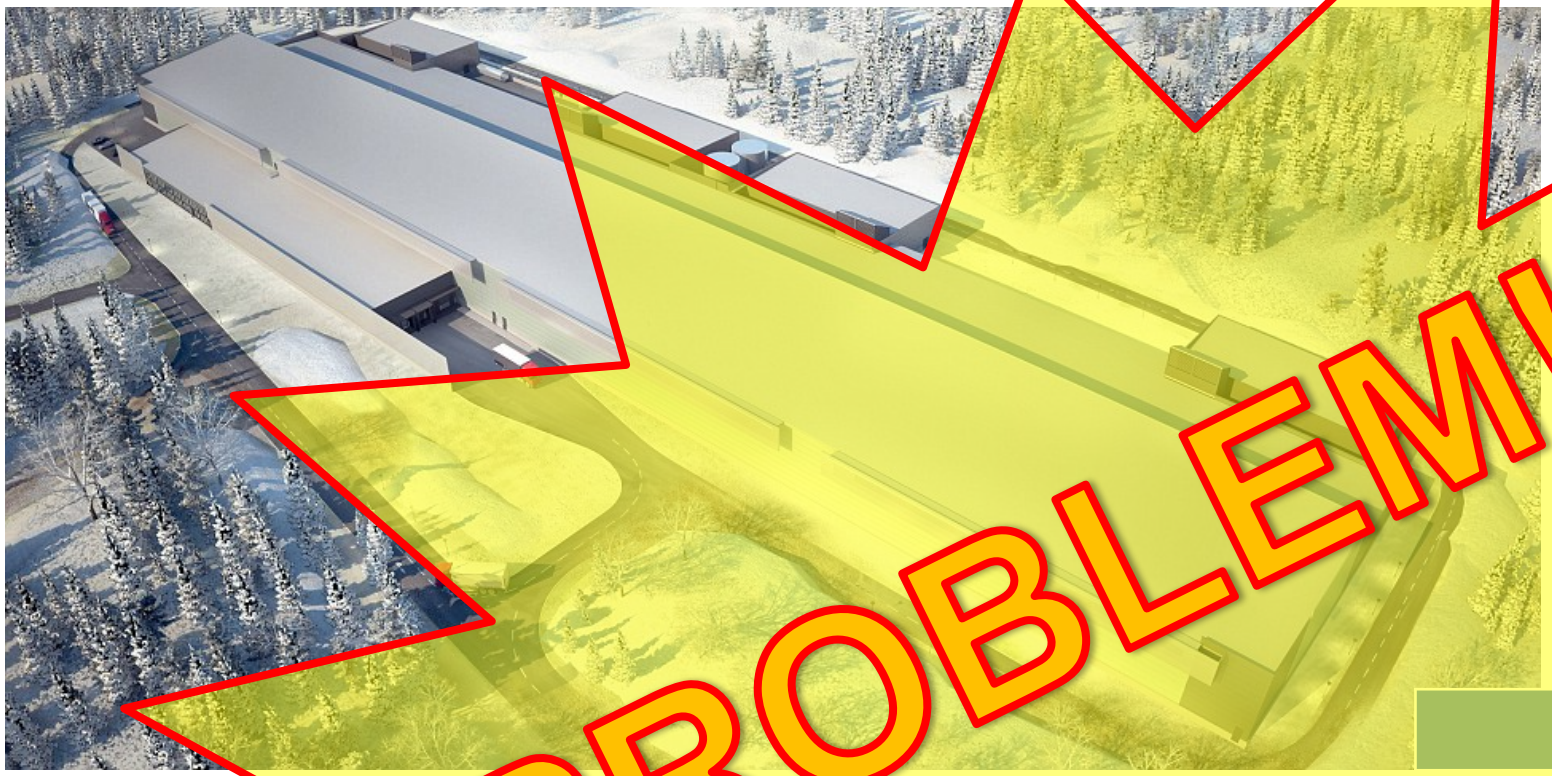
Outline

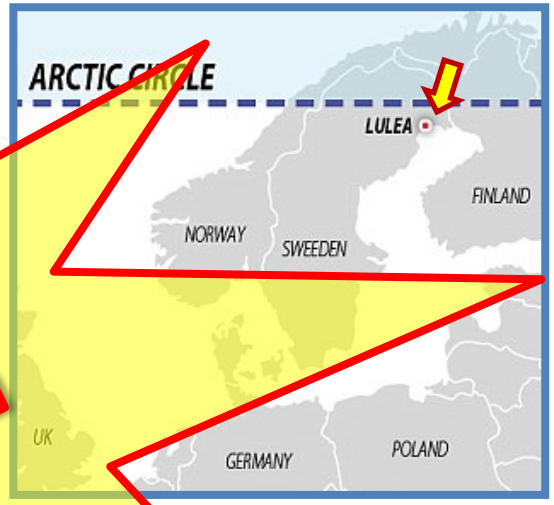
- IARPA Cryogenic Computing Complexity (C3) Program
- Related Work
- Challenges Remaining for Superconductor Electronics (SCE)
- Future Prospects



IARPA Cryogenic Computing Complexity (C3) Program

Facebook Data Center, Luleå, Sweden





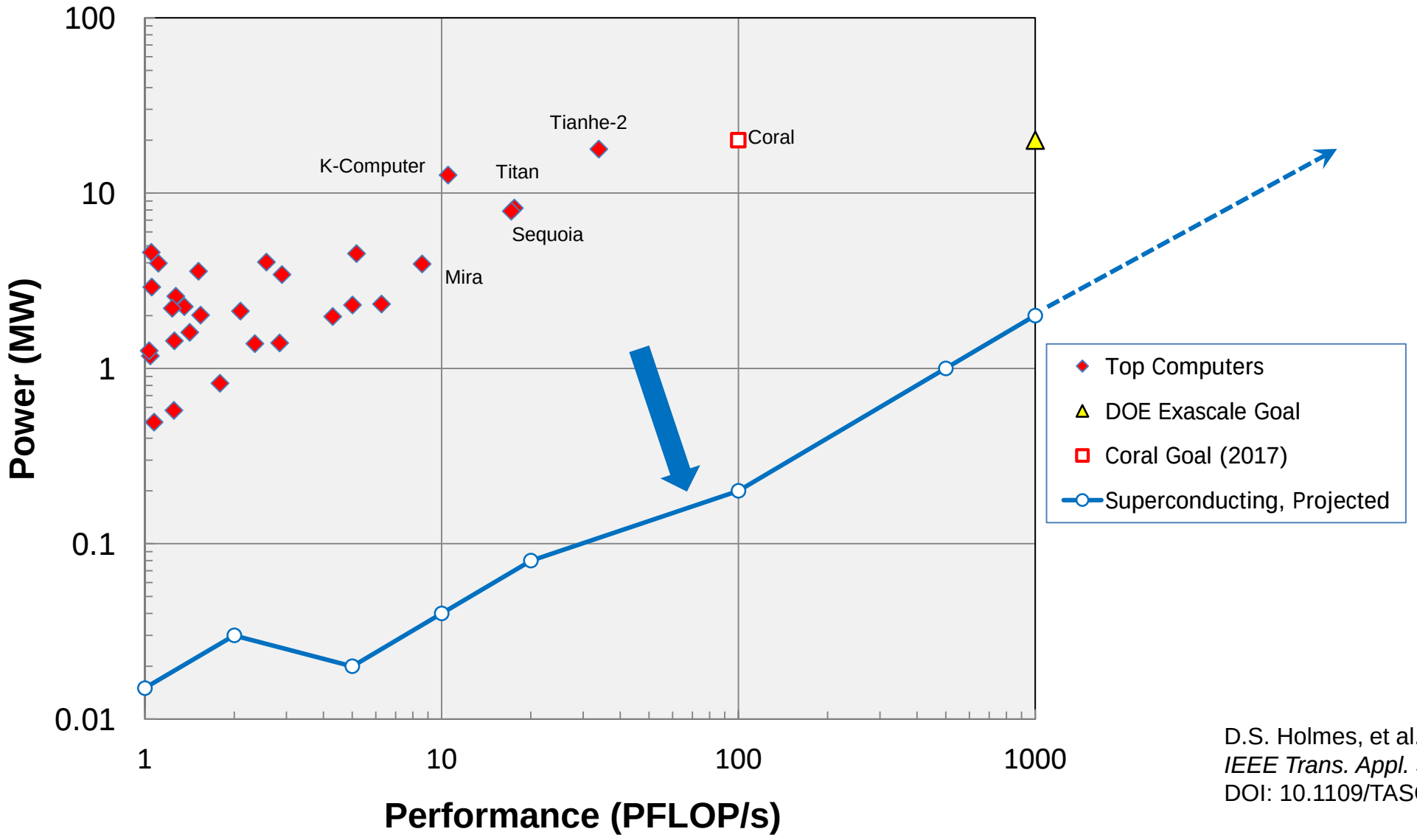
PROBLEM!

- 2013 construction start
- Cost: ~760 M$
- Nearby Lule River generates 9% of Sweden's electricity (~4.23 GW)
- Average annual temperature: 1.3 °C

	Specifications
Performance*	**27-51 PFLOP/s**
Memory*	**21-27** PB RAM **1900-6800** PB disk
Power	**84** MW avg* (120 MW max)
Space	**290,000** ft^2 (27,000 m^2)
Cooling*	~1.07 PUE

* estimated

Superconductor computing looks promising



D.S. Holmes, et al.,
IEEE Trans. Appl. Supercond., 2013,
DOI: 10.1109/TASC.2013.2244634

Interconnect Requirements (Superconductor HPC)

Desirable architectural metrics for supercomputers designed for floating-point-intensive applications

- Main memory:
  0.1 to 1 B s/FLOP
- Main memory latency (access time):
  < 100 cycles
- Main memory data access rate:
  1 B/FLOP
- Input/Output data rate:
  10^{-5} to 10^{-3} B/FLOP
- Parallelism:
  fewer processors is generally better

TABLE II
INTERCONNECT POWER DISSIPATION AT 4 K

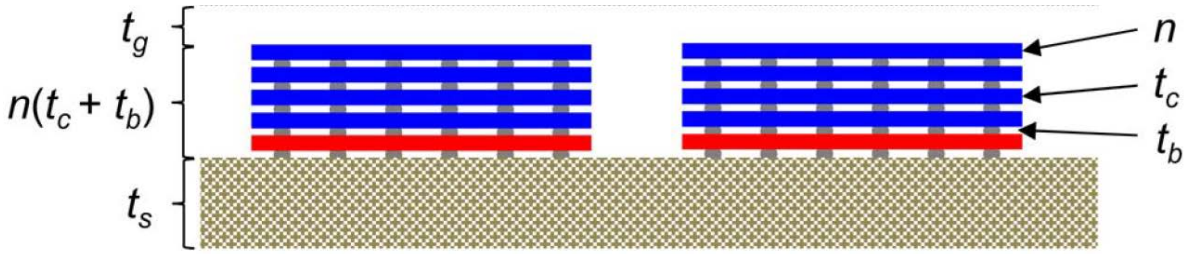
	System Performance (PFLOP/s)			
	1	10	100	1,000
I/O data rate [a] (Tbit/s)	0.8	8	80	800
• Channels [b], 20 Gbit/s	• 80	• 800	• 8,000	• 80,000
Power leads	c	c	c	c
Input data	c	c	c	c
Cache memory access	18 mW	180 mW	1.8 W	18 W
Main memory access	9 mW	90 mW	0.9 W	9 W
Output data	10 mW	100 mW	1.0 W	10 W
• Drivers, eSFQ-to-DC [d]	• 0.024	• 0.24	• 0.002	• 0.024
• Ribbon cable to 40 K	• 8.3	• 83	• 0.83	• 8.3
• VCSEL array at 40 K [d]	• 0 [e]	• 0 [e]	• 0 [e]	• 0 [e]
Interconnects, total	**0.1 W**	**1 W**	**10 W**	**100 W**
I/O budget	0.4 W	3 W	30 W	300 W

[a] Specified using the mid-range I/O data rate (10^{-4} B/FLOP)·(8 bit/B).
[b] Channel capacity is 2 times the specified I/O data rate.
[c] No estimate made. [d] [47].
[e] Vertical-cavity surface-emitting laser (VCSEL) heat load is less than refrigerator intermediate stage capacity, so no effect on 4 K capacity.

D.S. Holmes, et al.,
IEEE Trans. Appl. Supercond., 2013,
DOI: 10.1109/TASC.2013.2244634

Area and Volume (Superconductor HPC)

- Ranges calculated for stacks of 1 to 5 chips



- Packaged volume (V) relationship to active circuit area (A_a)

$$\left(\frac{V}{A_a}\right)_{MCM} = [t_g + t_s + n(t_c + t_b)]\,(f \cdot n)^{-1} \qquad (3)$$

where:

t_g	2 to 10 mm; vertical gap between stacked MCMs
t_s	0.5 to 1 mm; thickness of the MCM substrate
t_c	50 to 200 μm; thickness of a circuit chip
t_b	10 to 30 μm; thickness added by bump bonds
n	1 to 5; number of chips in a stack
f	0.4 to 0.6; effective in-plane area fraction covered by chips, including MCM-to-MCM horizontal spacing

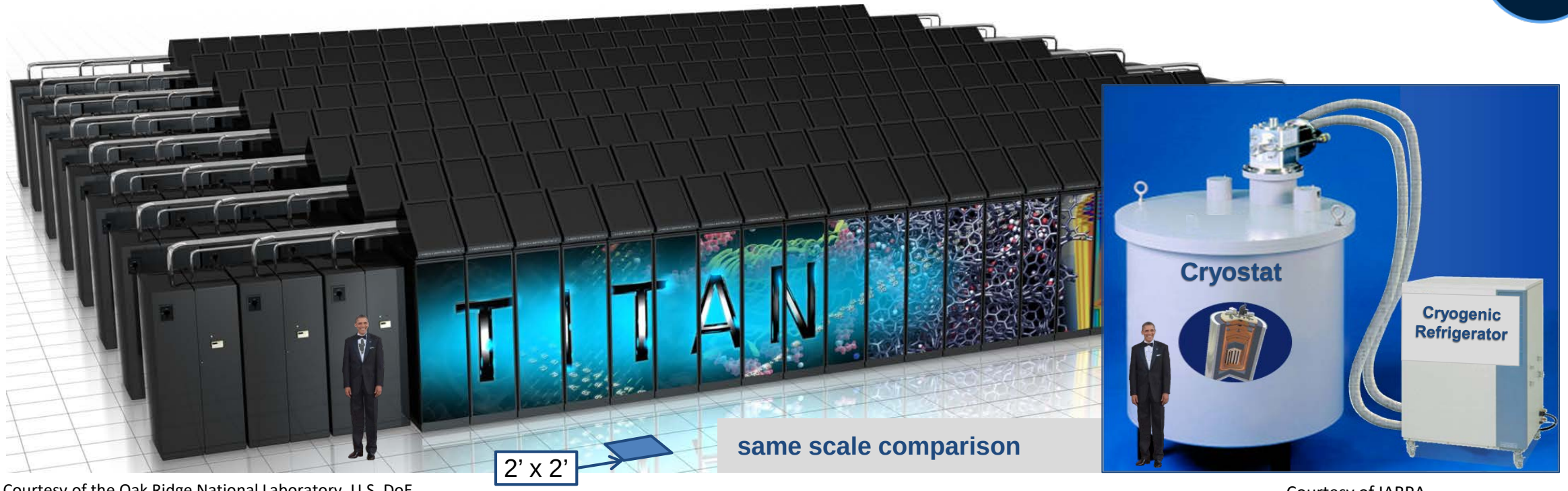
D.S. Holmes, et al., *IEEE Trans. Appl. Supercond.*, 2013.
DOI: 10.1109/TASC.2013.2244634

TABLE III
CIRCUIT AREA AND CRYOSTAT VOLUME RANGES

	System Performance (PFLOP/s)			
	1	10	100	1,000
Logic, processors [a]	40,200	402,000	4,020,000	40,200,000
• circuit area [b] (m^2)	80.4	804	8,040	80,400
• MCM volume (m^3)	0.08-2.4	0.8-24	8-240	80-2,400
Memory [c] (PB)	1	10	100	1,000
• circuit area (m^2)	1.1e+3	1.1e+4	1.1e+5	1.1e+6
• MCM volume (m^3)	1.1-33	11-330	110-3,300	1,100-33,000
Interconnect channels [d]	80	800	8,000	80,000
• circuit area (m^2)	1.2	12	120	1,200
• MCM volume (m^3)	0.002-0.06	0.02-0.6	0.2-6	2-60
Other [e] (m^3)	0.1-3.3	1-33	10-330	100-3,300
System volume				
• high (m^3)	39	390	3,900	39,000
• low (m^3)	1.3	13	130	1,300

[a] RQL, $I_c = 25$ µA, 8.3 GHz [48].
[b] 2×10^7 Josephson junctions per processor, 10^{10} JJ/m^2.
[c] Josephson MRAM [48], 1 byte per FLOP/s, 900 GB/m^2.
[d] Specifications in Table II, circuit area is 5% of logic area.
[e] Cryostat + structure estimated as 10% of total MCM volume.

Power-Space-Cooling Comparison



Courtesy of the Oak Ridge National Laboratory, U.S. DoE

Courtesy of IARPA

	Titan at ORNL	Superconductor Supercomputer	
Performance	**17.6** PFLOP/s (#2 in world*)	**20** PFLOP/s	~1x
Memory	**710** TB (0.04 B/FLOPS)	**5** PB (0.25 B/FLOPS)	7x
Power	**8,200** kW avg. (not included: cooling, storage memory)	**80** kW total power (includes cooling)	0.01x
Space	**4,350** ft^2 (404 m^2, not including cooling)	~**200** ft^2 (19 m^2, includes cooling)	0.05x
Cooling	additional power, space and infrastructure required	All cooling shown	

* #1 in Top500, 2012-11 (17.6 PFLOP/s)

C3 program goals

- Develop technologies for a computer based on superconducting logic with cryogenic memory, and
- Integrate a prototype that can answer these questions:

1) Can we build a superconducting computer capable of solving important problems?
2) Does it provide a sufficient advantage over conventional computing that we want to build it?

Technical Challenges 1

- **Memory**: energy-efficient, fast, dense, useful capacity, compatible with superconducting single flux quantum (SFQ) logic for direct integration
  - C3 ideas include MRAM, spin Hall effect, JMRAM, nMEM
  - Requires interface circuits of significant complexity in SFQ technology
  - Requires understanding new physics with interplay of spintronics and superconductivity

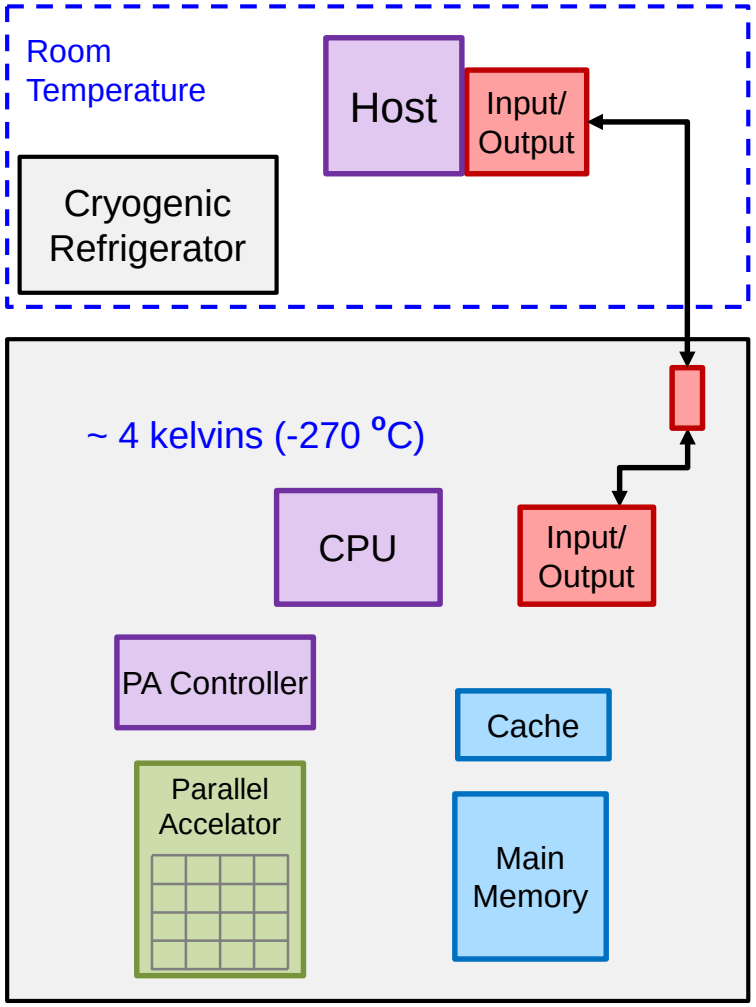
- **Logic complexity**: designing superconducting integrated circuits with far more elements on a single chip than previously achieved
  - In SFQ computing, the devices are Josephson junctions and the logic elements are picosecond wide pulses; these present new design challenges.
  - Electronic design automation tools are either missing or not scalable to very large scale integration

Technical Challenges 2

- **Advanced fabrication process:** multilayer, sub-micrometer feature size with specialty layers (high kinetic inductance, milliohm resistance ...)
  - Variance of key fabrication parameters (J_C, inductance) must be improved
  - Must develop detailed simulation module that includes process variations
  - Close coupling between circuit design-test and process design rules is key
  - Need to develop close coupling between foundry and failure analysis team

- **System**: demonstrate a superconducting computer with multiple processors and memory in MCM packaging; beyond C3 challenges include:
  - scalable system design
  - wafer-scale stacking with superconducting through silicon vias
  - high data-rate interconnect between 4 K and room temperature

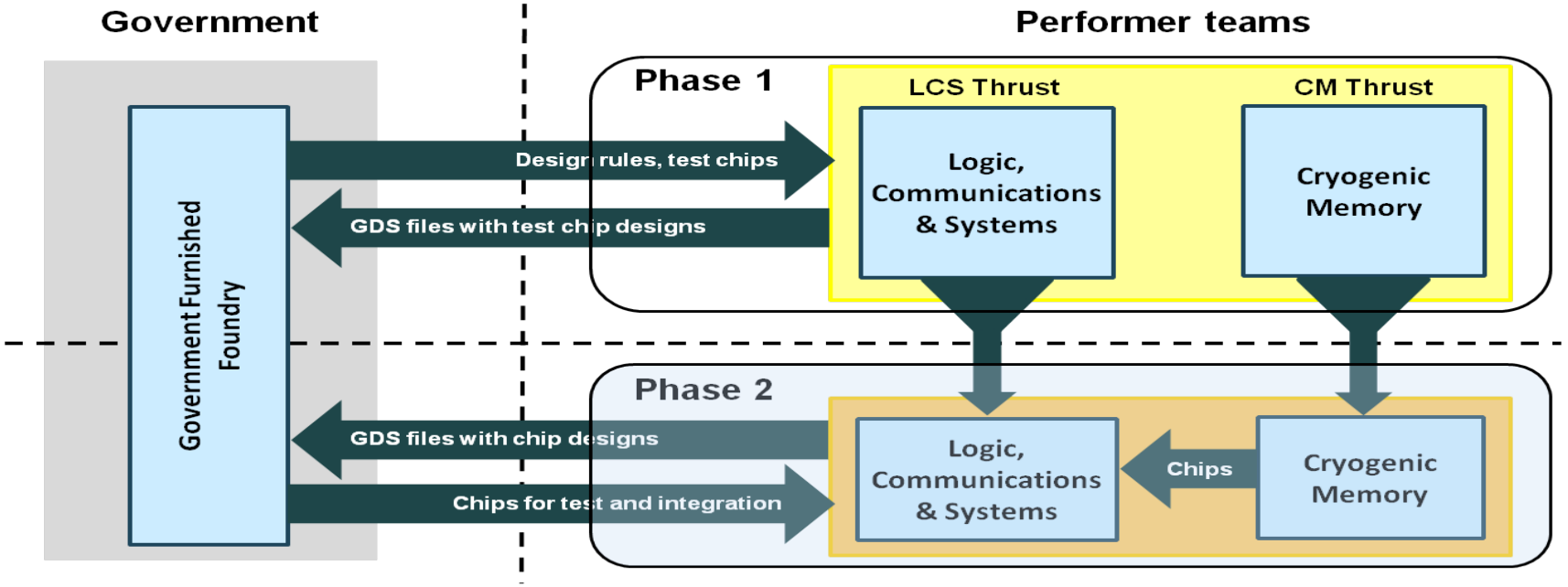
C3 Notional System, Metrics, and Goals



Metric	Goal
Clock rate for superconducting logic	10 GHz
Throughput (bit-op/s)	10^{13}
Efficiency @ 4 K (bit-op/J)	10^{15}
CPU count	1
Word size (bit)	64
Parallel Accelerator count	2
Main Memory (B)	2^{28}
Input/Output (bit/s)	10^{9}

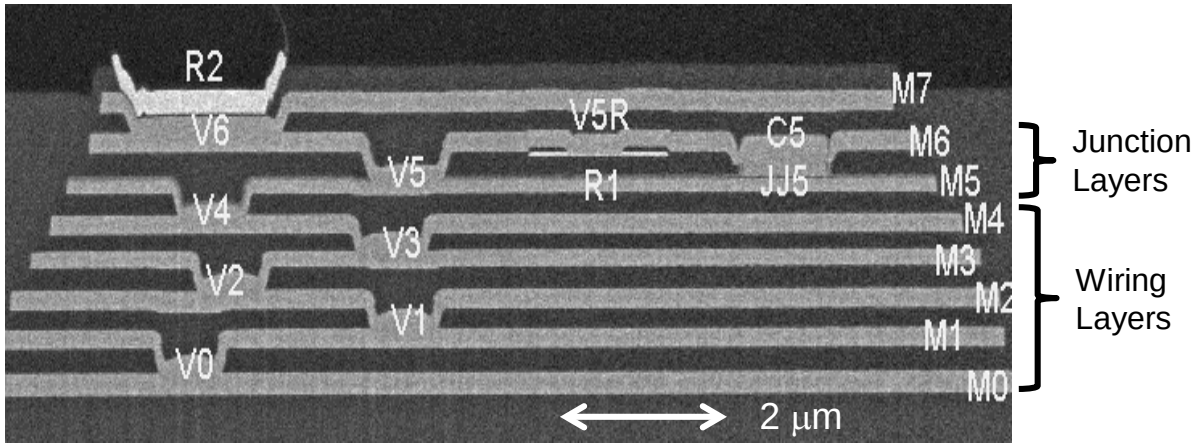
C3 Organization

- Two thrusts:
  - Logic, communications and systems (**LCS**)
  - Cryogenic memory (**CM**)
- Two phases:
  - Phase 1, performers develop technology for subsystems
  - Phase 2, performers scale up and integrate technology into a working prototype



Advanced fabrication process for SCE

- No commercial foundry exists that can fabricate circuits at the required level of complexity.
- MIT Lincoln Laboratory (LL) has a niobium superconductor circuit foundry that IARPA is upgrading to meet the aggressive program goals.
- With 200 mm wafers and 8+ planarized niobium layers, **the MIT LL superconducting foundry is now the most advanced in the world – and continues to advance.**
- LL will transfer the technology elsewhere as directed.
- ✓ Test chips with up to **810,000** JJs all working have been successfully demonstrated in the 8-Nb-layer process.



8 niobium layer cross-section

SFQ Technology Roadmap for IARPA C3

Fabrication Process Attribute		Units	Process Node					
			SFQ3ee	SFQ4ee	SFQ5ee	SFQ6ee	SFQ5hs	SFQ7ee
Critical current density		MA/m^2	100	100	100	100	200	100
JJ diameter (surround)		nm	700 (500)	700 (500)	700 (500)	700 (300)	700 (500)	500 (200)
Nb metal layers		-	4	8	8	9	8	10
Line width (space)	Critical layers	nm	500 (1000)	500 (700)	350 (500)	350 (400)	350 (500)	250 (250)
	Other layers	nm			500 (700)	500 (700)	500 (700)	350 (500)
Metal thickness		nm	200	200	200	200	200	200
Dielectric thickness		nm	200	200	200	200	200	200
Resistor width (space)		nm	1000 (2000)	500 (700)	500 (500)	500 (500)	500 (700)	350 (350)
Shunt resistor value		Ω/sq	2	2	2 or 6	2 or 6	2 or 6	2 or 6
mΩ resistor		mΩ	-	-	3 - 10	3 - 10	3 - 10	3 - 10
High kinetic inductance layer		pH/sq	-	-	8	8	8	8
Via diameter (surround)		nm	700 (500)	700 (500)	600 (300)	500 (250)	500 (350)	350 (250)
Via type, stacking		-	Etched, Staggered	Etched, Stacked \2/	Etched, Stacked \2/	Stud Stacked \2/	Etched, Stacked \2/	Stud, Stacked
Early access availability		-	2013	2014	2015	2016	2017	2018

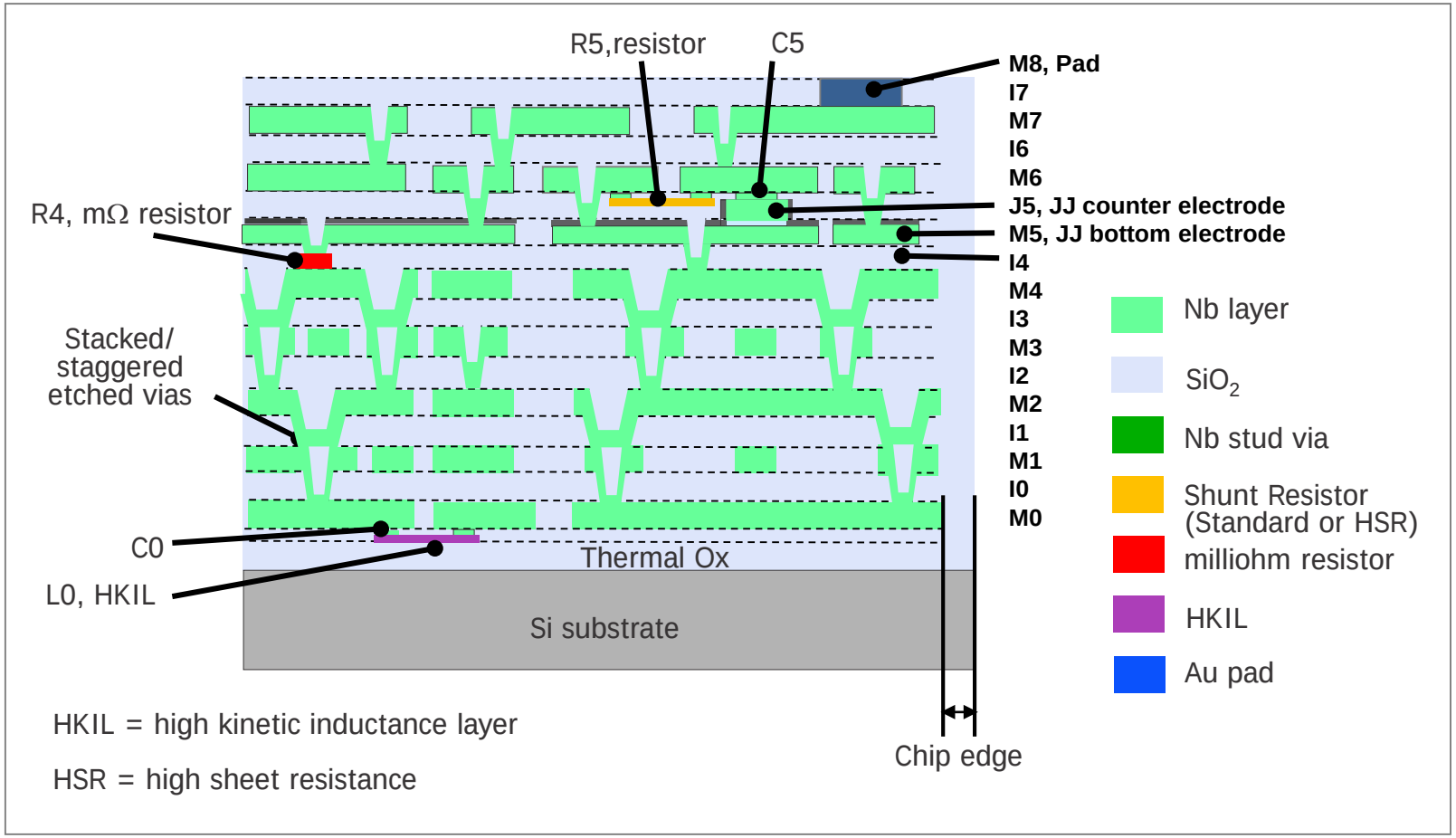
October 2017 update

Changes from the previous process

Stopped here!

SFQ5ee Process Node at MIT-LL

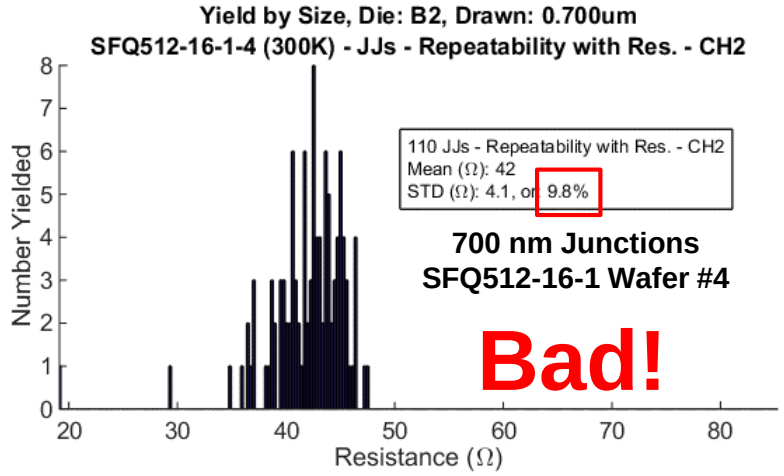
- 8 Nb layers
- 700 nm (min.) Josephson junctions
- JC target: 100 μA/mm2
- Wiring (min.): 350 nm width, 500 nm spacing
- Options:
  - High kinetic inductance (HKI) layer
  - High sheet resistance (HSR) layer



Junction Resistance Distributions

700 nm Junctions
SFQ511-15-1 Wafer #1

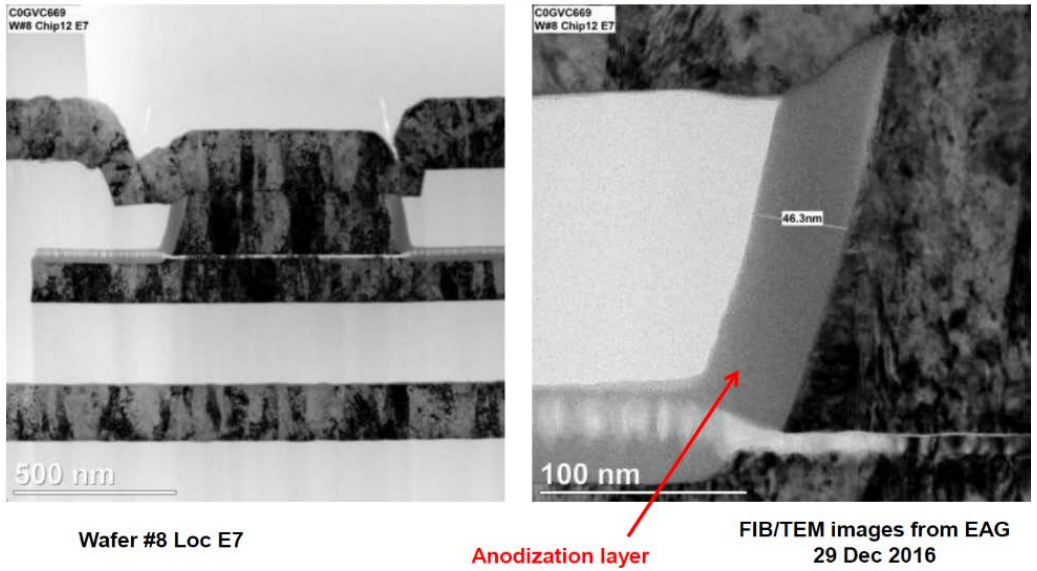
Good



700 nm Junctions
SFQ512-16-1 Wafer #4

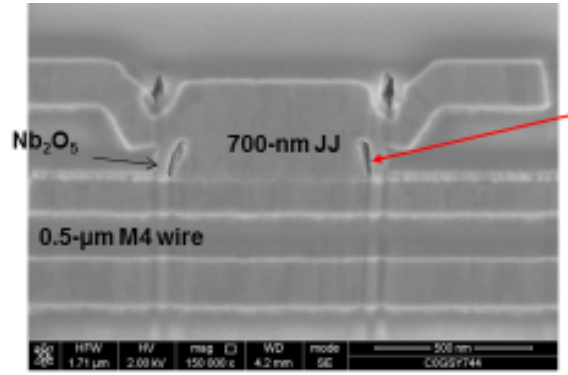
Bad!

SFQ515-16-2, PCM Chip 12, 0.7 μm JJ



Wafer #8 Loc E7

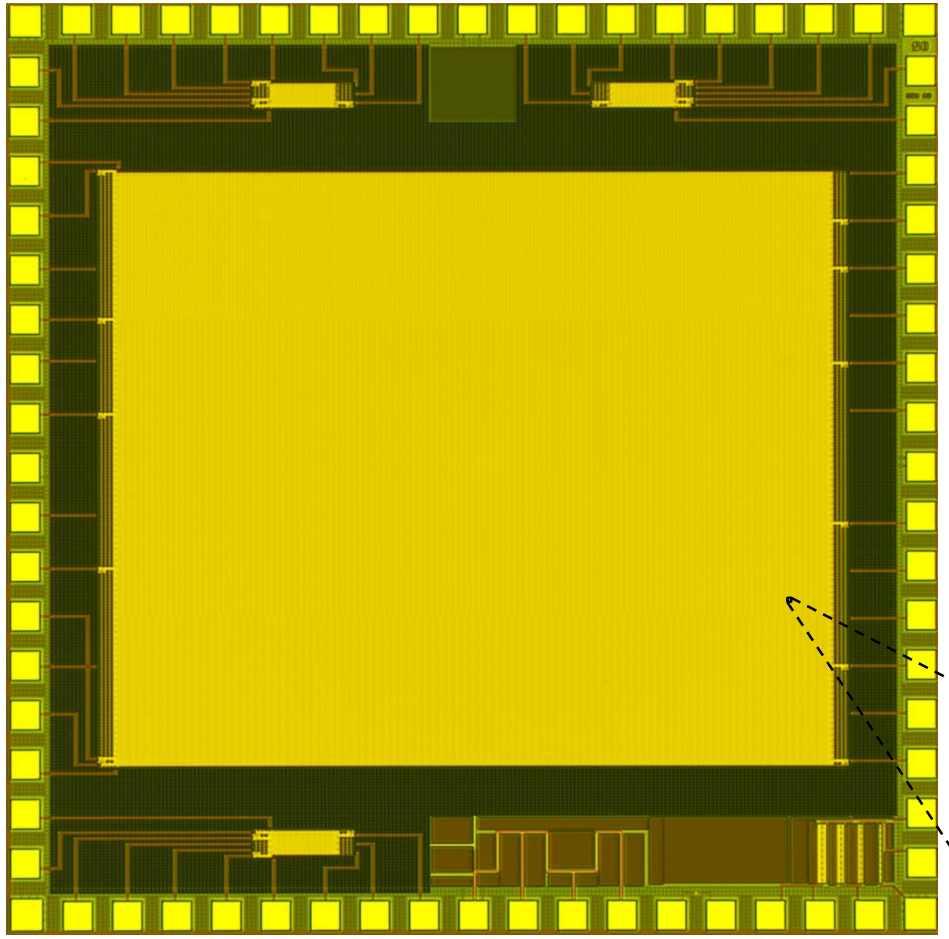
FIB/TEM images from EAG
29 Dec 2016

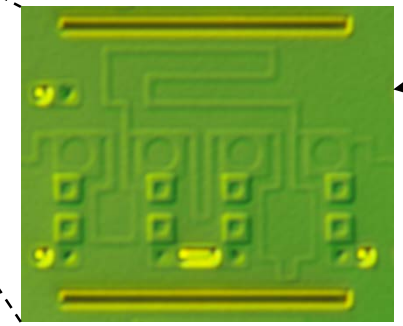


Delamination of anodized Nb_2O_5 possibly due to topography-related stress during CMP

- FIB cross sections of the damaged junctions on M4 and on M3+M4 wires indicate Nb_2O_5 delamination/cracking in 100% of the cross-sectioned JJs
- Possible damage mechanism
  - delamination (cracking) of the anodization layer protecting the JJ interior
  - reaction of the exposed AlO_x tunnel barrier with the environment

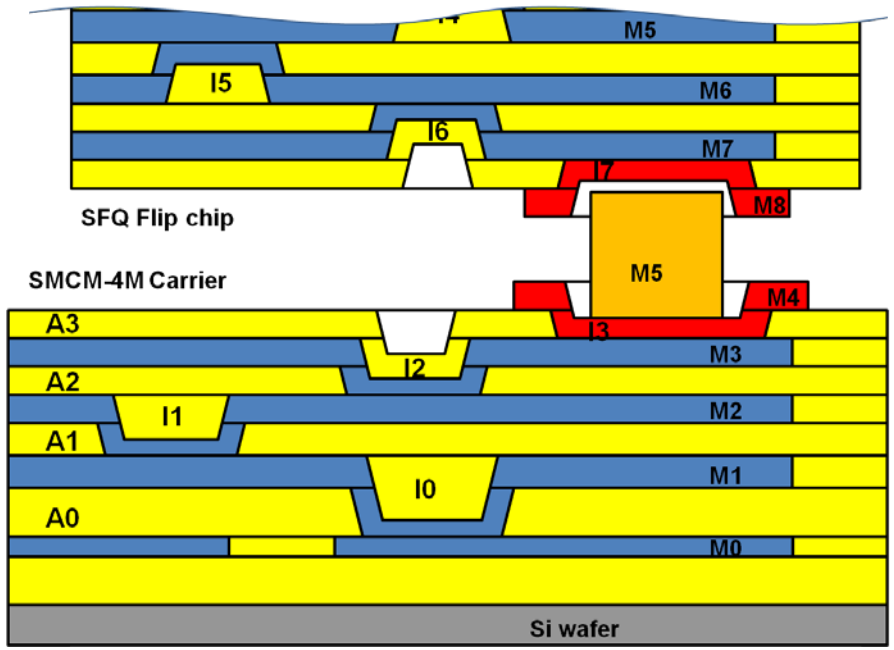
New record for Josephson junction (JJ) circuit complexity

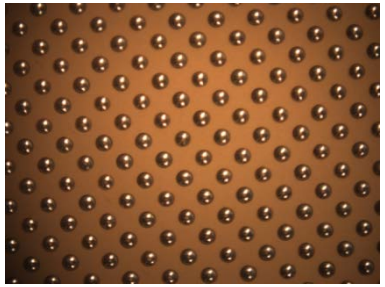




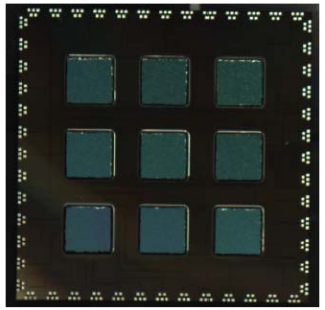
- MIT LL process monitor circuit
- 202,280-bit shift register
- 810,000+ JJs on 1 cm^2 chip
- Cell size: 20 μm x 15 μm
- JJ density: $1.33 \cdot 10^6$ JJ/cm^2
- Status: fabricated, operational with margins
- **Integration scale**: close to Intel's 1993 Pentium: 0.8 μm process, 3.1 M transistors on a 294 mm^2 chip

Flip-Chip Superconducting MCM Packaging





15-μm indium bumps on 35 μm pitch



9-chip (SFQ) on S-MCM assembly

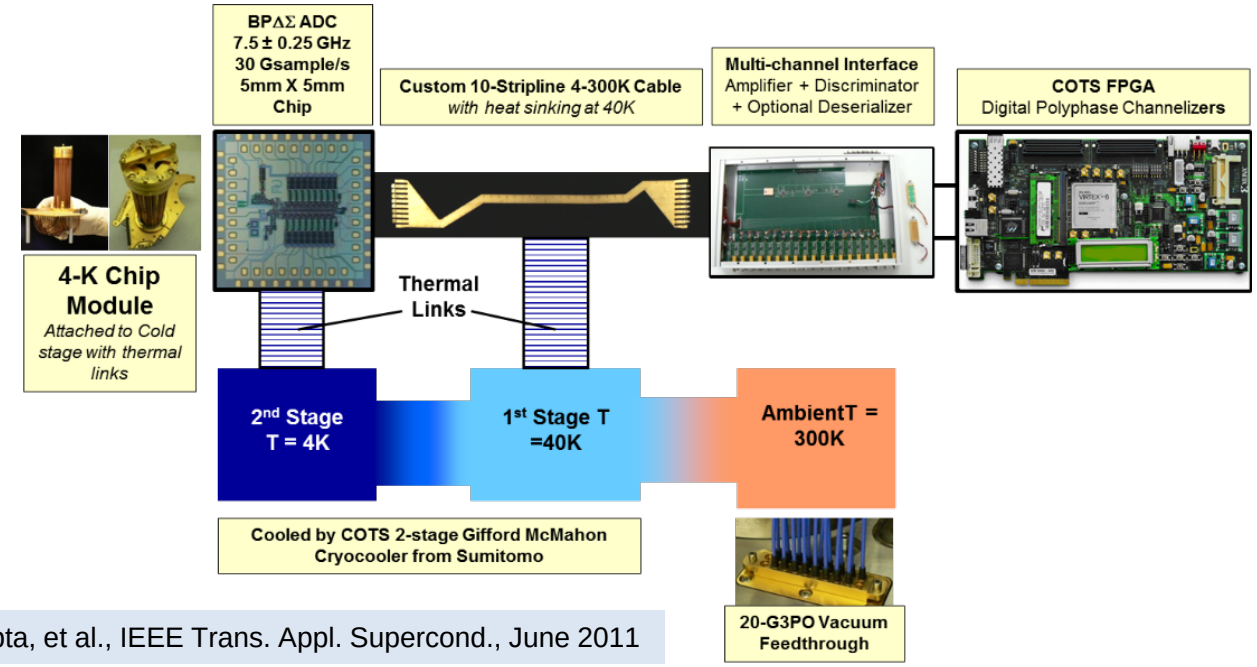
MIT Lincoln Laboratory

- **Flip-chip attachment of SFQ chips to S-MCM carriers**
- **Indium bumps: 8-15 mm diameter on 35 mm pitch**
- **Up to $7 \cdot 10^4$ bumps per chip in flip-chip MCMs demonstrated**
- **32 mm x 32 mm MCM size (up to 5 cm by 5 cm possible), i-line photolithography**

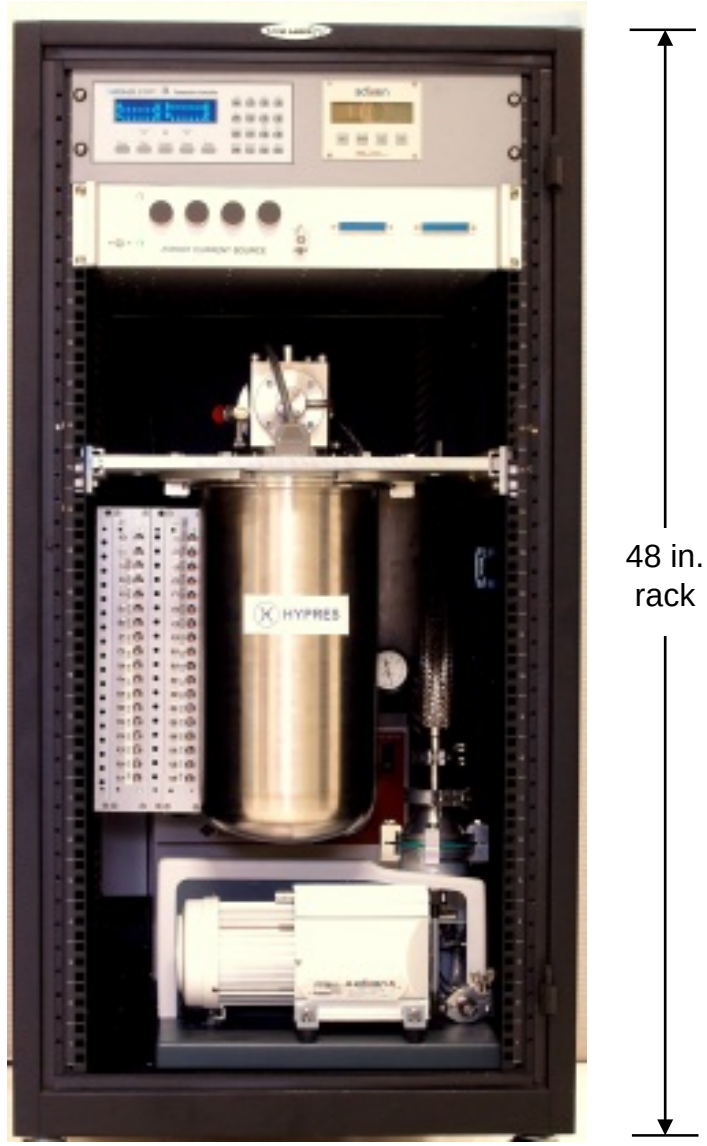
Related Work

Digital-RF receiver (Hypres)

- Commercial product with applications in:
  - Software-defined radio, satellite communications
- Directly digitizes RF (no analog down-conversion)
  - Ultra-wide bandwidth, multi-band, multi-carrier
- Hybrid temperature heterogeneous technology
  - Different technologies between ambient and 4 K
  - Closed-cycle cryogenic refrigerator

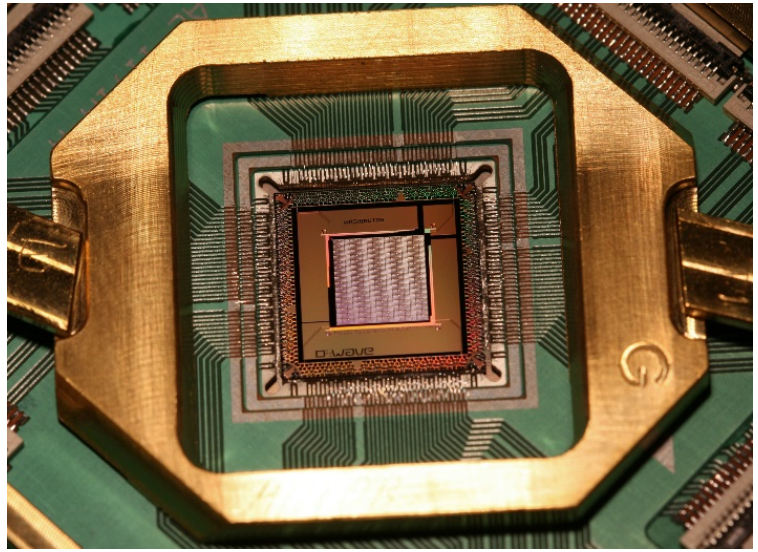


Gupta, et al., IEEE Trans. Appl. Supercond., June 2011



Quantum annealing (D-Wave Systems)

- D-Wave® TwoXTM (2015 August 20), a commercial superconducting quantum annealing processor
- 128,000 Josephson junctions
- 1000 qubit array
- 15-20 mK operating temperature



“Washington” chip

D-Wave® TwoX™ quantum annealing processor

Chinese announce effort in August 2018

Can China build a US$145 million superconducting computer that will change the world?

Chinese scientists are embarking on a one-billion yuan, high-risk, high-reward plan to build low-energy top-performance computing systems

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COMMENTS: 57

https://www.scmp.com/news/china/society/article/2161390/can-china-build-us145-million-superconducting-computer-will

- Superconducting digital circuits and superconducting computers
- 100 mm foundry (currently)

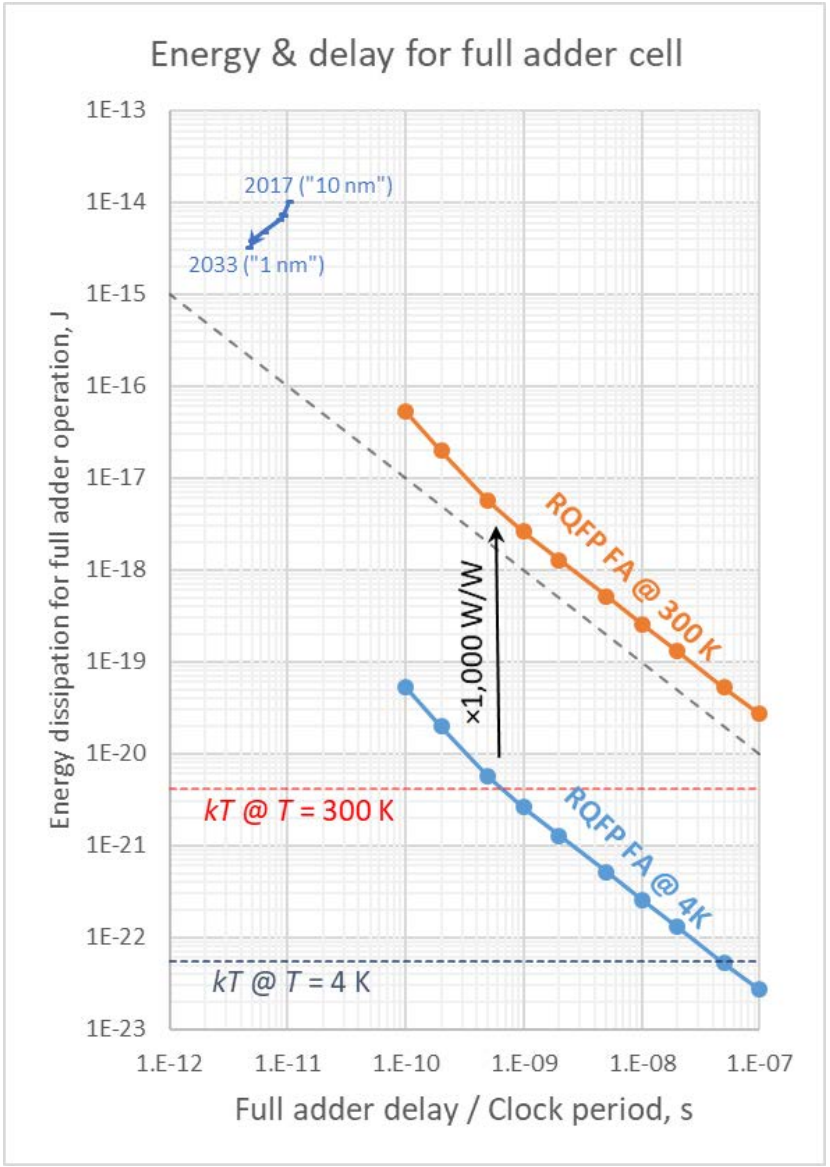
AQFP logic is achieving extremely low energy computation

ics Letters

An adiabatic superconductor 8-bit adder with $24k_BT$ energy dissipation per junction

Cite as: Appl. Phys. Lett. **114**, 042602 (2019); https://doi.org/10.1063/1.5080753
Submitted: 12 November 2018 . Accepted: 14 January 2019 . Published Online: 29 January 2019

Naoki Takeuchi, Taiki Yamae, Christopher L. Ayala, Hideo Suzuki, and Nobuyuki Yoshikawa



Plot by M. Frank, Sandia National Laboratories

International Roadmap for Devices and Systems (IRDS)

2. Superconductor Electronics (SCE)

2.1. Introduction

2.2. Applications and Market Drivers for SCE

- 2.2.1. Cloud (Digital Computing)
- 2.2.2. Measurement & Calibration Systems
- 2.2.3. Communications

2.3. Present Status for SCE

- 2.3.1. Logic
- 2.3.2. Memory
- 2.3.3. Other Circuit Elements for SCE
- 2.3.4. Architecture
- 2.3.5. Fabrication for SCE
- 2.3.6. Electronic Design Automation (EDA) for SCE
- 2.3.7. Packaging and Testing for SCE
- 2.3.9. Interconnects for SCE
- 2.3.10. Refrigeration

2.4. Benchmarking and Metrics for SCE

- 2.4.1. Device and Circuit Benchmarking
- 2.4.2. System and Application Benchmarking

2.5. Active Research Questions for SCE

2.6. Roadmap for SCE

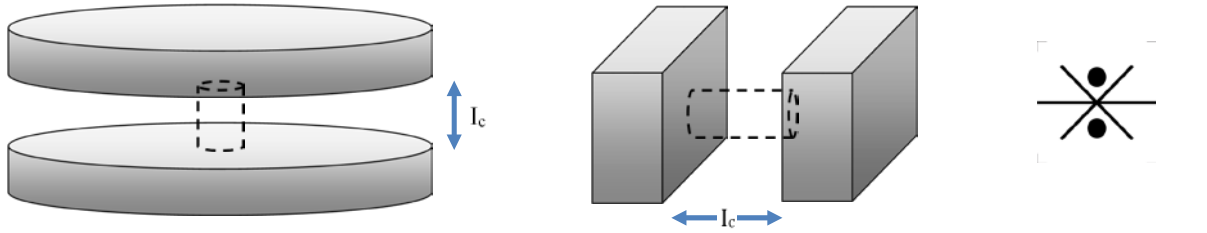
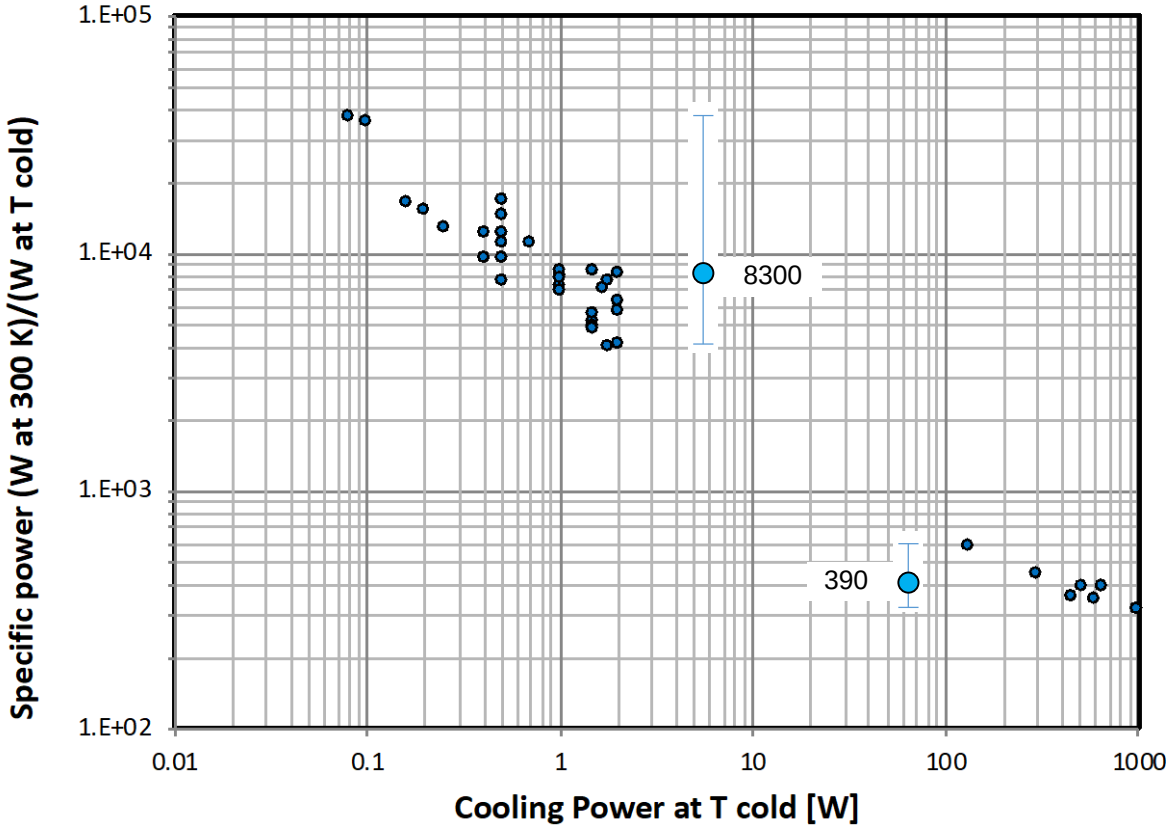


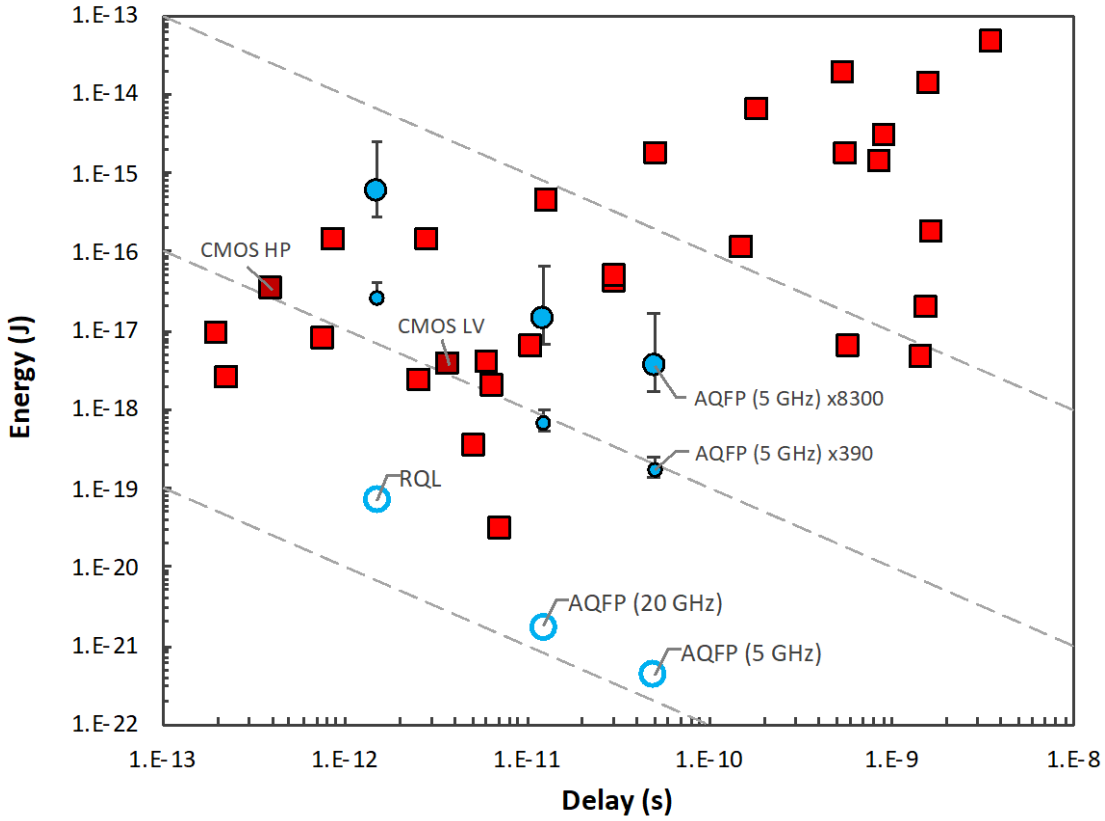
Figure CEQIP-1. Josephson Junction Device Structures

Benchmarking and Metrics for SCE (IRDS CEQIP 2018)

Methodology established for comparison with other technologies



Cryogenic Refrigeration Systems for T ~ 4 K



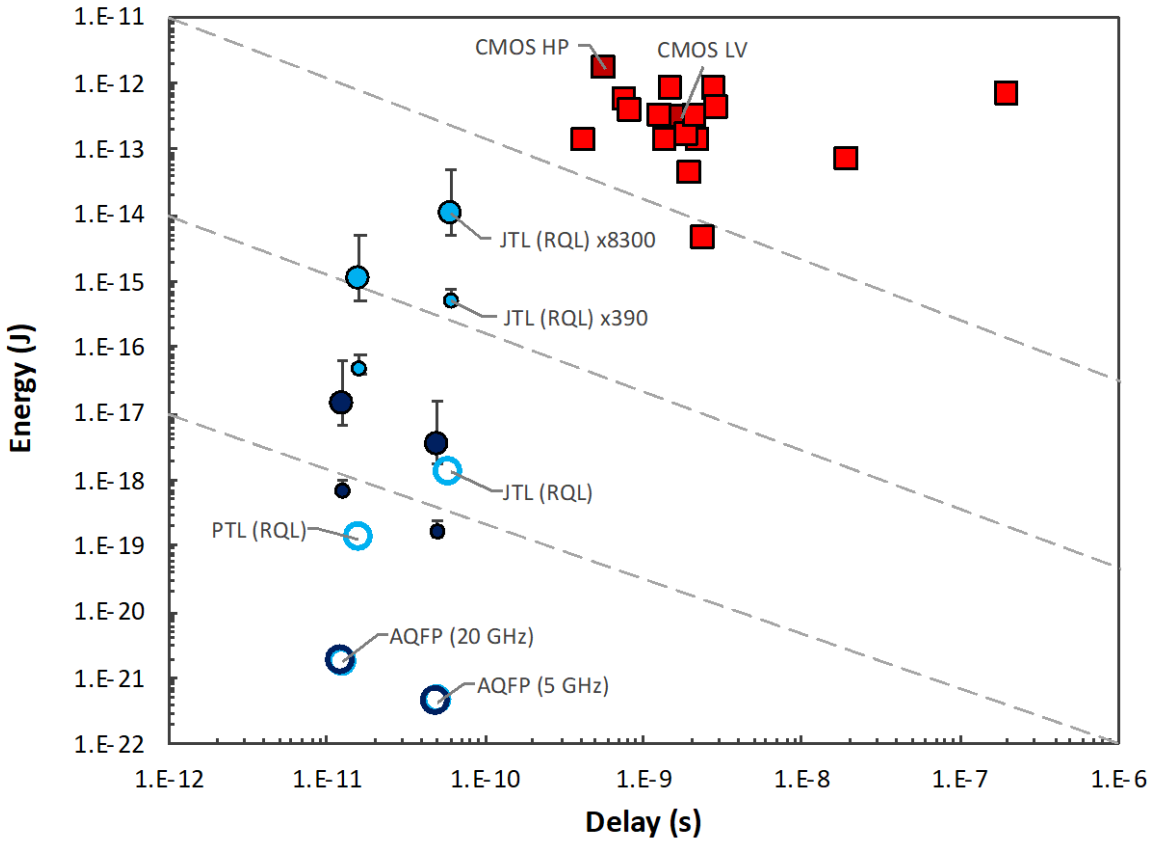
Energy versus delay for intrinsic elements

Note: Superconductor devices (AQFP, RQL) have open circles for operation at ~4 K and solid circles with whiskers showing ranges including refrigeration power from Table CEQIP-7. The upper solid circles with ranges are for small-scale refrigerators (cryocoolers) with cooling powers less than 10 W. All other devices are from [359]. Dashed lines show constant energy-delay products.

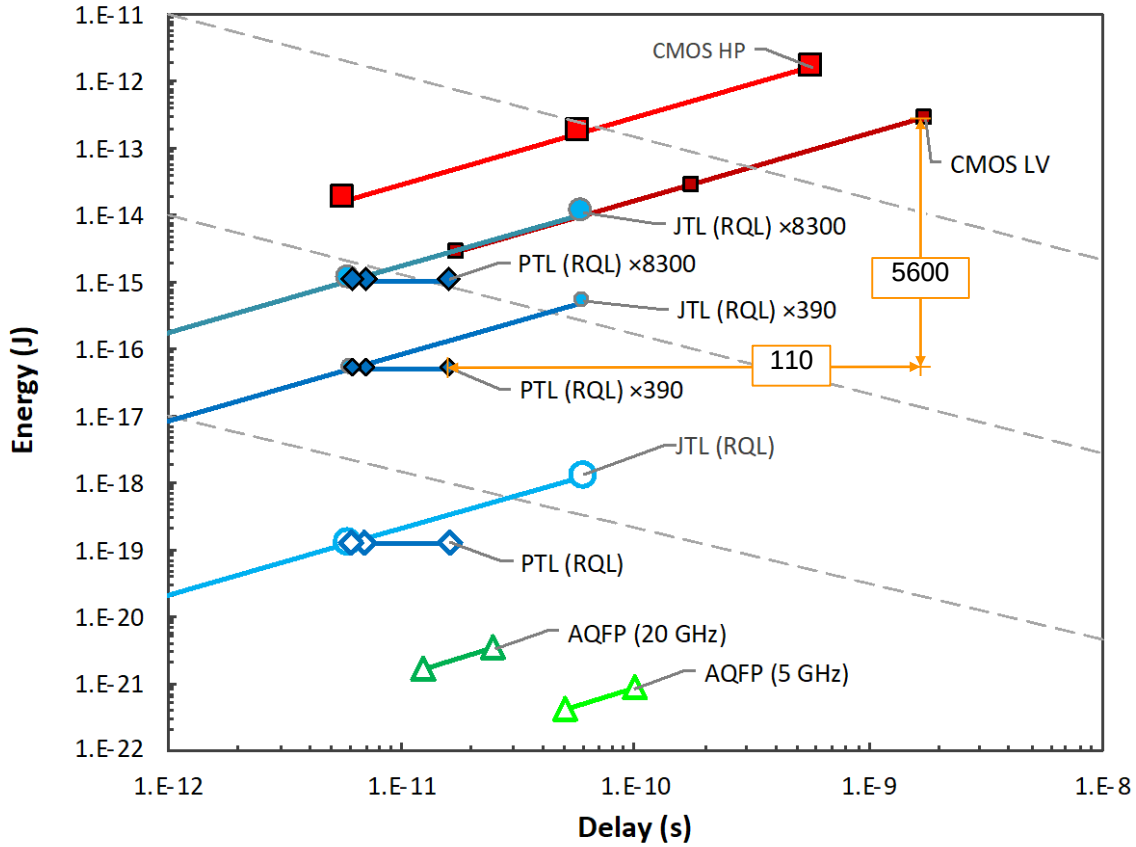
https://irds.ieee.org/

Benchmarking and Metrics for SCE (IRDS CEQIP 2018)

Methodology established for comparison with other technologies



Energy versus Delay for Interconnects of 1 mm Length



Energy versus delay for 0.01 to 1 mm Length

Note: Superconductor devices (AQFP, RQL) have open circles for operation at ~4 K and solid circles with whiskers showing ranges including refrigeration power from Table CEQIP-7. The upper solid circles with ranges are for small-scale refrigerators (cryocoolers) with cooling powers less than 10 W. All other devices are from [359]. Dashed lines show constant energy-delay products.

2019 Next Steps for SCE (IRDS CEQIP 2018)

- **Models** for devices and circuits
  - Variety of superconductor technologies (e.g., RSFQ, AQFP)
  - Core metrics: circuit area, delay, and energy
  - Scaling models
- **Models** for applications
  - Logic, Memory, Interconnects
- **Roadmap**
- Connect to SA, AB, ORTC, ORSC

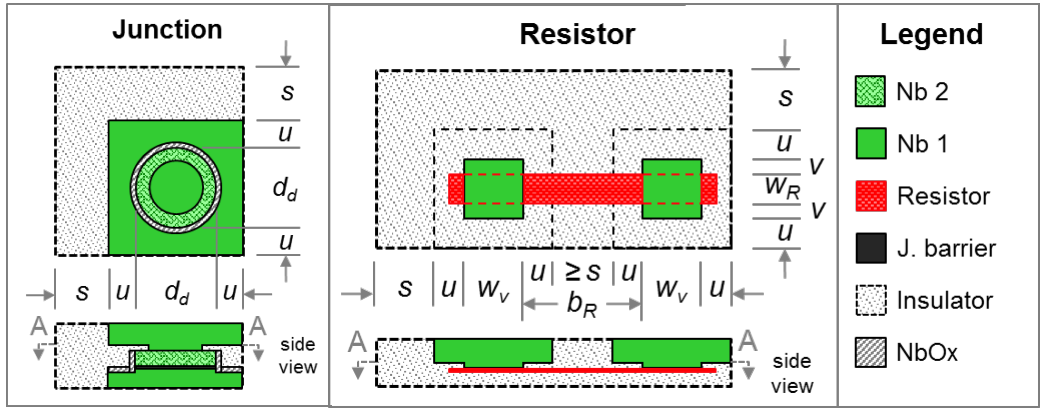
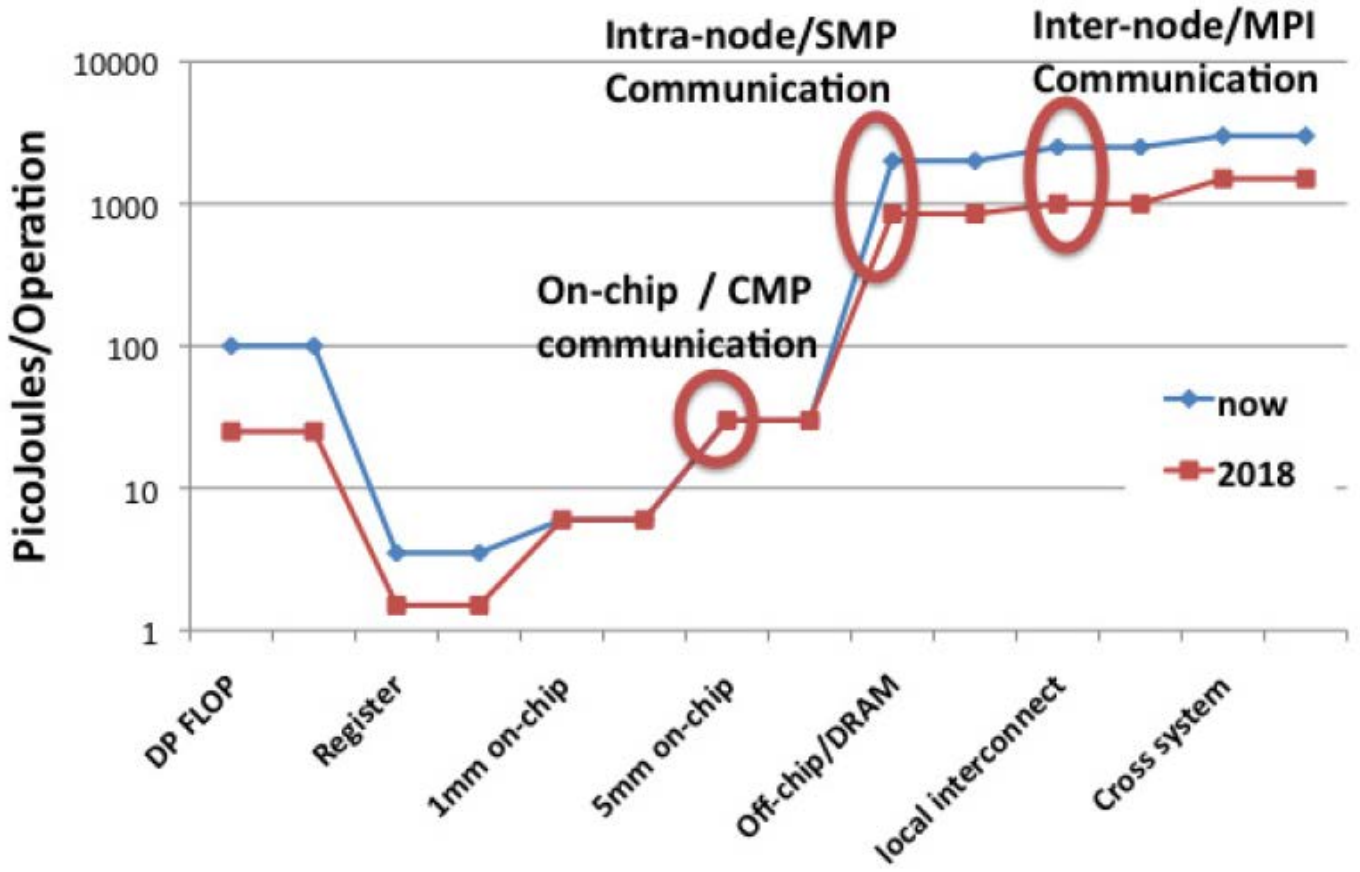


Table 2. IC technology roadmap.

	1998	2001	2004	2007	SIA 1992
Mininum feature size (μm)	1.5	0.8	0.50	0.25	0.50
Junction size (μm)	2.5	0.8	0.80	0.80	—
Critical current (A cm^{-2})	2k	20k	20k	20k	—
Gates per chip (logic)	5k	120k	600k	2M	300k
Bits per chip (SRAM)	16k	400k	2M	6M	4M
Chip size (mm^2)	100	400	400	400	250
Wafer diameter (mm)	100	150	150	150	200
Defects per cm^2	< 2	< 0.2	< 0.1	< 0.05	< 0.1
Number of interconnect levels	3	4–5	5–6	6	3
Number of resistor layers	2	2	2	2	—
Planarization	No	Yes	Yes	Yes	Yes
Vertical resistors	No	No	Yes	Yes	—
I/O count	128	2k	2–5k	2–5k	500
Wafer starts per month	12	200	1k	1k	$>$ 20k
	SCE				**CMOS**

Abelson et al. (1999) “Manufacturability ...” doi: 10.1088/0953-2048/12/11/363

Energy vs. distance: conventional technology (IRDS CEQIP 2018)



- Needed: comparison with SCE!

Fig. 2. Energy cost of data movement relative to the cost of a flop for current and 2018 systems

Plot: Shalf, Dosanjh, Morrison, "Exascale Computing Technology Challenges," 2011, doi:10.1007/978-3-642-19328-6_1
Slide: IRDS_Spring2019_Read-out_CE&QIP

DIFFICULT CHALLENGES for SCE (IRDS CEQIP 2018)

Technology Road Blocks…Highlight gaps and showstoppers, possible disconnects within the roadmap

- Near term
  - EDA tools for superconductor electronics
    - EDA tools for CMOS are not adequate for SCE. Inductance is critical in superconducting circuits and connecting wires must have inductance values within a specified range. Circuit simulators and timing analysis must be modified for pulse-based logic.
  - PDKs for fabrication processes
    - Complete process design kits (PDKs) are needed for fabrication processes for superconductor electronics.
  - Yield improvement of circuits with > 1 M Josephson junctions (switching devices)
    - Variation in device parameters reduces the operating margins of circuits. Needed is better process control, better device designs, or circuit designs that tolerate or compensate for device variability.
- Long term
  - Temperature limits compatible with CMOS fabrication processes
    - Nb/Al-AlO_x/Nb Josephson junctions are sensitive to temperature. Fabrication processing temperatures are currently limited to less than 200 °C, which requires different processes than those used in CMOS technology, which has a limit of 400 °C.
  - Optical input/output (I/O)
    - Communication with room-temperature systems and networks will require a high-data-rate I/O, but interconnection cannot introduce significant heat into a low-temperature environment. Optical fiber digital links would be ideal, but efficient SFQ-to-optical converters must be developed.
  - Magnetic materials fabrication process integration
    - Magnetic materials are desired to make both memory and passive devices. Integrating magnetic materials into foundry processes will be difficult.

Challenges Remaining for Superconductor Electronics (SCE)

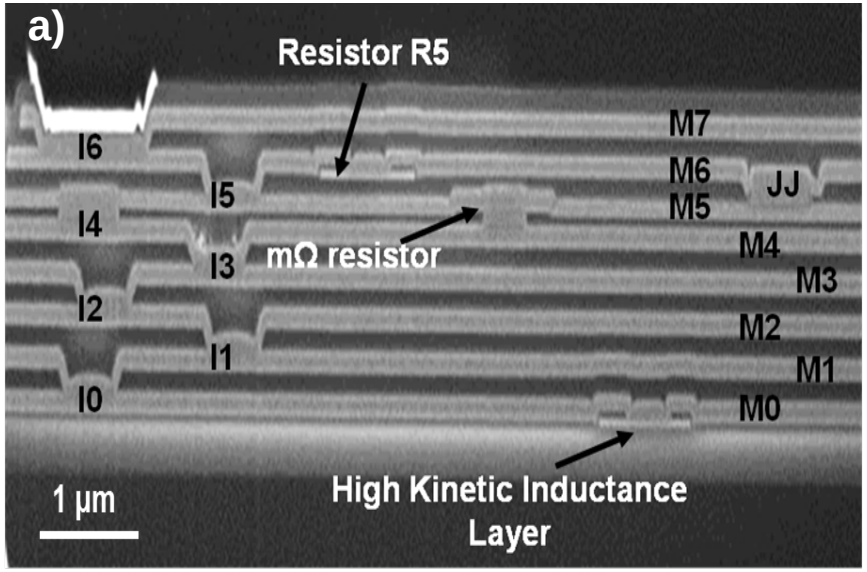
Challenges

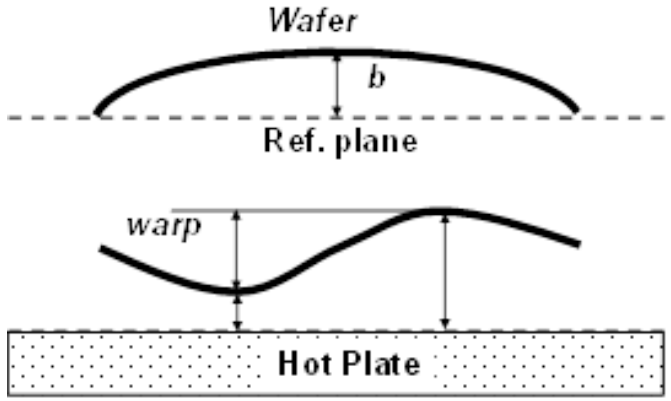
- Fabrication
- Memory
  - Magnetic memory device physics and fabrication
  - Cell size
- Superconducting circuit physics
  - Coupled current and inductance
  - Low gain from JJs
- Electronic design automation (EDA) tools } Subject of other talks
- Input/Output
  - Optical needed
  - High-speed, low heat leak
- Circuit complexity, density
- Cryogenic and (non-) magnetic environment
  - Materials and packaging
  - Refrigeration

} Future

Drawbacks of MIT-LL SFQee Process Layer Stack

- JJs are near the top of layer stack in SFQ5ee and SFQ6ee processes
- 6 to 7 patterned metal layers below
- Signal routing challenges with split wiring layers above and below the JJs
- JJ parameter spreads above patterned wires are ~ 1% larger than for JJs above ground plane
- 6 layers of SiO_2 dielectric with ~ 1 μm total thickness below the JJs
- Residual stress in PECVD SiO_2 ~ −200 MPa (compressive) and higher for HD PECVD
- Residual stress creates wafer bow of 60 μm to 70 μm
- Patterned and planarized metal layers create nonuniform stress because of nonuniform thickness of dielectric
- Wafers warp: ~ 60 μm typical

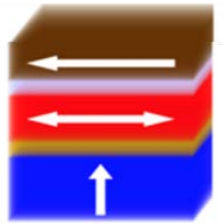


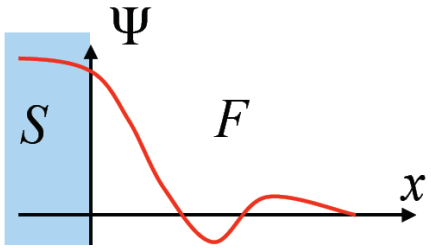


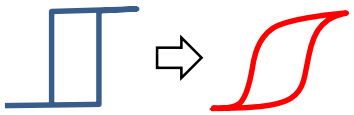
Wafer bow and warp

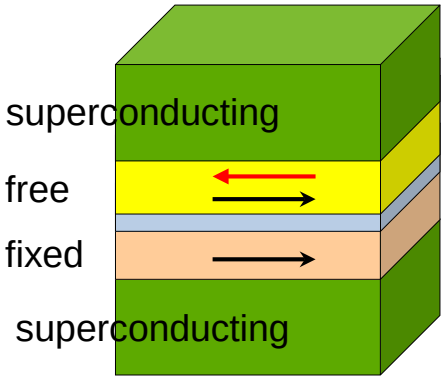
Challenges: Memory #1

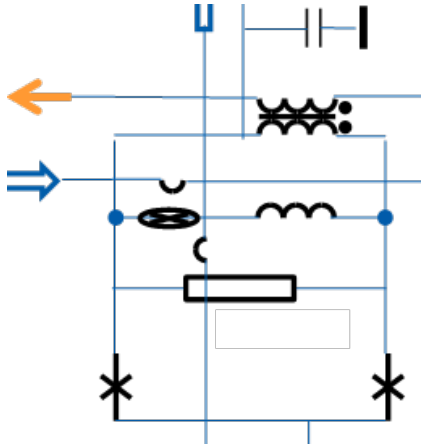
- Variety of device types with no clear winner
  - Magnetic spin valve (SV), spin Hall effect (SHE), spin-transfer torque (STT), …
  - New materials: NiFeMo, NiFeCu, NiFeNb, Co/Ru/Co, [Co/Ni]n, …
  - New physics combining spintronics and superconductivity
- Process control
  - Low energy operation and superconductivity demand thin layers
  - Thickness (~ 1 nm) exponentially affects device parameters
  - Interfacial roughness degrades properties and increases spreads
  - Properties change from room temperature to 4 K
- Memory cell size
  - Multiple devices per cell
  - No equivalent to DRAM yet





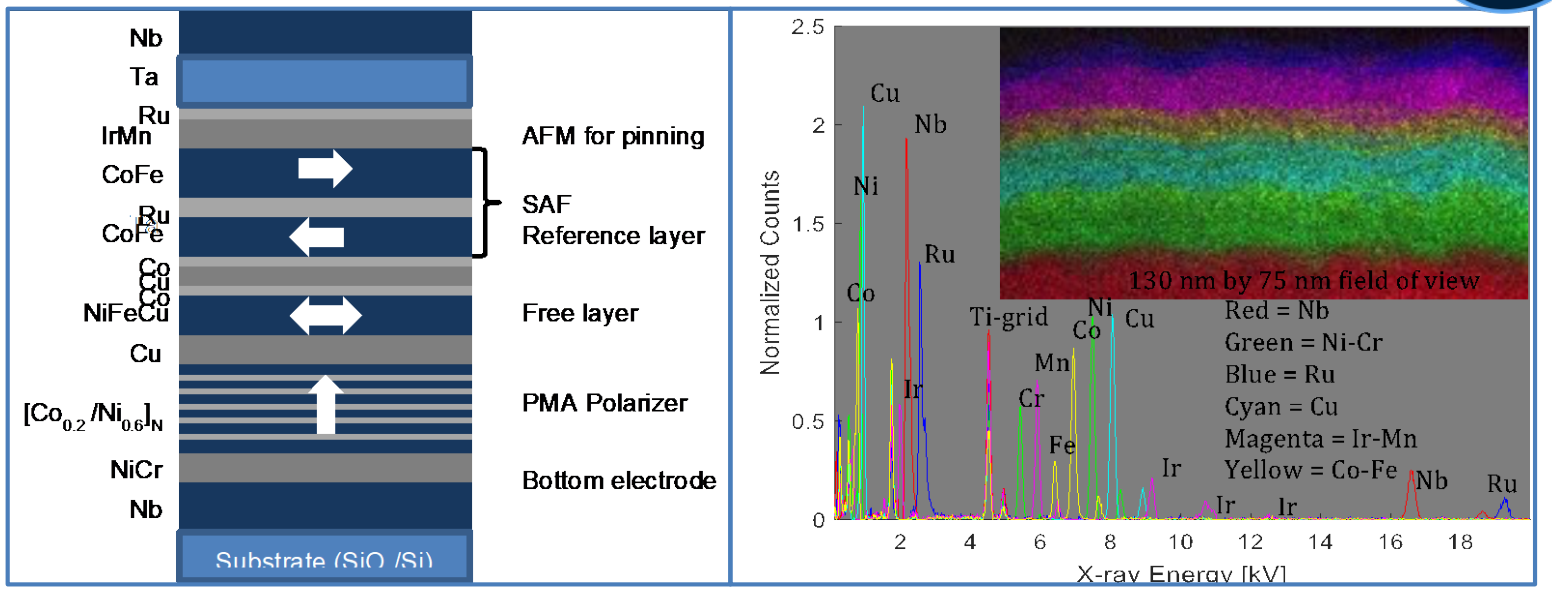


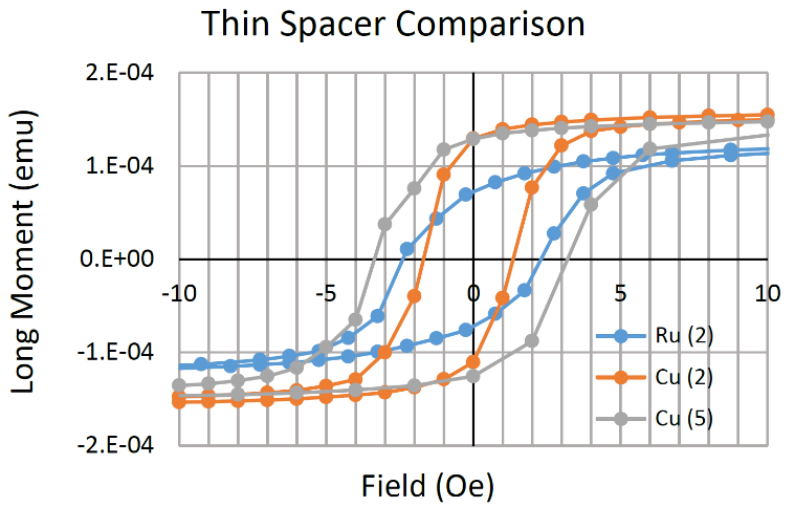




Magnetic Memory Optimization

- Optimizing magnetic layers
  - Shape, size
  - Thickness
  - Materials
  - Temperature dependence
  - Fabrication
    - Crystalline anisotropy
    - Smoothness
    - Uniformity
    - Hygiene effects
- Decoders
- Drivers
- System requires integration of diverse technologies onto a single substrate

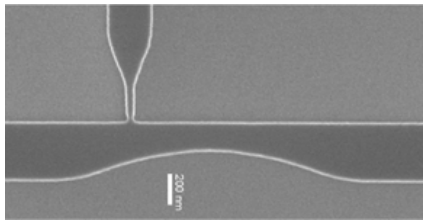




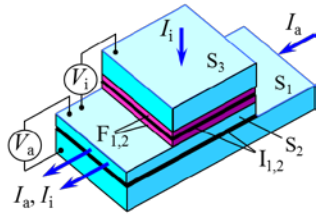
[Nb(25)/Al(2.4)]3/Nb(20)/Spacer/NiFe(1.5)/Spacer/Nb(5)

Challenges: Superconductor Circuits

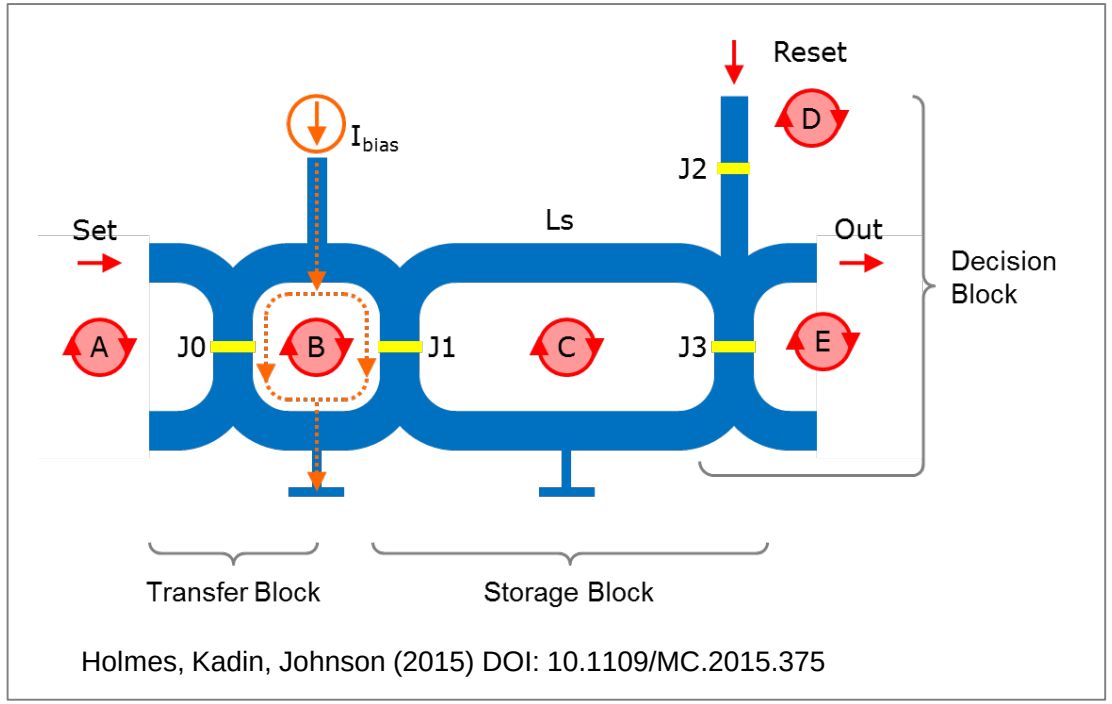
- Inductance (L) and critical current (I_c) are linked for SFQ circuits
  - SFQ: Single Flux Quantum, Φ_0 = 2.07 fWb (mV·ps or mA·pH)
  - Flux: $I \cdot L = \Phi = \alpha\Phi_0 \approx \Phi_0$ **required for circuit operation**!
  - Switching energy: $E_{sw} = I_c \cdot \Phi_0$
  - Decreasing I_c (more energy efficient!) requires increasing L
- Low gain
  - Fan-out > 1 requires splitters
  - Low gain from Josephson junctions (3 JJs to make a 2:1 splitter)
  - Low isolation across JJs
  - Alternatives are being explored



3-terminal nanowire switch



S-F transistor

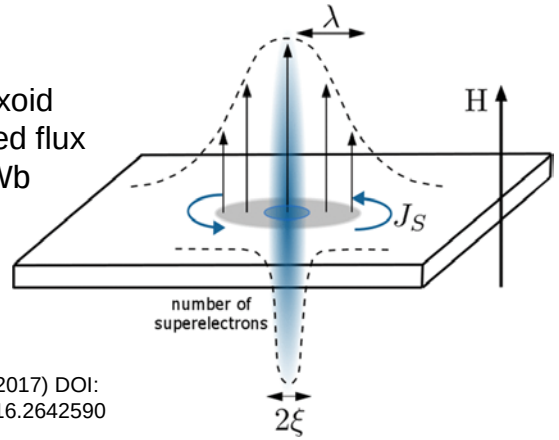


Holmes, Kadin, Johnson (2015) DOI: 10.1109/MC.2015.375

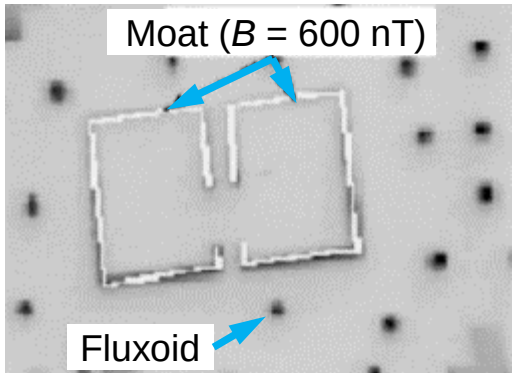
Fault or Failure Mechanisms for Superconductor Digital Electronics

- Currents (*I*) and inductances (*L*) are important in superconductor digital logic compare to voltages (*V*) and capacitances (*C*) for CMOS
- Fault or failure mechanisms are different for superconductor circuits
  - Cosmic rays, radiation? No problem.
  - Magnetic fields from Earth or electric currents? Can cause faults due to trapped flux.
- Fault characteristics: circuit behavior is not as designed and varies by cooldown
- Magnetic flux in superconductors
  - Excluded at low magnetic flux density (*B*), but penetrate as quantized fluxoids above a critical value (B_{c1})
  - Mitigation: “moats” (holes in the superconducting ground plane) that trap flux away from sensitive circuits
  - Worst case: circuit must be warmed above superconducting temperature (Nb T_c ~ 9 K)

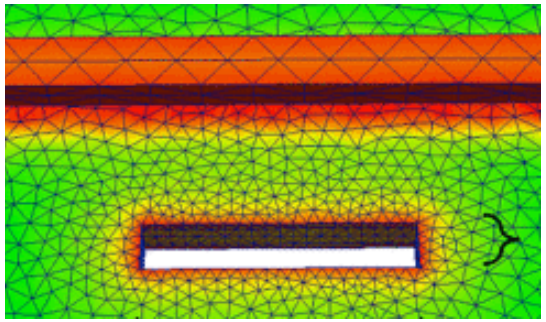
Magnetic fluxoid with quantized flux Φ_0 = 2.07 fWb



Jackman, Fourie (2017) DOI: 10.1109/TASC.2016.2642590



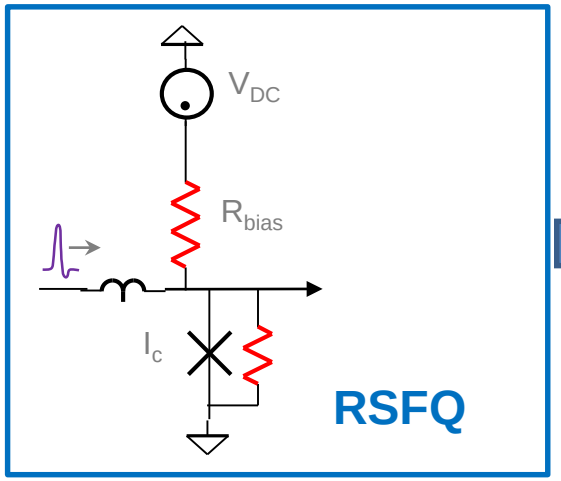
Kirtley, Wilkswo (1999) DOI: 10.1146/annurev.matsci.29.1.117



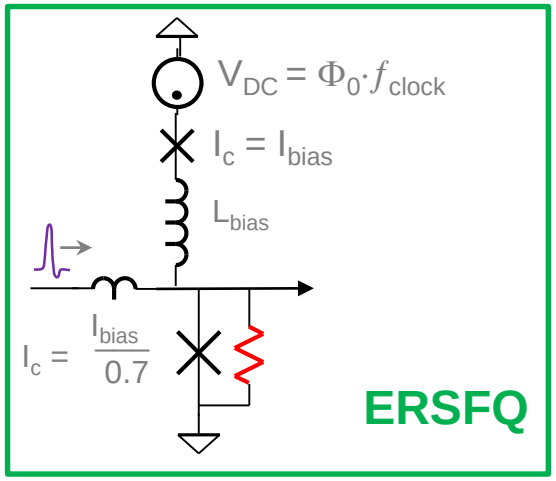
Fluxon trapped in a moat and away from a stripline
Jackman, Fourie (2017) DOI: 10.1109/TASC.2016.2642590

SFQ logic families

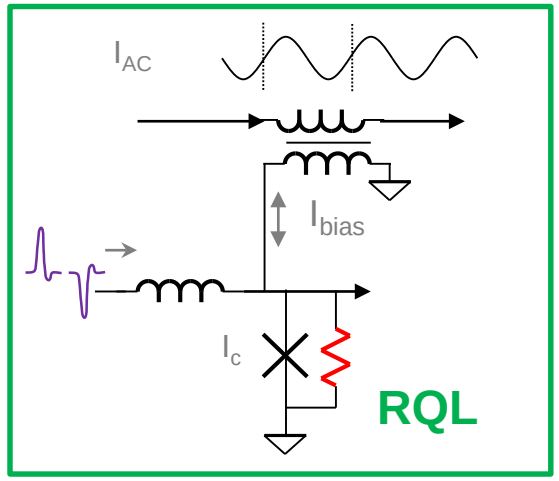
- RSFQ was the original, high-speed SFQ logic (770 GHz small circuit)
- New SFQ logic with no static power dissipation
- Each has merits



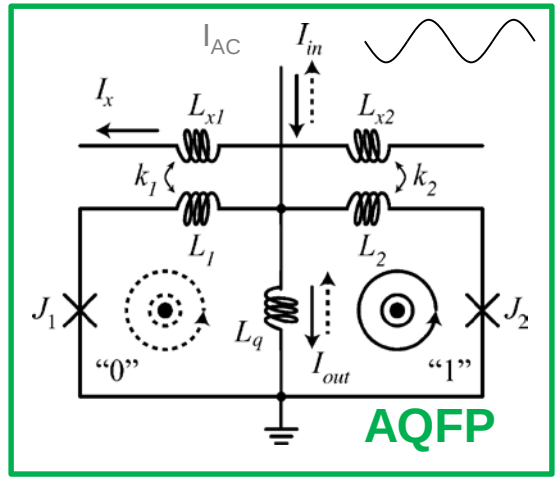
Rapid Single Flux Quantum



Energy-efficient Rapid Single Flux Quantum (Hypres)



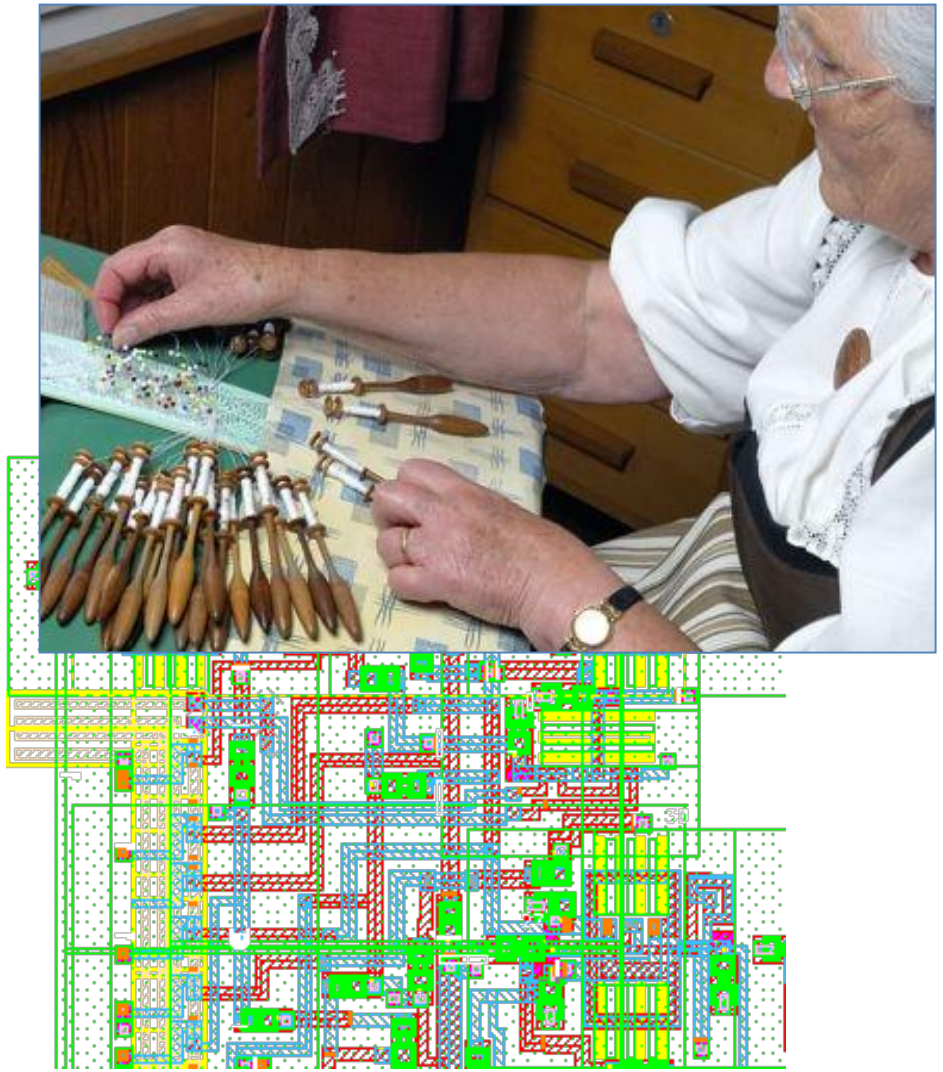
Reciprocal Quantum Logic (NGC)



Adiabatic Quantum Flux Parametron (Yokohama Nat. U.)

Challenges: EDA and Designers

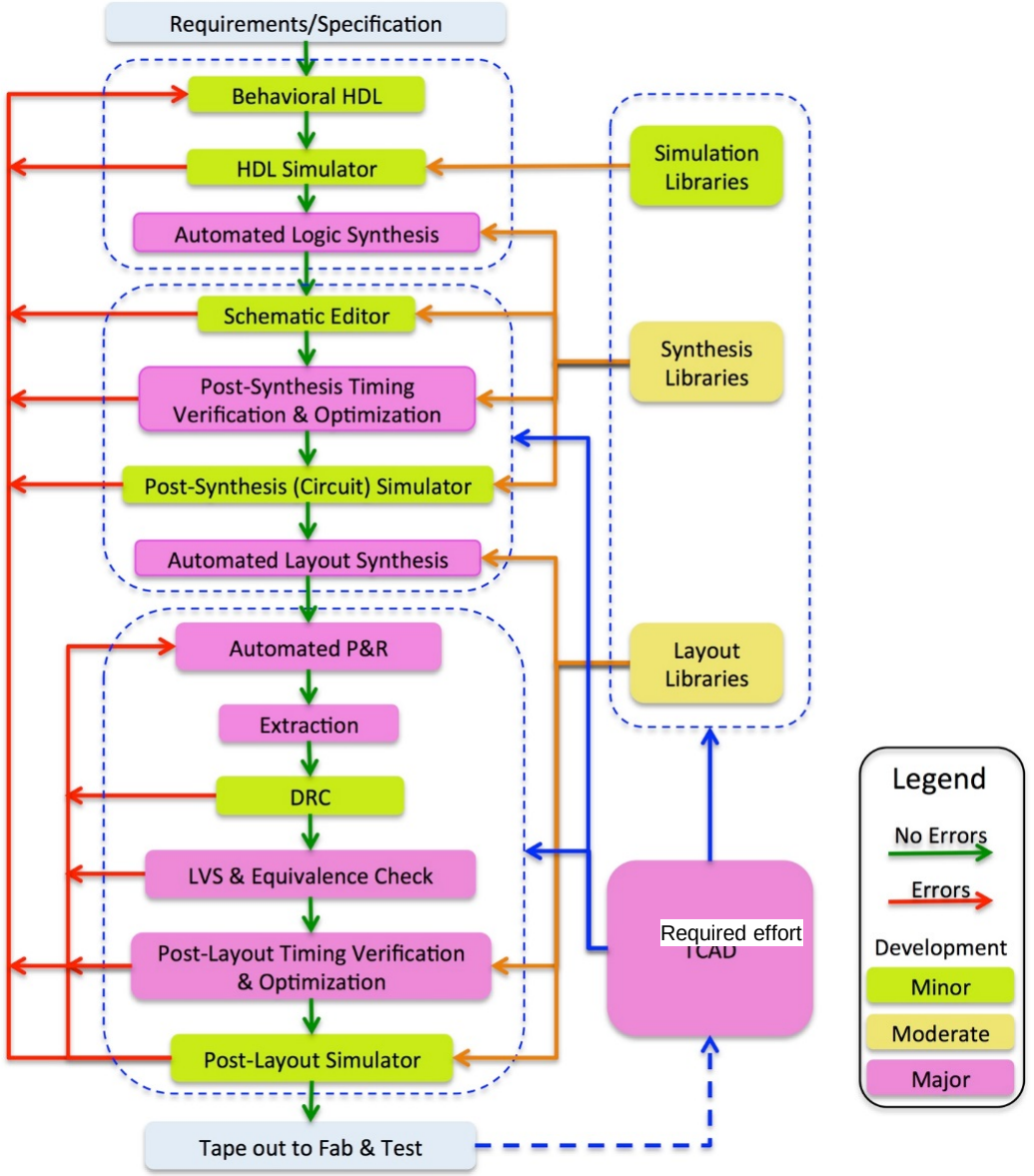
- Electronic design automation (EDA) tools missing or needing improvement:
  - Inductance extraction
  - Placement and routing (inductance range)
  - Synthesis
  - Timing analysis
  - Simulation
  - PDKs (not provided by foundry!)
- SFQ designers
  - No classes in the USA
  - Few designers



"Manual design is like making lace." (SFQ designer)

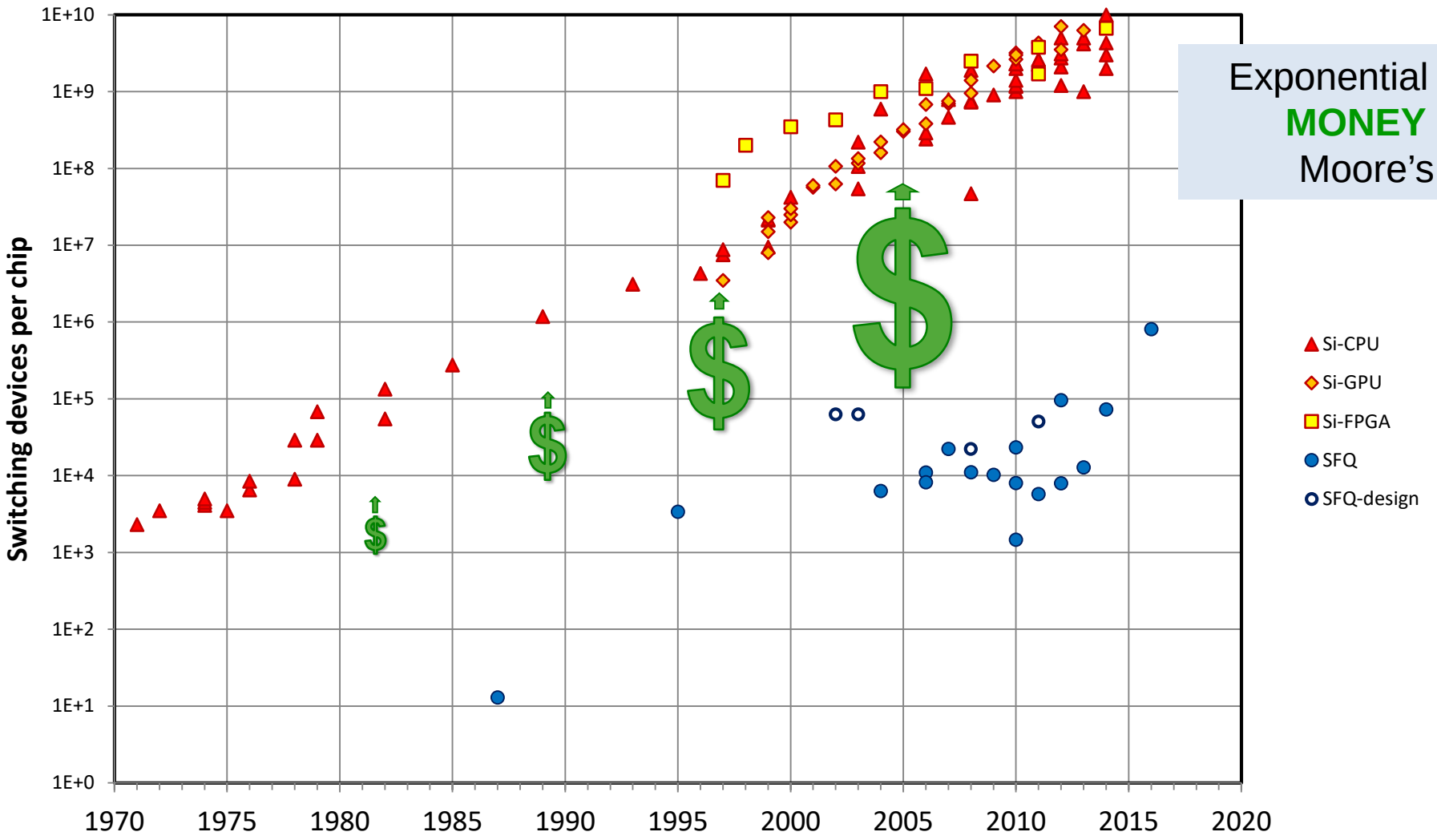
EDA Tool Status for SCE

- Design, analysis, and verification tools need to be developed into a comprehensive EDA tool set specific to very large scale superconductor integrated circuits.
- SuperTools Program (IARPA)
  - Mark Heiligman, Program Manager
  - Started in 2017



SCE = Superconductor Electronics
EDA = Electronic Design Automation
HDL = Hardware Description Language
P&R = Place-and-Route
DRC = Design Rule Check
LVS = Layout versus Schematic
TCAD = Technology CAD

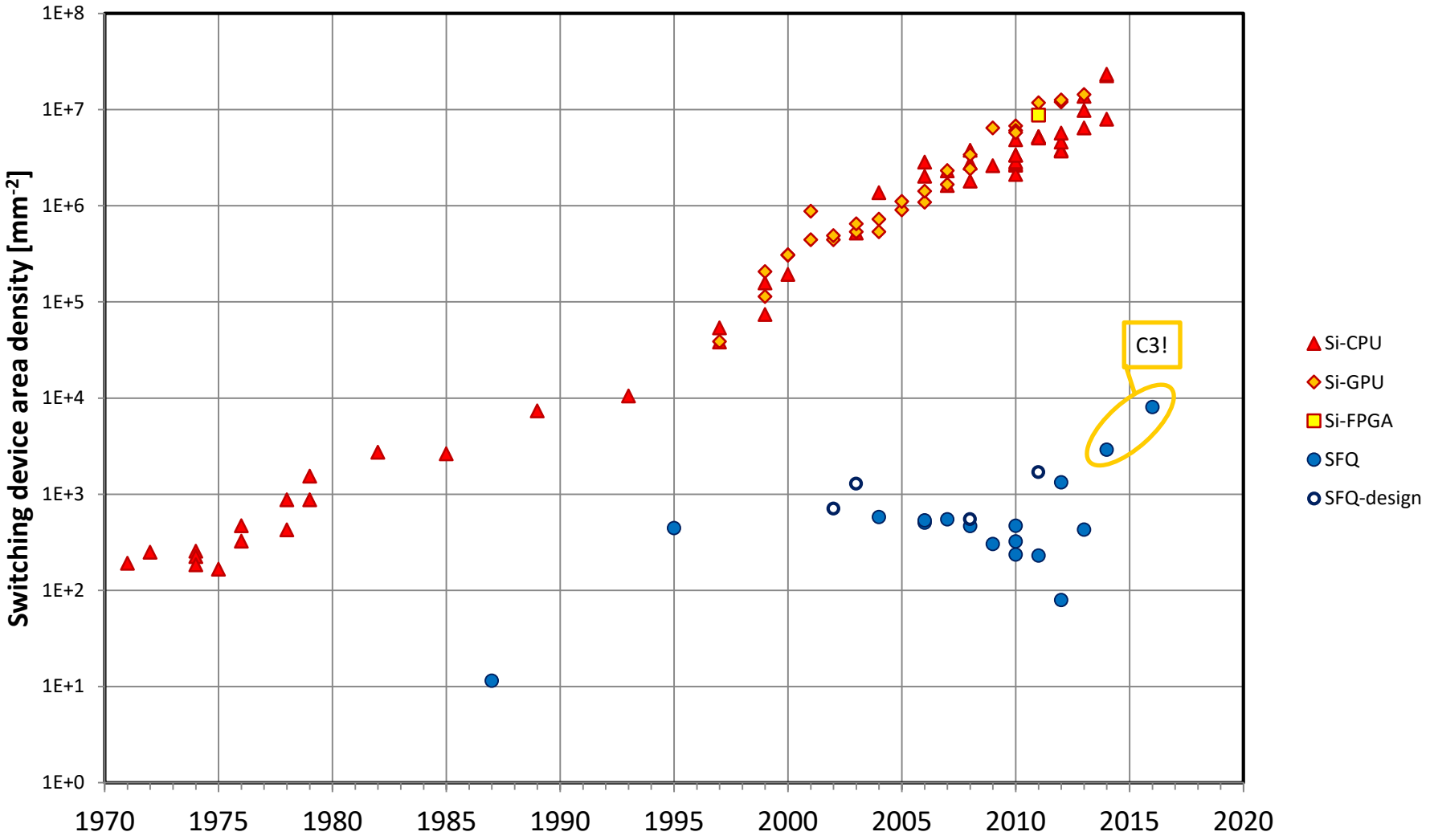
Complexity: SFQ lags semiconductors by ~ 10^4



Exponential growth in **MONEY** drives Moore's Law!

Nagy et al. (2013) **Statistical Basis for Predicting Technological Progress**. DOI: 10.1371/journal.pone.0052669

Density: SFQ lags semiconductors by ~ 10^4



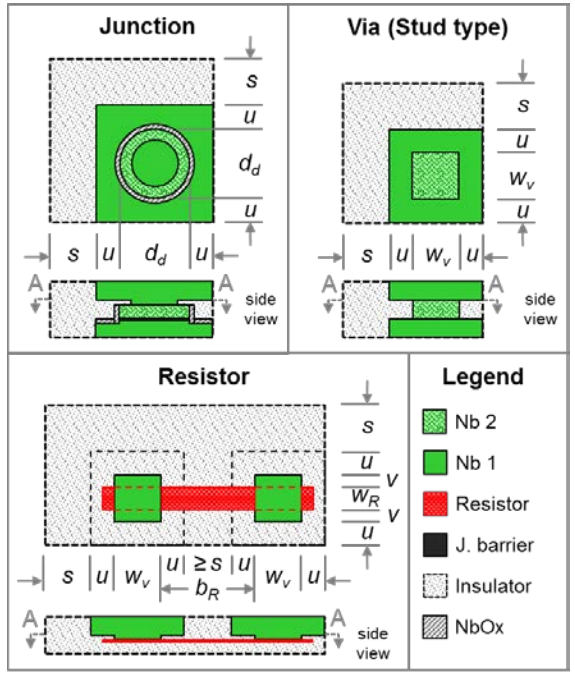
Can superconductor computing compete?

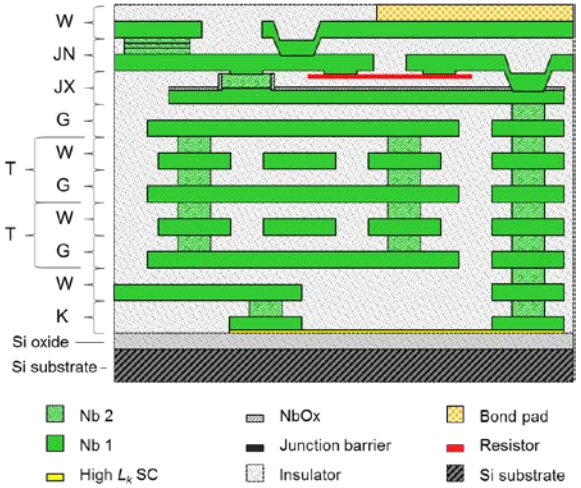
Shadow of the Colossus/
Wander to Kyozō
SCEI

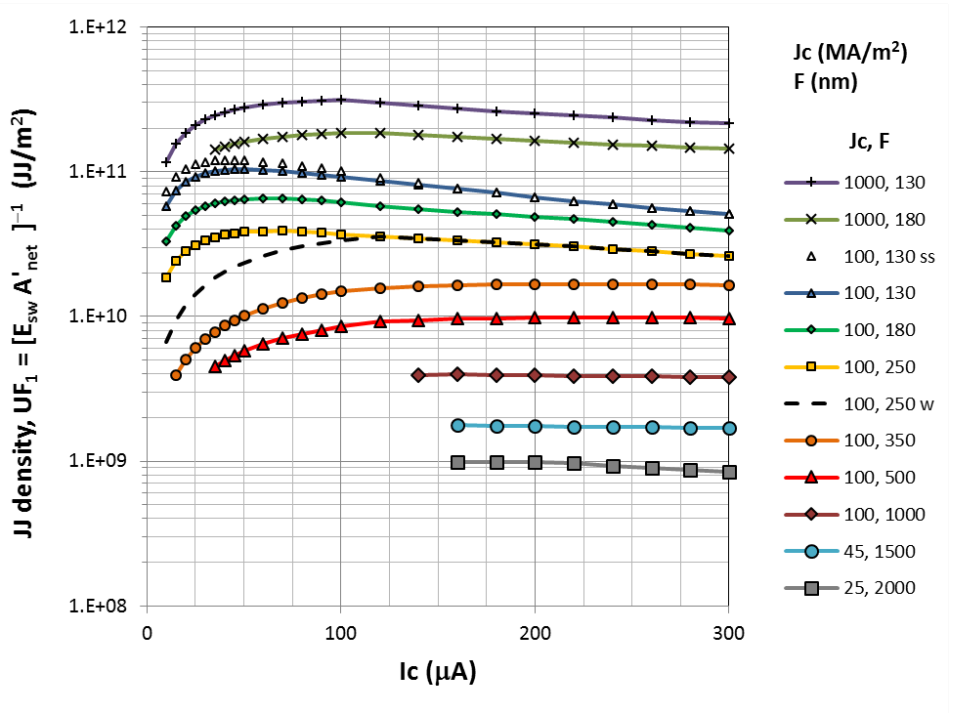
A better way to view the relationship

Future Prospects

Modeling Efforts







- Conclusions:
  - Going beyond 1011 JJ/m2 (107 JJ/cm2) requires significant changes
  - Co-development of designs and processes is needed

Nanobridge weak link Josephson junctions

- Conditions for adequate supercurrent
  - W ~ ξ
  - L < 3ξ
- Normal state resistance affects switching speed and energy dissipated in the weak link
  - Fastest switching with β_c ~ 1
  - Material can be different in the weak link

Material	T_c [K] Bulk	Coherence length, ξ [nm]	Mag. pen. depth, λ_L [nm]	J_c [mA/μm^2]	Crystal structure
Al	1.18	1600	16		fcc, A1
MgB_2	39	3.7-12 ab 1.6-3.6 c	85-180		C32
MoGe	7.4			12 (250 mK)	amorphous
MoSi	7.5			11–25 (1.7 K)	amorphous
Nb	9.2	38	90		bcc, A2
NbN	16	5	270	20–40 (4.2 K)	cubic, B1
NbTiN	12–16				
NbSi	3.1			0.14 (300 mK)	amorphous
NbTi	9.0	5	150		

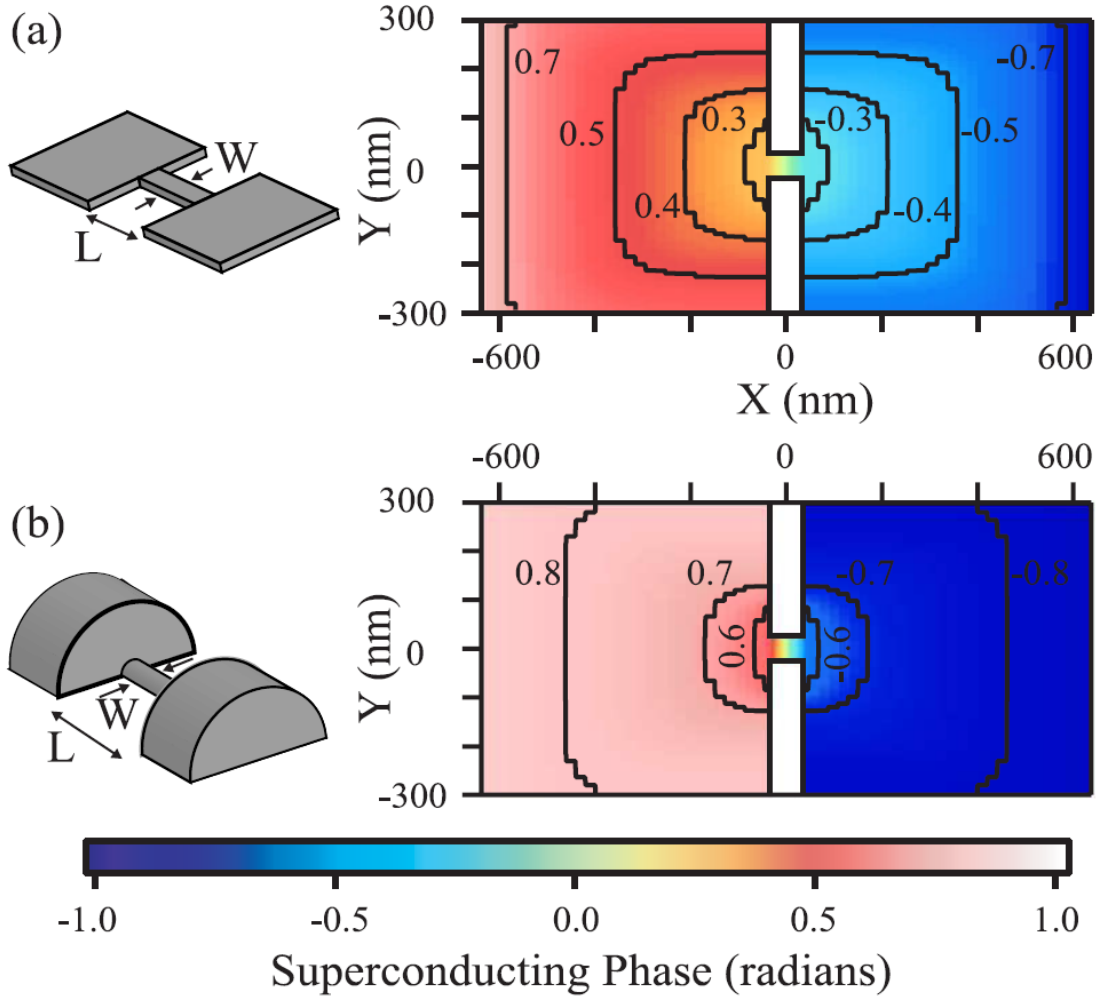


FIG. 2. Superconducting phase (color) as a function of position for an Al nanobridge with L = 75 nm and W = 45 nm.
Vijay et al., 2009, DOI:10.1103/PhysRevLett.103.087003

Direct write junction formation

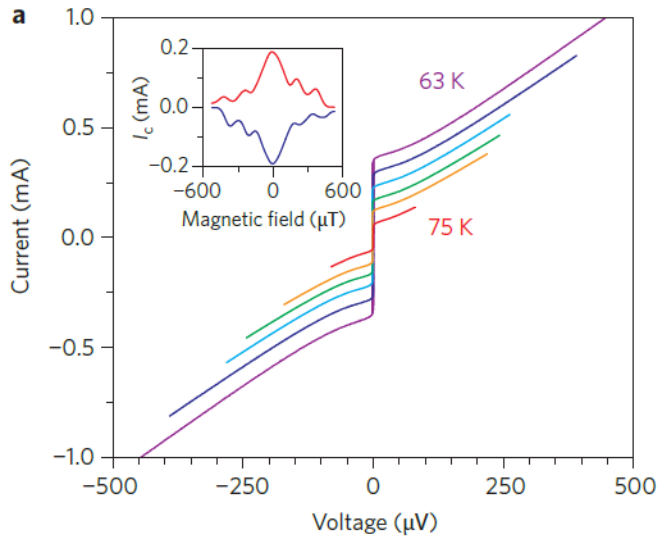
nature nanotechnology

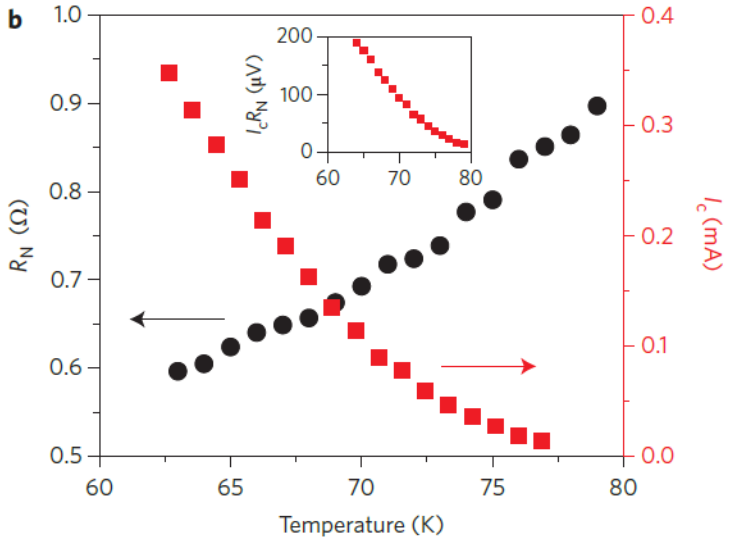
LETTERS

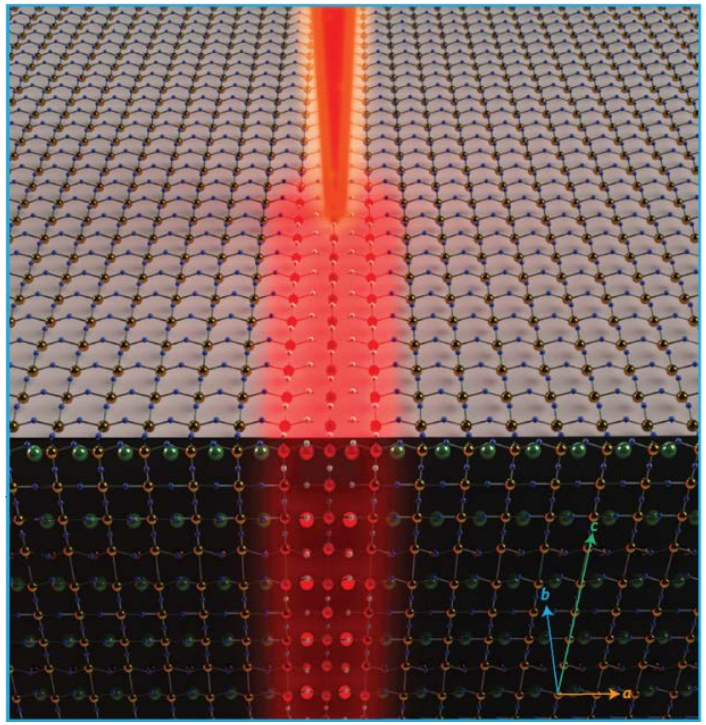
PUBLISHED ONLINE: 27 APRIL 2015 | DOI: 10.1038/NNANO.2015.76

Nano Josephson superconducting tunnel junctions in $YBa_2Cu_3O_{7-\delta}$ directly patterned with a focused helium ion beam

Shane A. Cybart[1,2]*, E. Y. Cho[1], T. J. Wong[1], Björn H. Wehlin[1], Meng K. Ma[1], Chuong Huynh[3] and R. C. Dynes[1,2]







Superconductor electronics within crystalline semiconductors

nature COMMUNICATIONS

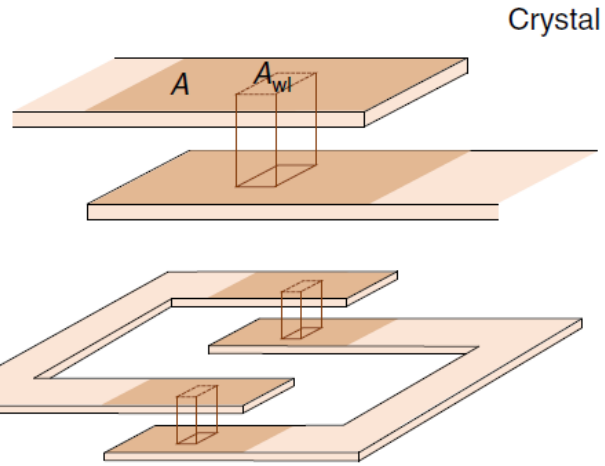
Received 11 Oct 2013 | Accepted 28 May 2014 | Published 2 Jul 2014

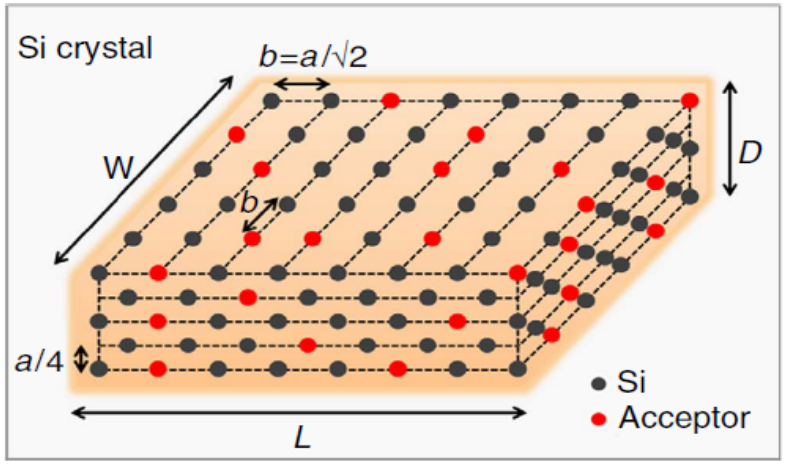
DOI: 10.1038/ncomms5225

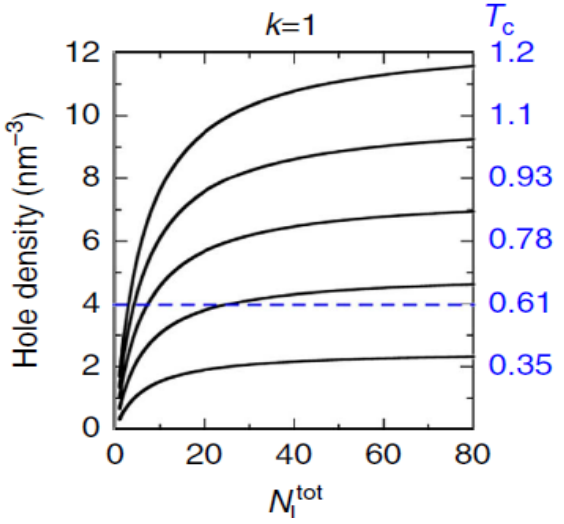
Bottom-up superconducting and Josephson junction devices inside a group-IV semiconductor

Yun-Pil Shim[1,2] & Charles Tahan[1]

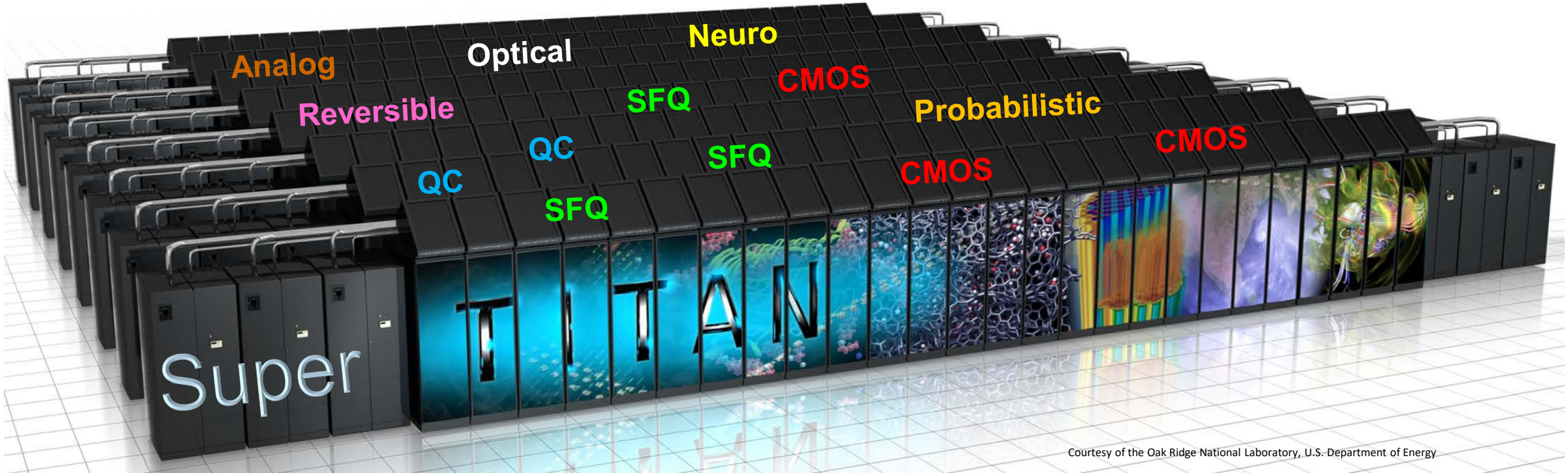
- Concept paper
- Superconducting devices formed in single crystal Si (or Ge)
- Atomistic fabrication techniques and precision hole-doped regions







Future Supercomputing Vision



Courtesy of the Oak Ridge National Laboratory, U.S. Department of Energy

- Hybrid technologies: digital (CMOS, SFQ), probabilistic, analog, neuromorphic, reversible, and quantum computing (QC)
  — whatever works best!
- SFQ digital platform supports multiple cryogenic technologies
- Requires optical interconnects between room temperature and cryogenic nodes

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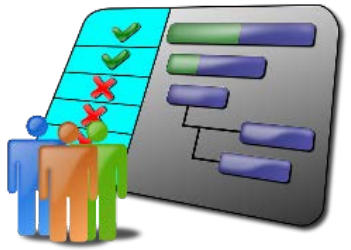
Lessons from an Emerging Technology

- Fair **metrics** are needed to evaluate alternative computing technologies
  - level the playing field to allow different technologies to compete
  - relevant lessons from hiring for diversity?
- Ramping up requires time **and resources**
  - the real Moore's Law
- Government funding alone is not sufficient
  - cost to develop energy-efficient, large-scale computers is large
  - ramp up using smaller products and markets
- Don't go it alone
  - use your mother elephant
- Go big or go home!
  - small improvements are not worth the effort
  - large disruptions require even larger advantages



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