Superconductor Electronic Design Tools for Qubit Control

D. Scott Holmes (contractor)| JLab Workshop | 2022-11-28

Intelligence Advanced Research Projects Activity

I A R P A

Creating Advantage through Research and Technology

Superconductor Electronic Design Tools for Qubit Control

D. Scott Holmes

- Jefferson Laboratory
  Workshop on Superconducting Electronics and Detectors

  This workshop will be bringing specialists in superconducting electronics and detectors to meet with the nuclear physics users community.

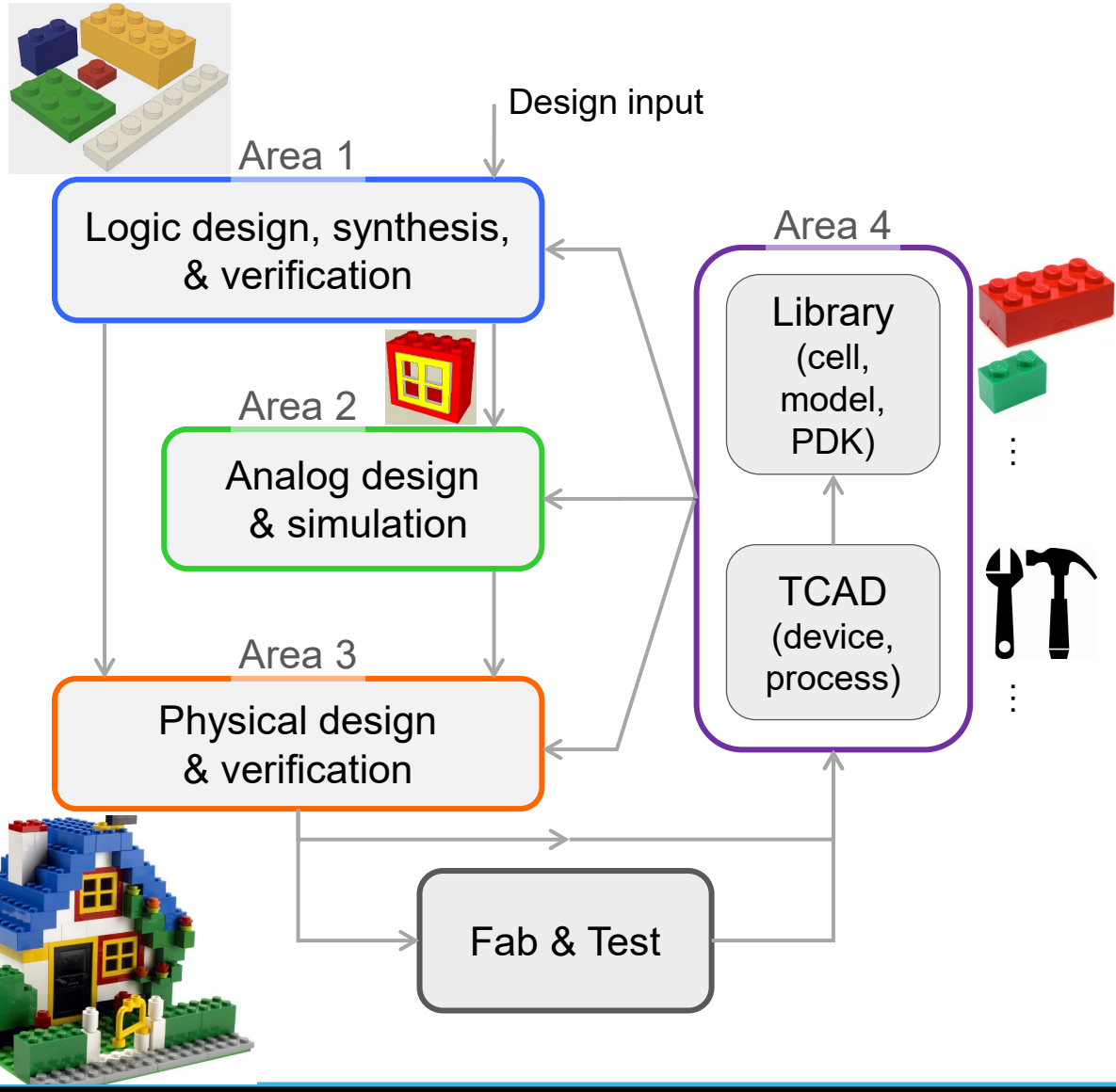
  Superconductors have always held many promises in terms of power savings with the advent of superconducting cavities and superconducting magnets. Since superconductivity is based on loosely bound Cooper pairs, some of the best energy and timing resolutions have been achieved with superconducting detectors such as Transition Edge Sensors and Superconducting Tunnel Junction, Superconducting Nanowires. The main drawback being the low temperature required for operation. This issue can be somewhat alleviated in places where cryogenics is readily available such as Jefferson Laboratory or other major Physics facilities. This can give an opportunity to take advantage of the performances of superconducting devices.

- Abstract

  Electronic design automation (EDA) tools newly developed under the IARPA SuperTools program can be used to design complex digital superconductor electronic circuits. Classical control systems for superconducting quantum computing would benefit from control systems operating in close physical proximity within the cryogenic environment. The opportunities and challenges are briefly reviewed.

IARPA SuperTools Program

- Goal: Develop a complete set of electronic design automation (EDA) tools for superconductor electronics
  - Digital logic focus, T ~ 4 K
  - Program focus areas address major steps in the design flow from high-level logic description to the physical layout that can be sent to a foundry for fabrication
- 5-year program (2017-2022) with 2 performer teams
  - **Synopsys** (commercial industry team)
  - **USC ColdFlux** (academic team)



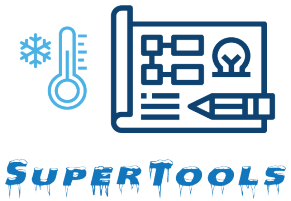
PDK: Process Design Kit
TCAD: Technology Computer-Aided Design (device-level)

SuperTools Key Goals by Technical Focus Area

1: Logic Design, Synthesis, and Verification	
Figure of Merit	Phase 3
Design complexity (logic gates)	≥ 10^6
Processor bit width	≥ 64
Processor level	complete
RAM (KiB)	≥ 1
Circuit clock frequency, max. (GHz)	≥ 30

2: Analog Design and Synthesis Circuit simulator, layout synthesis, timing, yield, and power analysis tools	
Figure of Merit	Phase 3
Design complexity (JJ count)	≥ 10^6
Clock frequency, maximum (GHz)	≥ 100

3: Physical Design and Verification Automated place-and-route (P&R), circuit optimization, and verification tools	
Figure of Merit	Phase 3
Device parameter extraction types	L, M, R, J, C, Z
Circuit parameter extraction: Devices	≥ 64
Area [μm^2]	complete
Fraction within band	≥ 1
P&R interconnect area (cm^2)	≥ 4

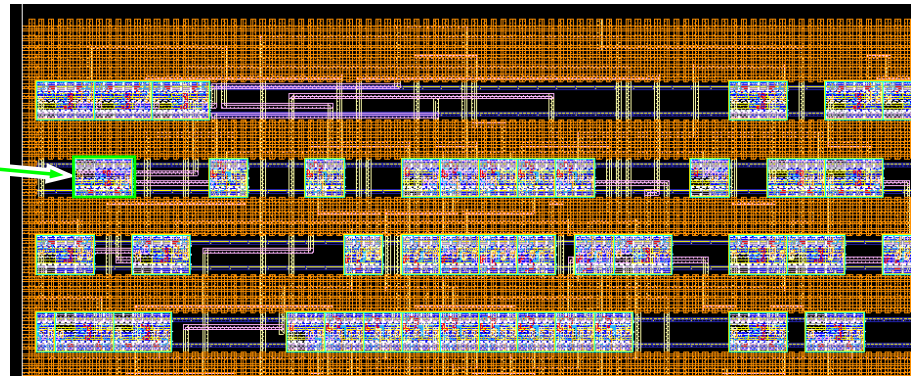


- Fills the gaps in the digital circuit design process (logic synthesis!)
- Huge improvement over the ~ 100 JJ limit of previous circuit simulators

4: TCAD and SuperTools Library development TCAD simulation, cell libraries, and extracting model parameters	
Figure of Merit	Phase 3
TCAD simulations (count, dimensions)	≥ 7, 3D
Library cells (count and functionality)	≥ 40 Standard, ≥ 10 Interoperable

Design Tool Examples (1)

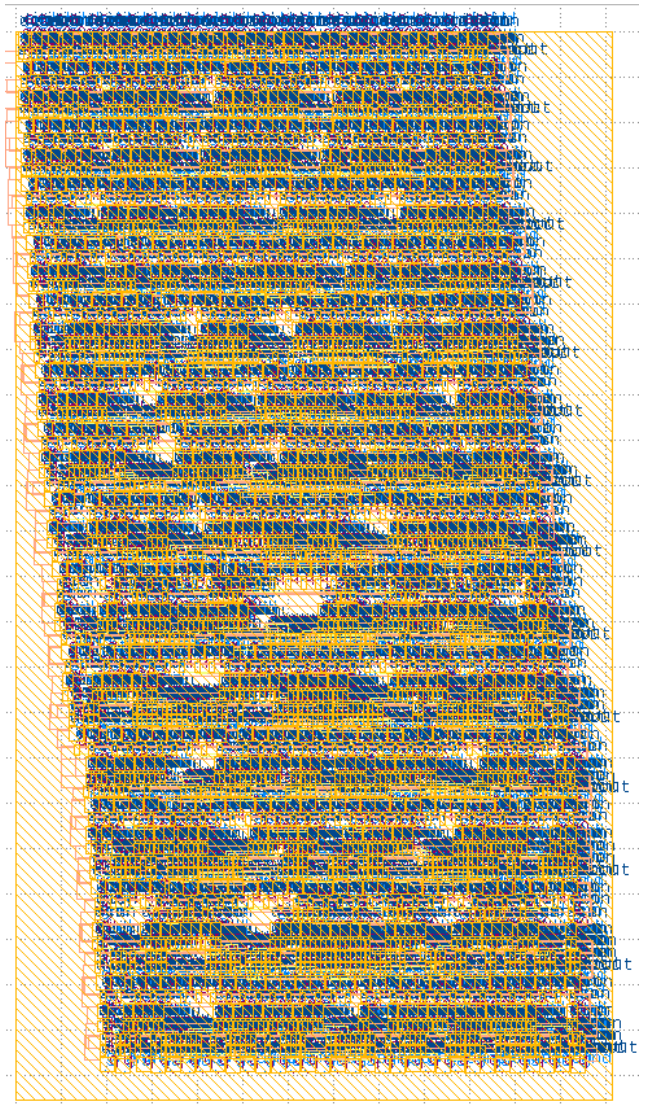
- Physical Design and Verification



AMD2901 4-bit processor design with 16,840 gates (upper left portion of overall layout)

Placed and routed in Synopsys **Fusion Compiler** (FC) and viewed in Custom Compiler

SYNOPSYS®



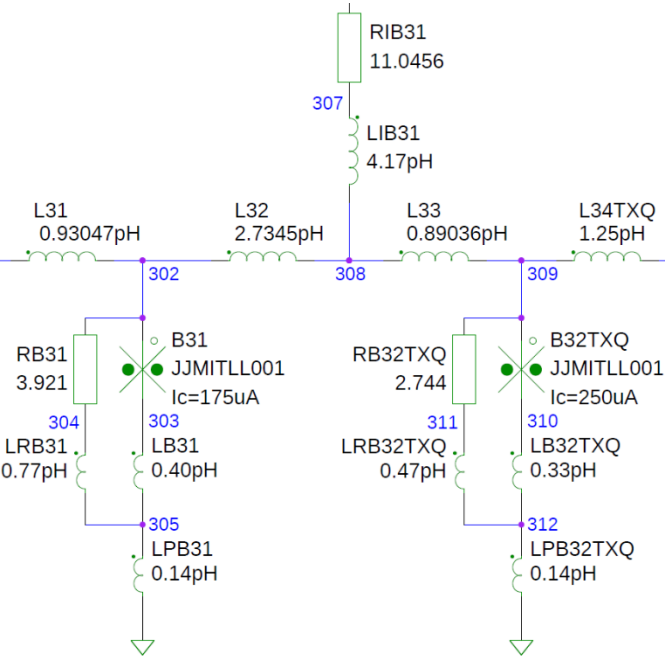
Sorter32 layout

qPALACE tool

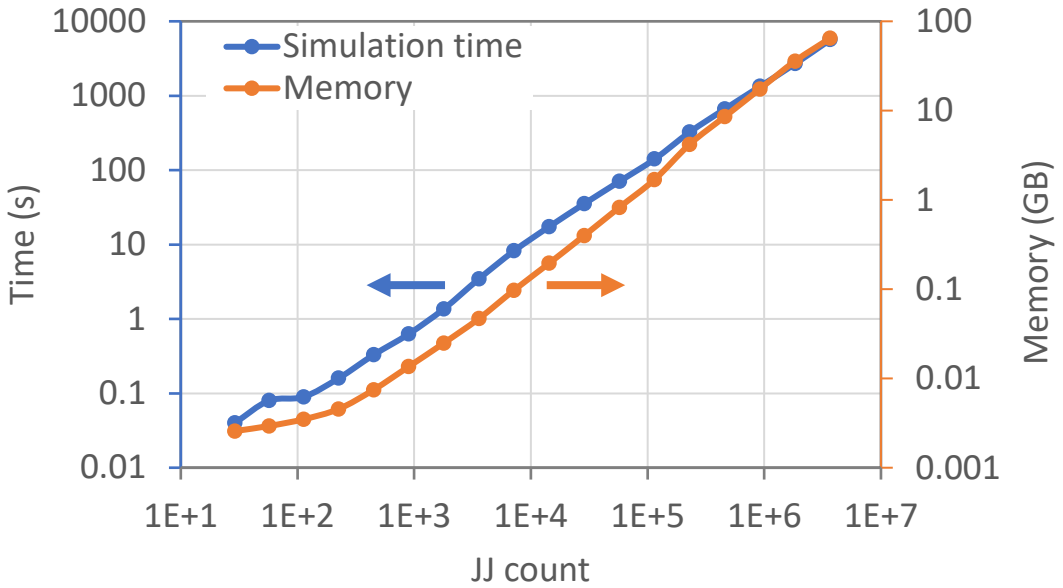
USC ColdFlux

Design Tool Examples (2)

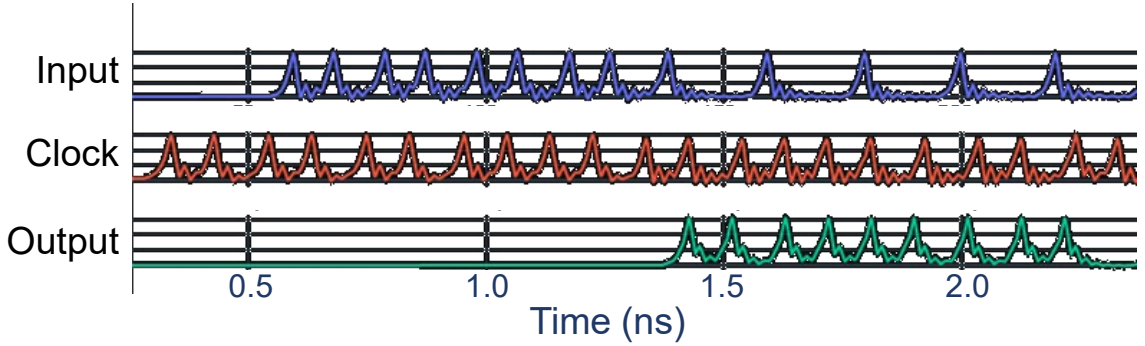
- Circuit simulation tools



JoSIM performance for 12,000 simulation steps at 0.25 ps per step



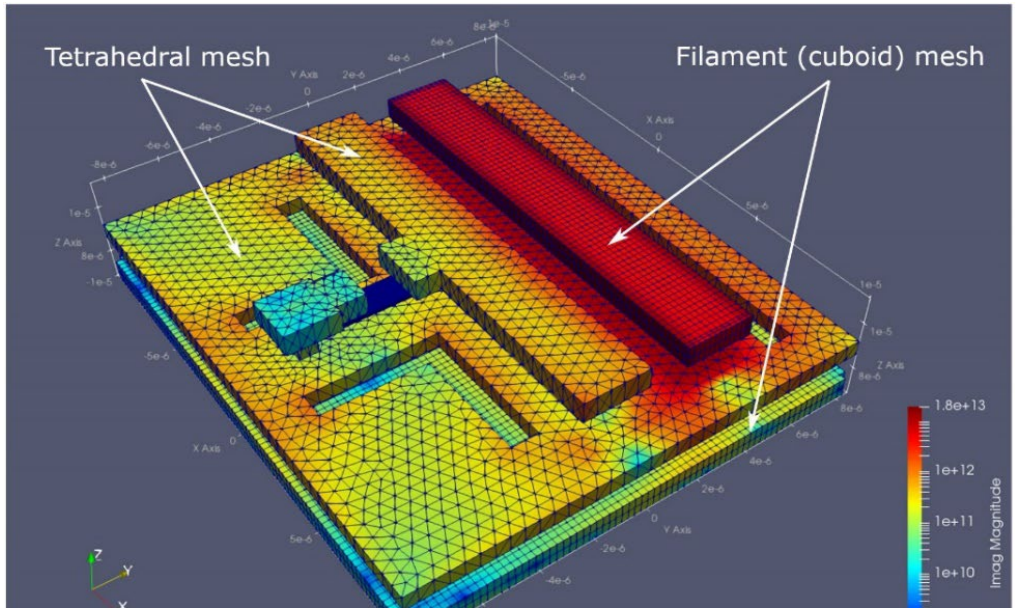
Simulation of a large clock distribution network at 100 GHz



USC ColdFlux https://github.com/JoeyDelp/JoSIM

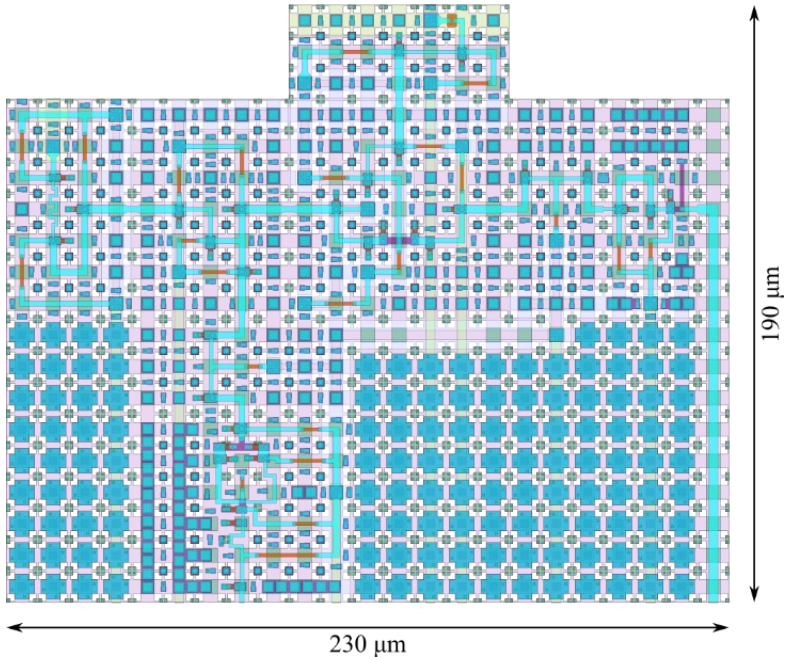
Design Tool Examples (3)

- Circuit parameter extraction and analysis tools



Current flows in a superconductor circuit (**InductEx**)

USC ColdFlux

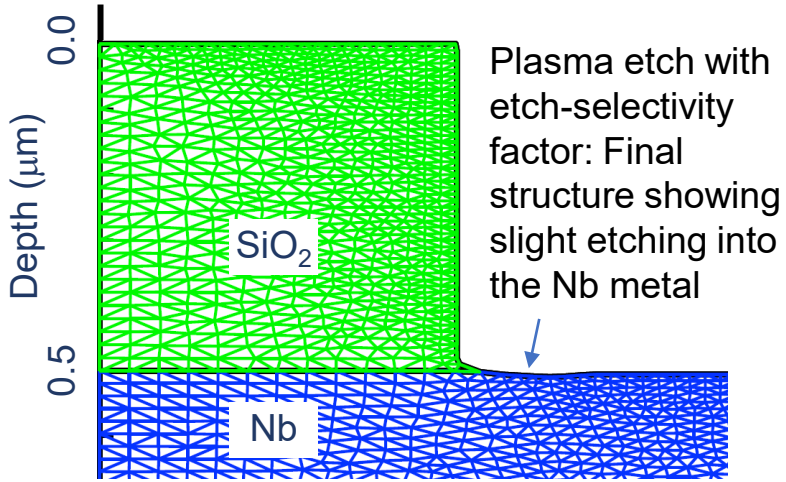


Ring Oscillator compact model extraction:

- Cells: 7
- Total area: 38,900 µm^2
- Component count: 174
  - with mutual (M): 3007
- Time: 58 min
- Memory 15.8 GB

Design Tool Examples (4)

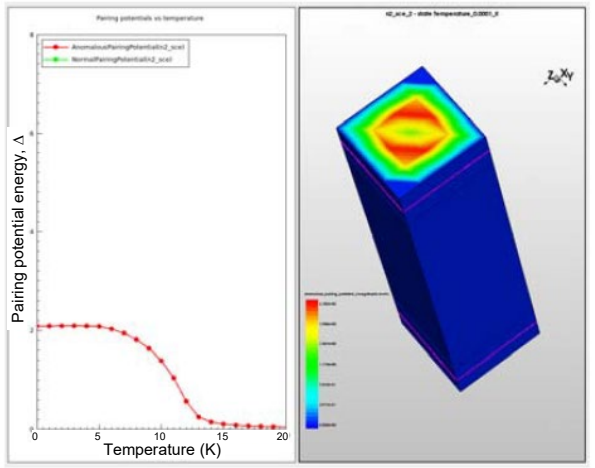
- TCAD: Technology Computer-Aided Design (device-level)



Plasma etch process simulation

FLOOSS tool (http://www.flooxs.ece.ufl.edu/)

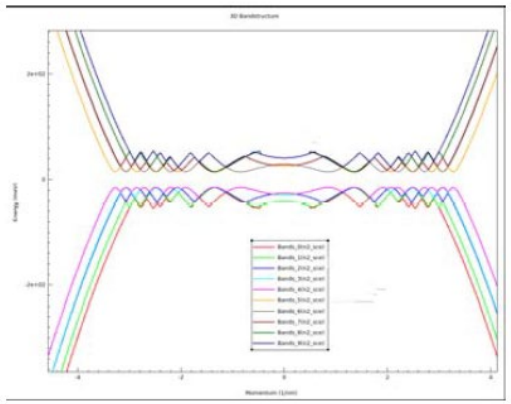
USC ColdFlux



Self-consistent computation of Delta-vs-T

Self-consistent simulation of a homogeneous 3D nanowire
Synopsys **Sentaurus**

SYNOPSYS®

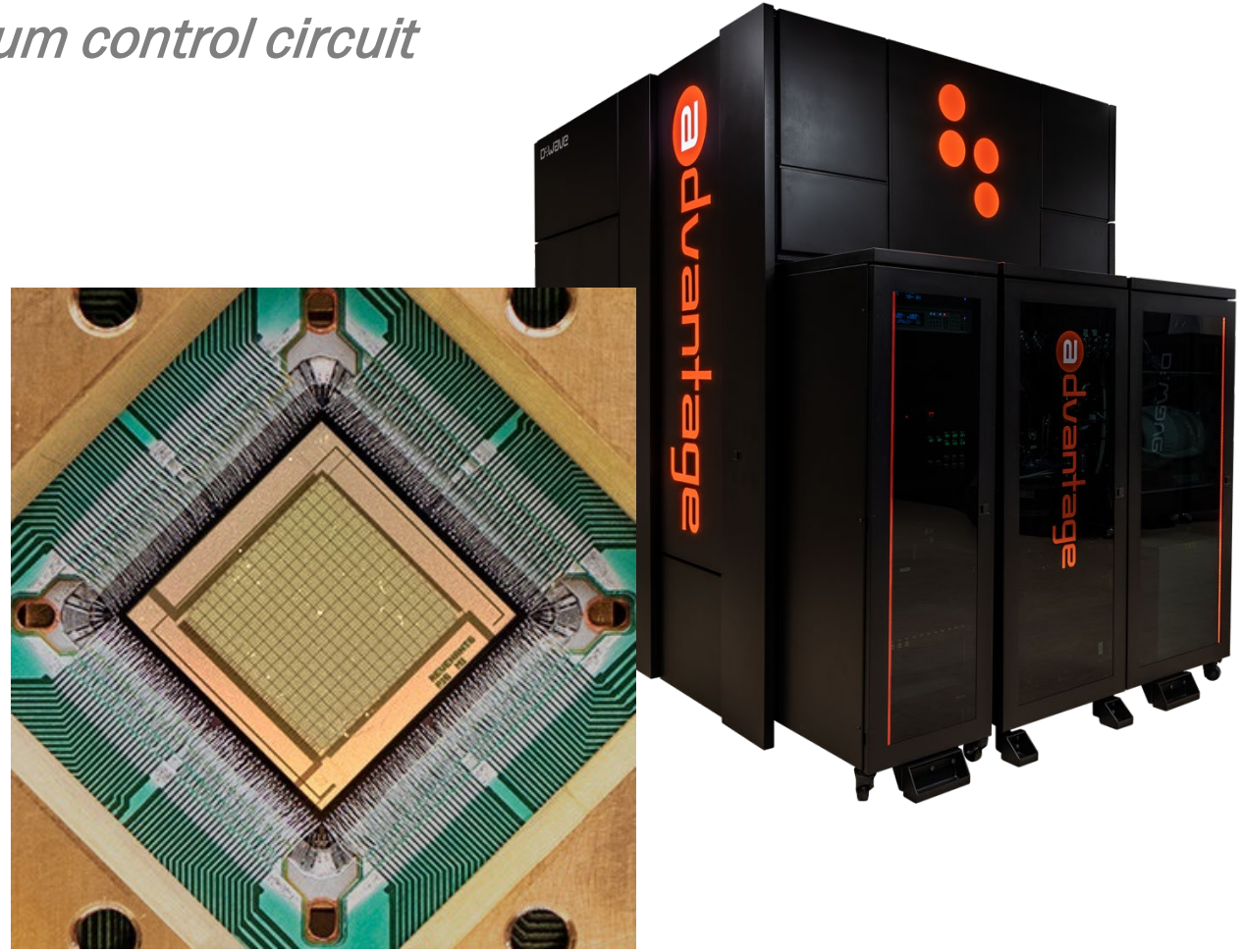


Bandstructure simulation

Quantum Processing Unit (D-Wave Systems)

Example superconductor electronic quantum control circuit

- D-Wave Advantage, Pegasus P16 quantum processing unit (QPU) using superconductor electronics
- 1,030,000 Josephson junctions
- 5640 qubit array
- 15 couplers per qubit
- Active area: 8.4 mm × 8.4 mm
- 15-20 mK operating temperature



(No known use of SuperTools products)

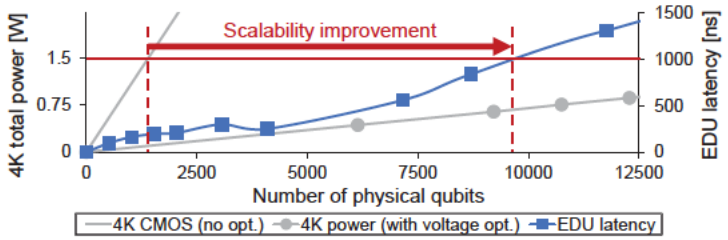
https://www.dwavesys.com/solutions-and-products/systems/

https://en.wikipedia.org/wiki/D-Wave_Systems#Pegasus

Limits for superconducting qubit control

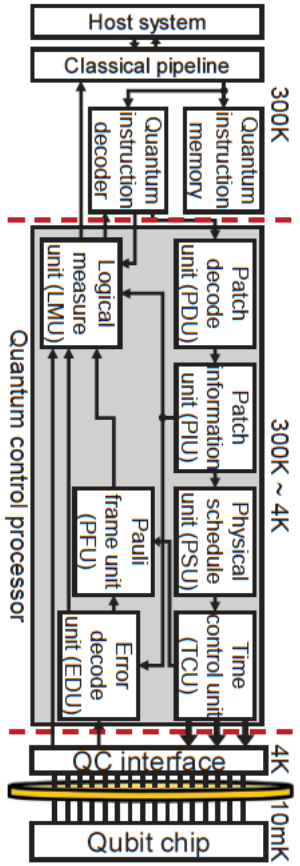
Where are the breakpoints?

- **XQsim**: quantum control processor simulator (open-source, cross-technology)
- Scalability analysis
  - Maximum number of qubits subject to constraints (delay, power, area)
  - Did not include QC interface



CMOS @ 4 K scalability analysis [1, Fig. 17b]

[1] Byun +, "XQsim: modeling cross-technology control processors for 10+K qubit quantum computers," Jun. 2022, doi: 10.1145/3470496.3527417.



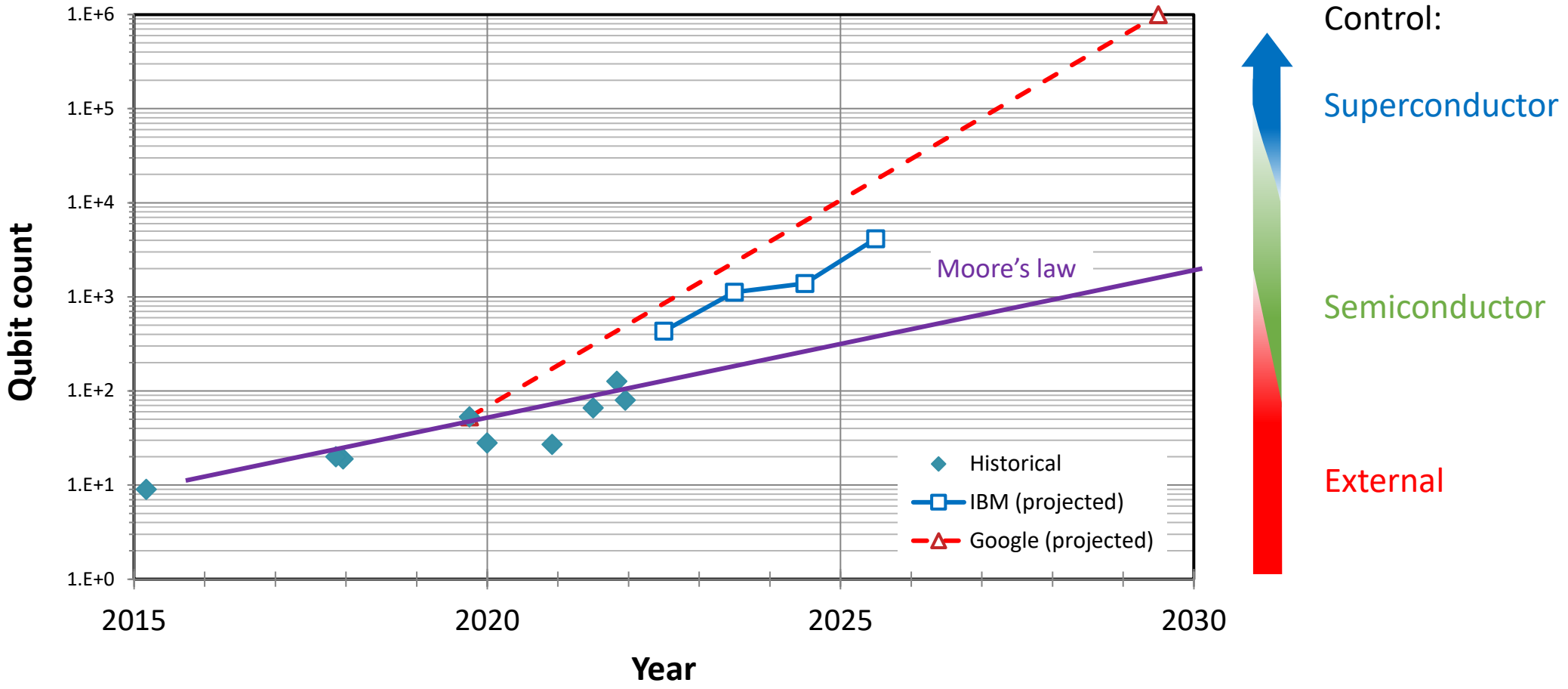
Fault-tolerant quantum computer system overview [1, Fig. 1]

Error decoder	
1e-3	Phys. error rate
15	Code distance
QECOOL:	Baseline error decoder
Physical quantum gate latency	
14 ns	1-qubit gate
26 ns	2-qubit gate
600 ns	Measurement
Refrigeration and wiring	
1.5 W	4 K power budget
620 cm^2	4 K area budget
31 mW, 10 Gb/s coaxial cable 300-4 K	
Clock frequency	
1.5 GHz	CMOS @ 4 K or 300 K
21 GHz	RSFQ or ERSFQ @ 4 K
Qubits controllable (limiting factor)	
1,700	CMOS @ 300 K (heat leak)
9,800	CMOS @ 4 K (delay)
4,600	RSFQ @ 4 K (power)
59,000	ERSFQ @ 4 K (power)
?	AQFP @ 4 K (?)

Superconducting Qubit Roadmaps

What is reasonable?

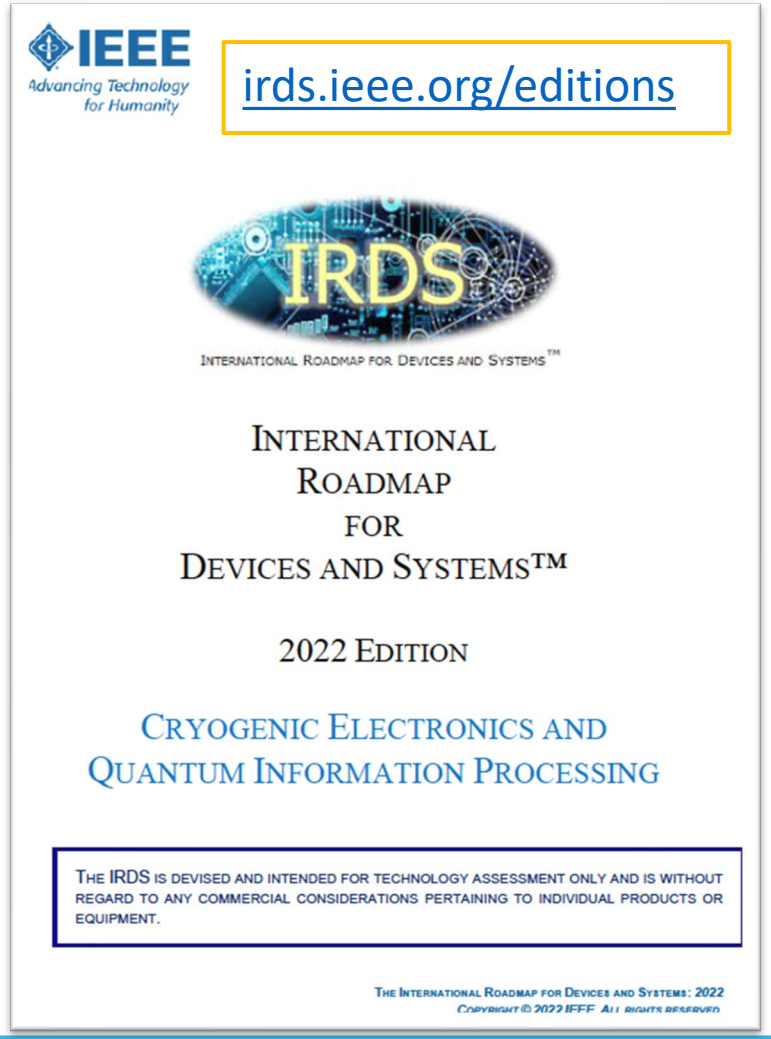
~ 10x every 2 years (5x Moore's law)



IBM: https://research.ibm.com/blog/ibm-quantum-roadmap-2025 Google: https://www.cnet.com/tech/computing/quantum-computer-makers-like-their-odds-for-big-progress-soon/

Fabrication Roadmap for Superconductor Electronics (SCE)

Application requirements guide roadmap development



2022 Table CEQIP-17

Year	2022	2023	2024	2025	2026	2027	2028
Digital SCE Fabrication							
"Node Range" label (nm)	**"250"**	**"250"**	**"150"**	**"150"**	**"150"**	**"150"**	**"90"**
Substrate material, maximum size (mm)	Si, 200	Si, 200	Si, 200	Si, 200	Si, 200	Si, 200	Si, 300
Wiring							
Superconductor	Nb	Nb	Nb	Nb	Nb	Nb	Nb
Superconductor layers	**8**	**8**	**10**	**10**	**10**	**10**	**12**
Linewidth, minimum (nm)	**250**	**250**	**150**	**150**	**150**	**150**	**90**
Ic, minimum (μA)	**200, 1200**	**200, 1200**	**100, 580**	**100, 580**	**100, 580**	**100, 580**	**50, 290**
Junctions, Switching							
Junction materials	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx
Junction layers	**1**	**1**	**2**	**2**	**2**	**2**	**2**
Junction critical current densities, Jc ($\mu A/\mu m^2$)	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**
Minimum junction diameter (nm)	**500**	**500**	**350**	**350**	**350**	**350**	**250**

Conclusions

Superconductor Electronic Design Tools for Qubit Control

- **Opportunities**
  - Design tools for superconductor electronics can now handle circuits of complexity expected for qubit control at ~ 4 K
- **Challenges**
  - Low circuit density due to:
    - Fabrication process: Large feature sizes, few routing layers, inductors, transformers
    - Automated place-and-route (P&R) using only PTL connections between gates
  - Clocking, especially with logic families that require clocking of most gates
  - Current supply: Large DC or GHz AC
  - TCAD tools: Sputter deposition, microstructure, magnetic materials

▸ Bottom line: Possible but will require time and effort to ramp up.