



# Cryogenic Readout Electronics in the DUNE experiment

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## Outline

- Overview of the DUNE experiment and cryogenic readout
- Design of the cryogenic readout and performance
- Quality control of the cryogenic electronics production
- Summary



## **DUNE experiment**

• Long baseline accelerator neutrino experiment



### **Primary Physics: Neutrino Oscillation**

## **DUNE experiment**

• Long baseline accelerator neutrino experiment



#### **Far Detectors**

- Neutrino oscillation
- Leptonic CP violation
- Supernova burst
- Proton decay

### **Near Detectors**

Neutrino-Nucleus interaction

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## **DUNE Far Detectors**



- 4850 ft underground
  - Sanford Underground Research Facility (SURF) in South Dakota
- Four detectors (10kt each):
  - May have four different designs
- Multiple phases
  - First two detectors will start operation around 2027
  - Both of them are Liquid Argon Time Projection Chambers (LArTPCs)
  - FD1 Horizontal Drift LArTPC
  - FD2 Vertical Drift LArTPC
  - Other two detectors are to be determined

## FD1 - Horizontal Drift LArTPC



A 10 kt DUNE FD SP module

• Anode plane :

four layers of wires: G (-665 V), U (-370 V), V (0 V), X (820 v)

• Cathode plane (-180 kV)



Wire number

## FD1 - Horizontal Drift LArTPC

### Anode plane assembly





- S/N ∝ dE/dx
  -> Calorimetry
  -> Particle identification
- Minimum-ionizing particle:
- ~ 20k-30k e- per channel
- —> noise below 1000 e-—> linear up to 500k e-
- Readout electronics of LArTPC are immersed in LAr and are directly mounted on APA
- $\rightarrow$  good S/N ratio (> 9)

### **FD1 - Cold Electronics**



Cryogenic electronics at the top APA

Cryogenic electronics at the Bottom APA



## **FD1 - Cold Electronics**

- Readout electronics of LArTPC are immersed in LAr and are directly mounted on APA —> good S/N
- Components of cold electronics
  - 1. In LAr (~ 87K)
    - Front-end Mother Board (FEMB)
    - Cold cables
- 2. Outside of cryostat
  - CE Flange
  - Warm Interface Electronics Crate (WIEC)
    - Warm Interface Board (WIB)
    - Power and Timing Card (PTC)
    - Power and Timing Backplane (PTB)





## **FD2 - Vertical Drift LArTPC**



**Charge readout planes (CRP)** 



### **FD2 Bottom CRP - Cold Electronics**

- Almost identical to FD1,
- Difference: Patch Panel, MINI-SAS cable, longer power cable and data cable







B. Abi et al 2020 JINST 15 T08010

### **Front-End Mother Board (FEMB)**

![](_page_13_Figure_1.jpeg)

- 128 channels, read 40 U wires, 40 V wires, and 48 X wires
- 2 baselines, 4 gains, 4 peaking time
- 4 data links with 1.25 Gbps each
- Power consumption: < 50 mW/channel in LAr
- Equivalent Noise Charge ~ 600 e- in LAr

## **Challenges of Cold Electronics**

- Operate in liquid Argon (87K)
- A huge number of electronics and cables, mechanical parts etc.
- Long lifetime ~ 20 years
- Dead channels <1%

### **Requires dedicated Quality Control (QC) tests for each components**

- Multiple test sites
- Standard QC procedures
- QC Results will be stored in a hardware database

![](_page_14_Picture_9.jpeg)

### Challenges of Cold Electronics Production

- 20 FEMBs per APA, and 24 FEMBs per CRP
- 4 FEMBs per WIB
- Each FEMB: 8 LArASIC, 8 ColdADC, 2 COLDATA

**ProtoDUNE-II HD ProtoDUNE-II VD BDE** DUNE FD1 + FD2-BDE

- 4 APAs •
- **80 SAMTEC FEMBs** •
- 20 WIBs •
- 640 LArASIC chips •
- 640 ColdADC chips •
- 160 COLDATA chips

![](_page_15_Picture_11.jpeg)

•	2	CRF	'S

- 48 MINI-SAS FEMBs
- 12 WIBs
- 384 LArASIC chips
- 384 ColdADC chips
- 96 COLDATA chips

  - **Happening Now**

- 150 APAs, 80 CRPs
- 3000 SAMTEC FEMBs
- **1920 MINI-SAS FEMBs**
- 1230 WIBs
- 39360 LArASIC chips
- 39360 ColdADC chips
- 9840 COLDATA chips

A huge amount of electronics! Haven't counted the cables and others yet !

## **LArASIC Quality Control**

- A detailed checkout script generates a QC report for each chip (~ 7 minutes per chip)
- QC tests are performed both in room temperature and in liquid Nitrogen (LN2)
- Immersing electronics into LN2 and warm up afterwards each takes about 30 minutes
- Test multiple electronics in one run saves time

![](_page_16_Picture_5.jpeg)

### automated Cryogenic Test System

![](_page_16_Picture_7.jpeg)

Test two LArASIC chips per run

## **LArASIC Quality Control**

- A detailed checkout script generates a QC report for each chip (~ 7 minutes per chip)
- QC tests are performed both in room temperature and in liquid Nitrogen (LN2)
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![](_page_17_Picture_5.jpeg)

Robotic Test System

![](_page_17_Picture_7.jpeg)

### DAT

Test 2 COLDATA, 8 ColdADC, 8 LArASIC
 per run

### **FEMB QC Procedures**

![](_page_18_Figure_1.jpeg)

• Four FEMBs are tested at the same time

![](_page_18_Picture_3.jpeg)

### **Cold Electronics Performance in ProtoDUNE**

![](_page_19_Picture_1.jpeg)

### **Cold Electronics Performance in ProtoDUNE**

### • ProtoDUNE-SP (2018-2020)

![](_page_20_Picture_2.jpeg)

- Validate the the design of the integrated cold electronics readout
- Measure the performance of the electronics system
- 99.7% of the readout channels functioned properly
- The measured ENC for a collection wire is about 550e-, and for an induction wire is about 650e-
- S/N ~ 38 for collection wires, and S/N~ 14 (U), ~17 (V)

#### $(0.3 - 7 \text{ GeV/c p/e^+/}\pi^+/\mu^+/K^+/\text{ beam})$

### **Cold Electronics Performance at ProtoDUNE**

- **ProtoDUNE II** (installation is ongoing, start operation in 2023)
  - The prototype detectors are arranged similar to the final Far Detector
  - New versions ColdADC and COLDATA are implemented
  - LArASIC has been further improved
  - Engineering and integration have been further advanced
  - Vertical Drift LArTPC will be tested as well

### Summary

- Cryogenic electronics readout is critical to reach the LArTPC performance goal
- The cryogenic electronics are mounted directly on the detectors, the performance exceeds the DUNE experiment requirements
- The cryogenic electronics will be tested in protoDUNE-II
- Dedicated QC tests are designed to ensure the delivery of high quality components to DUNE

![](_page_22_Picture_5.jpeg)