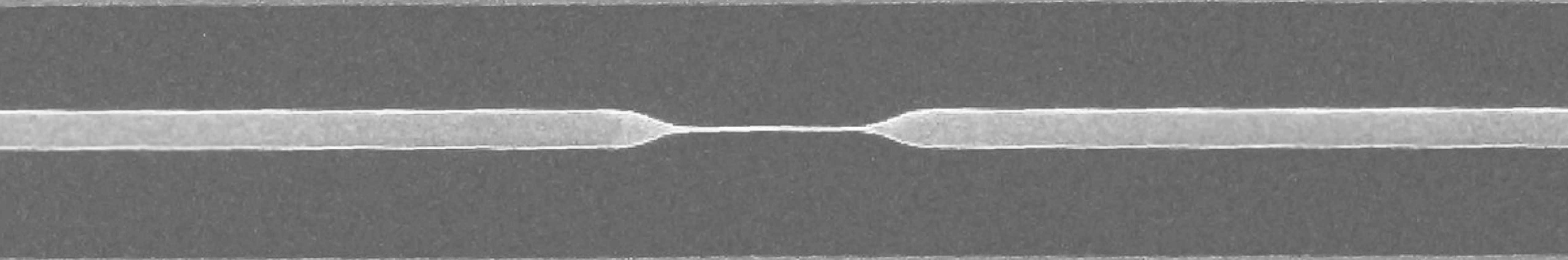
The Cryotron Reborn: Superconducting-Nanostrip-Based Electronics



Karl K. Berggren

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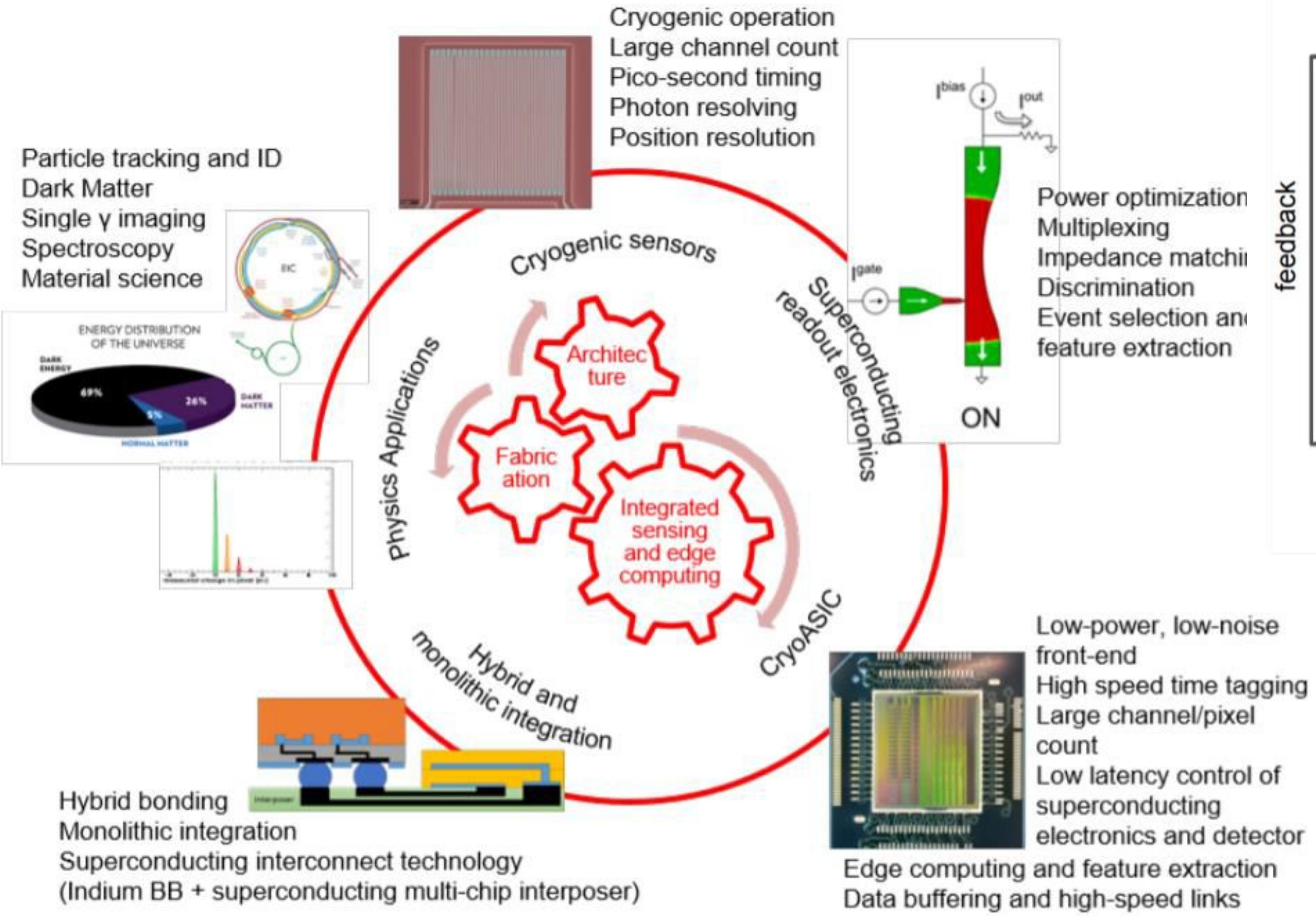
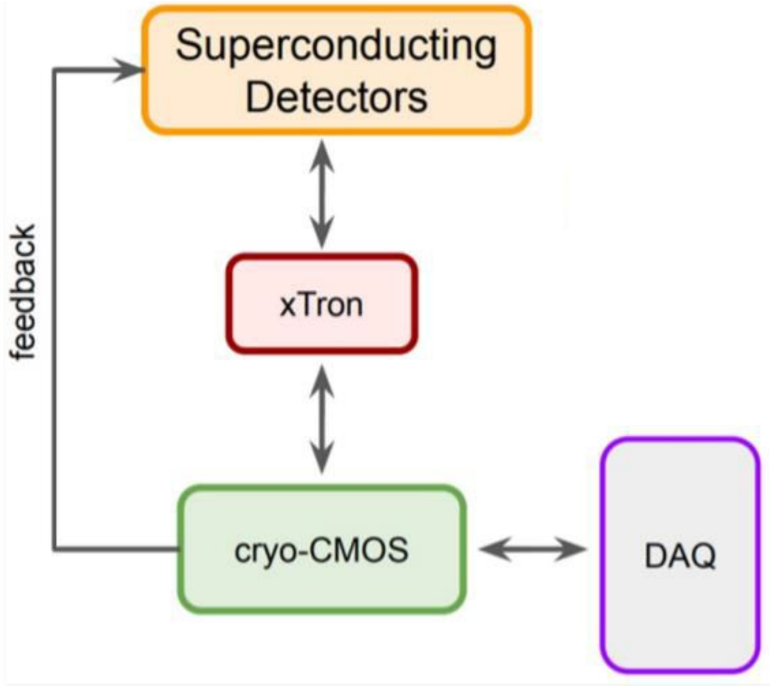
berggren@mit.edu

https://www.rle.mit.edu/qnn/

What do HEP Detectors Need that Superconducting Nanowires can Provide?

Hybrid superconducting detector platform



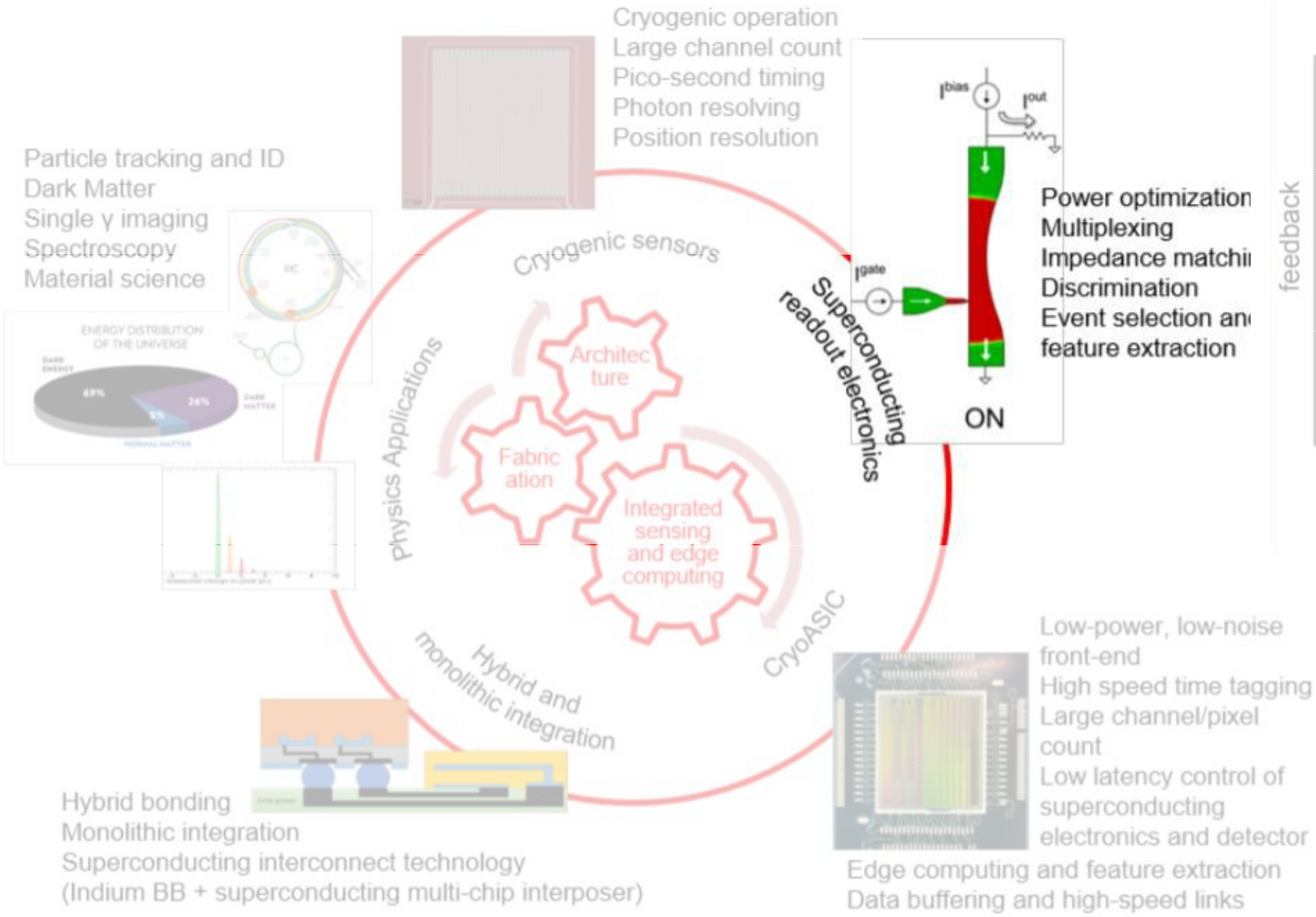


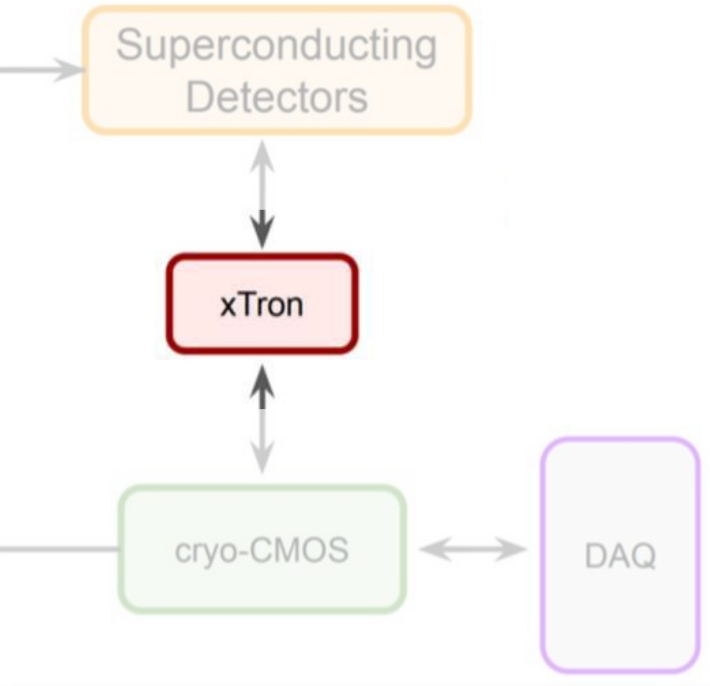
Project Leader, Davide Braga
Fermilab

Fermilab U.S. DEPARTMENT OF ENERGY Office of Science

Team members: MIT, JPL, NIST, Synopsys, Argonne National Lab

Hybrid superconducting detector platform





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Team members: MIT, JPL, NIST, Synopsys, Argonne National Lab

HEP Needs

- Operation in low-temperature environments
- Operation in high-radiation environments
- Operation in strong magnetic fields
- Basic digital functions (counting, shifting, mux/demux)
- Basic analog functions (amplification, threshold detection)
- Integration with superconducting detectors
- Integration with CMOS

What can be sacrificed?

- Ultra-high integration scale (warmer CMOS can be used, outside of the B field)
- Ultra-high speeds (need to keep up with data rate, not CMOS clock rate)

Home > AIP Advances > Volume 2, Issue 3 > 10.1063/1.4740074

Open • Submitted: 08 February 2012 • Accepted: 16 July 2012 • Published Online: 24 July 2012

Efficient single particle detection with a superconducting nanowire

Unconventional Applications of Superconducting Nanowire Single Photon Detectors

by Tomas Polakovic [1,2], Whitney Armstrong [1], Goran Karapetrov [2,3], Zein-Eddine Meziani [1] and Valentine Novosad [1,4,*]

[1] Physics Division, Argonne National Laboratory, Argonne, IL 60439, USA

[2] Department of Physics, Drexel University, Philadelphia, PA 19104, USA

[3] Department of Materials Science and Engineering, Drexel University, Philadelphia, PA 19104, USA

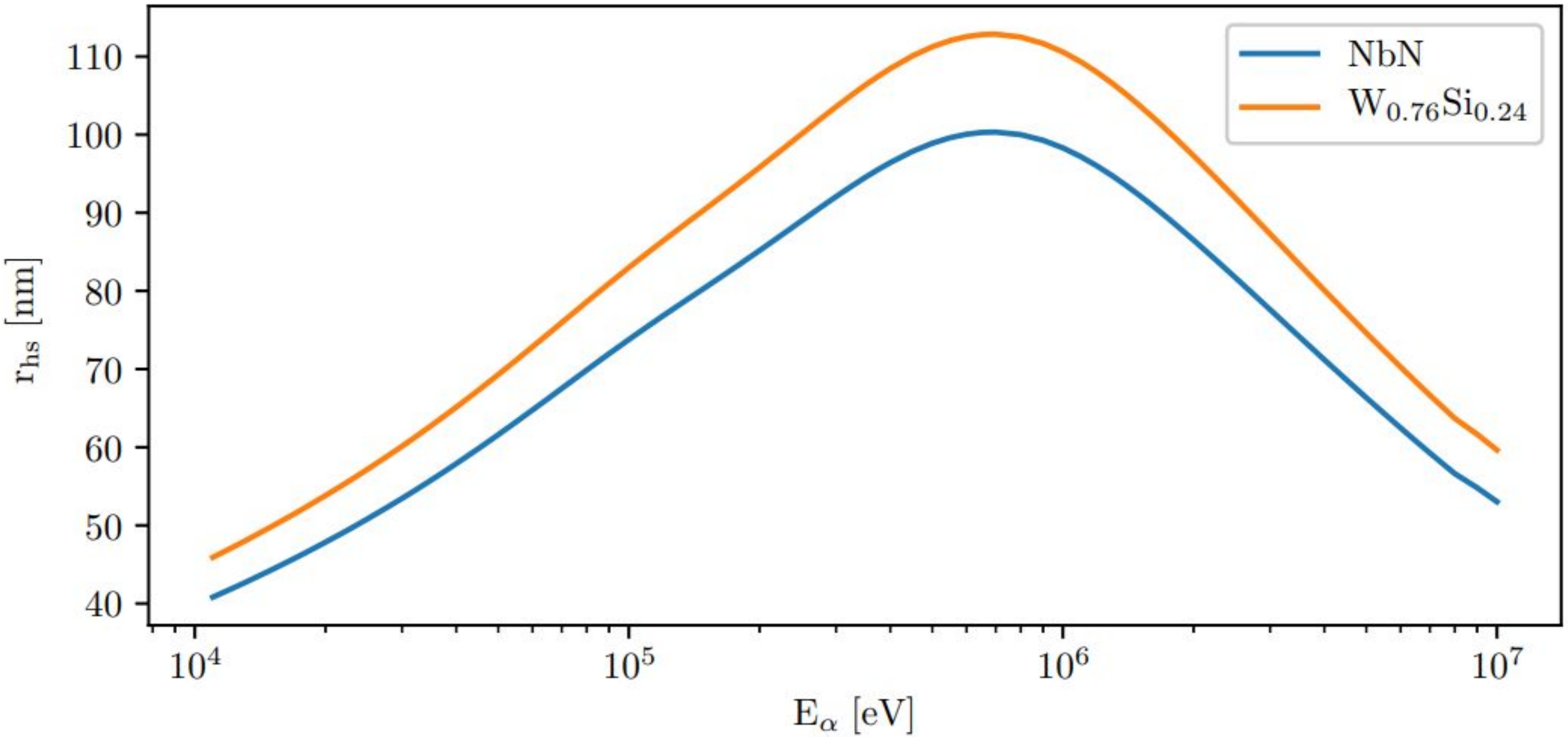
[4] Materials Science Division, Argonne National Laboratory, Argonne, IL 60439, USA

[*] Author to whom correspondence should be addressed.

Nanomaterials **2020**, *10*(6), 1198; **https://doi.org/10.3390/nano10061198**

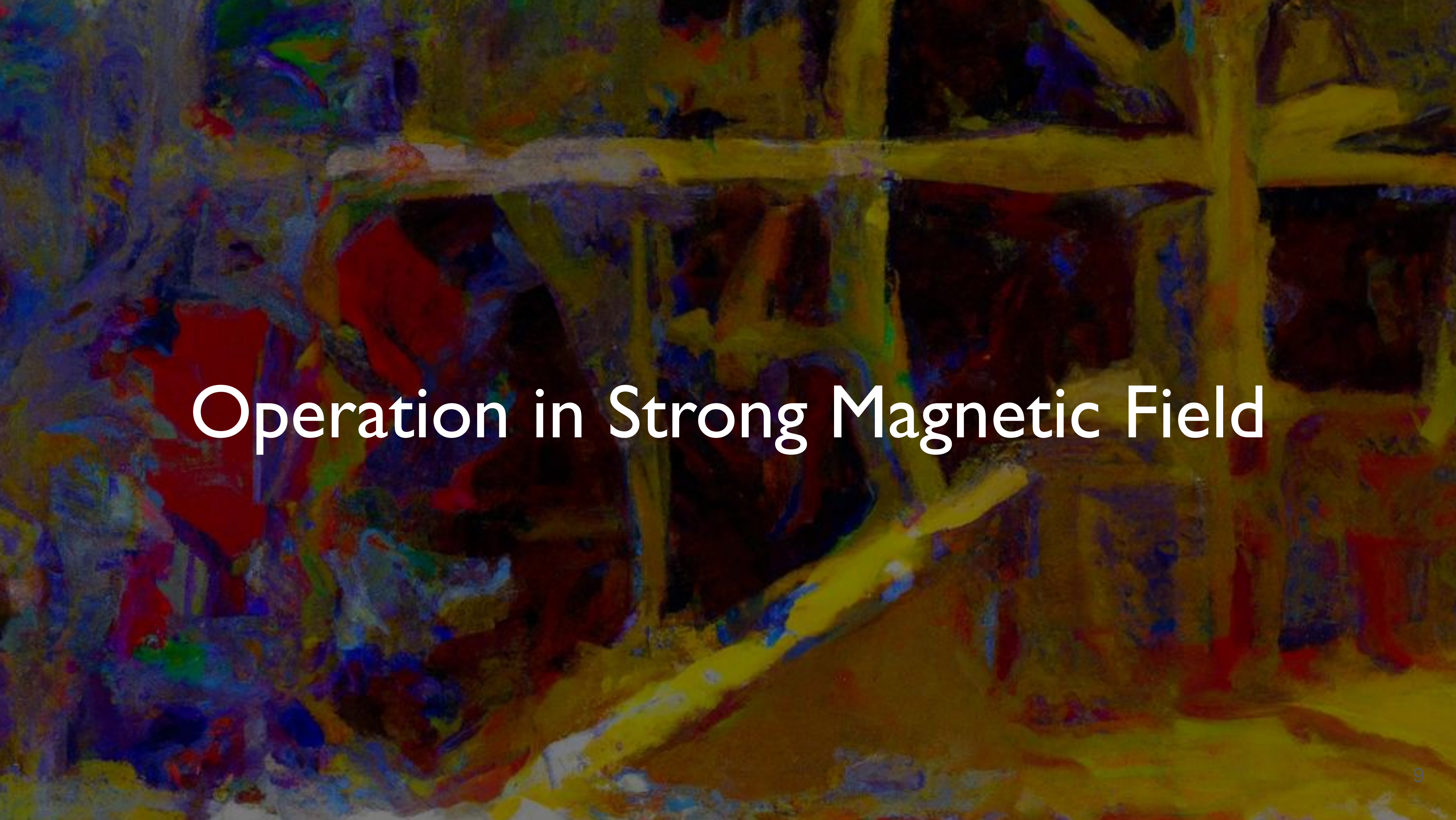
Received: 18 May 2020 / Revised: 7 June 2020 / Accepted: 8 June 2020 / Published: 19 June 2020

(This article belongs to the Special Issue **Superconductivity in Nanoscaled Systems**)



Polakovic 2020

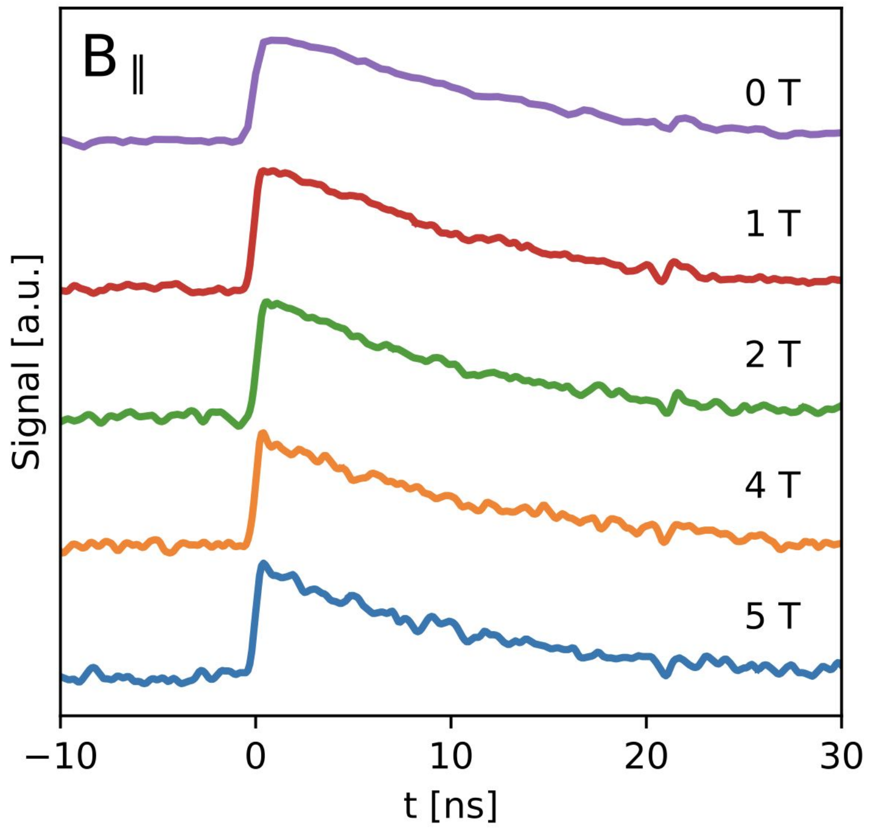
Figure 4. Approximate thermal hotspot radius r_{hs} as a function of α-particle kinetic energy in NbN film with T_C = 8K and $W_{0.76}Si_{0.24}$ film with T_C = 3.35 K. Both films are assumed to be held at $T_0 = \frac{T_C}{2}$.

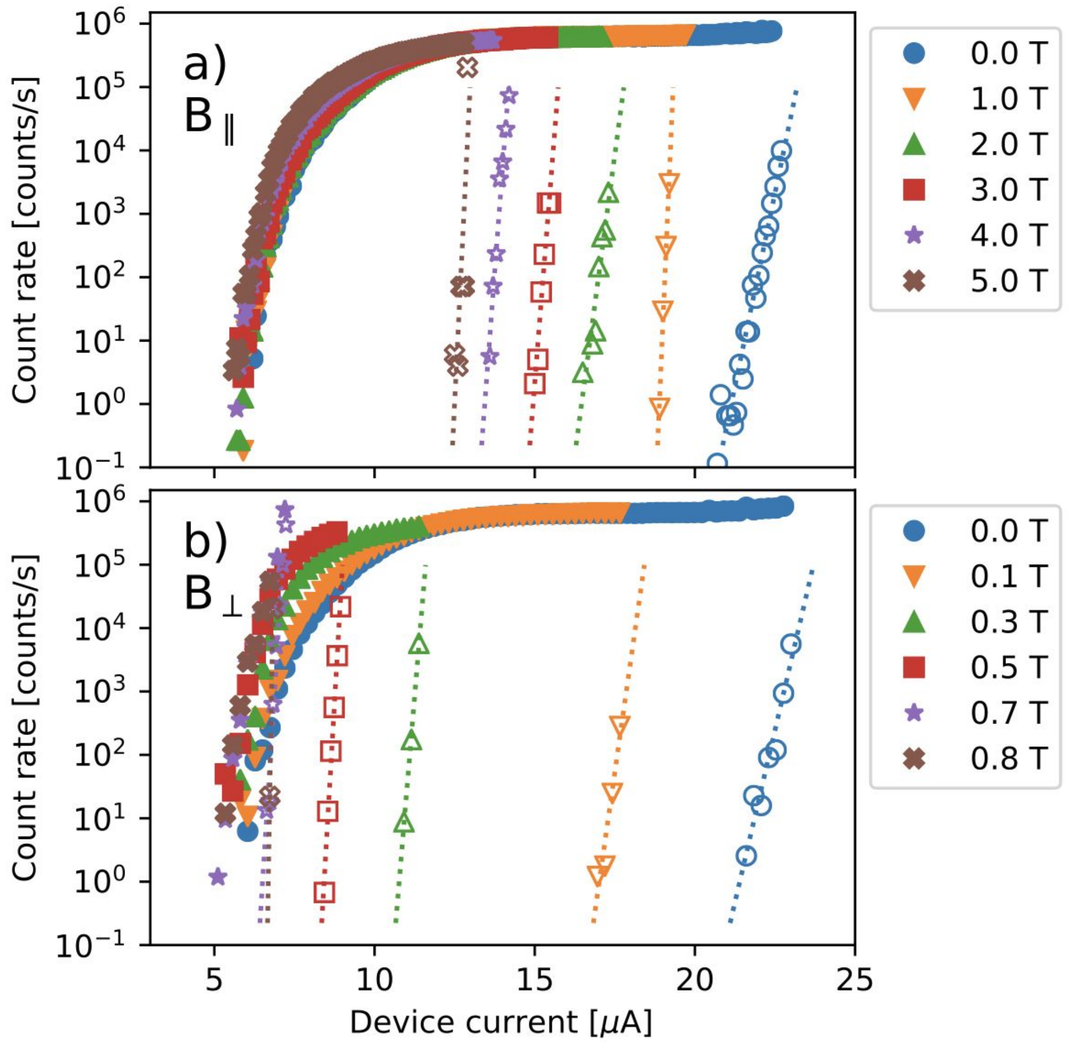


Operation in Strong Magnetic Field

Superconducting nanowires as high-rate photon detectors in strong magnetic fields

T. Polakovic[a,d], W.R. Armstrong[a], V. Yefremenko[b], J.E. Pearson[c], K. Hafidi[a], G. Karapetrov[d,e], Z.-E. Meziani[a], V. Novosad[c,*]





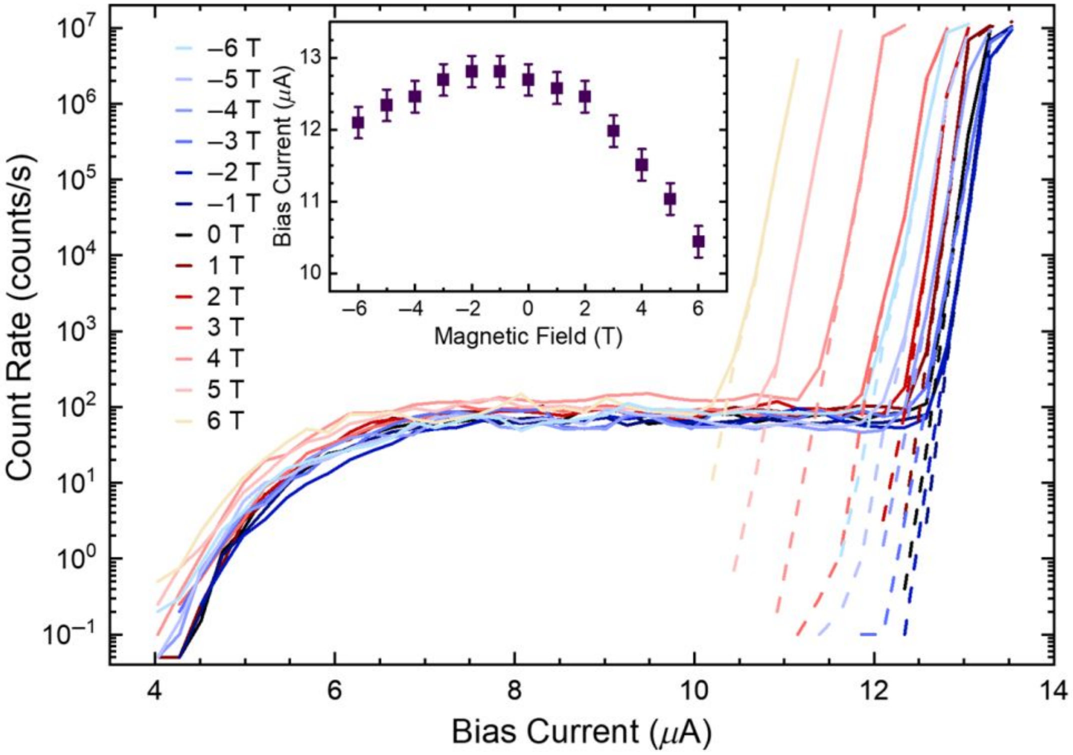
Polakovic, Tomas et al. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 959 (2020): 163543.

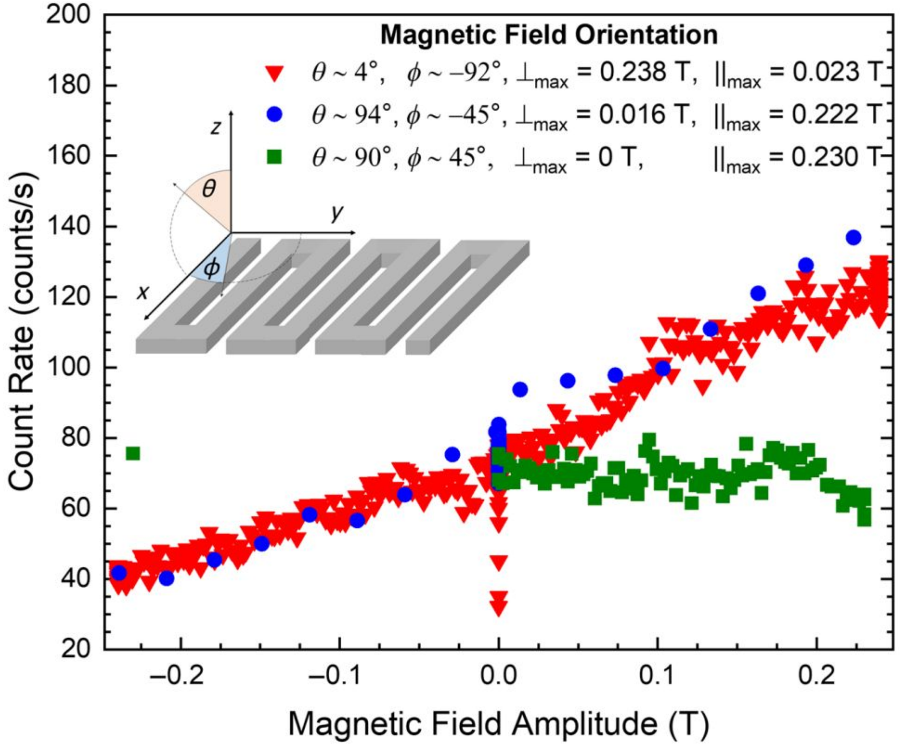
Multifunctional Superconducting Nanowire Quantum Sensors

Benjamin J. Lawrie,[1,*] Claire E. Marvinney,[1,†] Yun-Yi Pai,[1] Matthew A. Feldman,[1] Jie Zhang,[1]
Aaron J. Miller,[2] Chengyun Hua,[1] Eugene Dumitrescu,[3] and Gábor B. Halász[1]

[1] *Materials Science and Technology Division, Oak Ridge National Laboratory, 1 Bethel Valley Road, Oak Ridge, Tennessee 37831, USA*
[2] *Quantum Opus LLC, Novi, Michigan 48375, USA*
[3] *Computational Science and Engineering Division, Oak Ridge National Laboratory, 1 Bethel Valley Road, Oak Ridge, Tennessee 37831, USA*

(Received 18 March 2021; revised 19 September 2021; accepted 9 November 2021; published 23 December 2021)

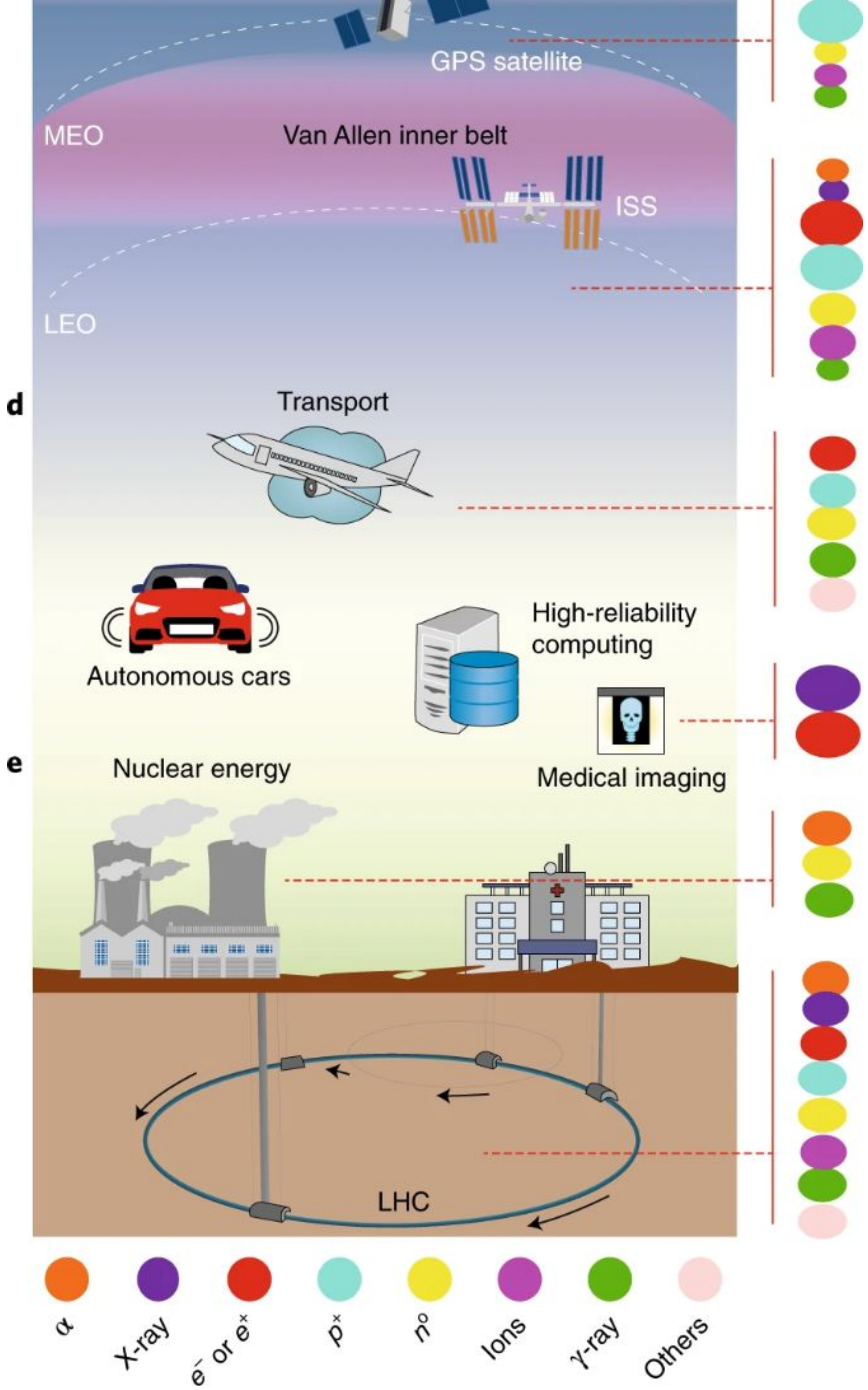




Benjamin J. Lawrie, et. al., "Multifunctional Superconducting Nanowire Quantum Sensors," Phys. Rev. Applied 16, 064059 (2021)

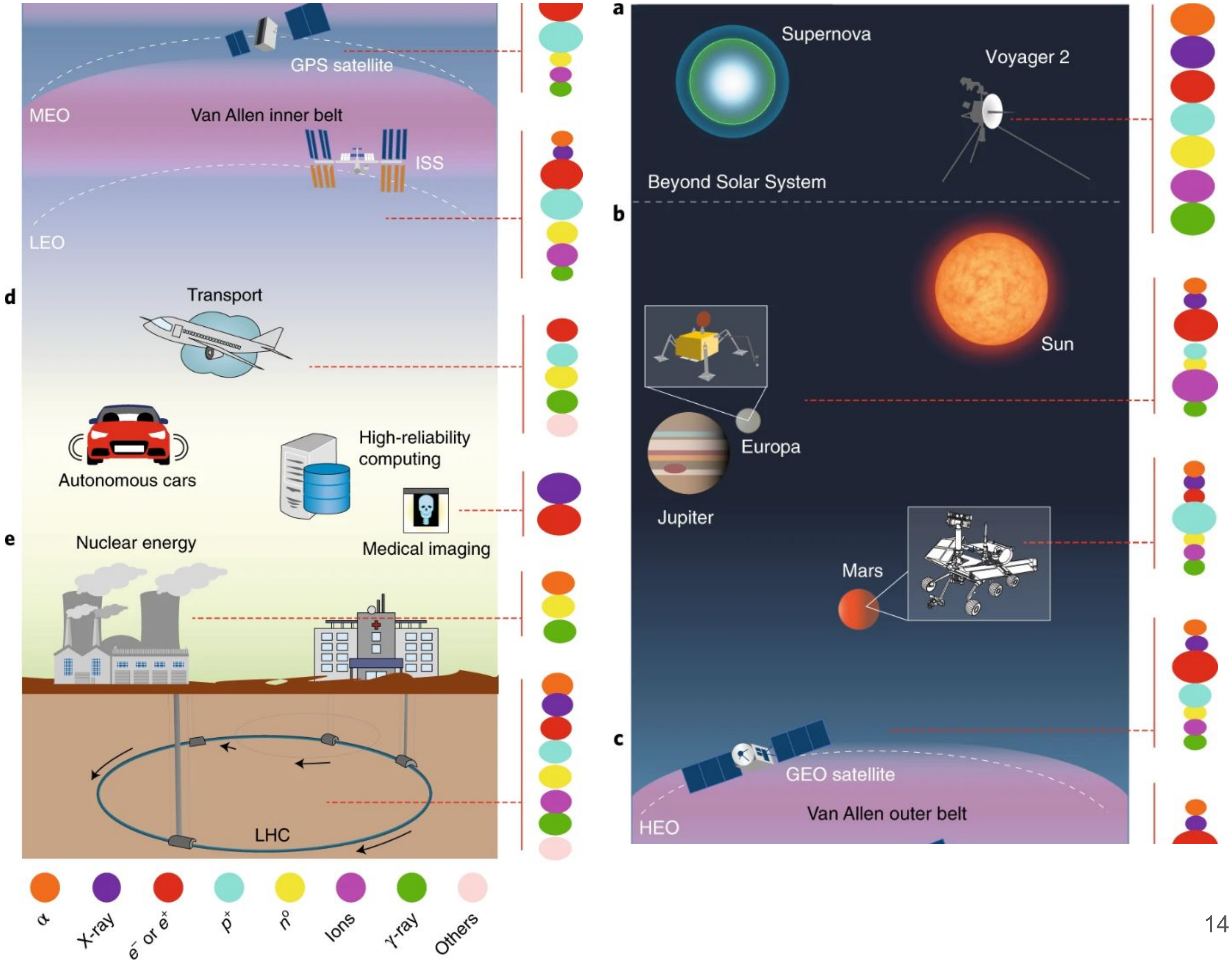
Radiation Hard

Radiation Environment



Prinzie, J., Simanjuntak, F.M., Leroux, P. *et al.* Low-power electronic technologies for harsh radiation environments. *Nat Electron* 4, 243–253 (2021). https://doi-org.libproxy.mit.edu/10.1038/s41928-021-00562-4

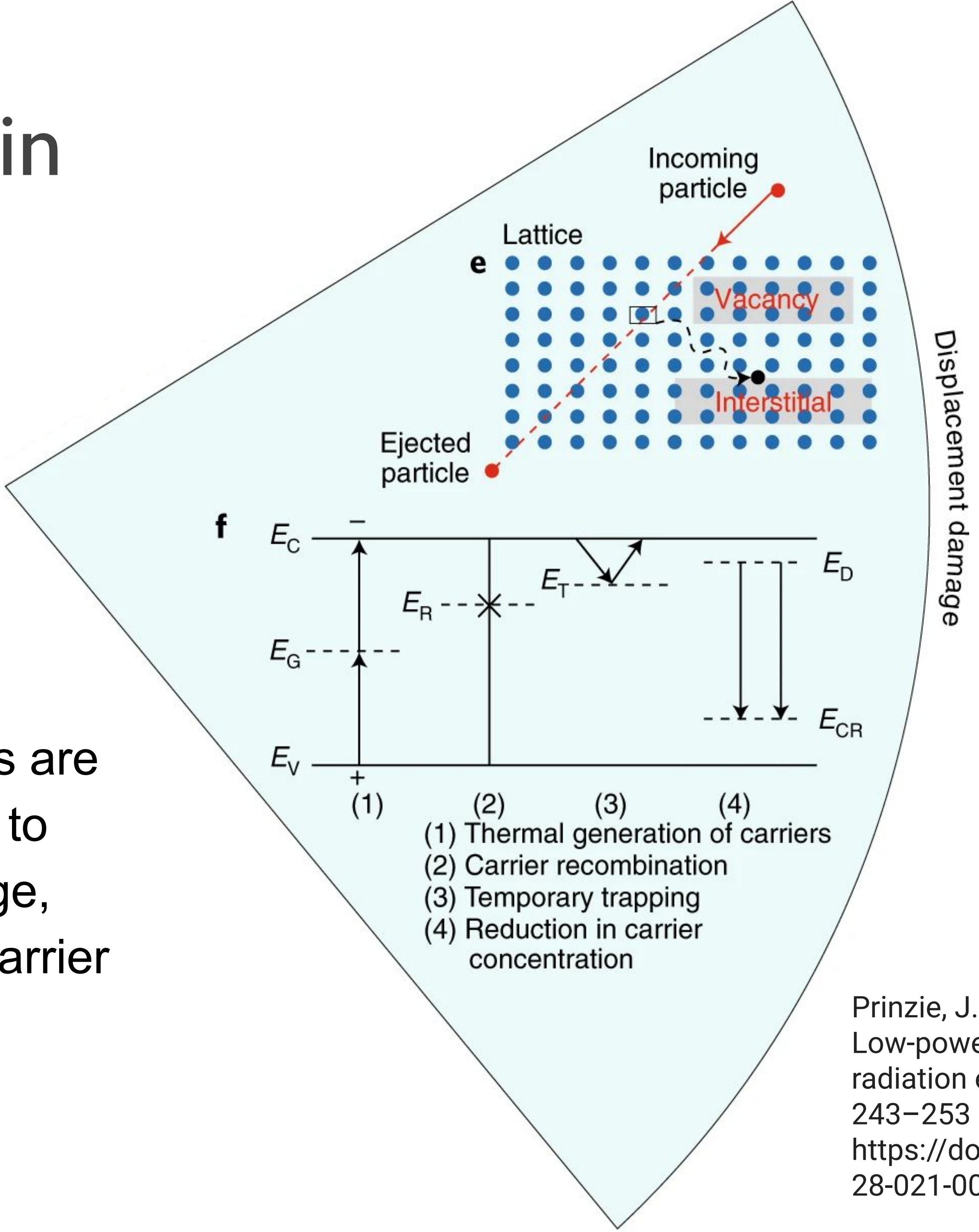
Radiation Environment



Prinzie, J., Simanjuntak, F.M., Leroux, P. *et al.* Low-power electronic technologies for harsh radiation environments. *Nat Electron* 4, 243–253 (2021). https://doi-org.libproxy.mit.edu/10.1038/s41928-021-00562-4

Lattice Damage in CMOS and JJs

- Josephson Junctions are likely to be sensitive to displacement damage, which will alter the barrier shape and height



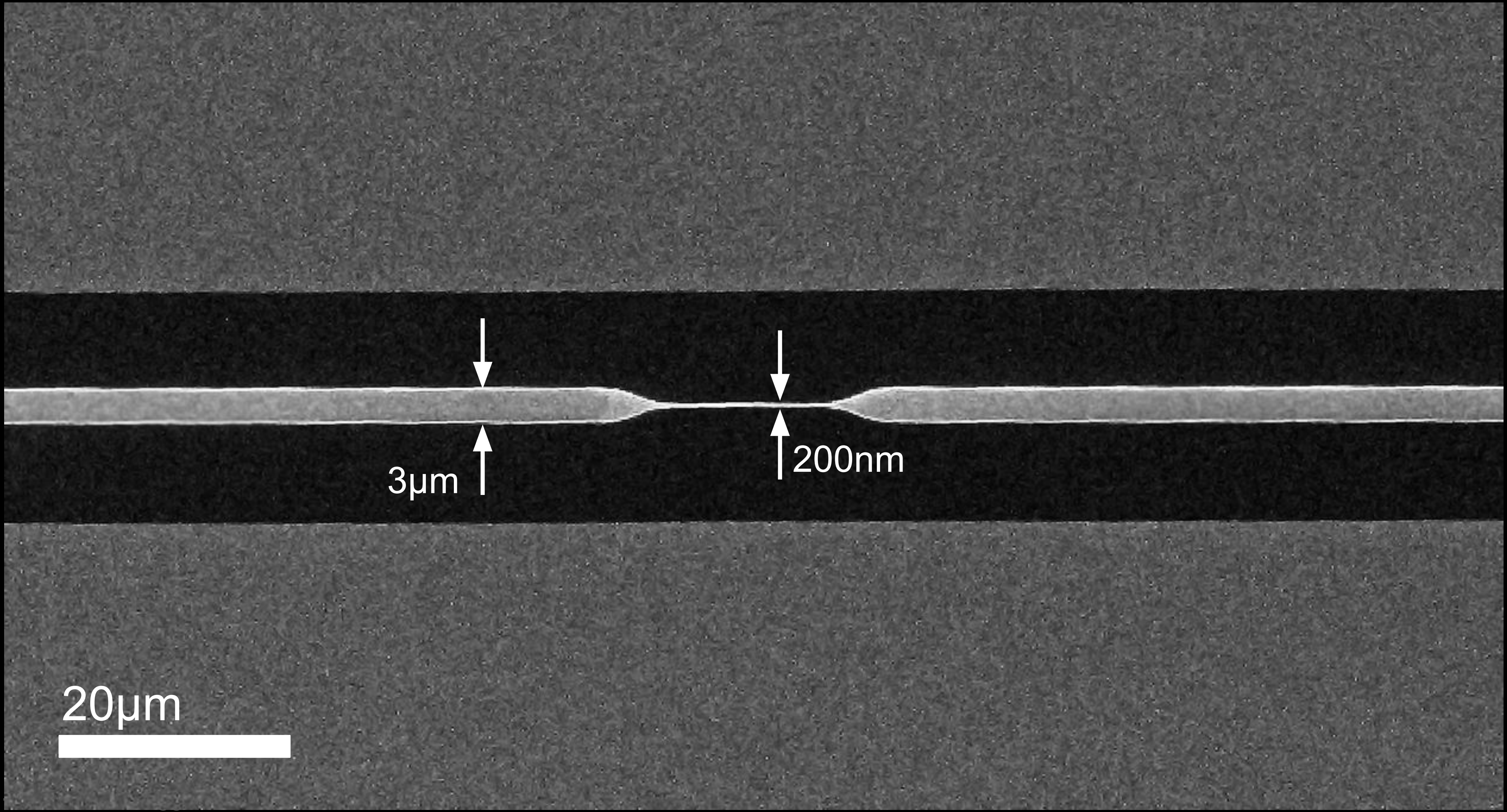
Prinzie, J., Simanjuntak, F.M., Leroux, P. *et al.* Low-power electronic technologies for harsh radiation environments. *Nat Electron* 4, 243–253 (2021). https://doi-org.libproxy.mit.edu/10.1038/s41928-021-00562-4

Radiation Tolerance of Niobium Nitride

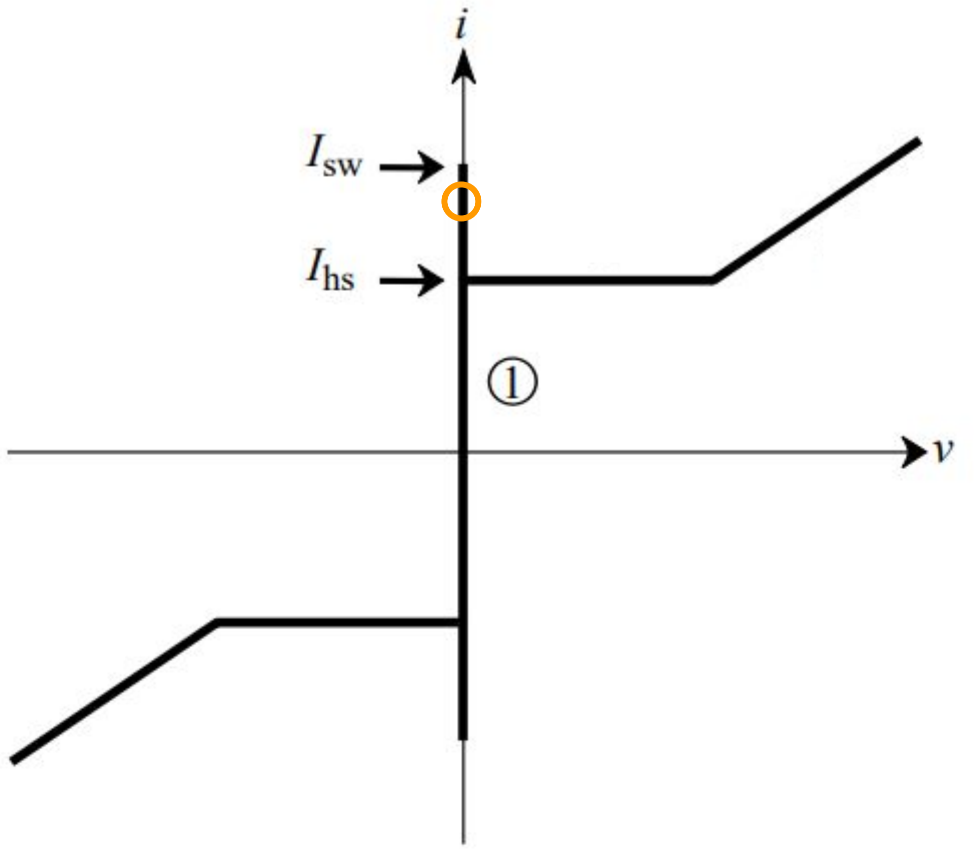
- Previous NbN radiation study[1] with fast neutron fluence of **10^{23}** m^{-2}
    - In low orbit (297 km altitude[2]), fast neutron flux of 3.4 x **10^{8}** $m^{-2}day^{-1}$
    - T_c decreased by 5.7%
    - ϱ increased by 6.3%
    - J_c did not change

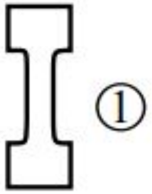
[1]*Journal of Applied Physics* **64**, 1301 (1988); https://doi.org/10.1063/1.341850
[2]*Nucl. Tracks Radiat. Meas.* **17**, 87-91 (1990)

Superconducting Nanowire Device

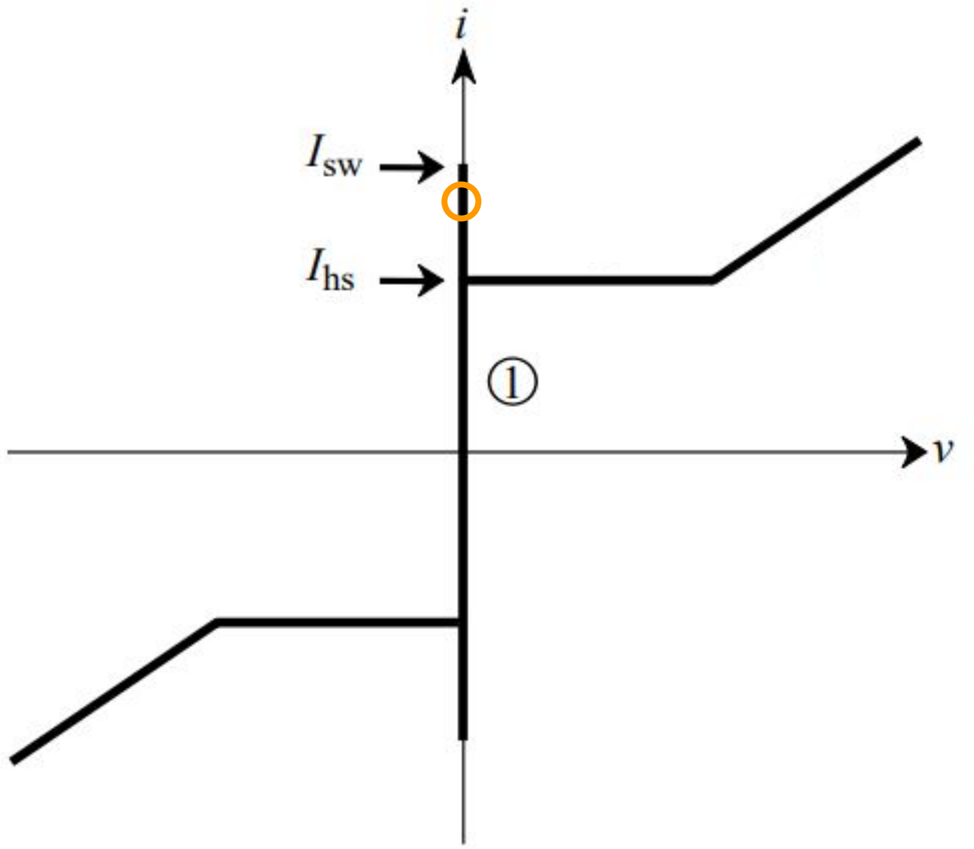


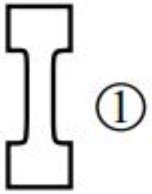
Initial Bias Condition



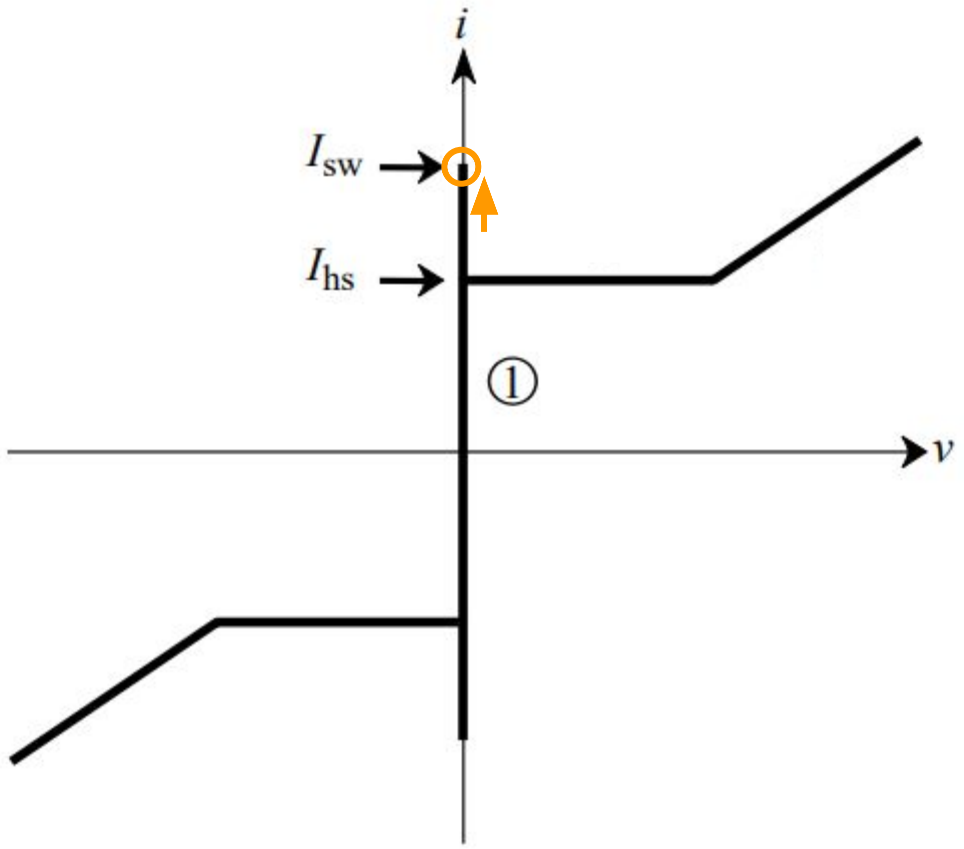


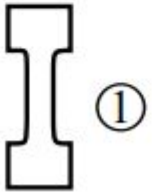
Initial Bias Condition



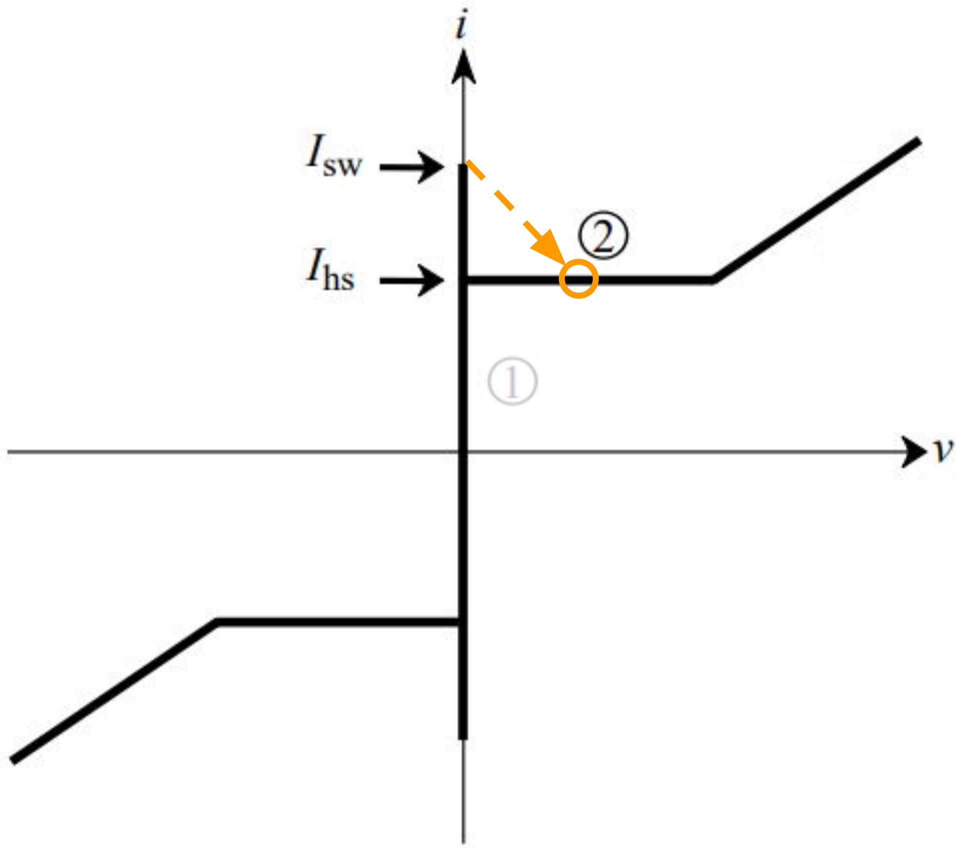


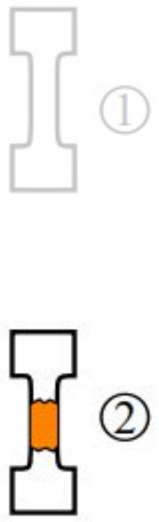
Trigger Event



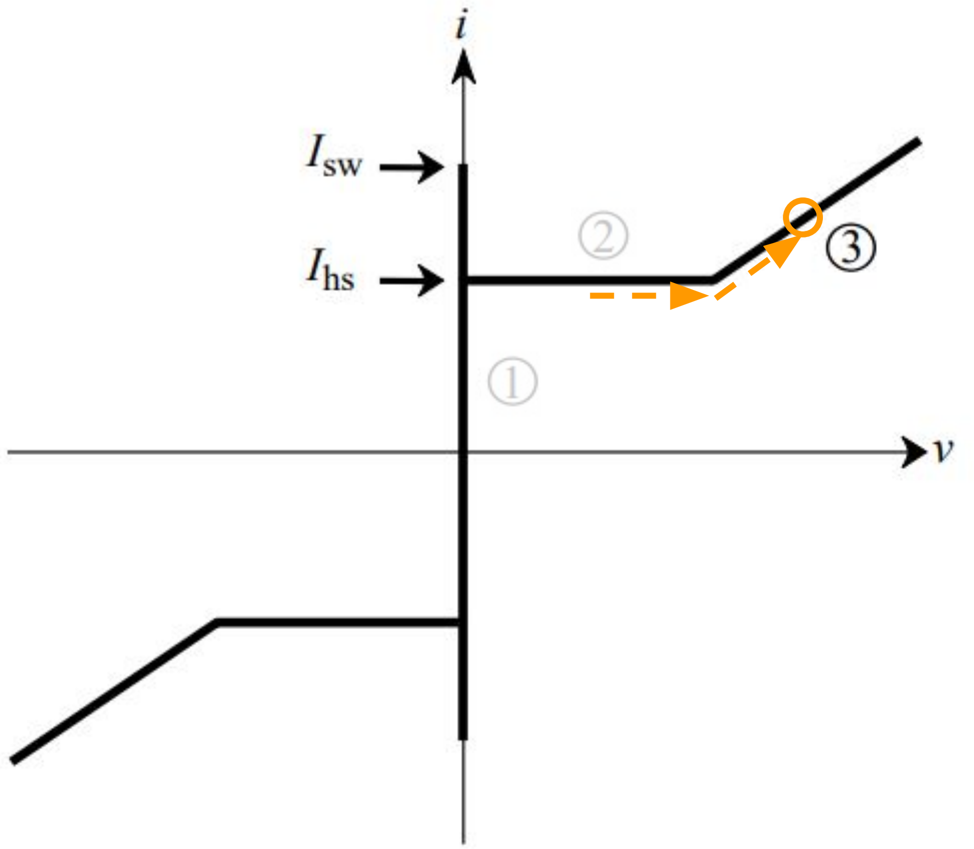


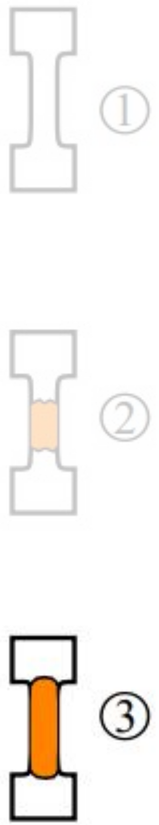
Hot Spot Creation and Growth



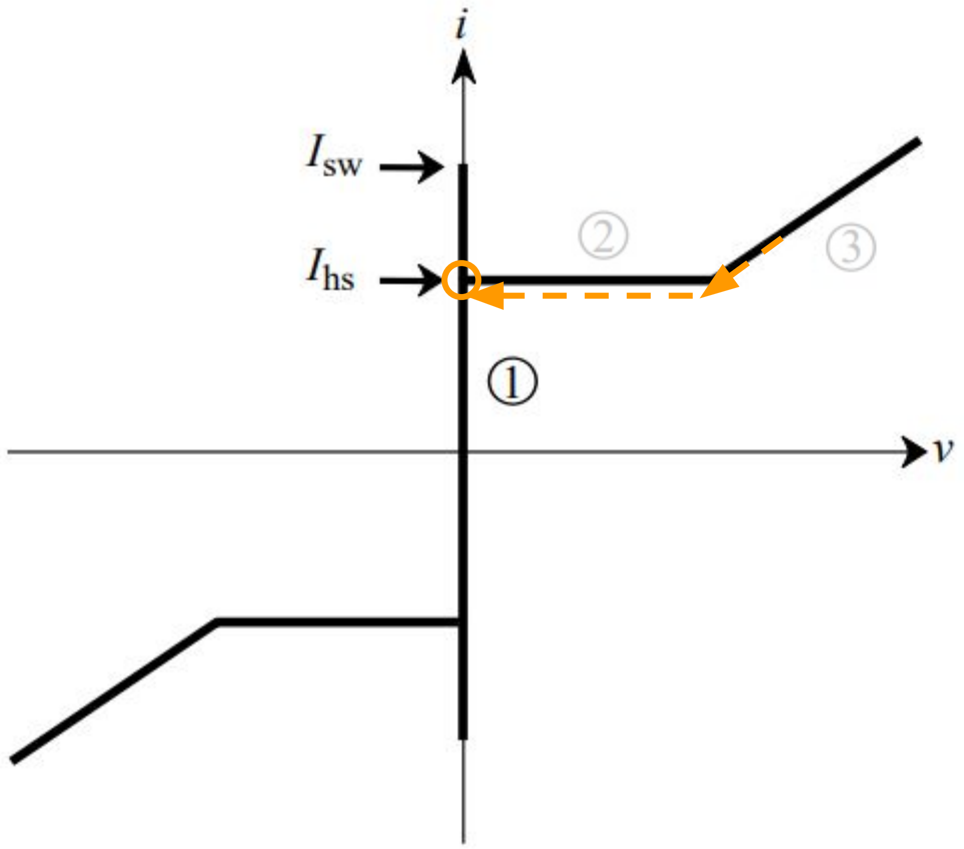


Hot Spot Saturation

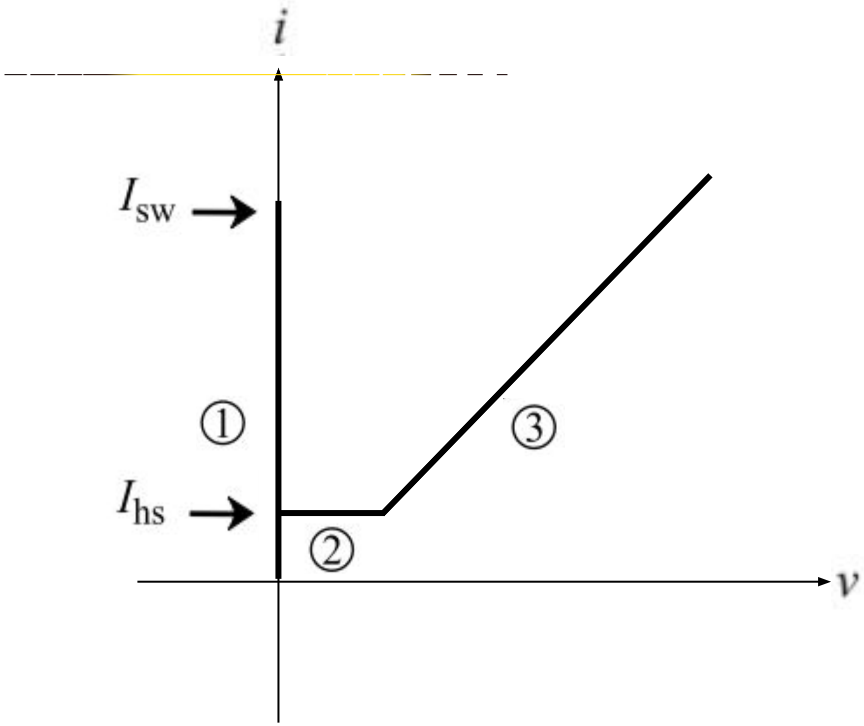


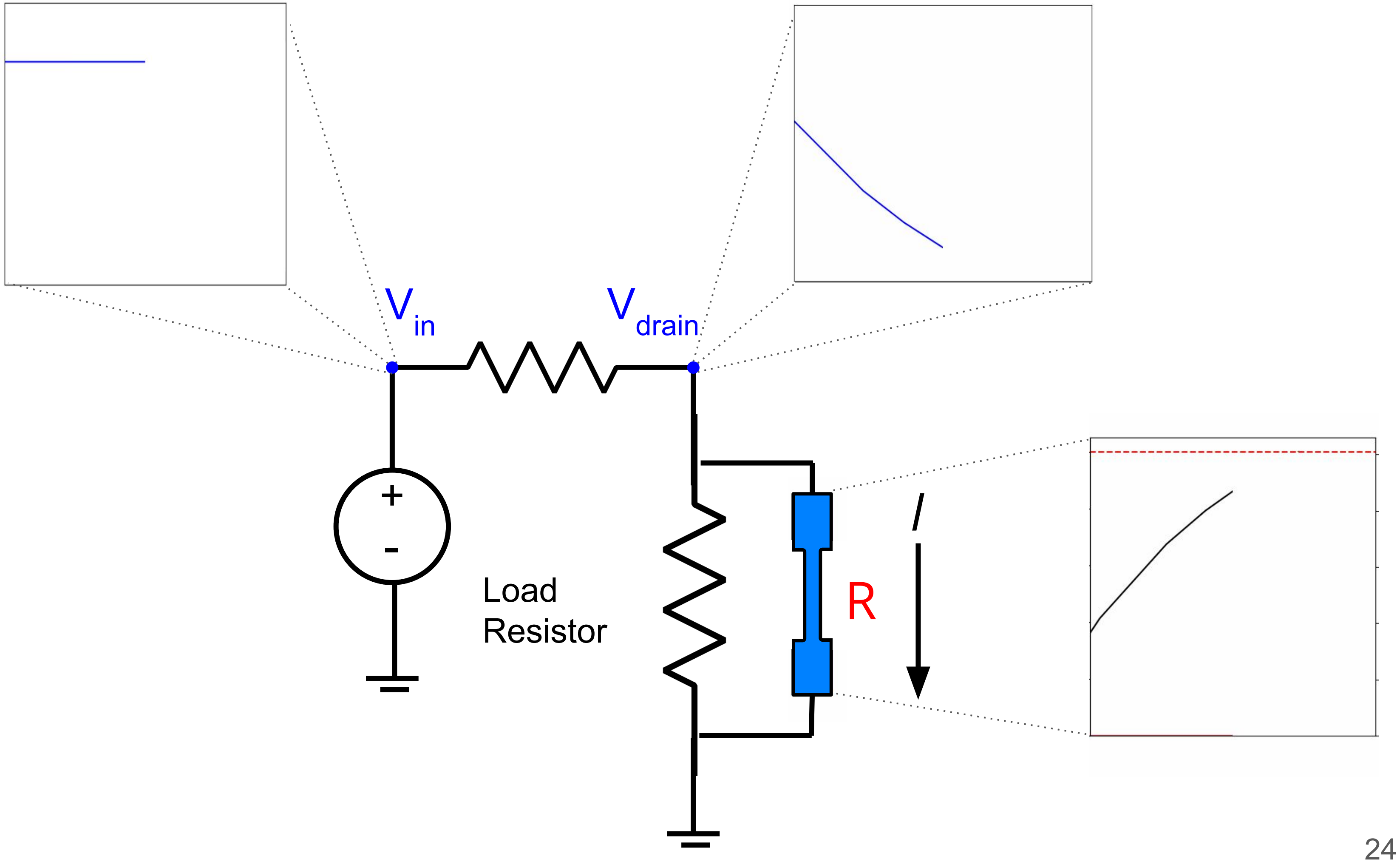


Collapse and Reset



Superconducting Nanowire in a Circuit





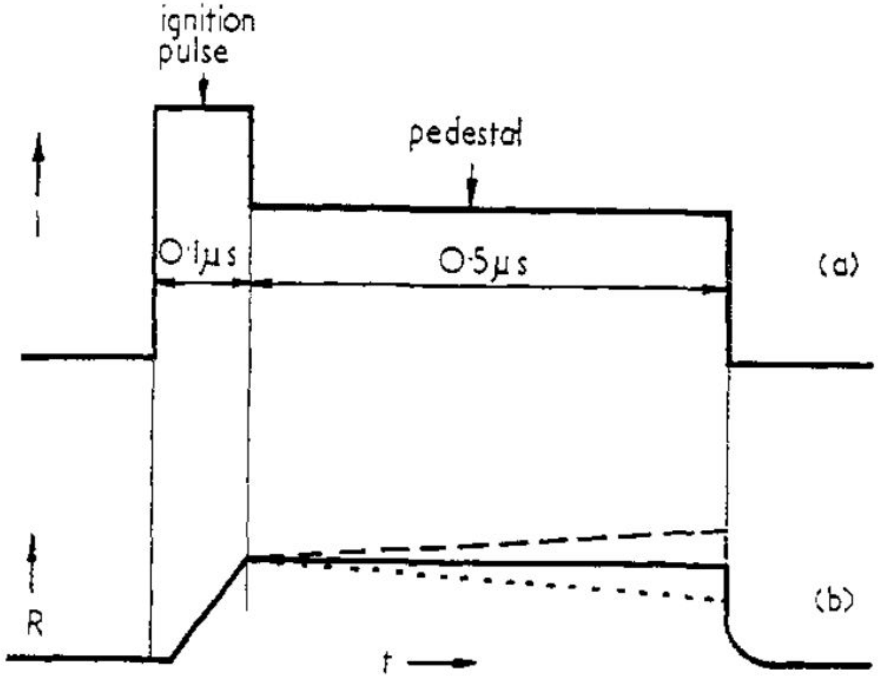
Calotron: Broom and Rhoderick 1960 Br. J. Appl. Phys 11 292

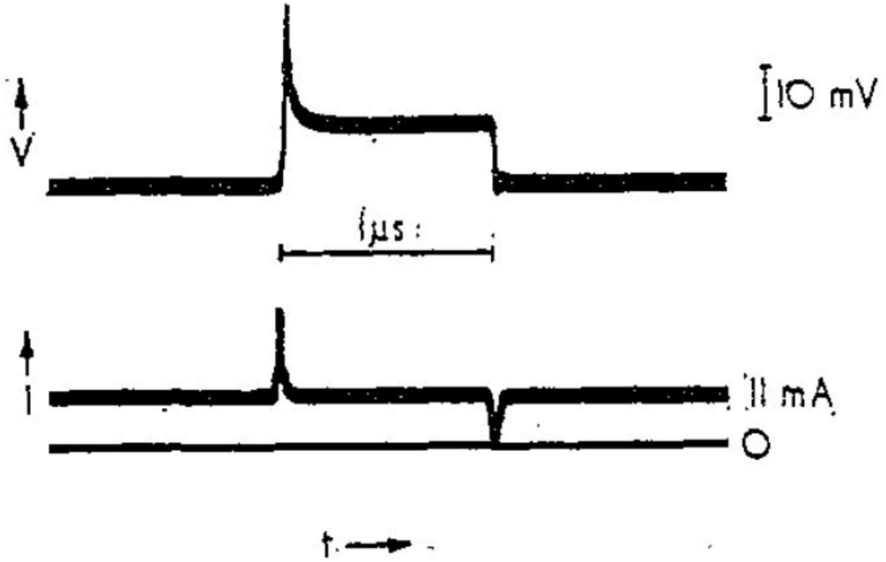
Thermal propagation of a normal region in a thin superconducting film and its application to a new type of bistable element

by R. F. BROOM, B.Sc., and E. H. RHODERICK, M.A., Ph.D., Services Electronics Research Laboratory, Baldock, Hertfordshire

[*Paper first received* 12 *January, and in final form* 13 *February*, 1960]

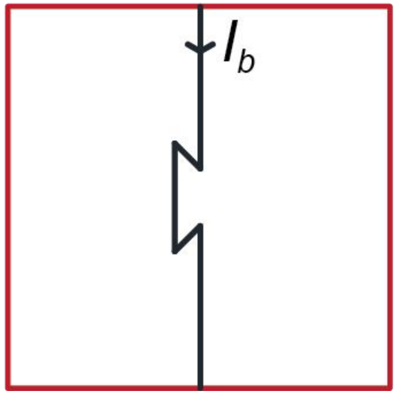
- Dual device to a DIAC





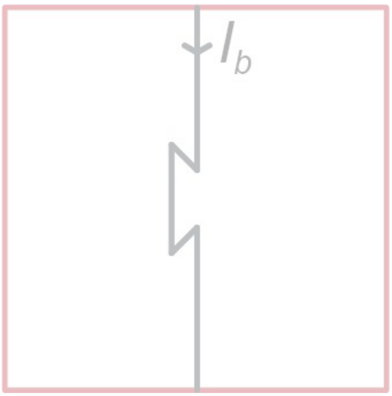
Bestiary of Nanowire Devices

constriction

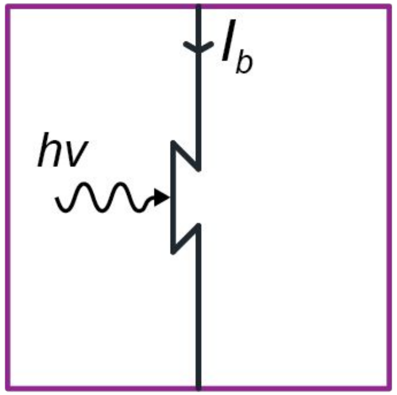


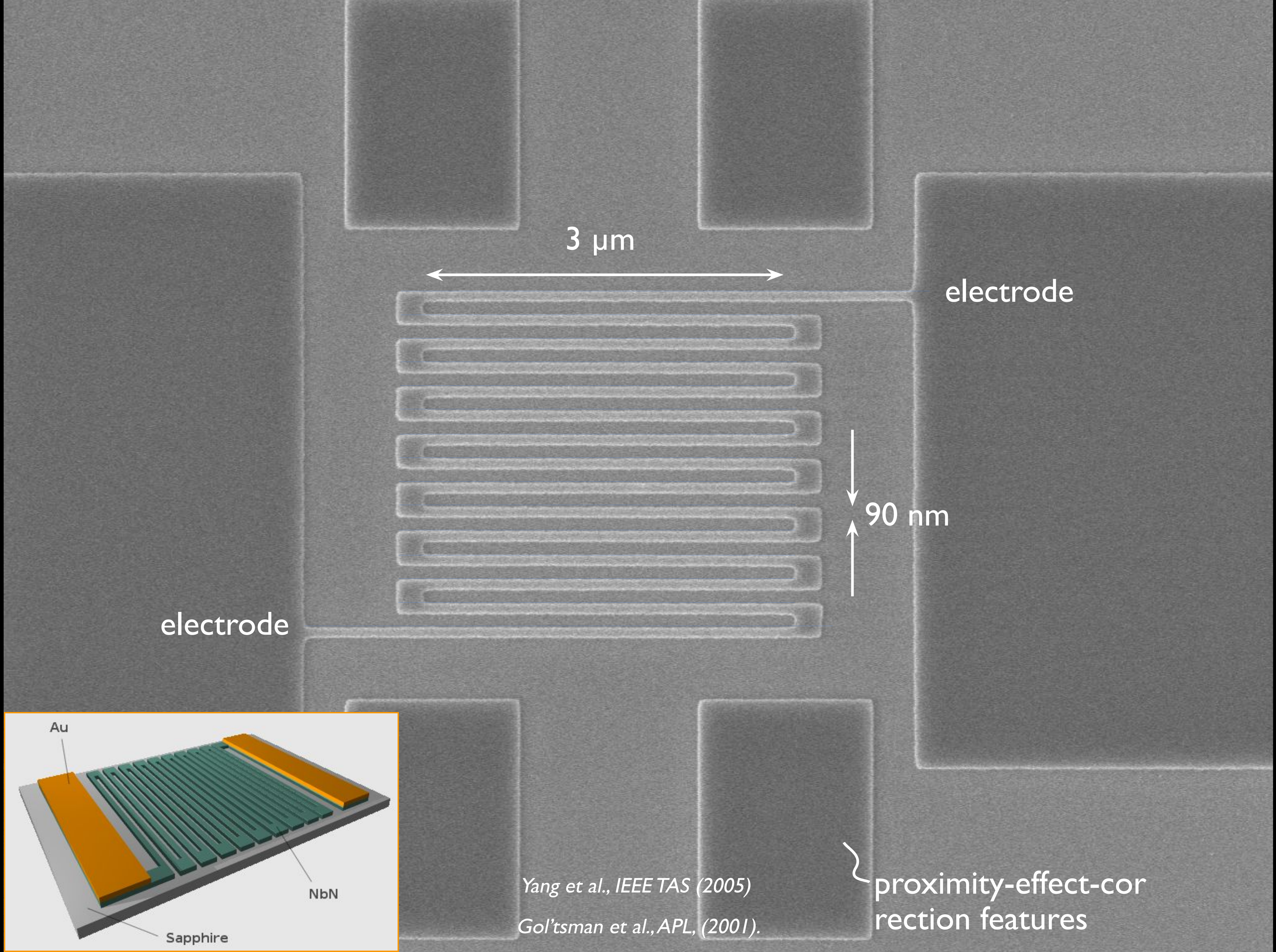
Bestiary of Nanowire Devices

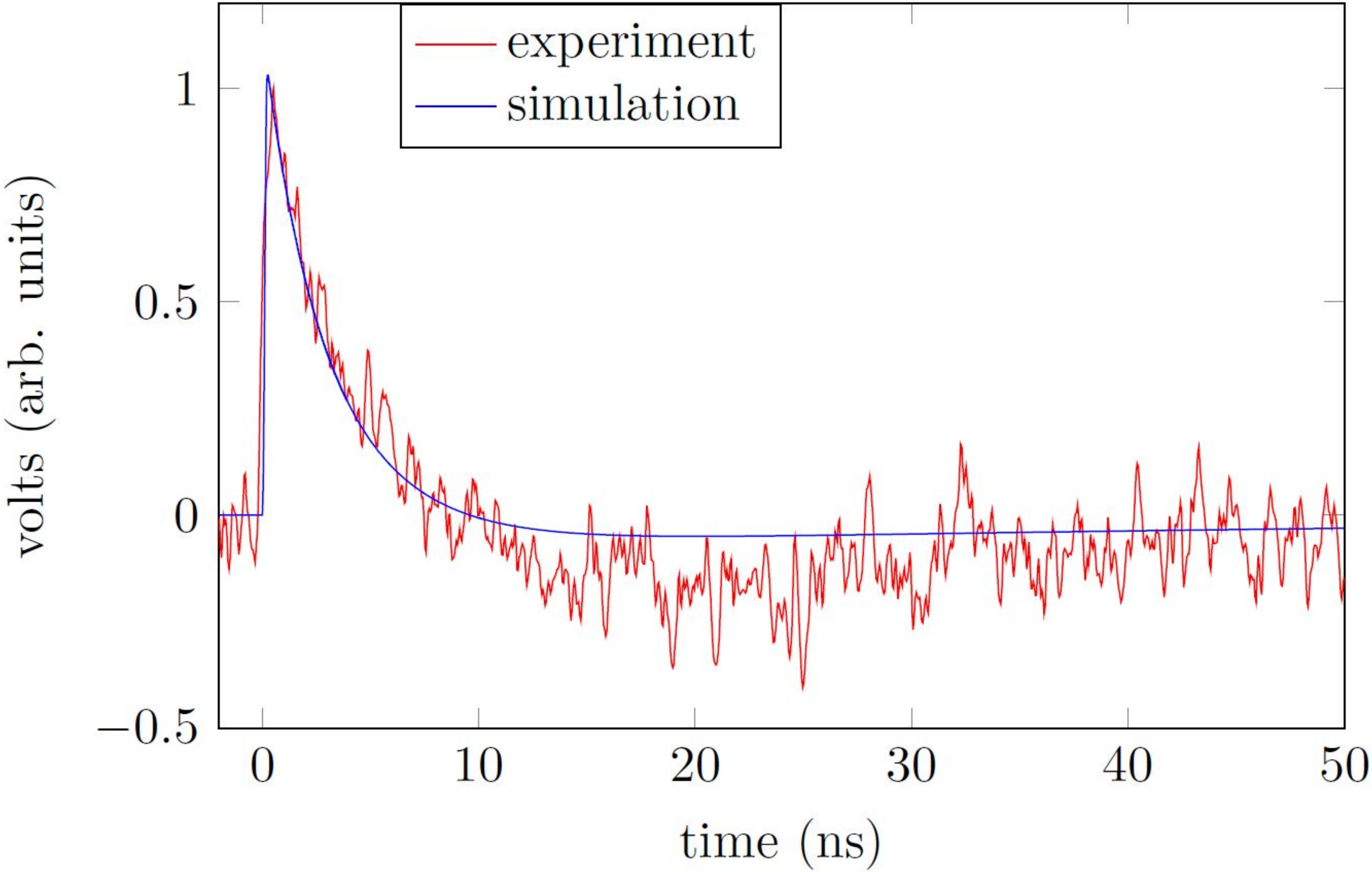
constriction



SNSPD



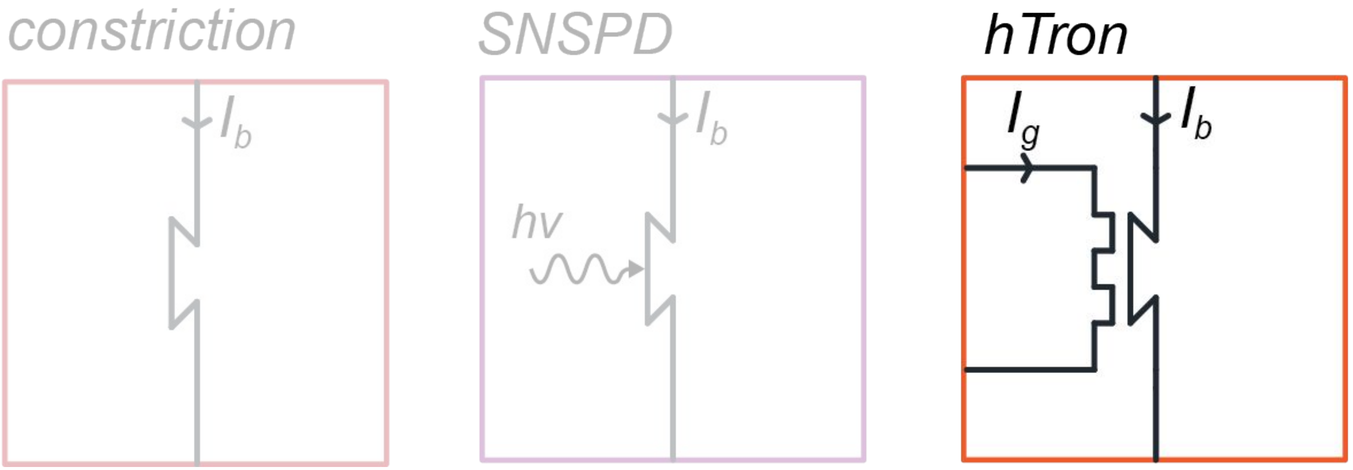

3 µm
electrode
90 nm
electrode
Au
NbN
Sapphire
Yang et al., IEEE TAS (2005)
Gol'tsman et al., APL, (2001).
proximity-effect-cor
rection features


experiment
simulation
volts (arb. units)
1
0.5
0
−0.5
0
10
20
30
40
50
time (ns)

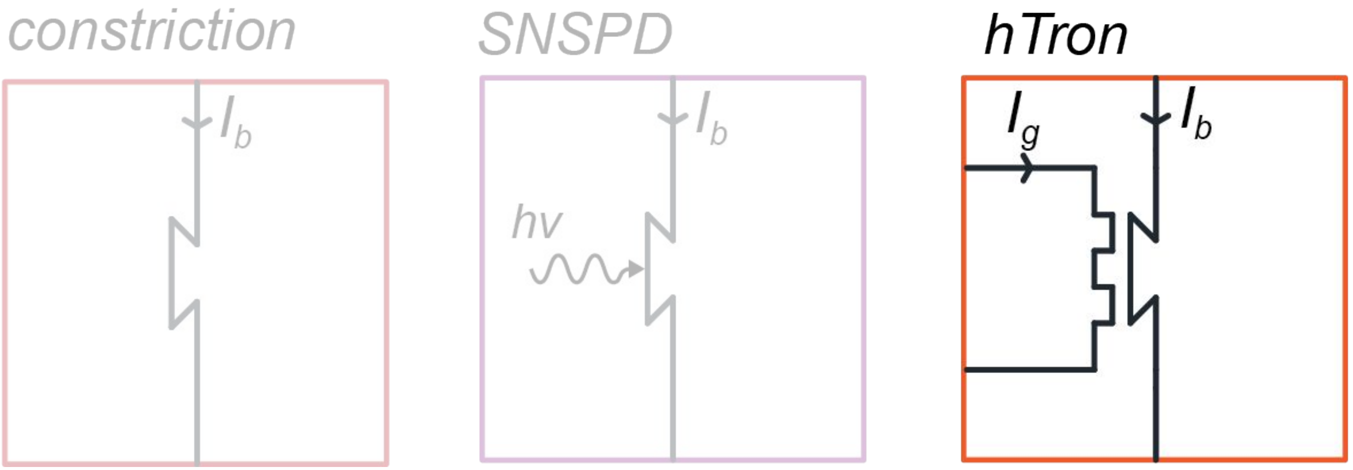
What SNSPDs tell us about Nanowire Logic

- Infrared efficiency for single photons up to 10 µm: single photon sensitivity ⇒ Narrow grey zone [Verma et al., APL Photonics, 2021]
- Jitter ≈ 3 ps [Korzh et. al. 2020]
- Reset time runs into thermal limits at ≈ 1.5 ns
    - Suggestions in MgB_2 it can be as low as 150 ps [Cherednichenko et al. SUST 2021]
- Dark-count rate (~ 1 per day) : consistent with cosmic rays [Chiles and Charaev, unpublished result]
- Convenient fabrication, shielding, amplification, temperature

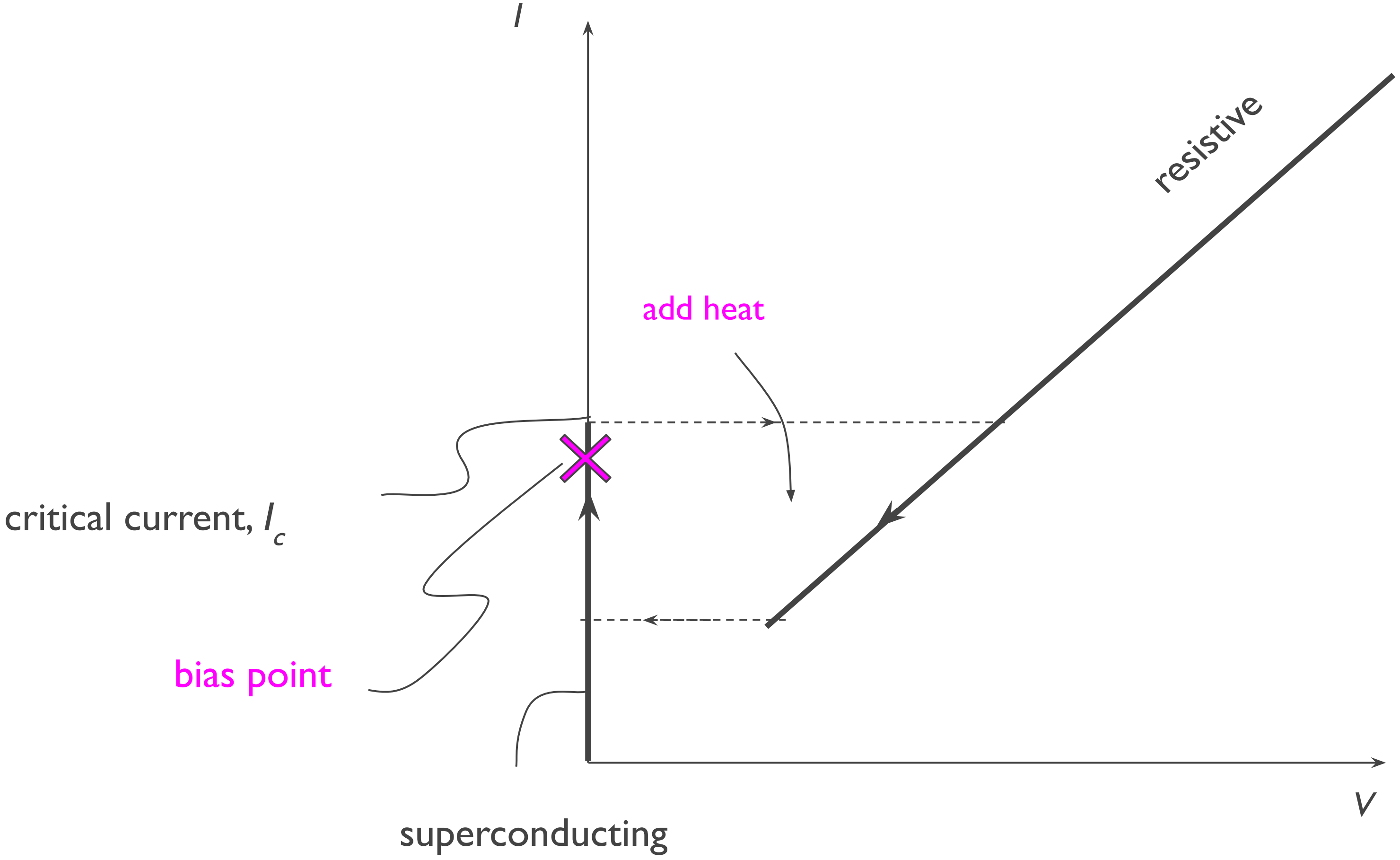
Bestiary of Nanowire Devices



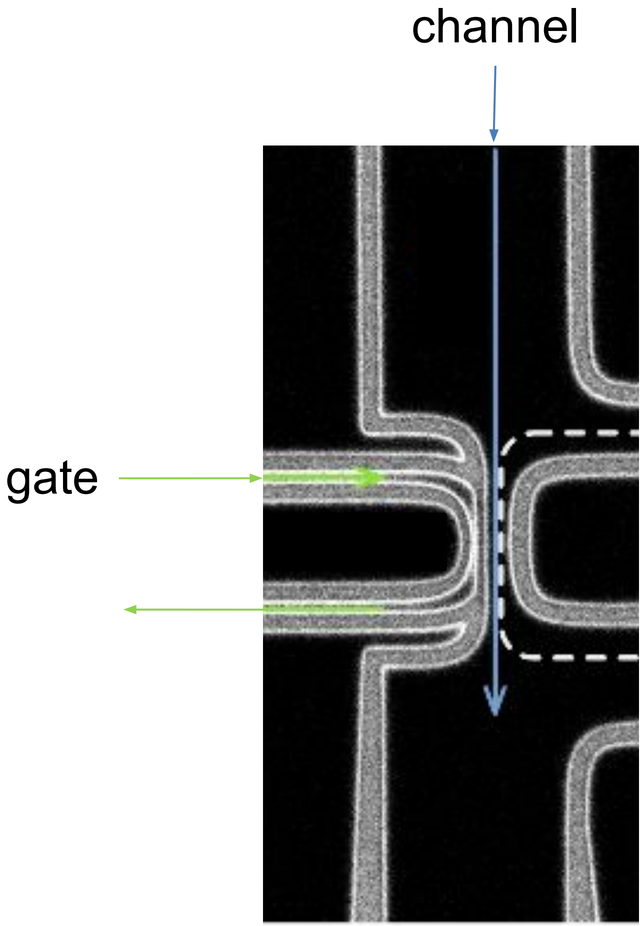
Bestiary of Nanowire Devices

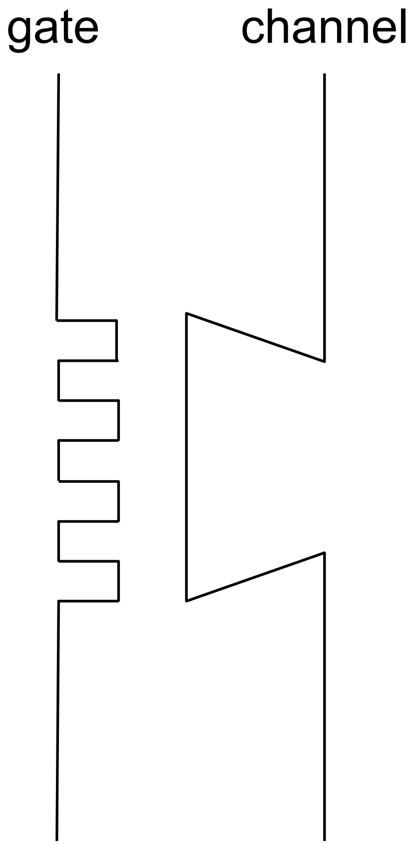


Thermo-Electric Switch



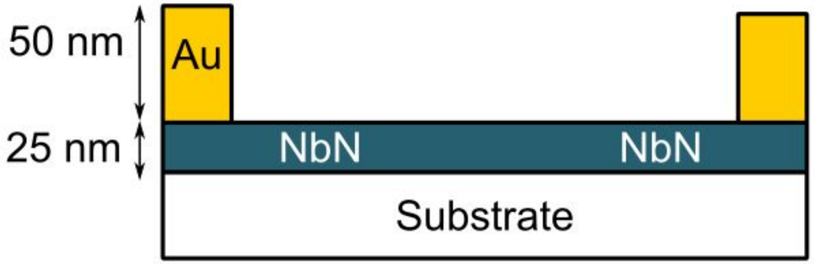
Thermal Cryotron: heater (h)Tron



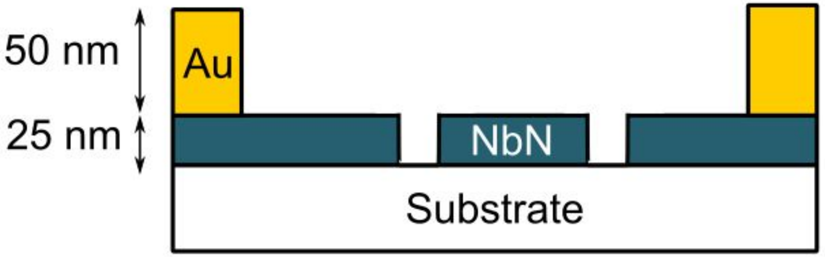


Fabrication process for making multilayer hTron devices

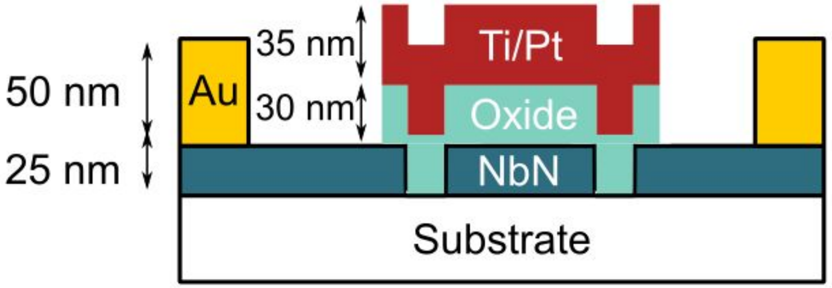
1 Define Au marks (lift-off).



2 Define the nanowire on NbN film (RIE).



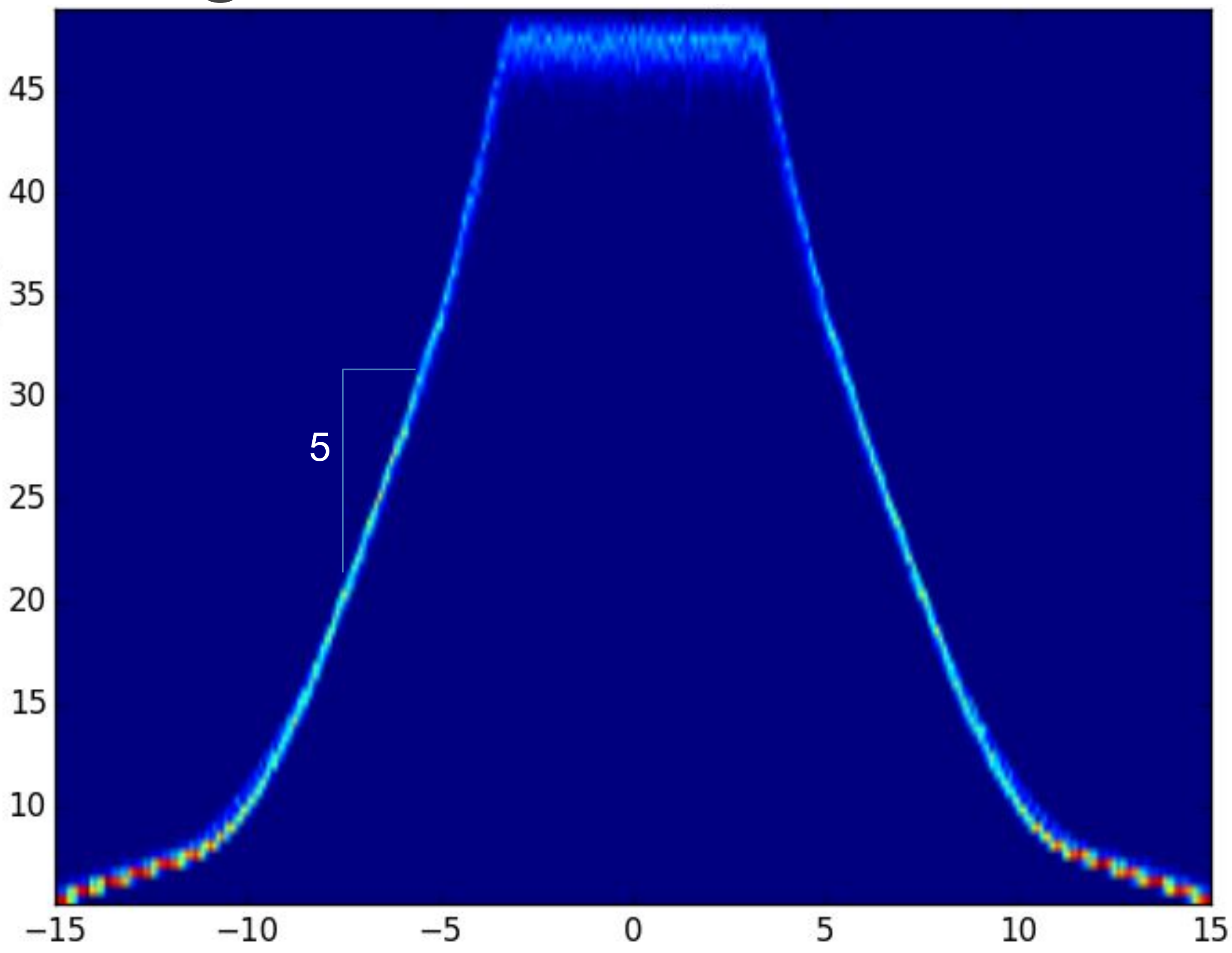
3 Define the heater on top of the nanowire (lift-off).



"Multilayered Heater Nanocryotron: A Superconducting-Nanowire-Based Thermal Switch" Phys. Rev. Applied 14, 054011 – Published 6 November 2020

Reza Baghdadi

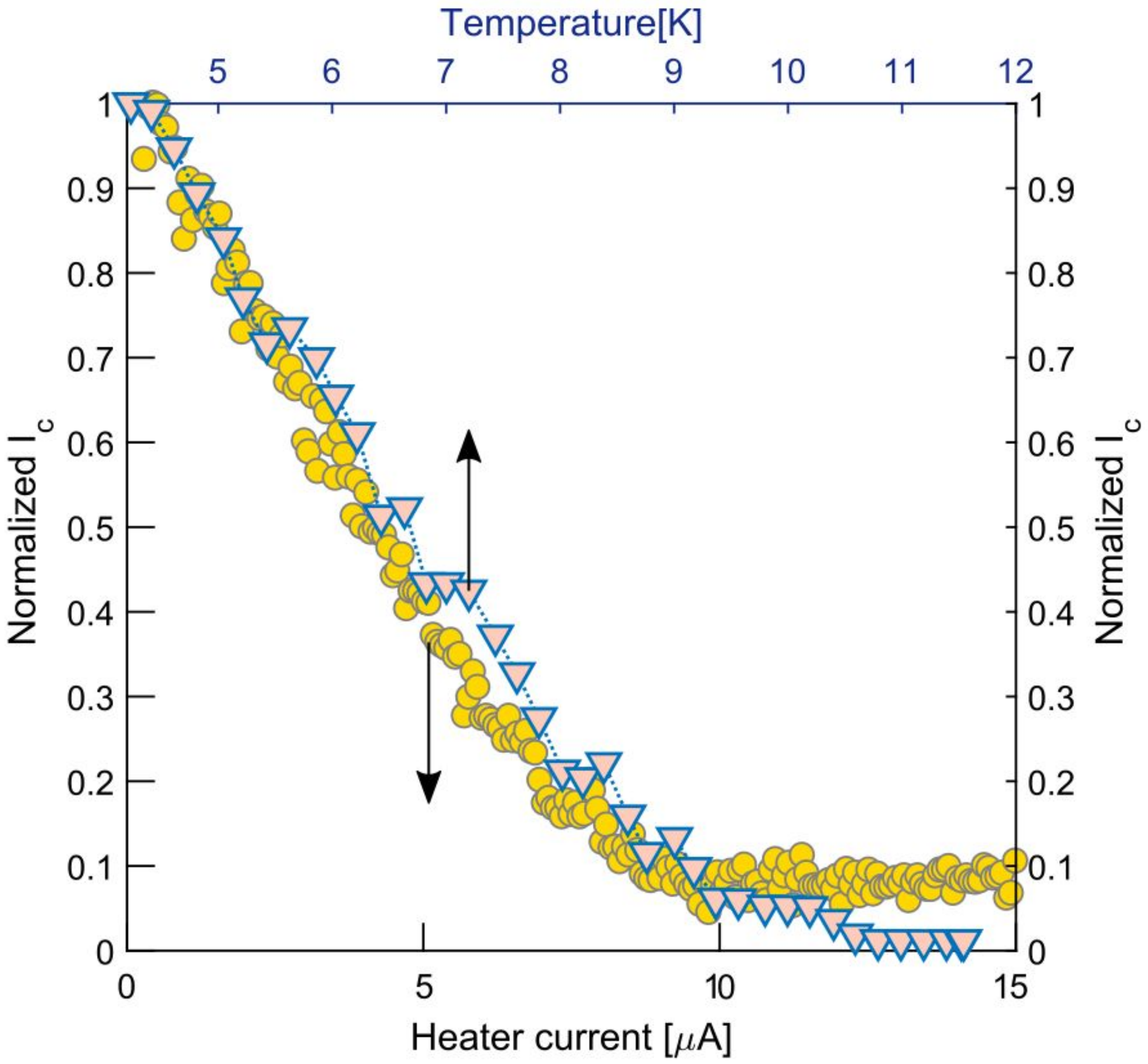
hTron Switching Characteristics



Channel Switching Current (µA)

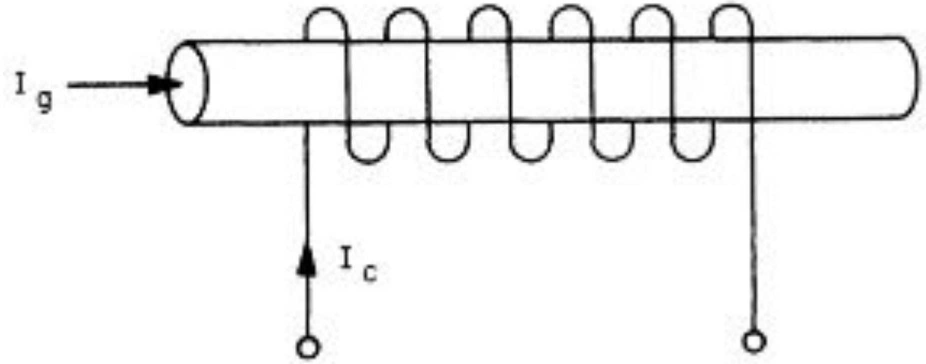
Current in Heater (Gate) (µA)

Operation of an hTron: Translate Joule heating to temperature



The cryotron: magnetic suppression

- **1956, Dudley Buck at MIT**
- **Gate induces magnetic field**
  - **Suppresses channel Ic**



Buck, D. (1956). The Cryotron - A Superconductive Computer Component. Proceedings of the IRE, 44(4), 482–493. doi:10.1109/JRPROC.1956.274

“A cryotron multi-level logic and memory circuit”

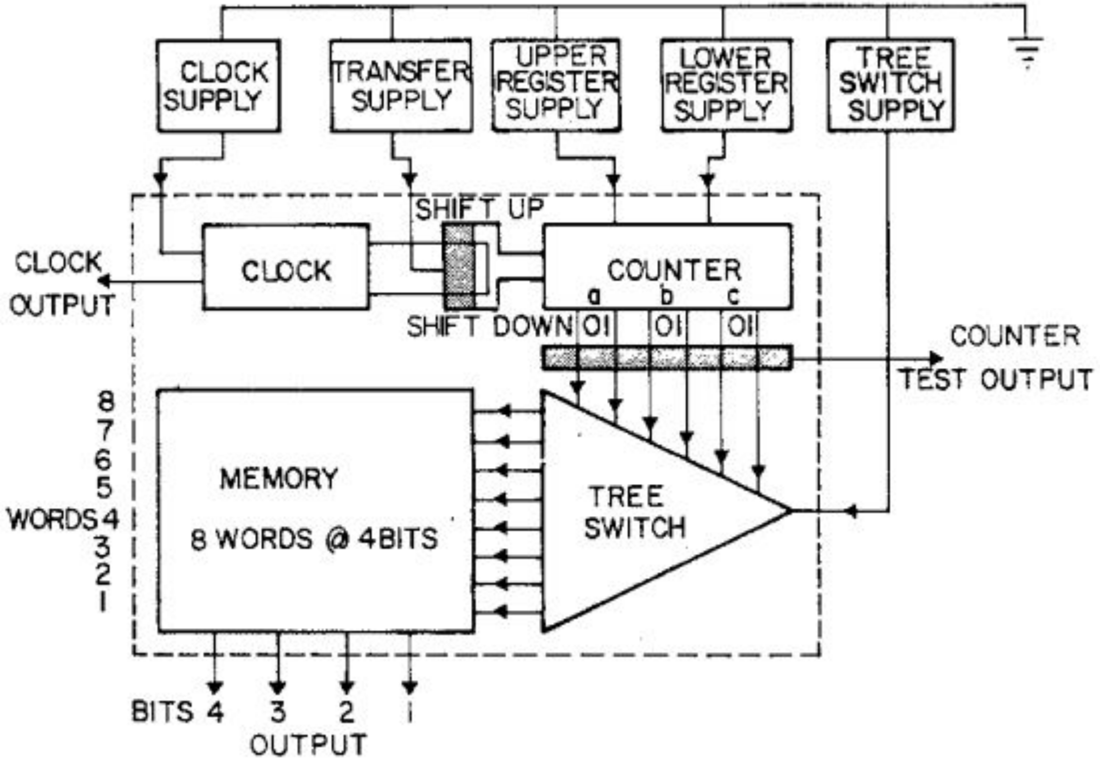


FIGURE 1—**Block diagram of cryotron logic and memory circuit.**

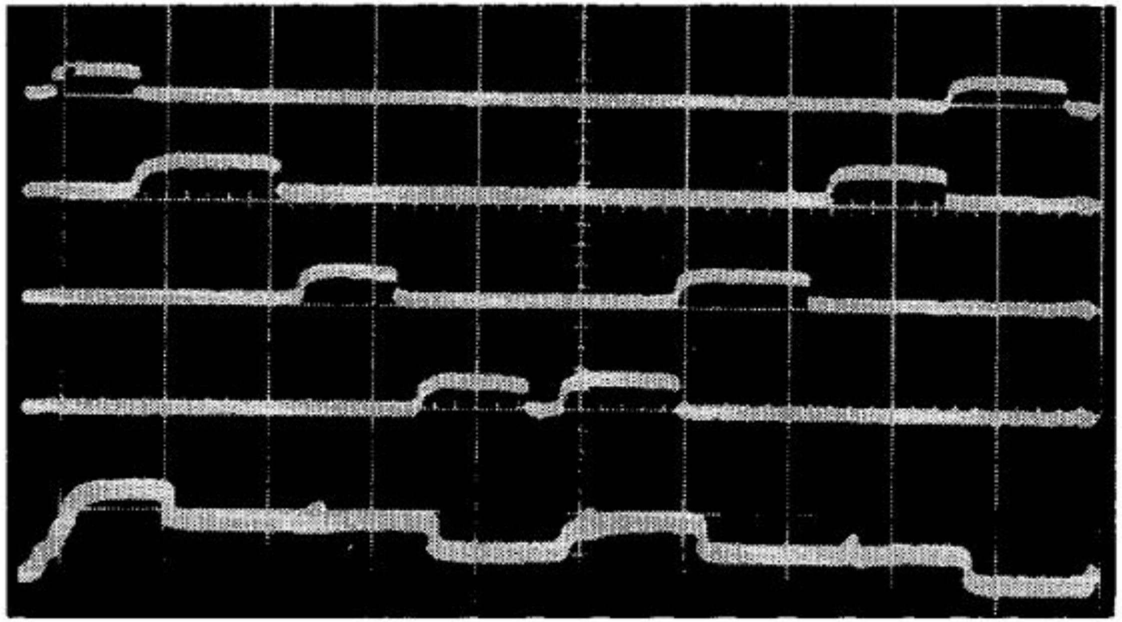
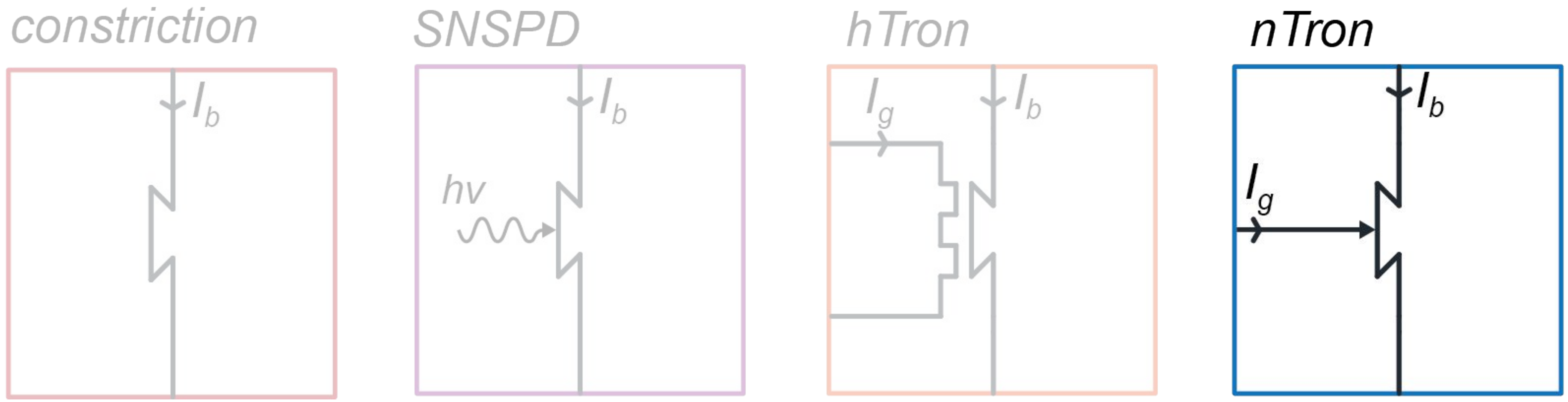


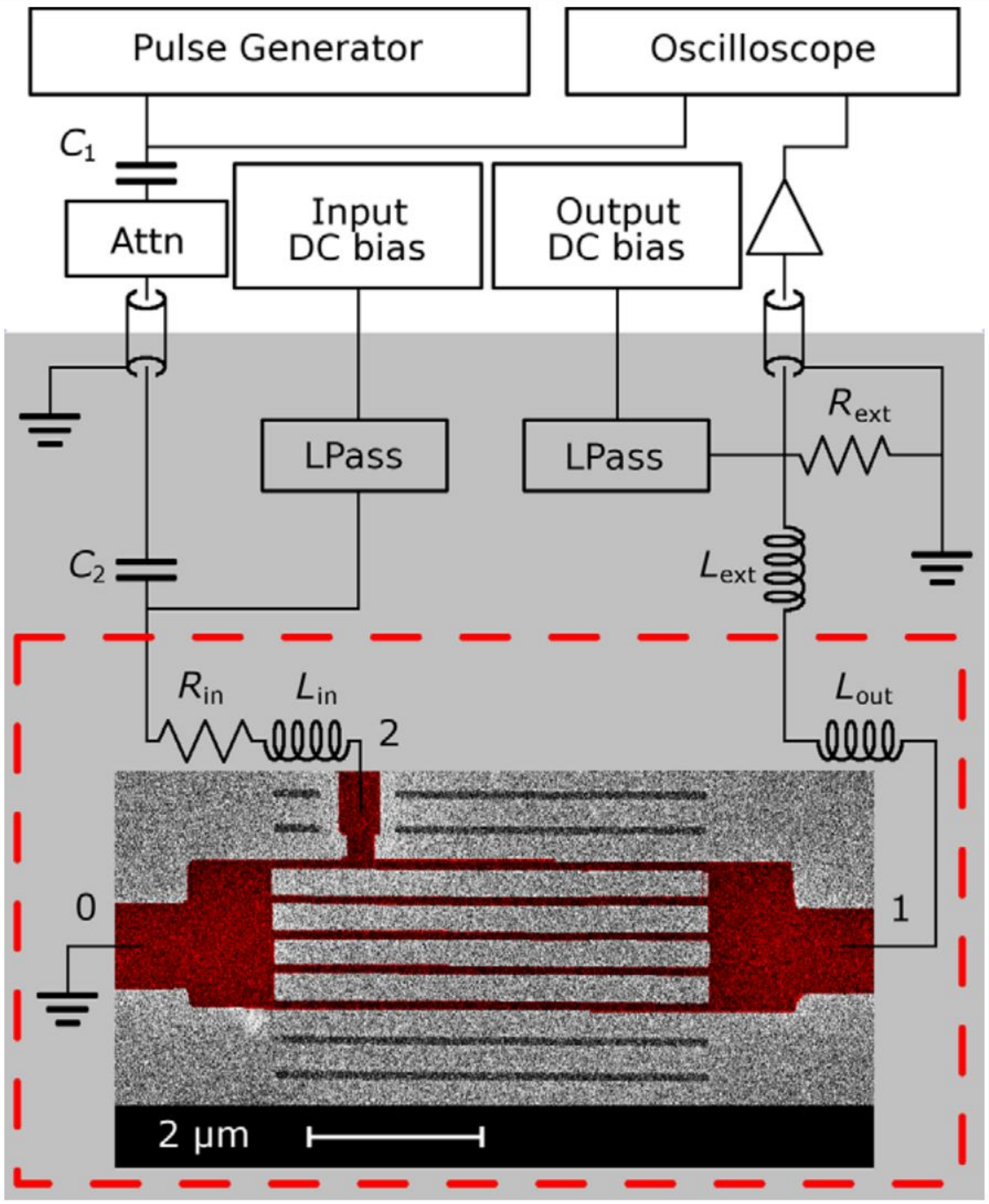
FIGURE 3—**Output waveforms at 200 kc; 5 μsec word time. Top to bottom: bit 1, bit 2, bit 3, bit 4, and counter test output. Vertical scale: 0.5 mv/em.**

M. Cohen, A. Slade and R. Varteresian, "A cryotron multi-level logic and memory circuit," *1964 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, Philadelphia, PA, USA, 1964, pp. 102-103, doi: 10.1109/ISSCC.1964.1157547.

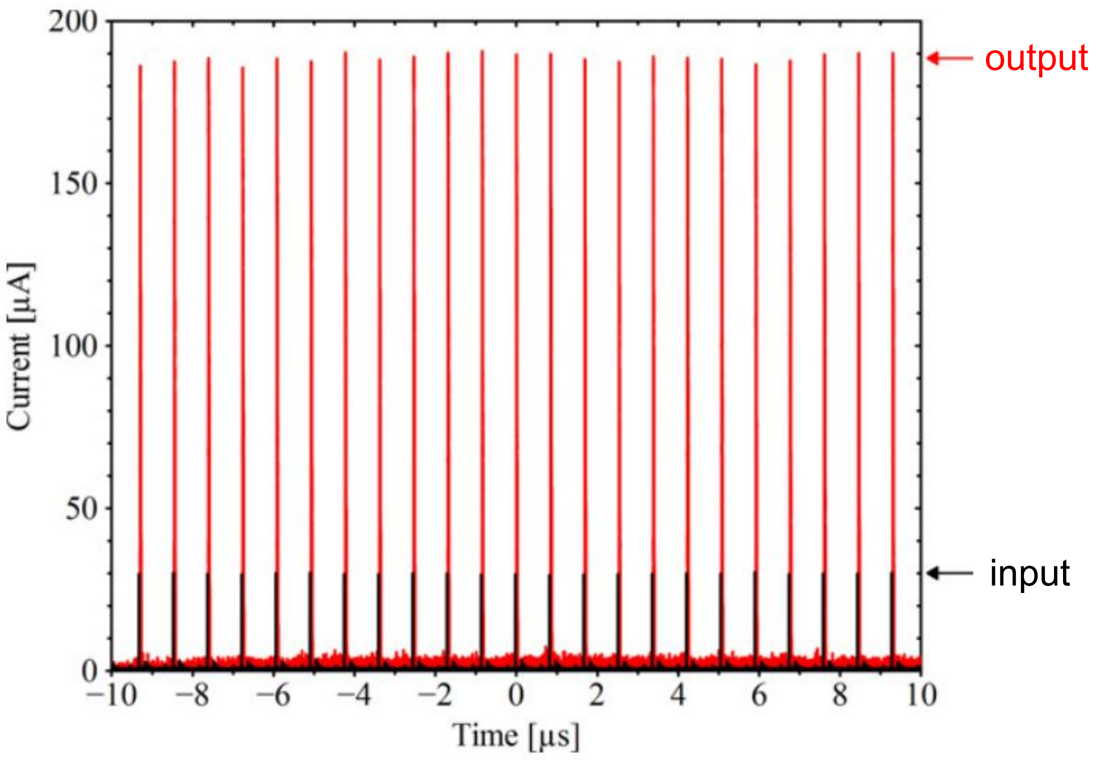
Bestiary of Nanowire Devices



Pulse Discriminator for SNSPD Readout



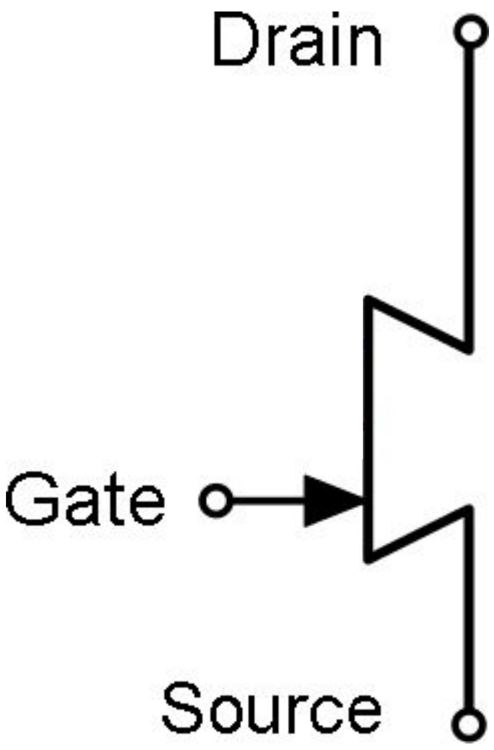
M Ejrnaes *et al* 2011 *Supercond. Sci. Technol.* 24 035018

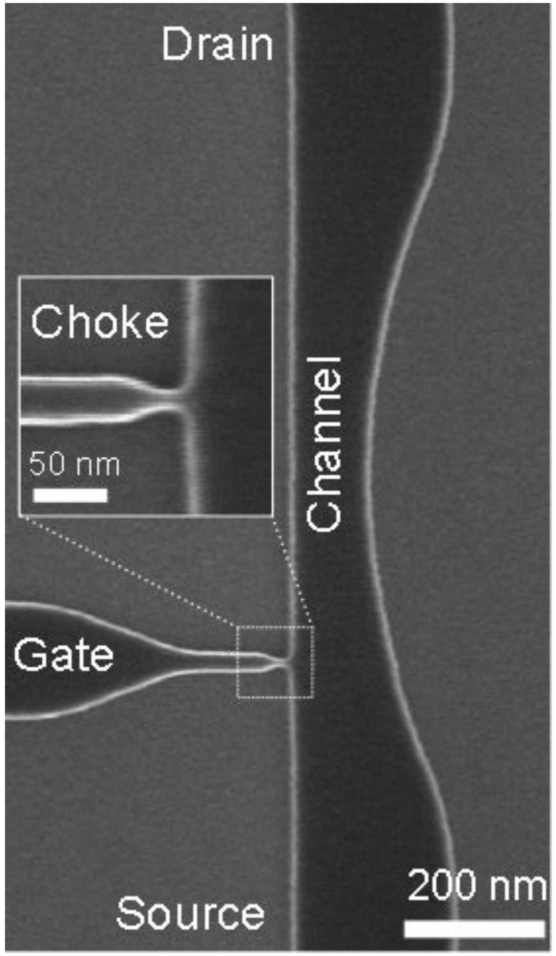


O. Qaranta

M. Ejrnaes

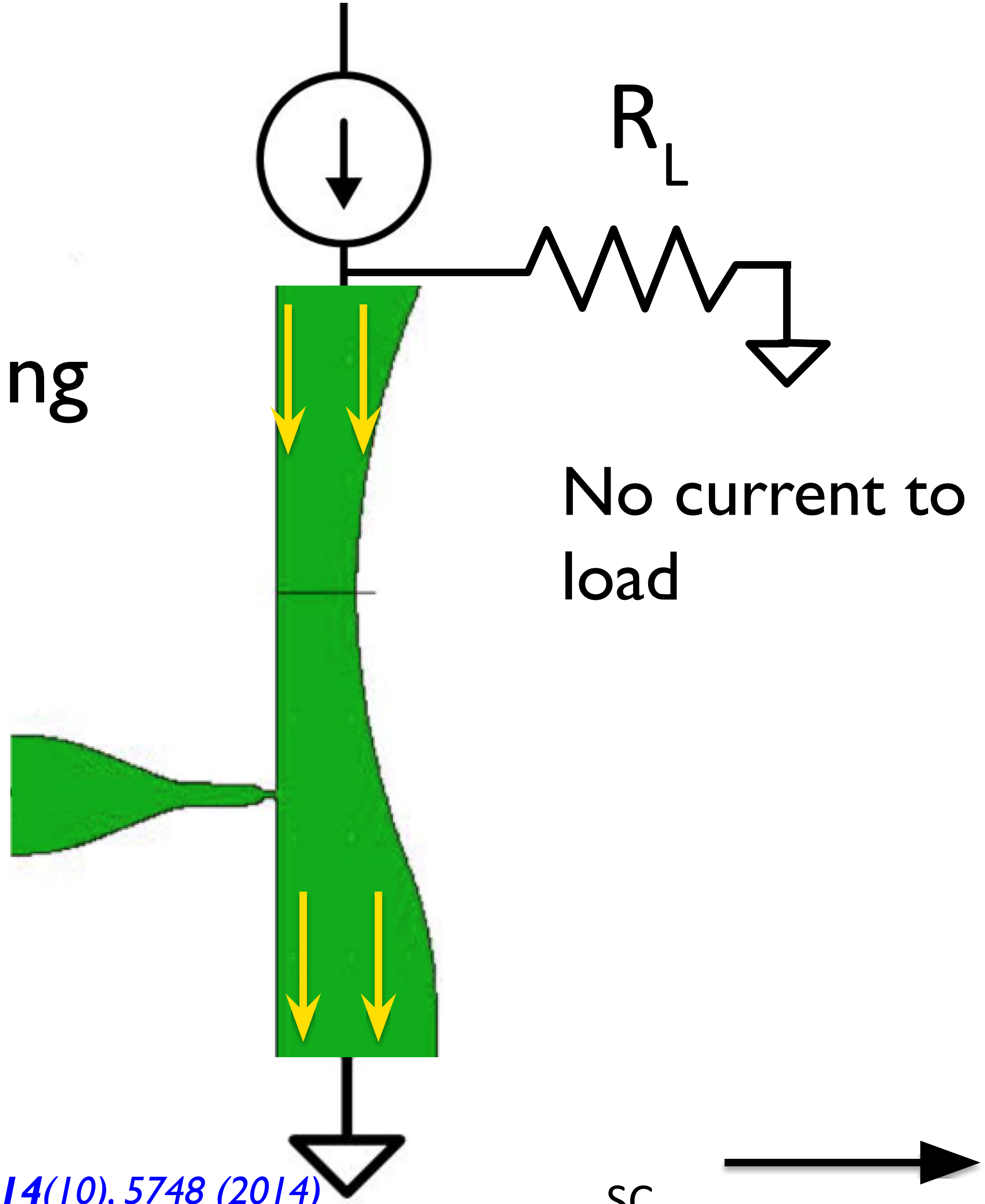
nTron geometry



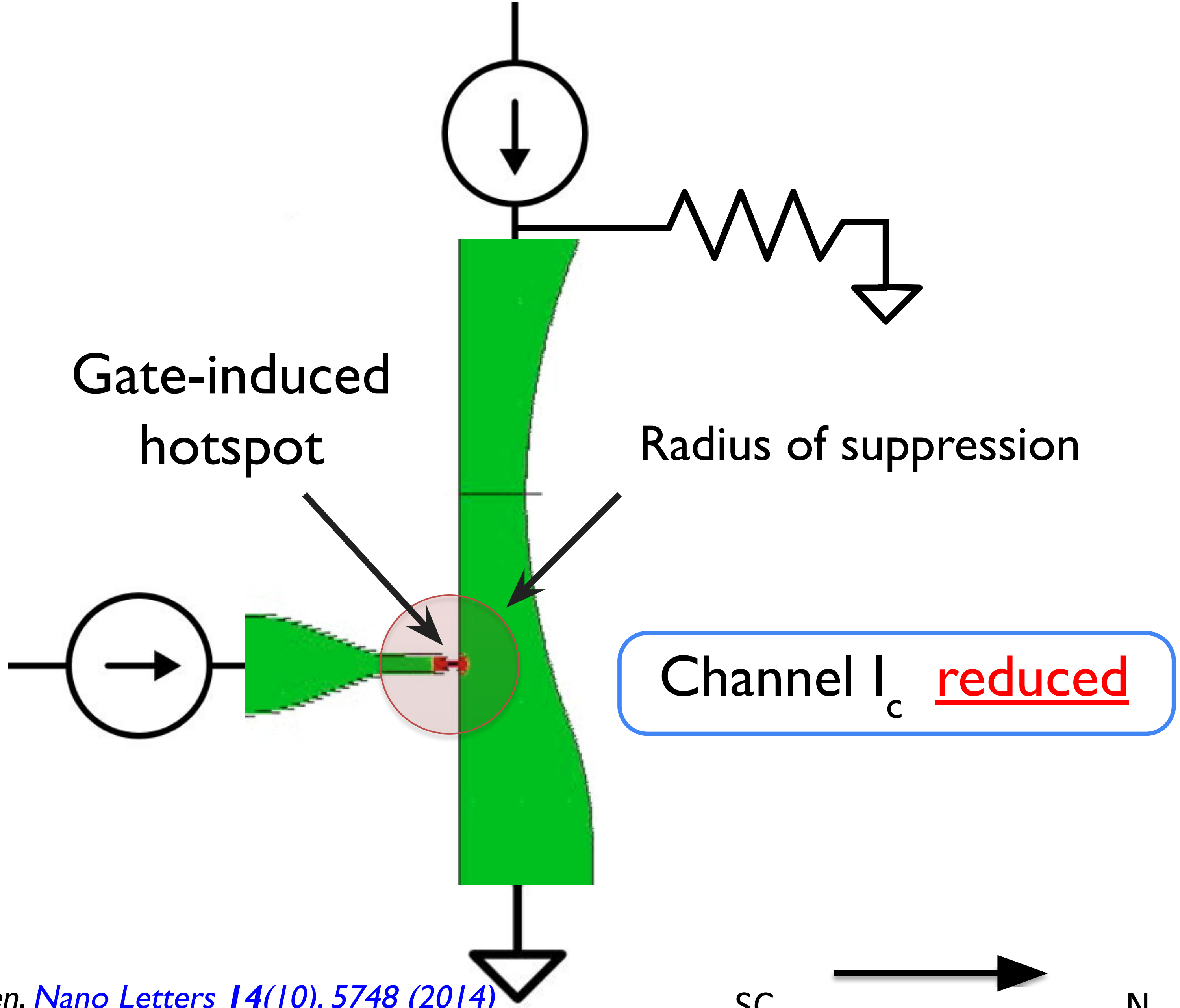


*A. N. McCaughan and K. K. Berggren, [Nano Letters **14**(10), 5748 (2014)]*

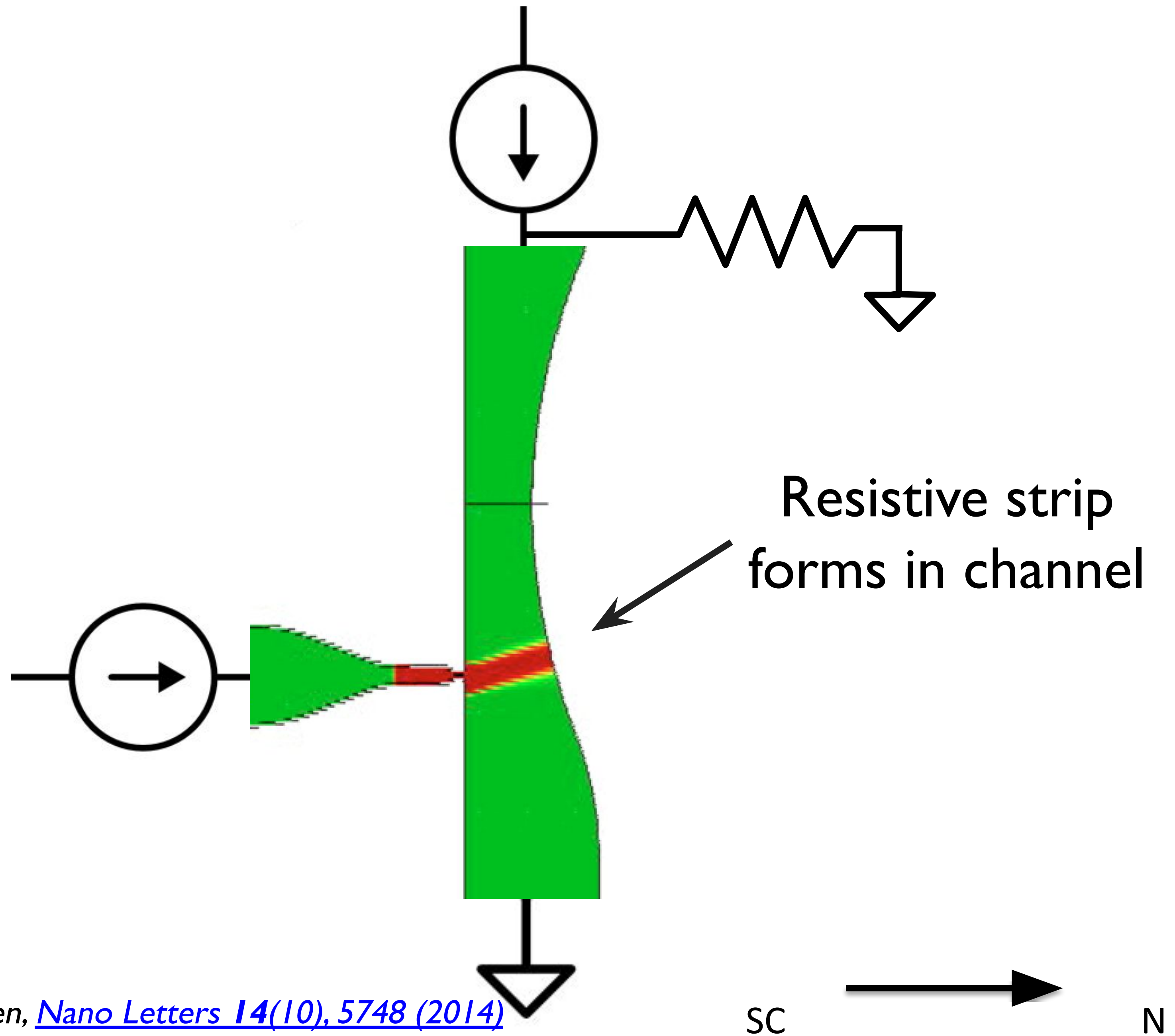
Device fully superconducting



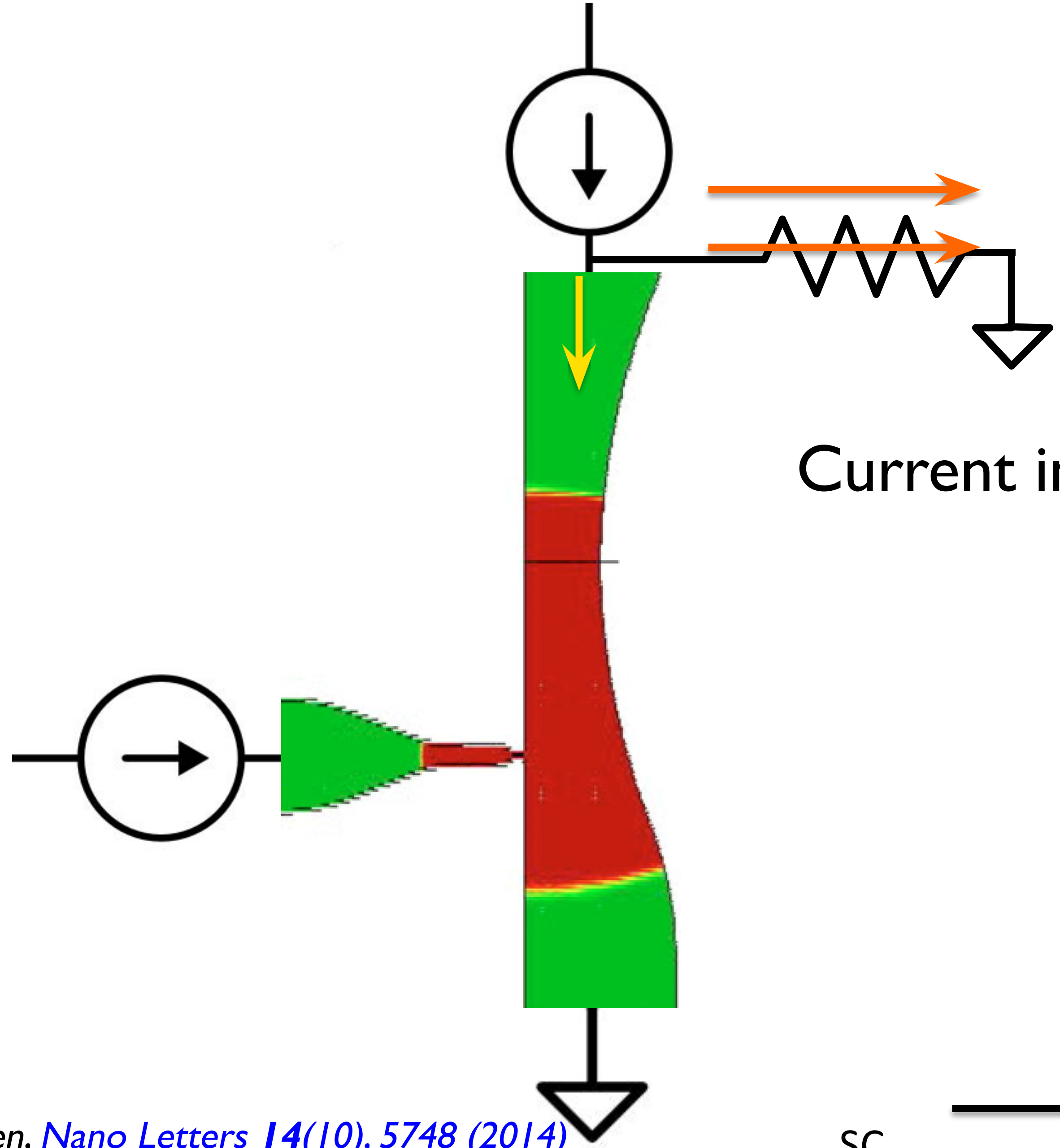
*A. N. McCaughan and K. K. Berggren, Nano Letters **14**(10), 5748 (2014)*



A. N. McCaughan and K. K. Berggren, [*Nano Letters* ***14****(10), 5748 (2014)*]



*A. N. McCaughan and K. K. Berggren, [Nano Letters **14**(10), 5748 (2014)]*



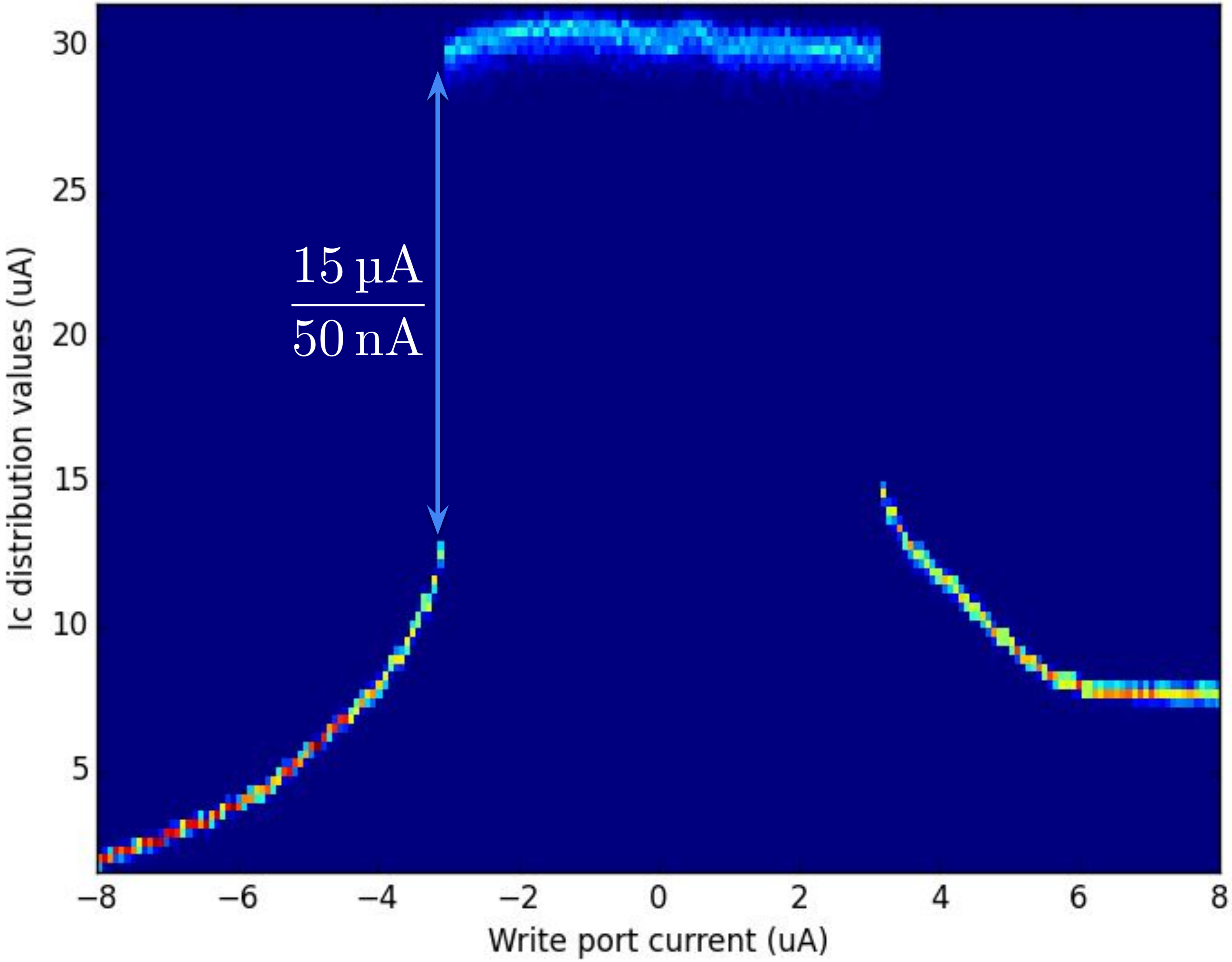
Current into load!

SC → N

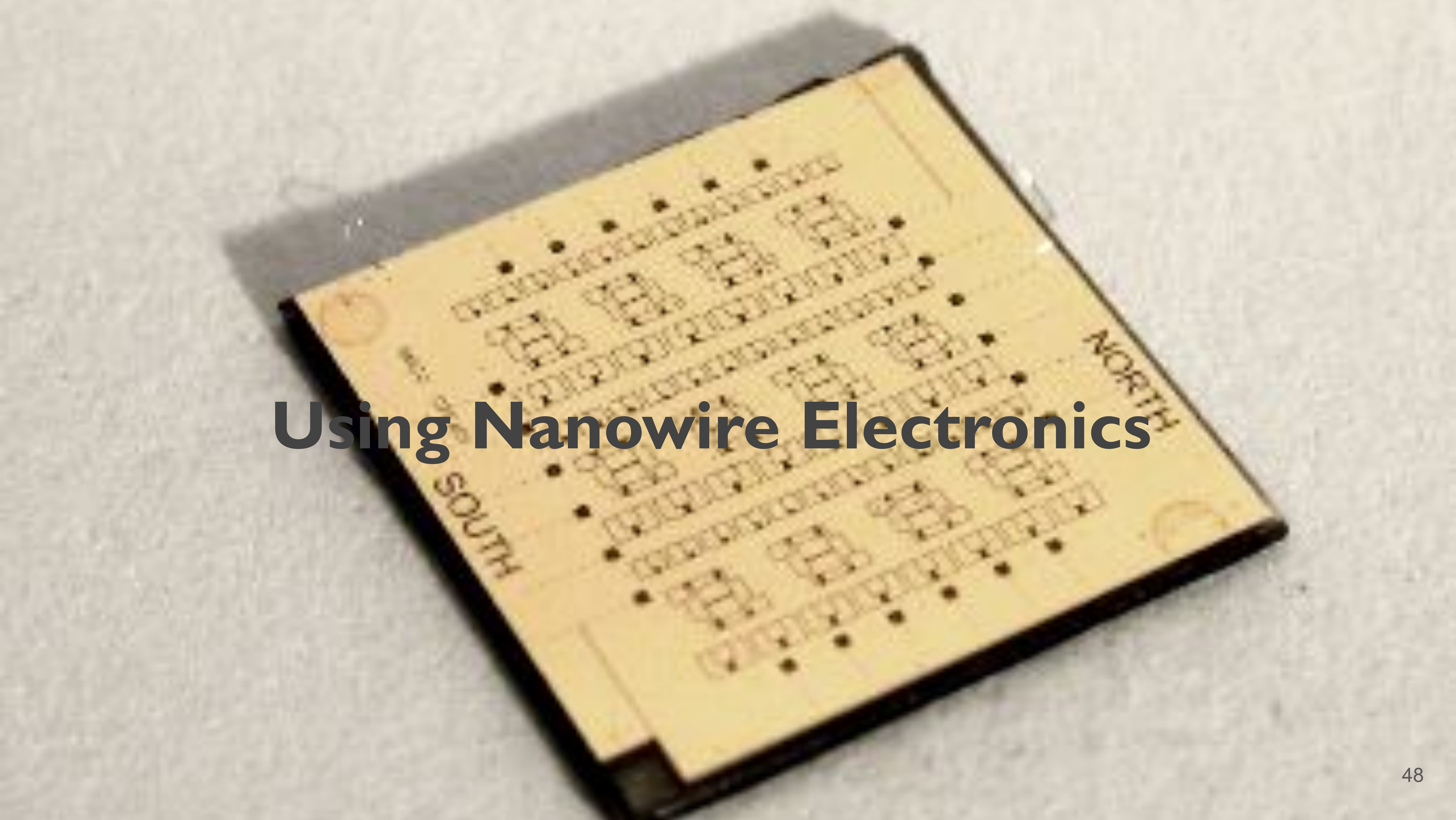
A. N. McCaughan and K. K. Berggren, [*Nano Letters* ***14****(10), 5748 (2014)*]

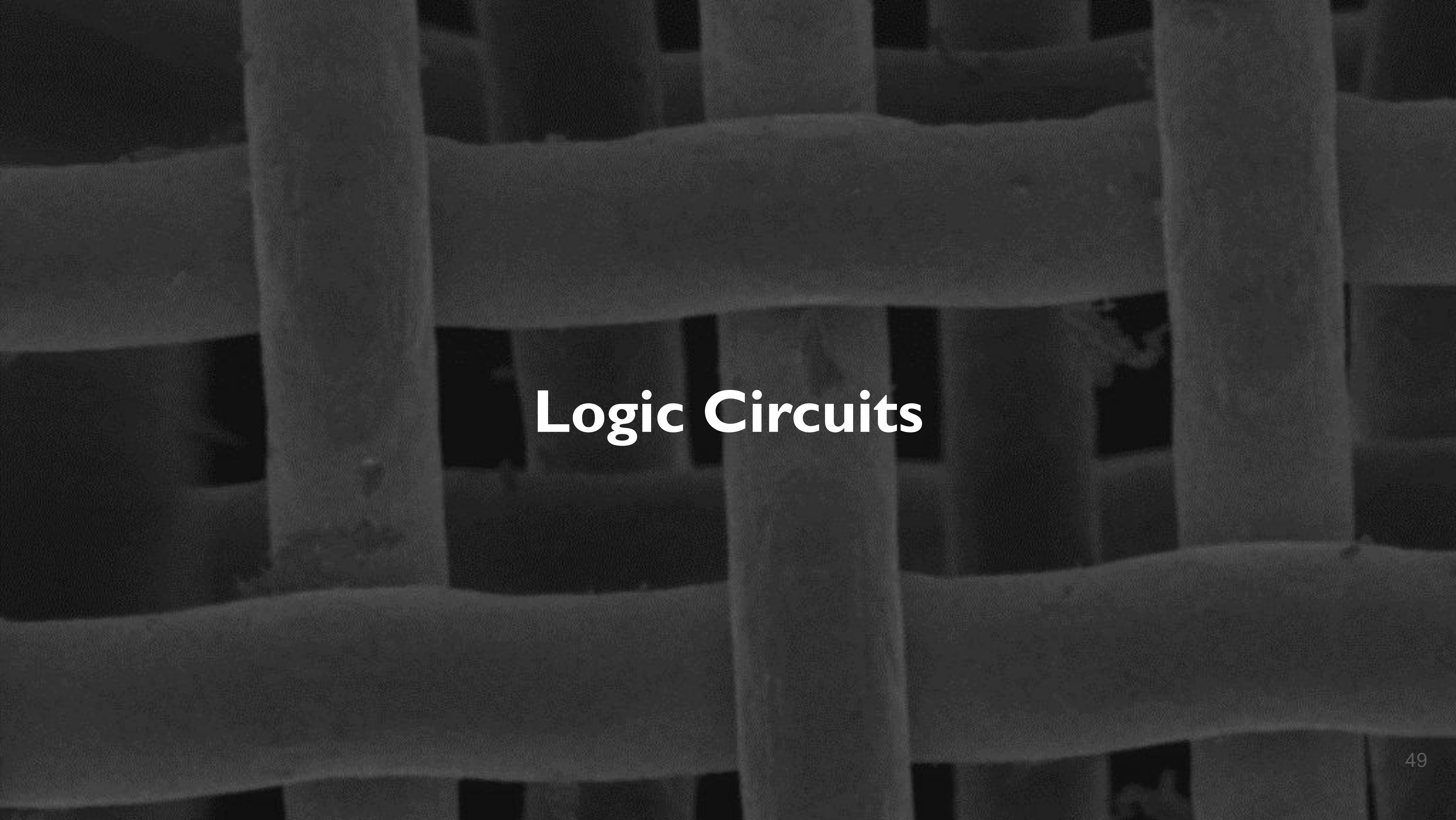
nanowire Cryotron Characteristics

Channel switching current I_c vs gate input current (write port current) for nTron reference device



Using Nanowire Electronics

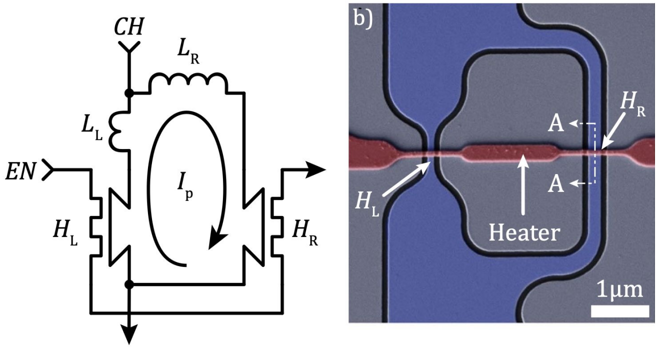




Logic Circuits

Superconducting nanowire electronics

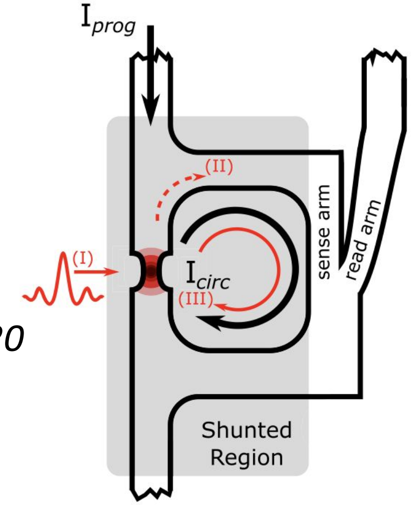
Non-volatile memory



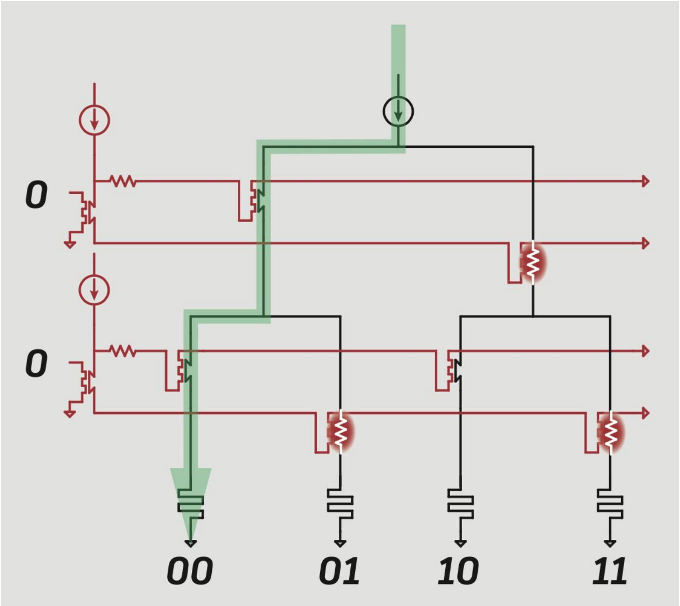
B. A. Butters *et al. SUST 34 2021*

Integrator

M. Onen *et al.*
Nano Lett. 2020



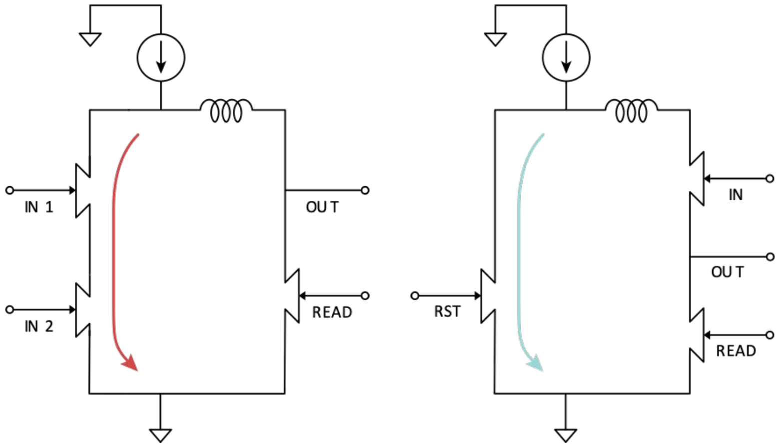
Multiplexer



O. Medeiros *et al. ASC 22*
SNSPD: Physics, Measurement, Readout, Applications

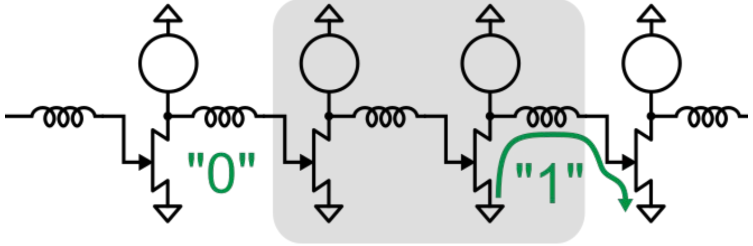
OR gate

NOT gate



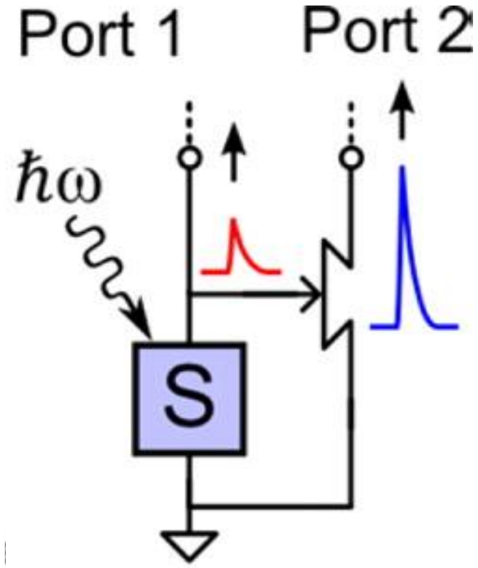
A. Buzzi *et al. WOLTE 22*

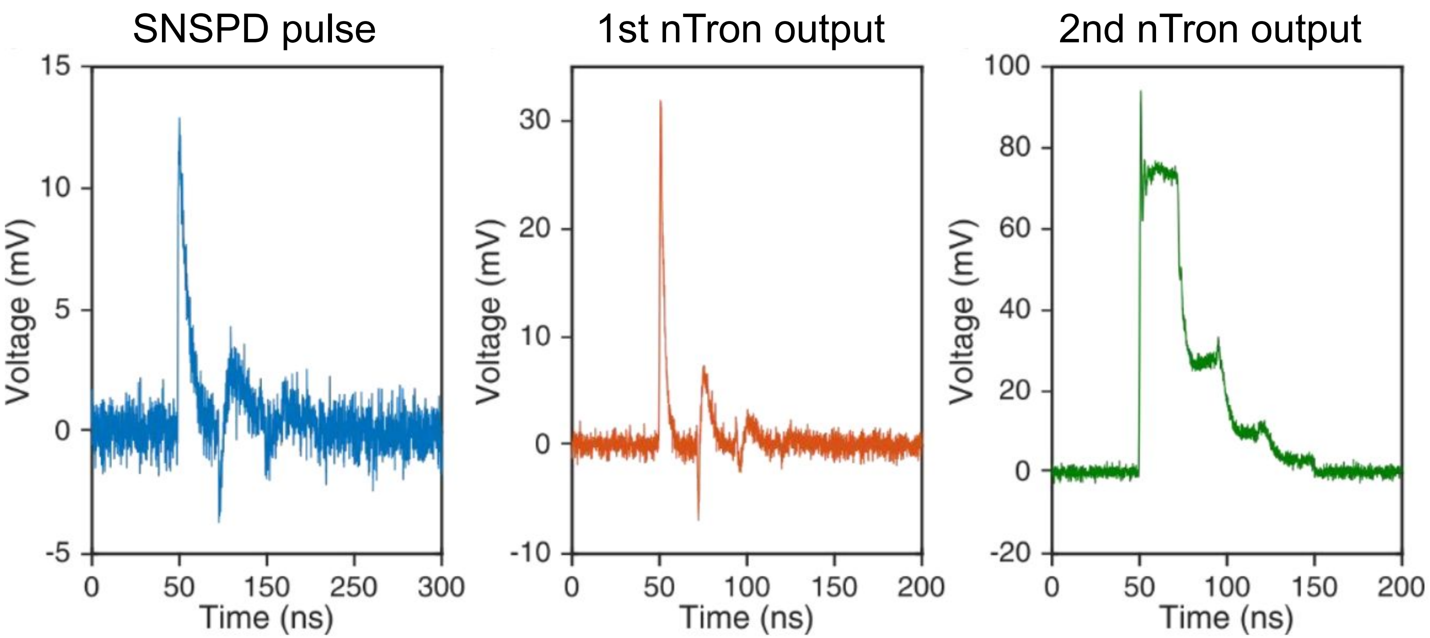
Shift-register



R. A. Foster *et al. WOLTE 22*

nTron Amplifier Example for SNSPDs

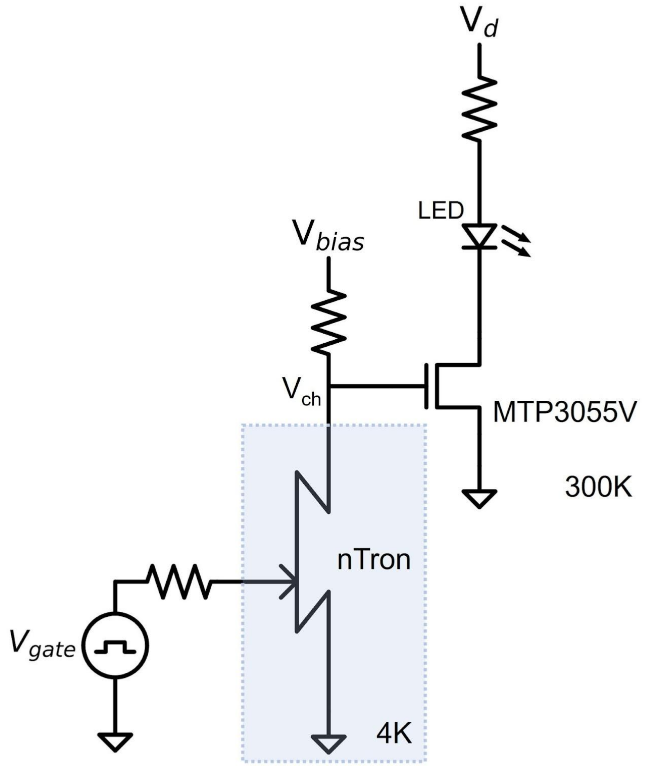


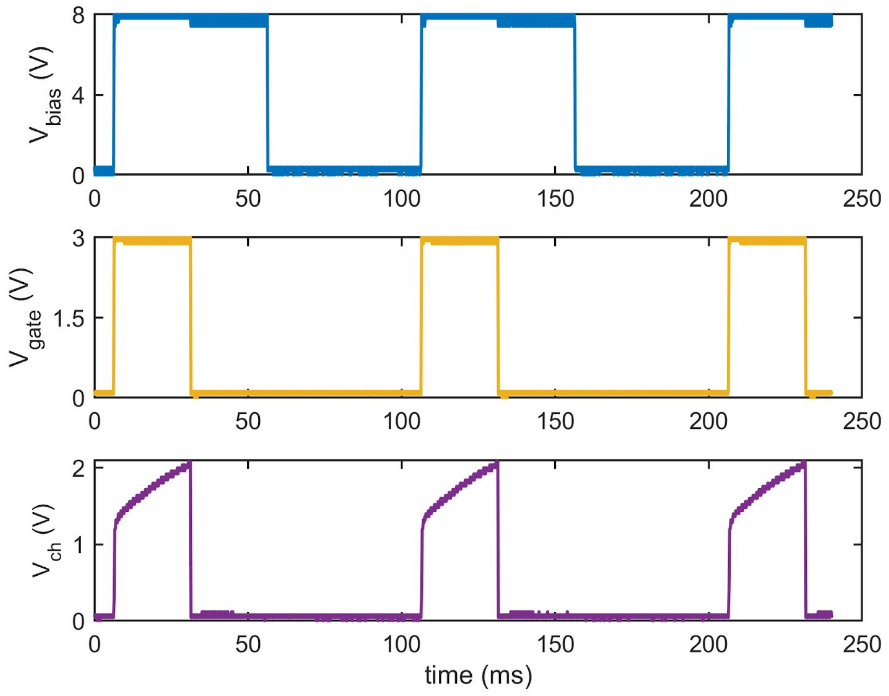


Zheng, K., Zhao, Q. Y., et al. "A Superconducting Binary Encoder with Multigate Nanowire Cryotrons." *Nano letters*, *20*(5), (2020) 3553-3559. (Supporting Information)

Tron-CMOS interfacing demo

Driving room-temp MOSFET and LED with nTron



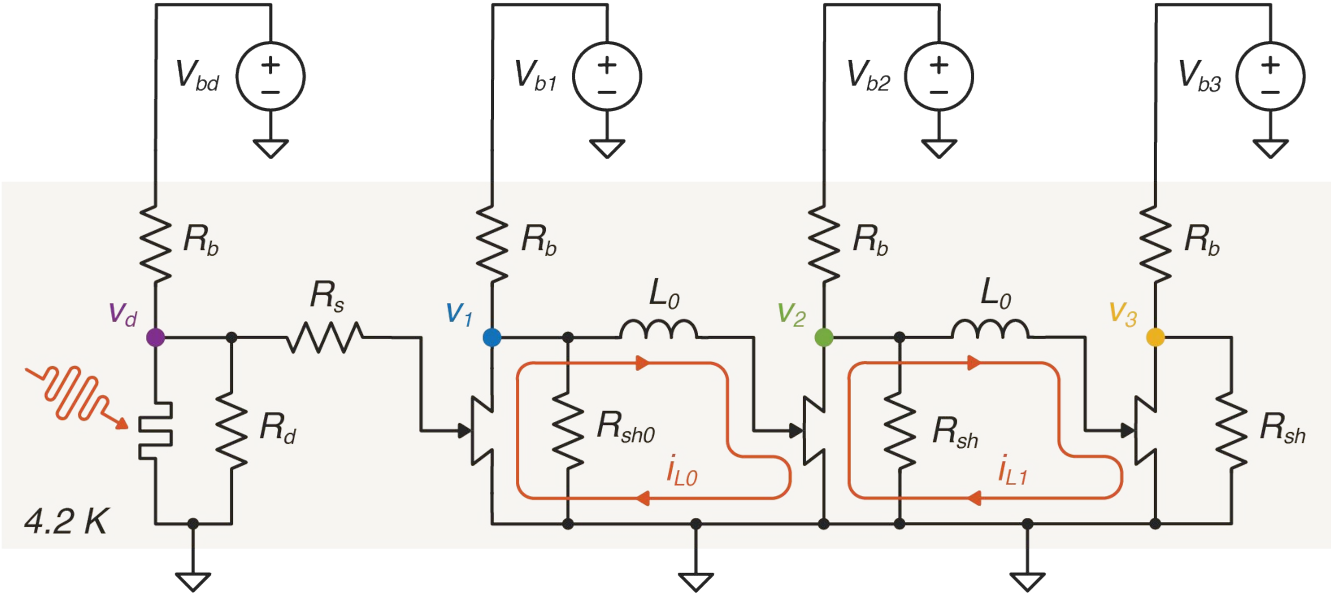


https://www.youtube.com/shorts/fJycxwcOsO0

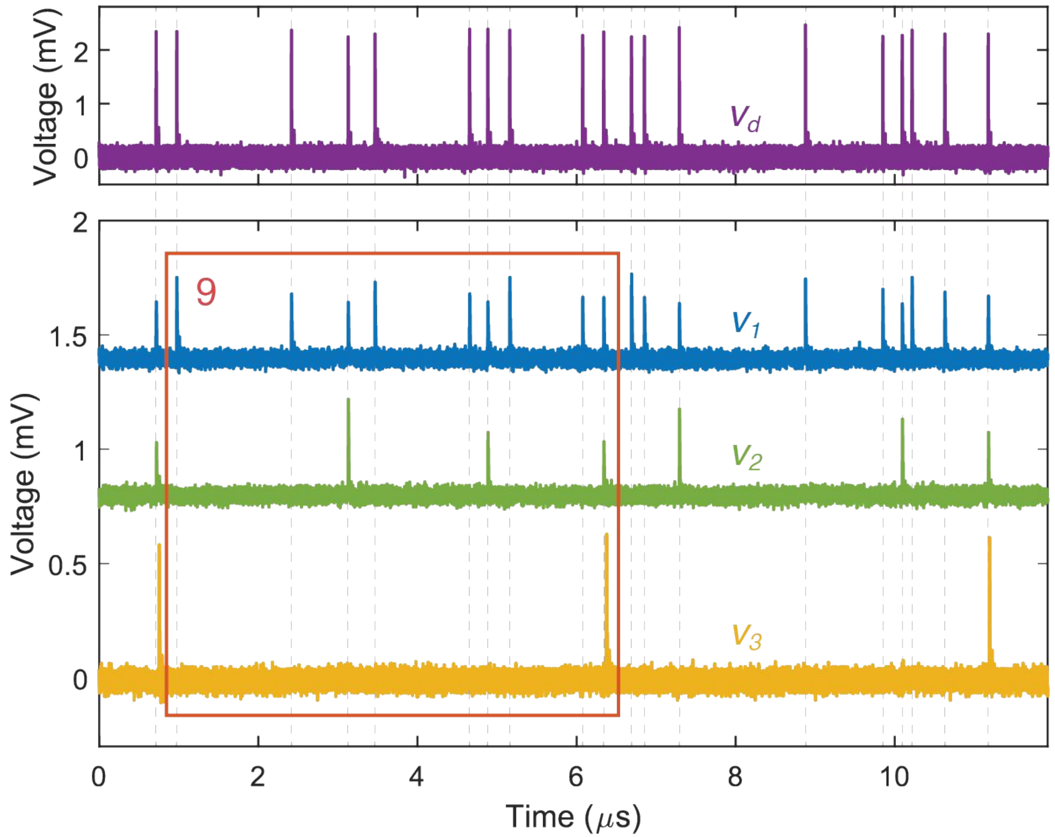
MOSFET is driven by the nTron gate pulse
FET V_{th} = 2 V. LED turns on, when $V_{ch} > V_{th}$

SNSPD + 2-digit counter

Tested at 1550 nm and 405 nm



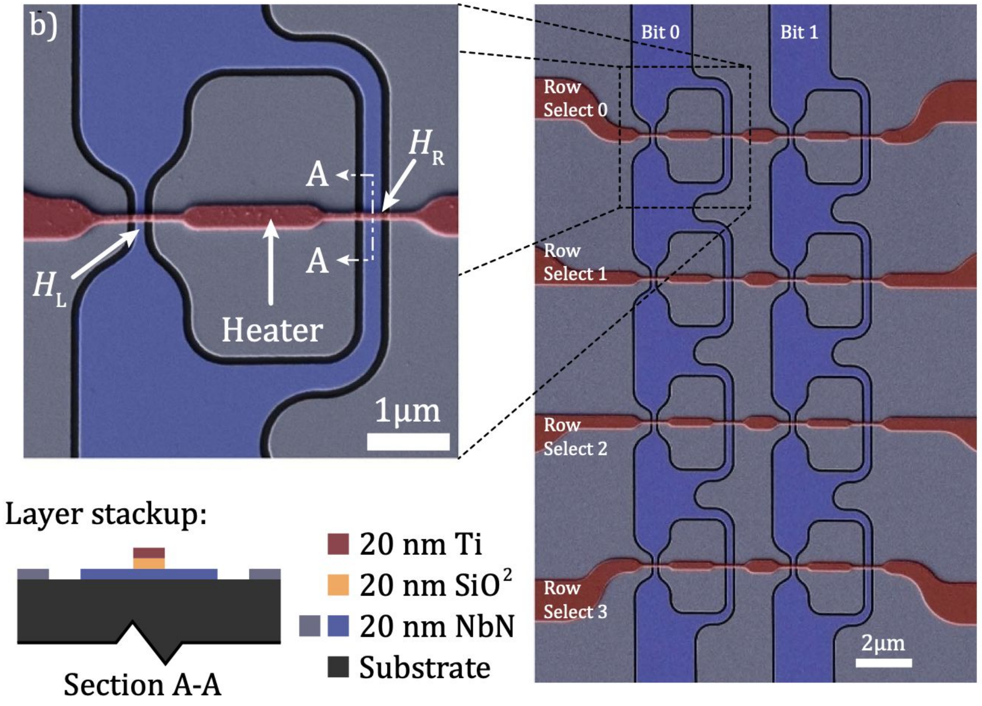
Base 3 at 405 nm



Nanowire Memory Element (nMem)

Superconducting Memories

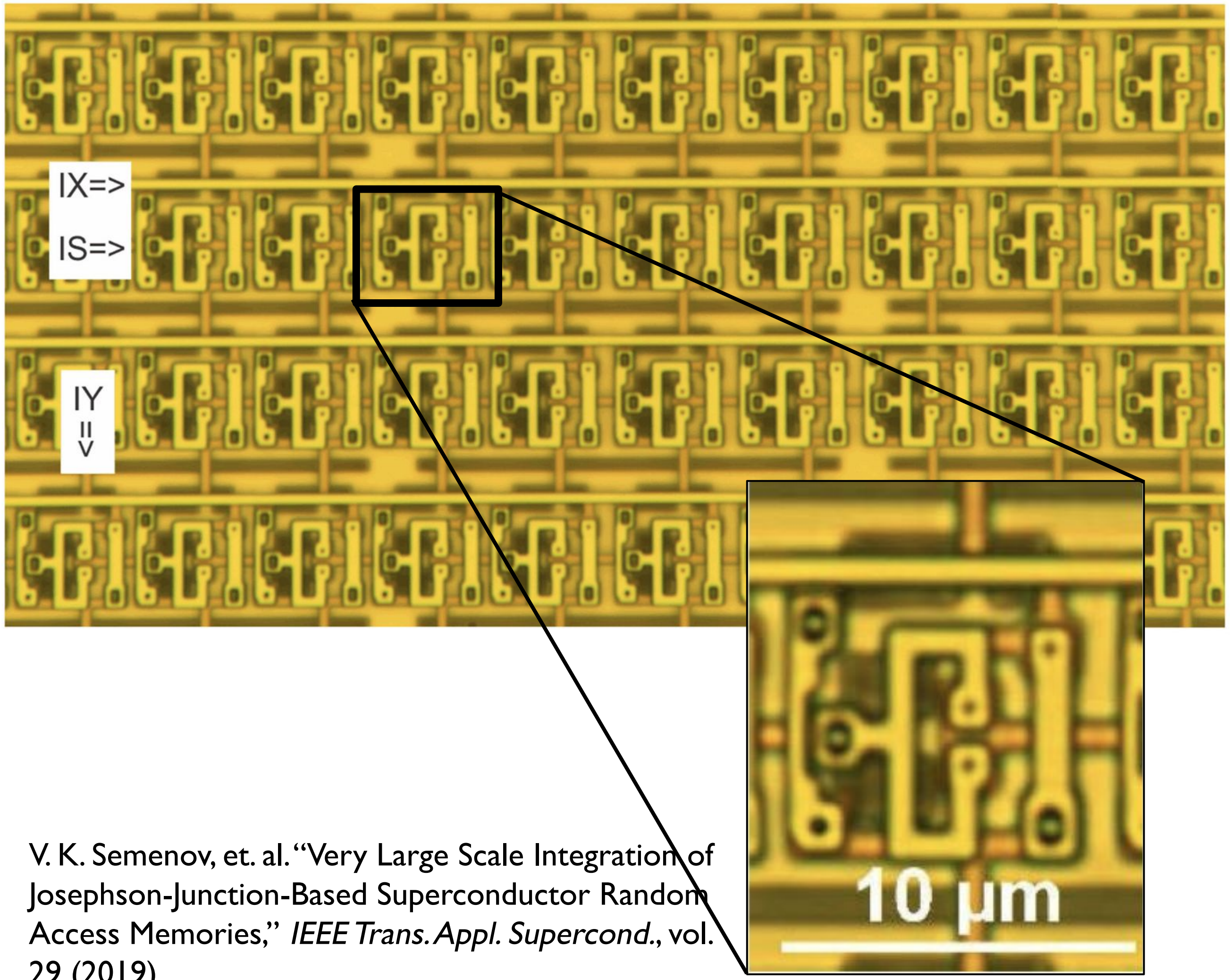
Superconducting nanowire memory



Work initiated under IARPA C3 Program

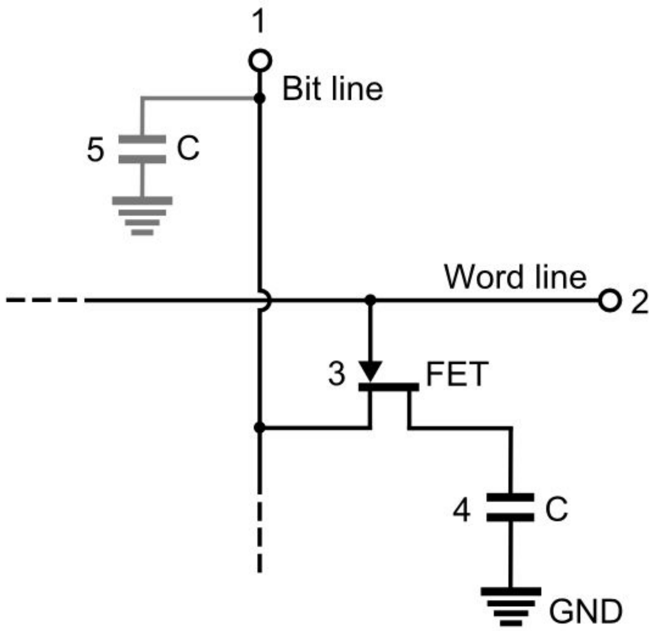
Butters, Brenden A., et al. "A scalable superconducting nanowire memory cell and preliminary array test." *Superconductor Science and Technology* 34.3 (2021)

Vortex-Transitional (VT) memory cells

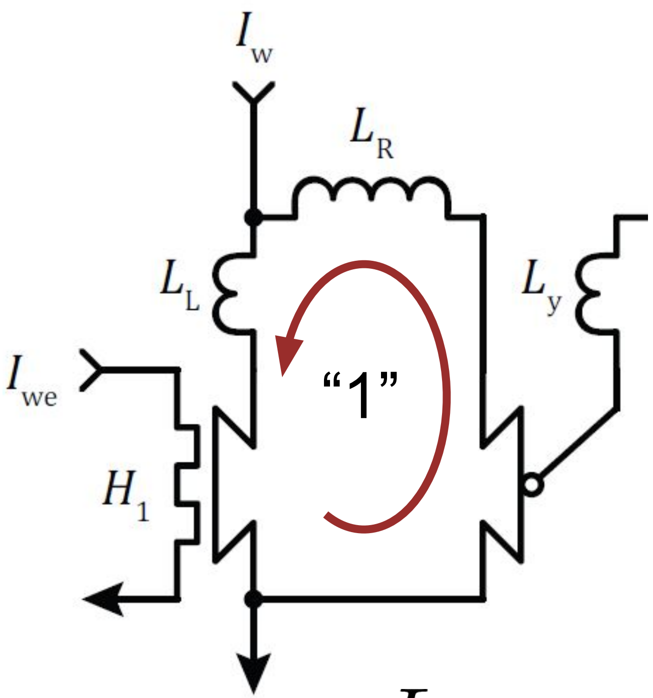


V. K. Semenov, et. al. "Very Large Scale Integration of Josephson-Junction-Based Superconductor Random Access Memories," *IEEE Trans. Appl. Supercond.*, vol. 29 (2019)

Persistent Current

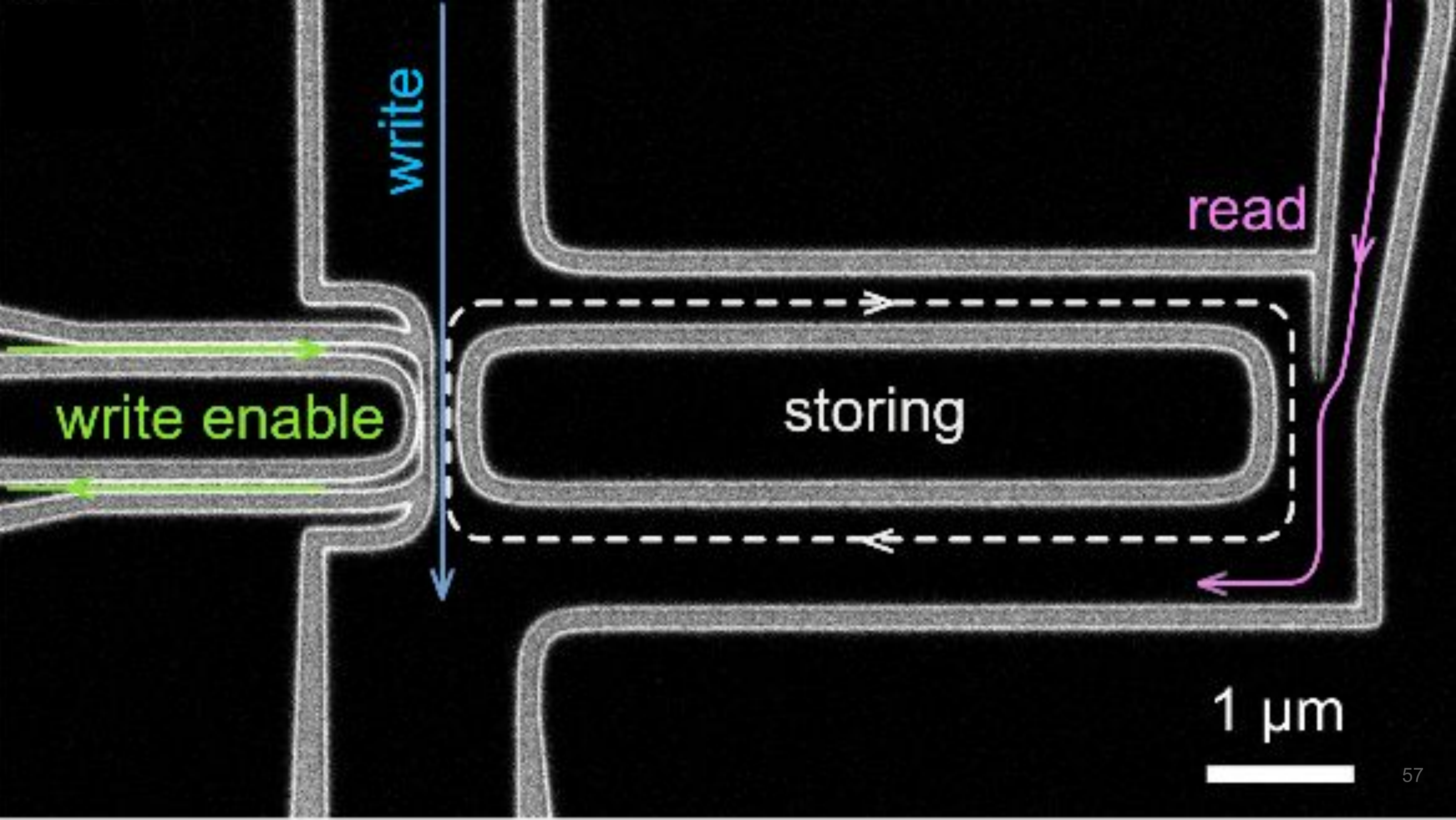


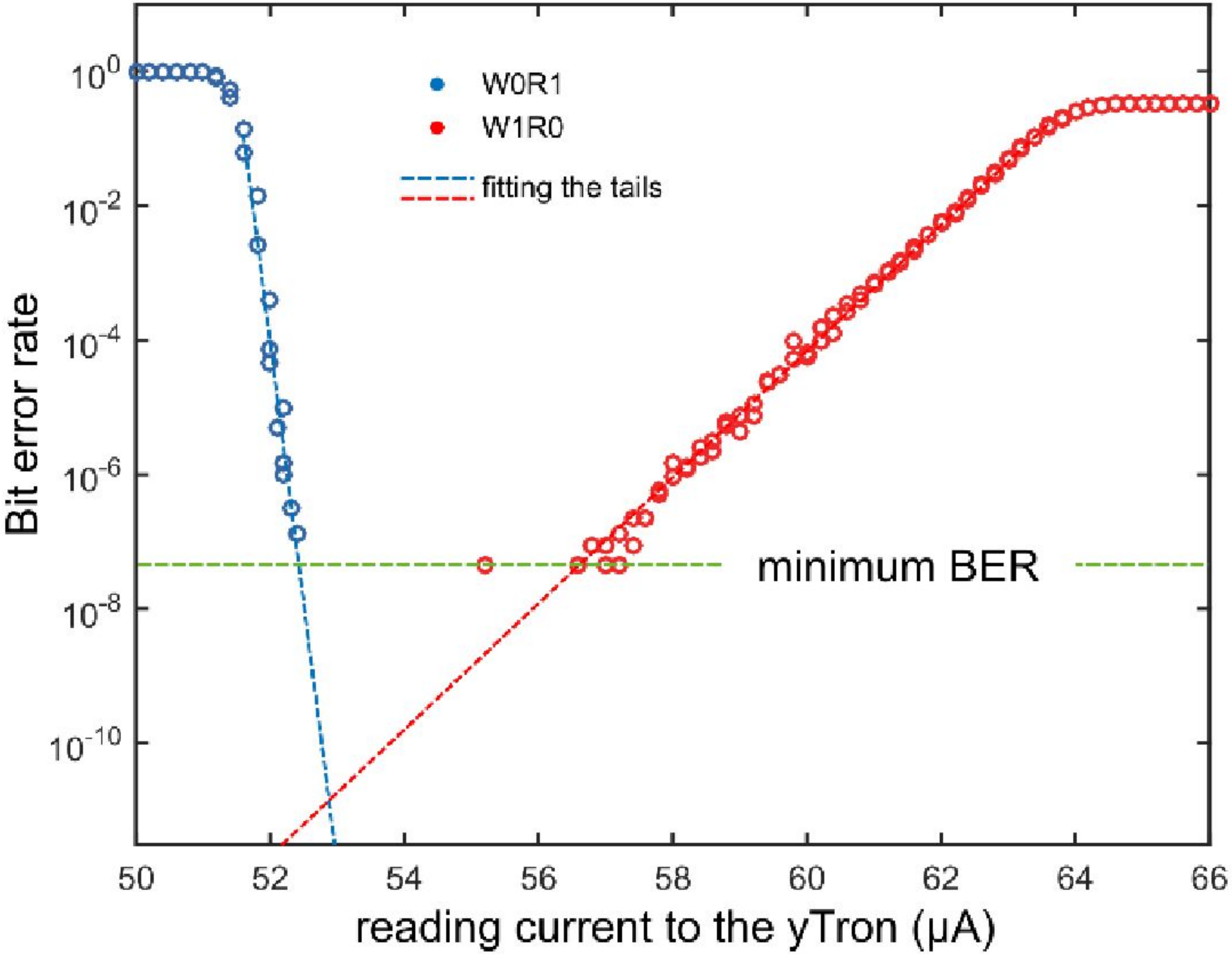
$$\tau = RC$$



$$\tau = \frac{L}{R}$$

Wikimedia Commons, DRAM Cell Structure (Model of Single Circuit Cell), Tosaka (2008)

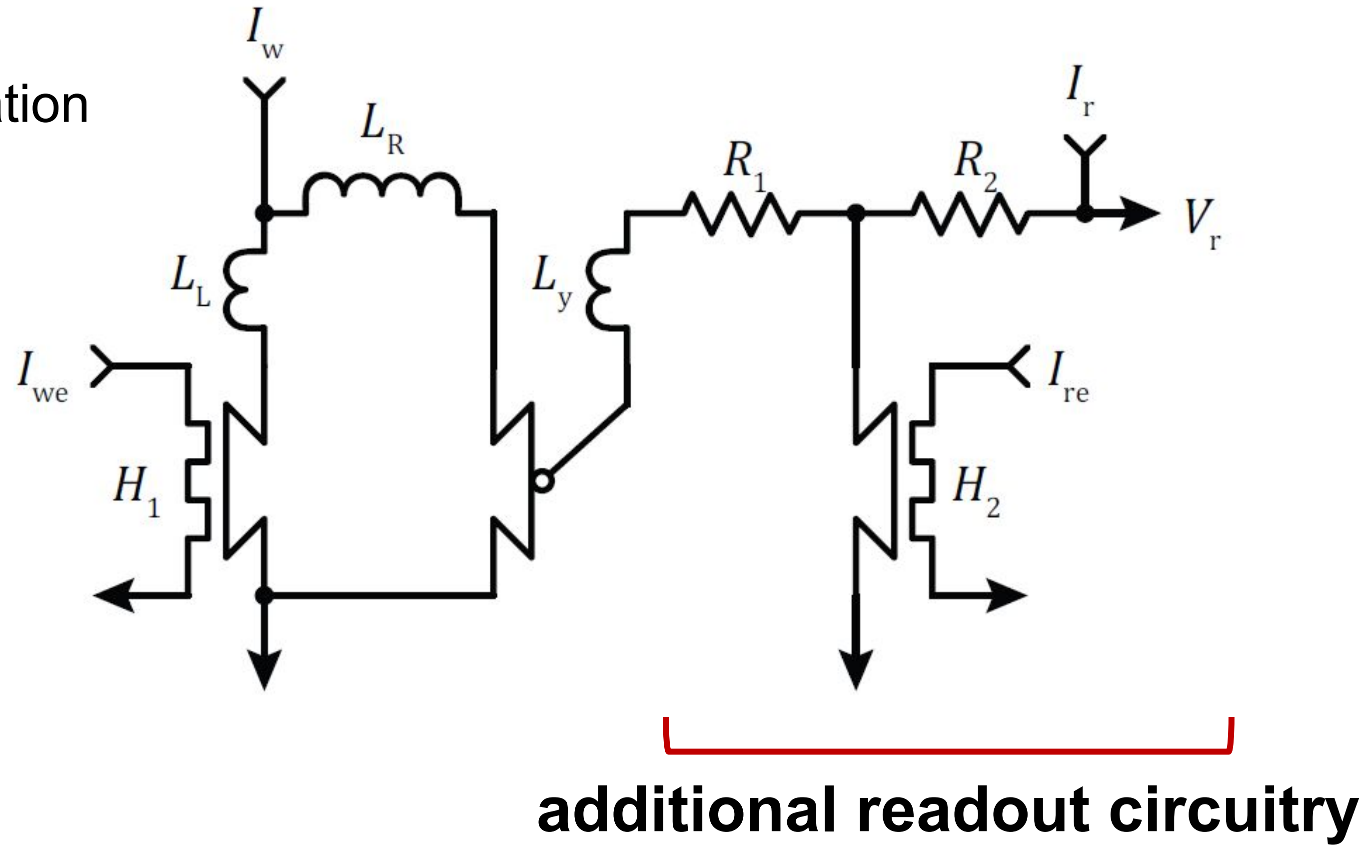

write
read
write enable
storing
1 μm



W0R1
W1R0
fitting the tails
minimum BER
Bit error rate
10^0
10^-2
10^-4
10^-6
10^-8
10^-10
50
52
54
56
58
60
62
64
66
reading current to the yTron (μA)

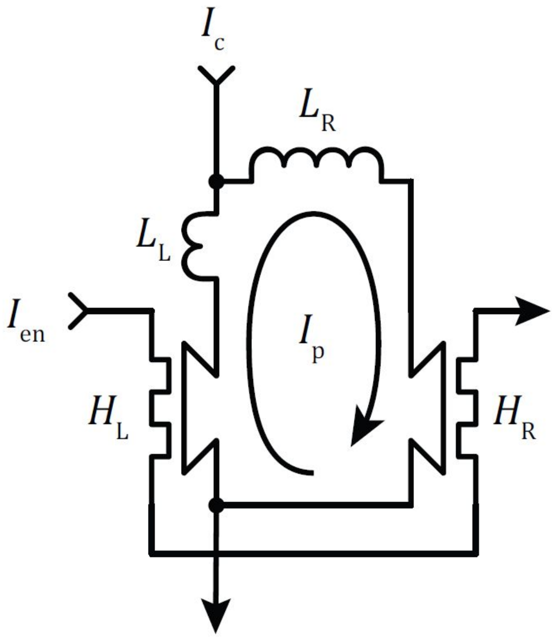
Problems with non-destructive read

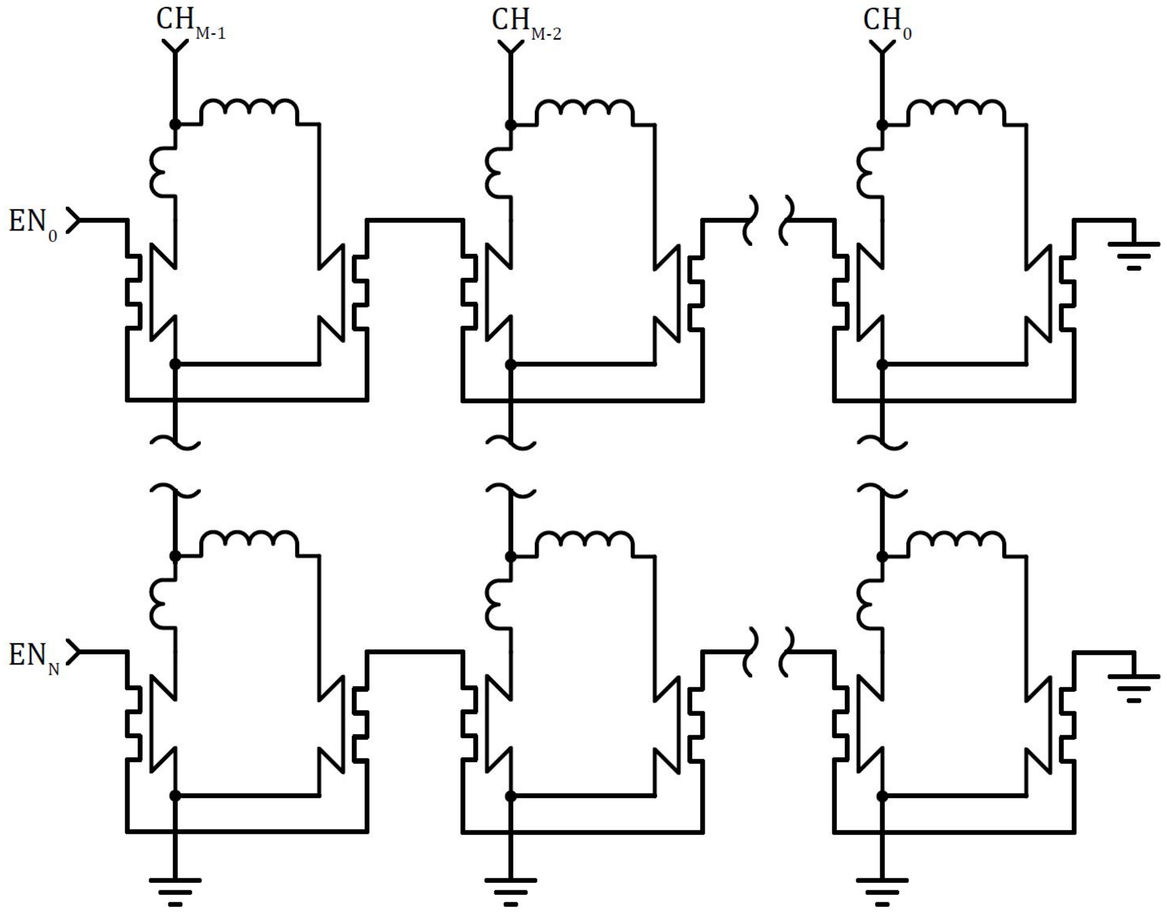
- **yTron makes sneak currents hard to avoid**
- **Forming an array requires addressing circuitry**
  - Increases cell size
  - Increases power dissipation
  - Reduces speed



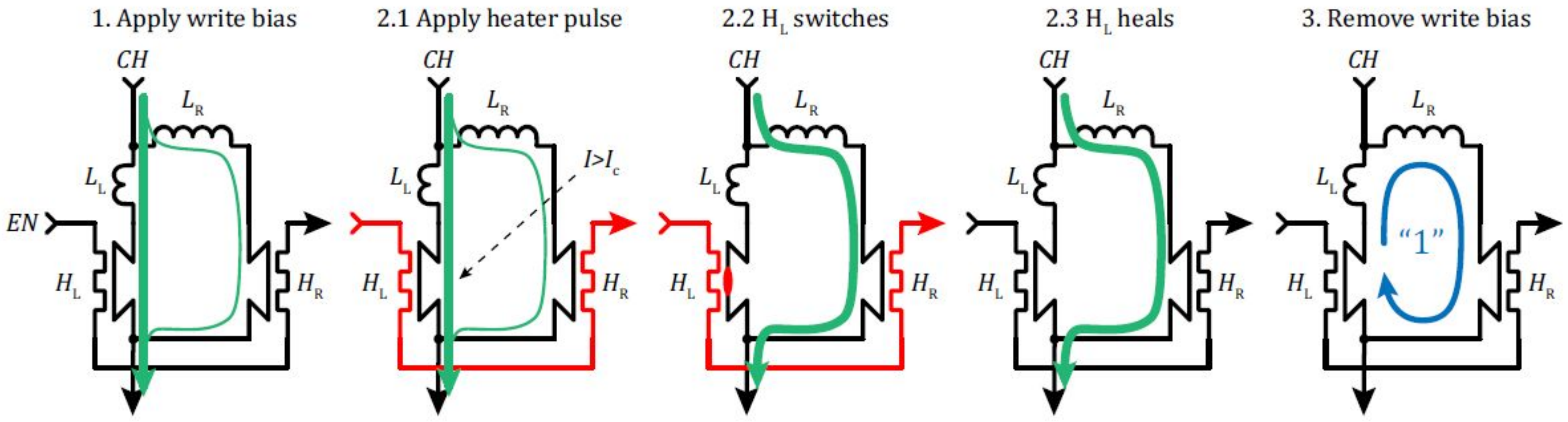
Destructive nanowire memory

Destructive-read memory allows for simplified array geometry.



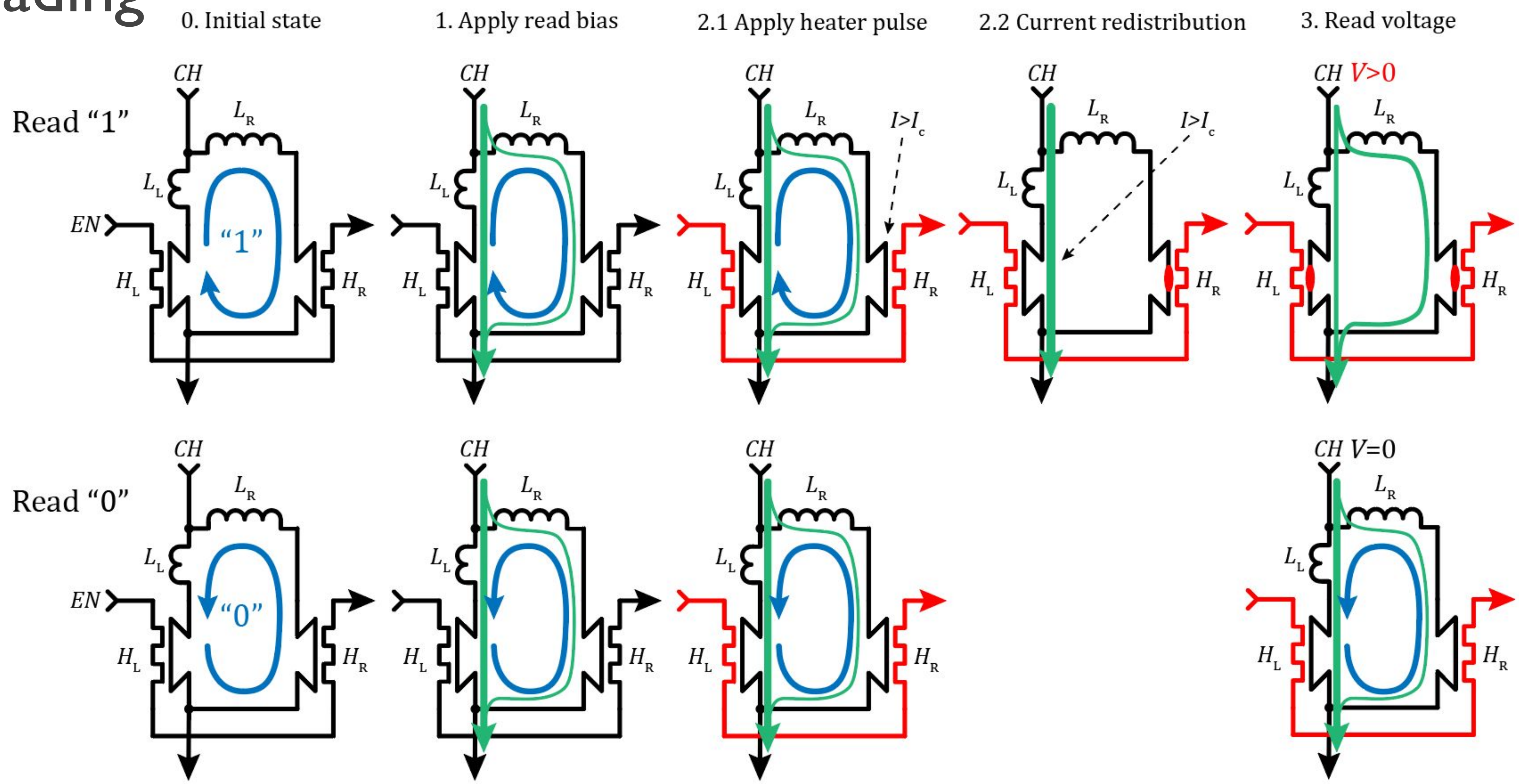


Writing

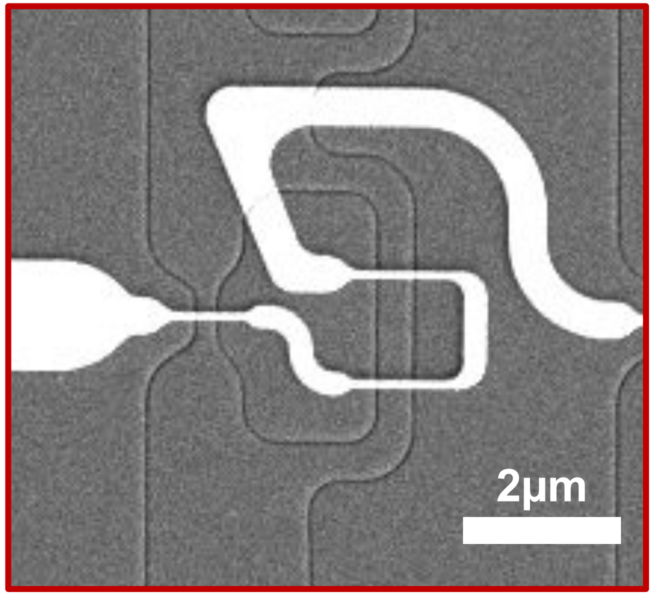


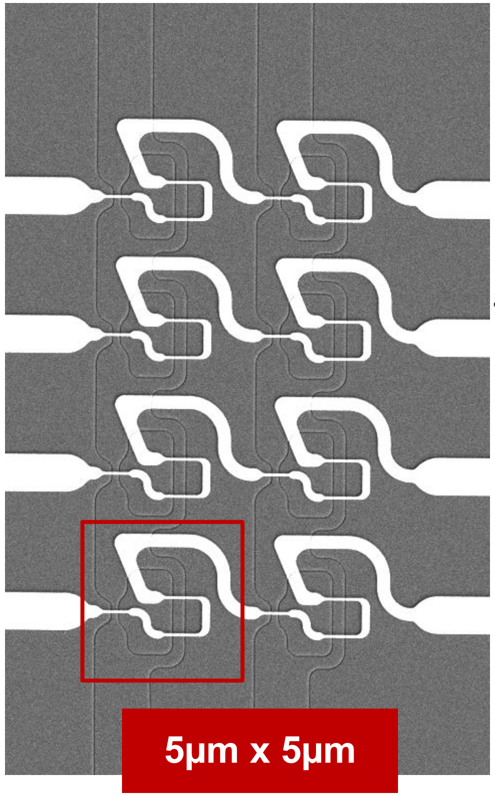
1. Apply write bias
2.1 Apply heater pulse
2.2 H_L switches
2.3 H_L heals
3. Remove write bias
CH
L_R
L_L
EN
H_L
H_R
I>I_c
"1"

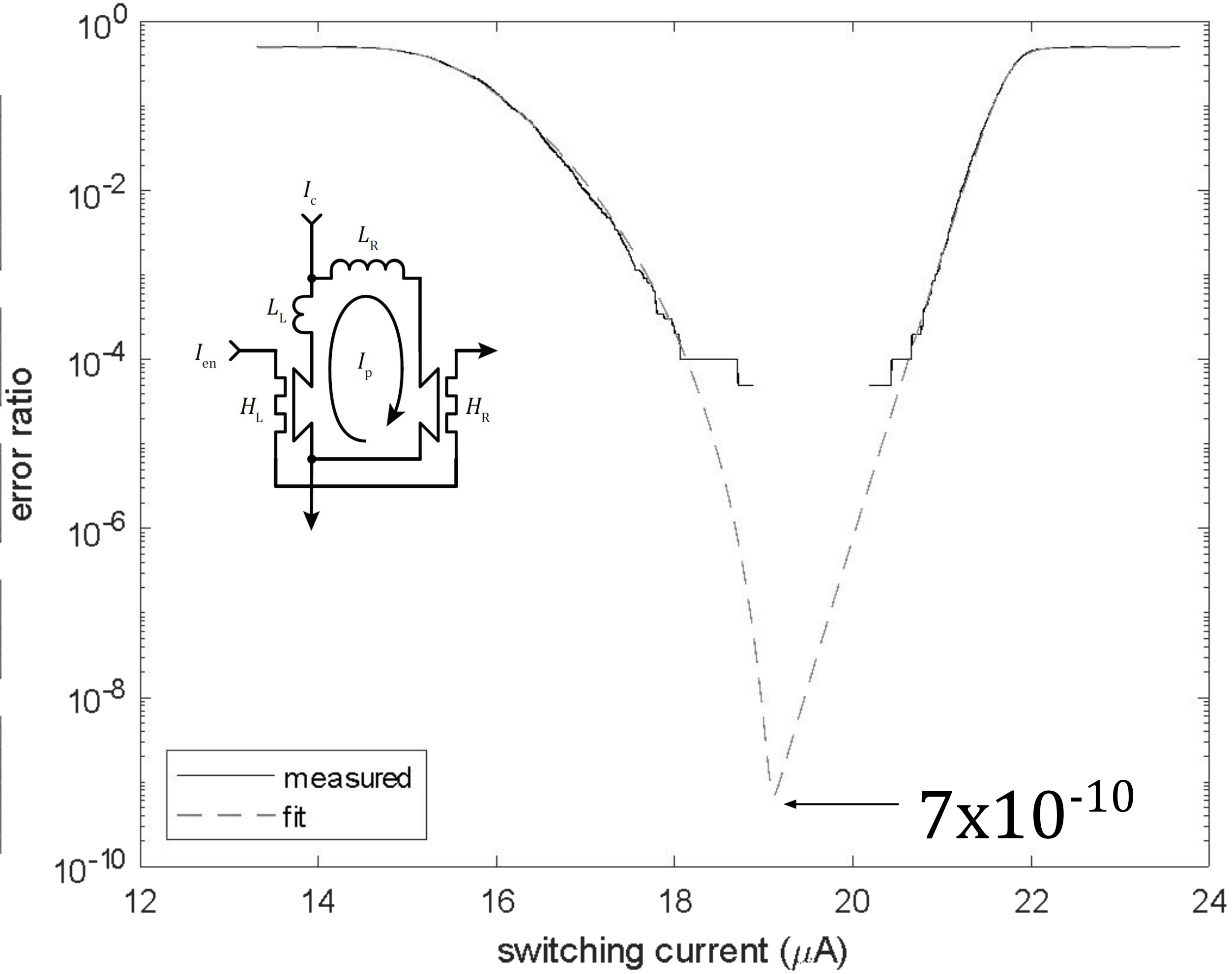
Reading


0. Initial state
1. Apply read bias
2.1 Apply heater pulse
2.2 Current redistribution
3. Read voltage
Read "1"
Read "0"
CH
CH V>0
CH V=0
EN
"1"
"0"
I>Ic
LR
LL
HL
HR

Switching Distributions







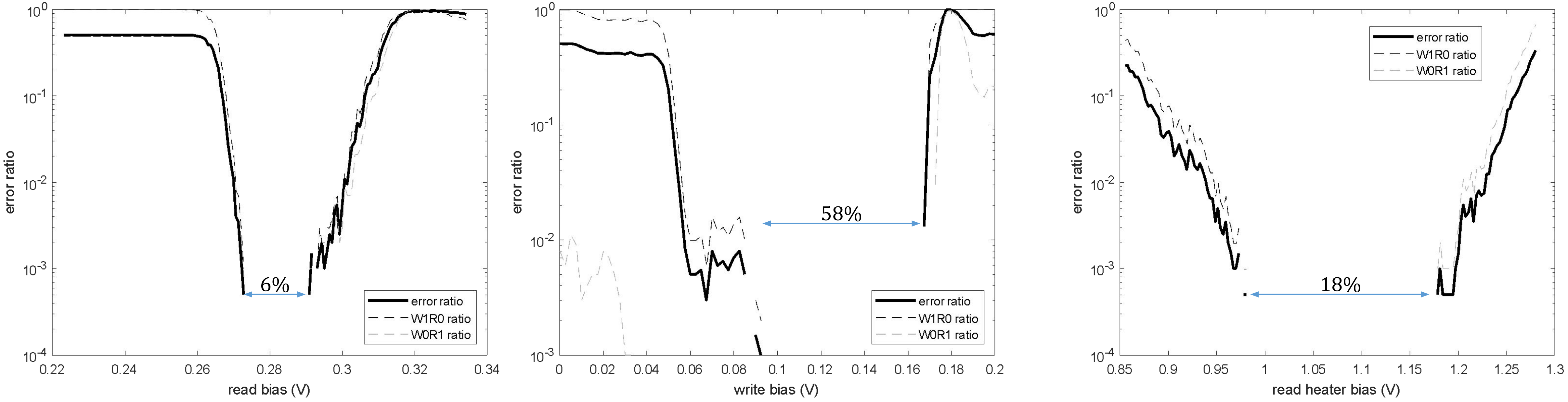
Butters, B A., et al. "A scalable superconducting nanowire memory cell and preliminary array test." *Superconductor Science and Technology* (2021)

Comparison to existing superconducting memories

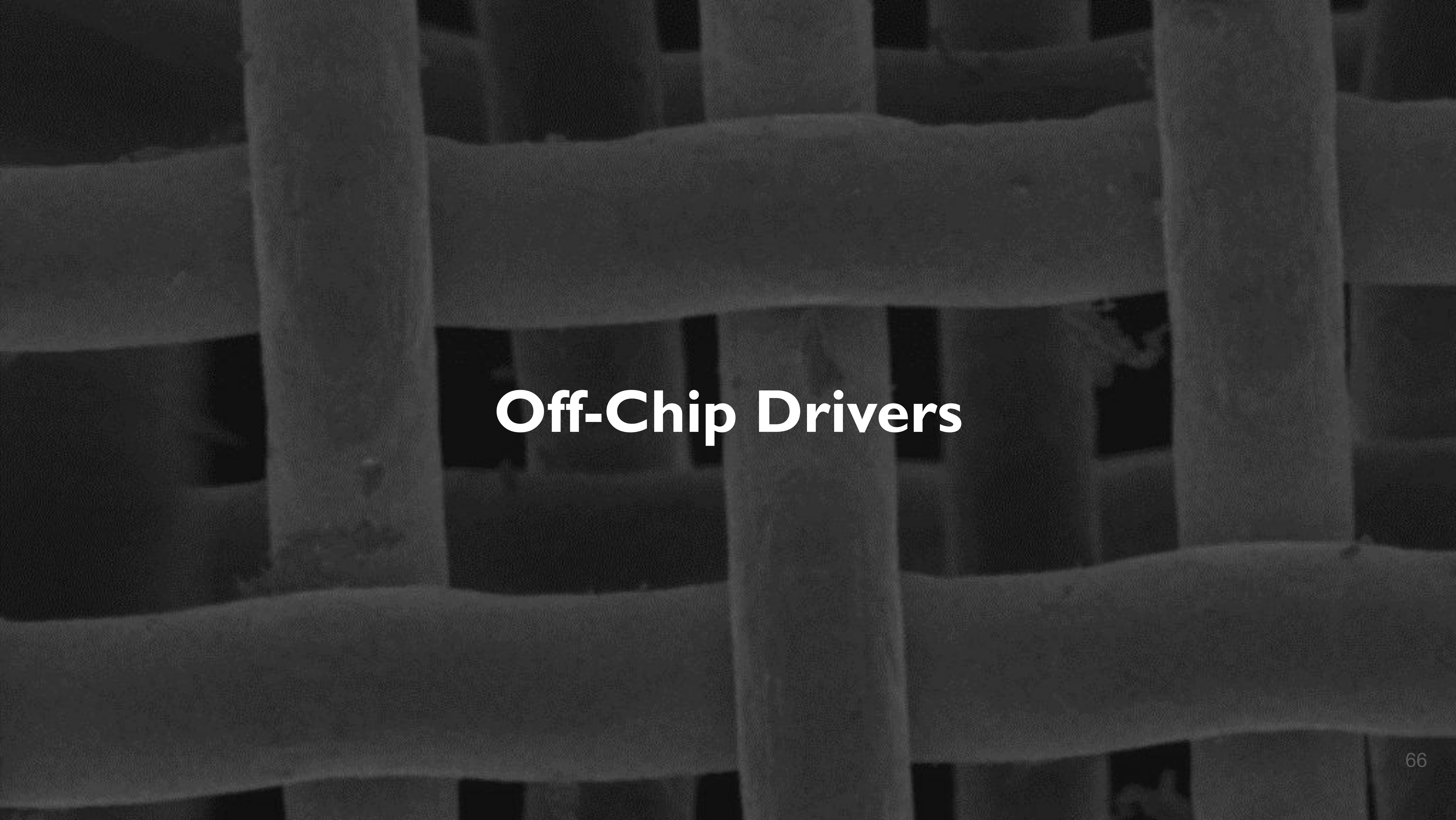
Table CEQIP-6 Superconductor Memory Status

Name	*References*	*RAM*	*Bit Cell Area [μm²]*	*Latency [ns]*		*Energy [fJ]*		*Static Power*	*Bits*
				Read	*Write*	*Read*	*Write*		
SR: shift register, ac-biased	[121]		300 (15×20)						202 280
SR: shift register	[339]			0.02	0.02	0.1	0.1	0.2 mW	64
VTM: vortex transition memory	[203 (VT2)]	✓	99 (9×11)	0.10	0.10	100	100		72
JJ-RAM: Josephson junction RAM	[199]	✓	484 (22×22)					4.5 mW	4096
RQL-RAM: reciprocal quantum logic	[200]	✓	1452 (33×44)						1024
PRAM: PTL-RAM	[201, 202]	✓	1452 (33×44)						512
SHE-MTJ: Spin Hall effect magnetic tunnel junction	[239]	✓	2470 (38×65)	0.10	2	1000	8000		16
SNM: superconducting nanowire memory	[107]	✓	26.5 (5×5.3)	0.10	3	10	10		8
Hybrid: JJ-CMOS	[659]	✓		2 ~ 4	2 ~ 4	100	100		65 536

Holmes, D. Scott. "Cryogenic Electronics And Quantum Information Processing." *2022 IEEE International Roadmap for Devices and Systems Outbriefs*. IEEE, 2022.

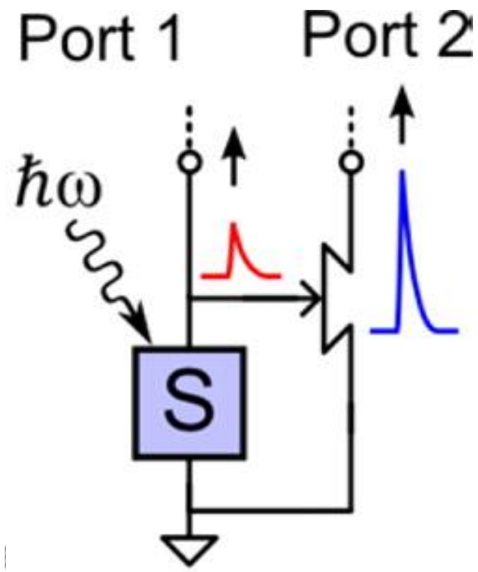


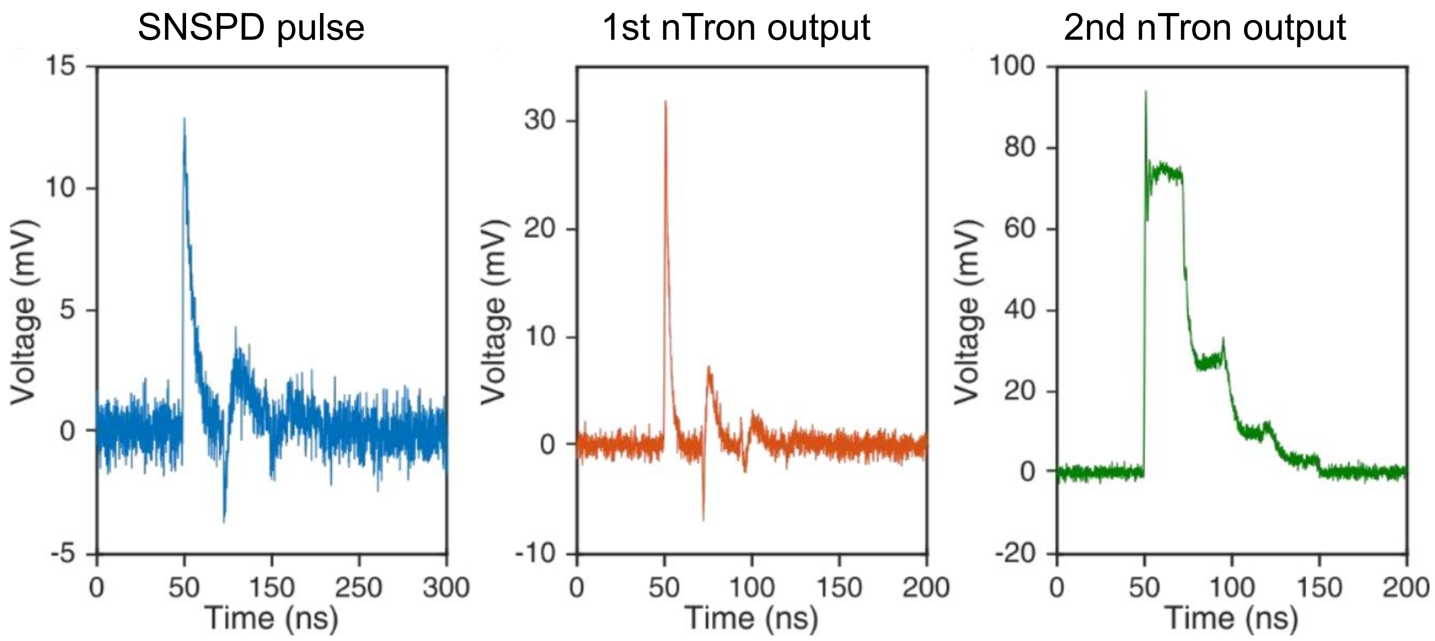
error ratio
read bias (V)
6%
error ratio
W1R0 ratio
W0R1 ratio
error ratio
write bias (V)
58%
error ratio
W1R0 ratio
W0R1 ratio
error ratio
read heater bias (V)
18%
error ratio
W1R0 ratio
W0R1 ratio



Off-Chip Drivers

nTron Amplifier Example for SNSPDs

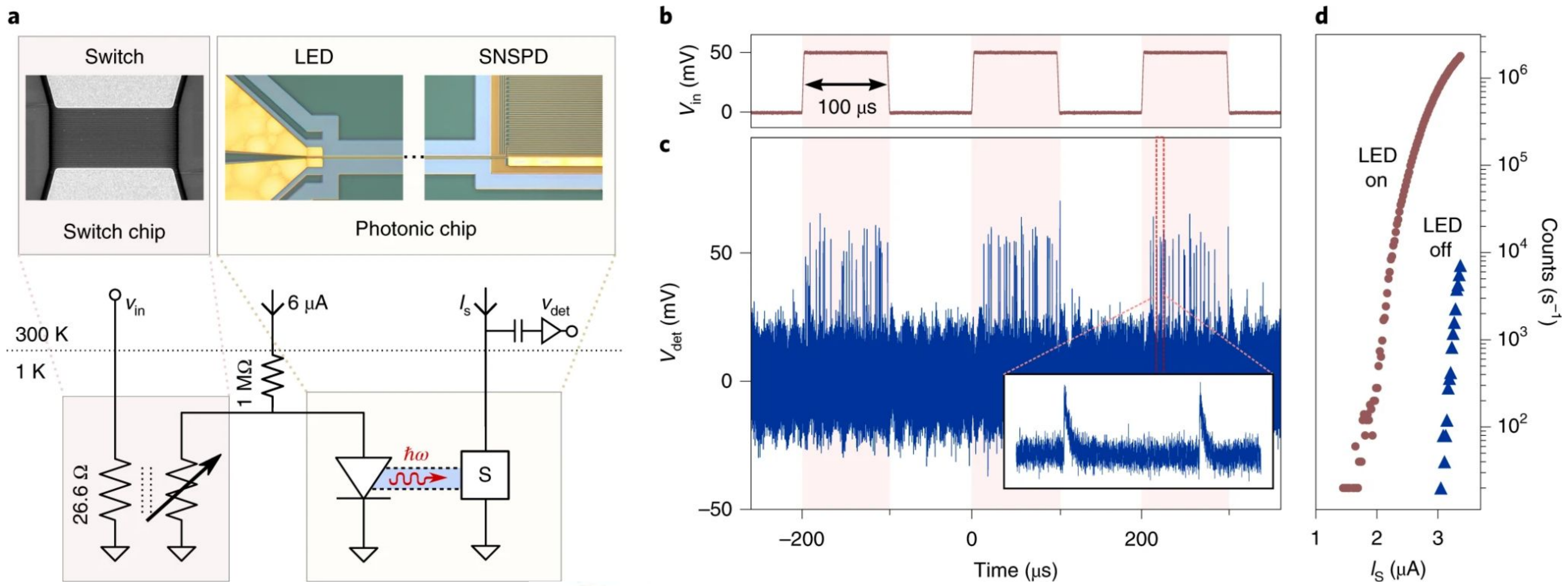




A. N. McCaughan and K. K. Berggren, Nano Letters 14(10), 5748 (2014)

Zheng, K., Zhao, Q. Y., et al. "A Superconducting Binary Encoder with Multigate Nanowire Cryotrons." *Nano letters*, *20*(5), (2020) 3553-3559. (Supporting Information)

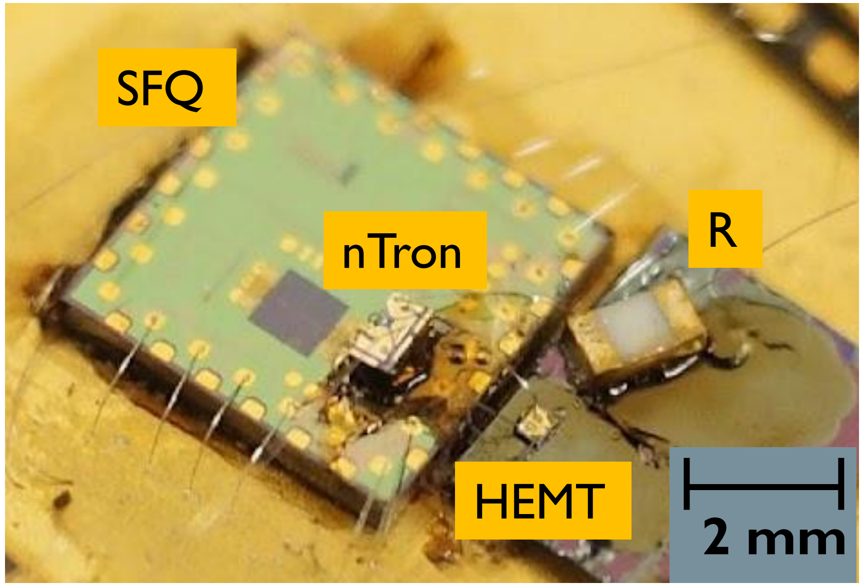
The NIST Thermal Switch (hTron)

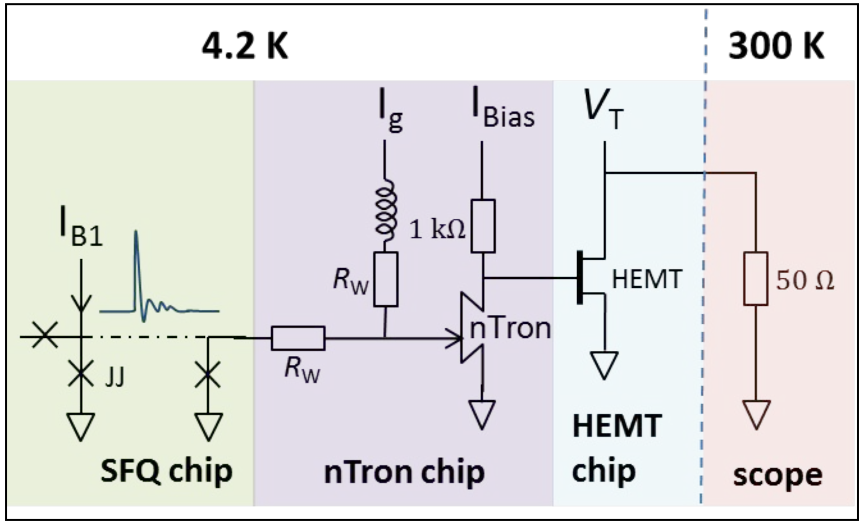


A. McCaughan

McCaughan, A.N., *et al.* "A superconducting thermal switch with ultrahigh impedance for interfacing superconductors to semiconductors." *Nat Electron* 2, 451–456 (2019).

Interface between RSFQ & Semiconductors

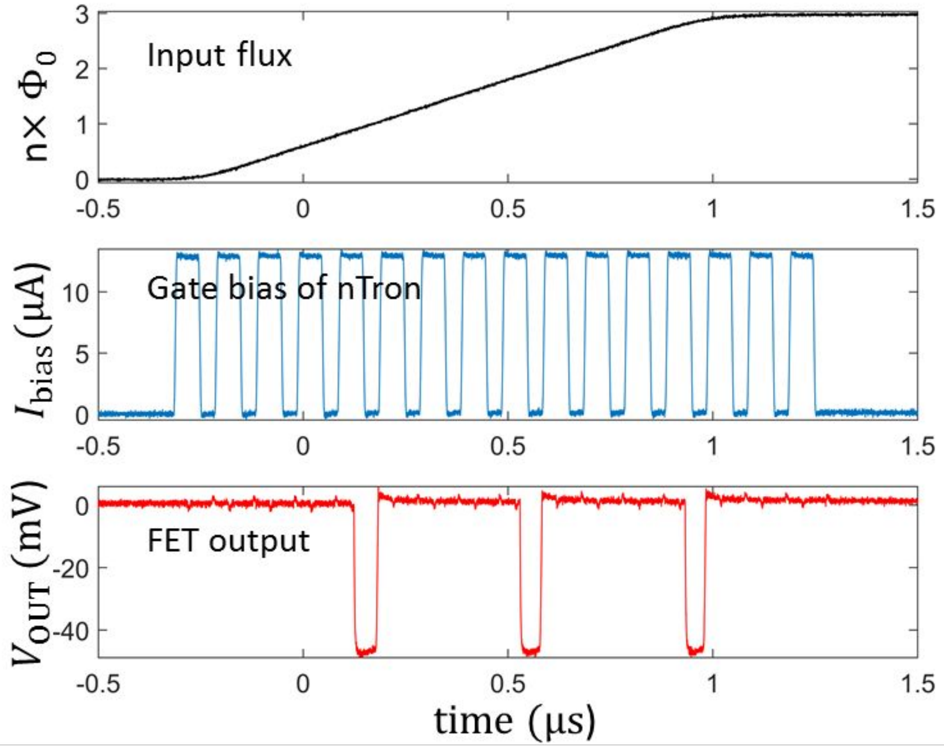




Experimental demonstration

SFQ→nTron→HEMT

Josephson junction → nanowire → transistor

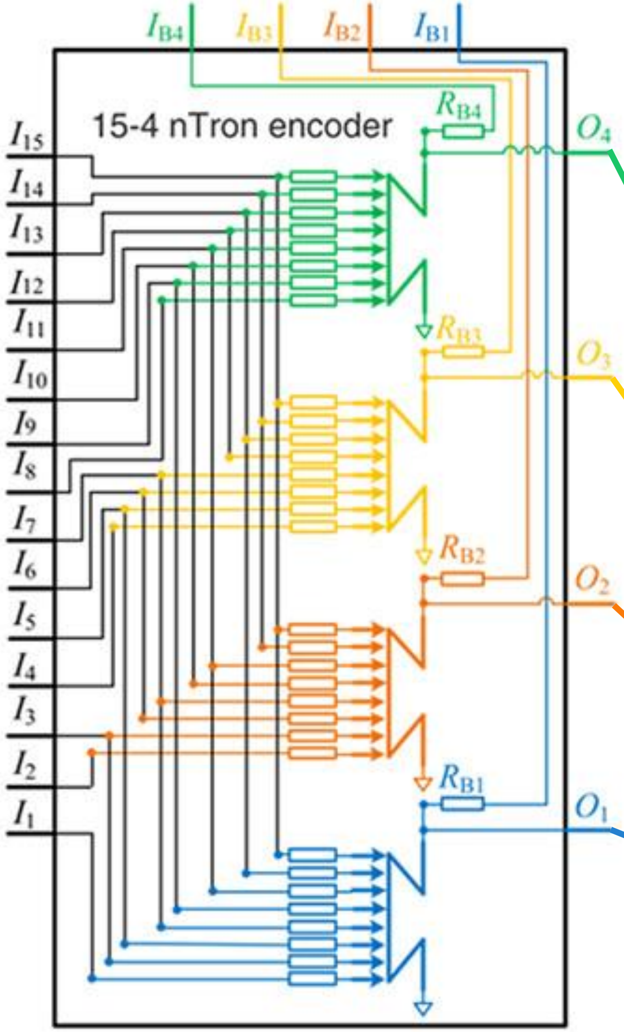


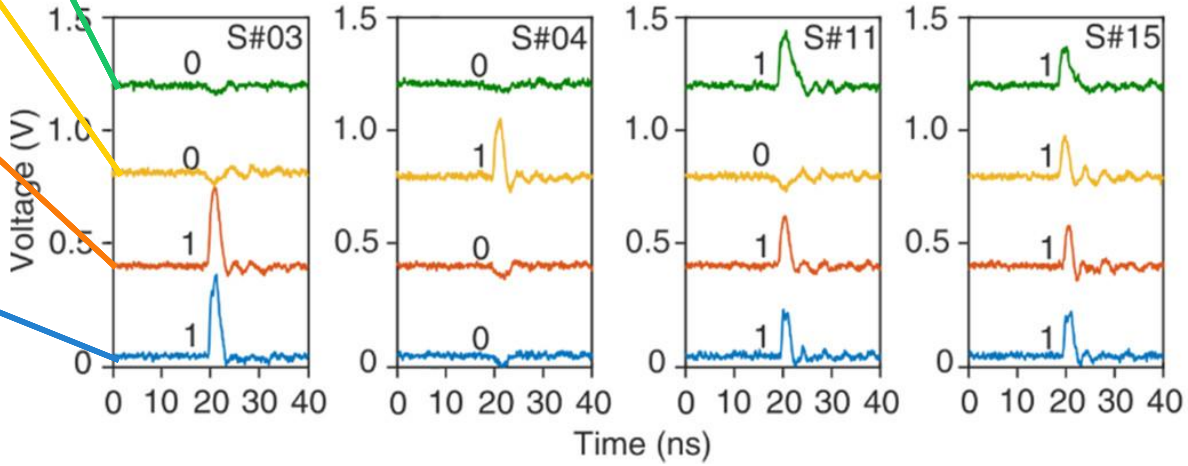
Collaborate with Thomas Ortlepp from CiS Research Institute for Microsensor Systems GmbH

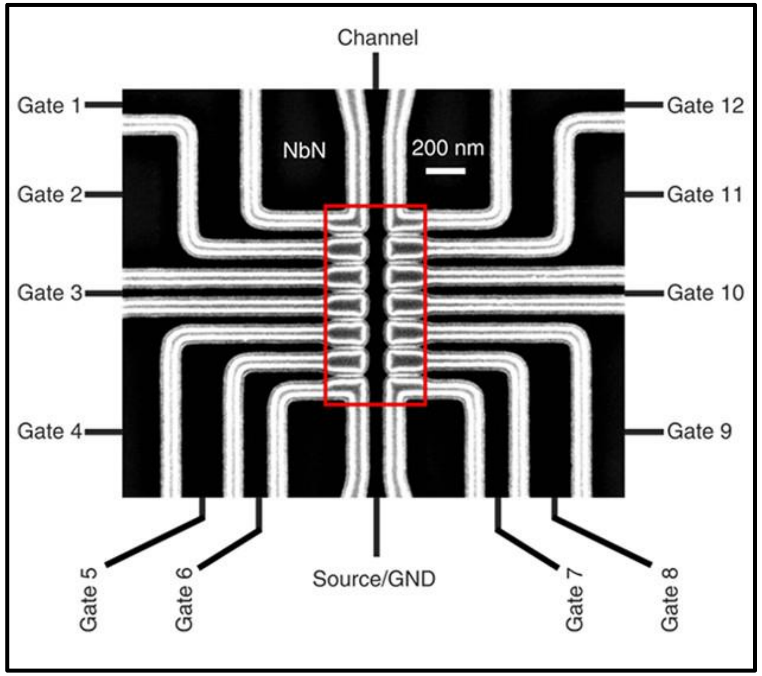
Encoders

A major need for superconducting electronics is the ability to do robust multiplexing onto and off chip.

The Nanjing Encoder



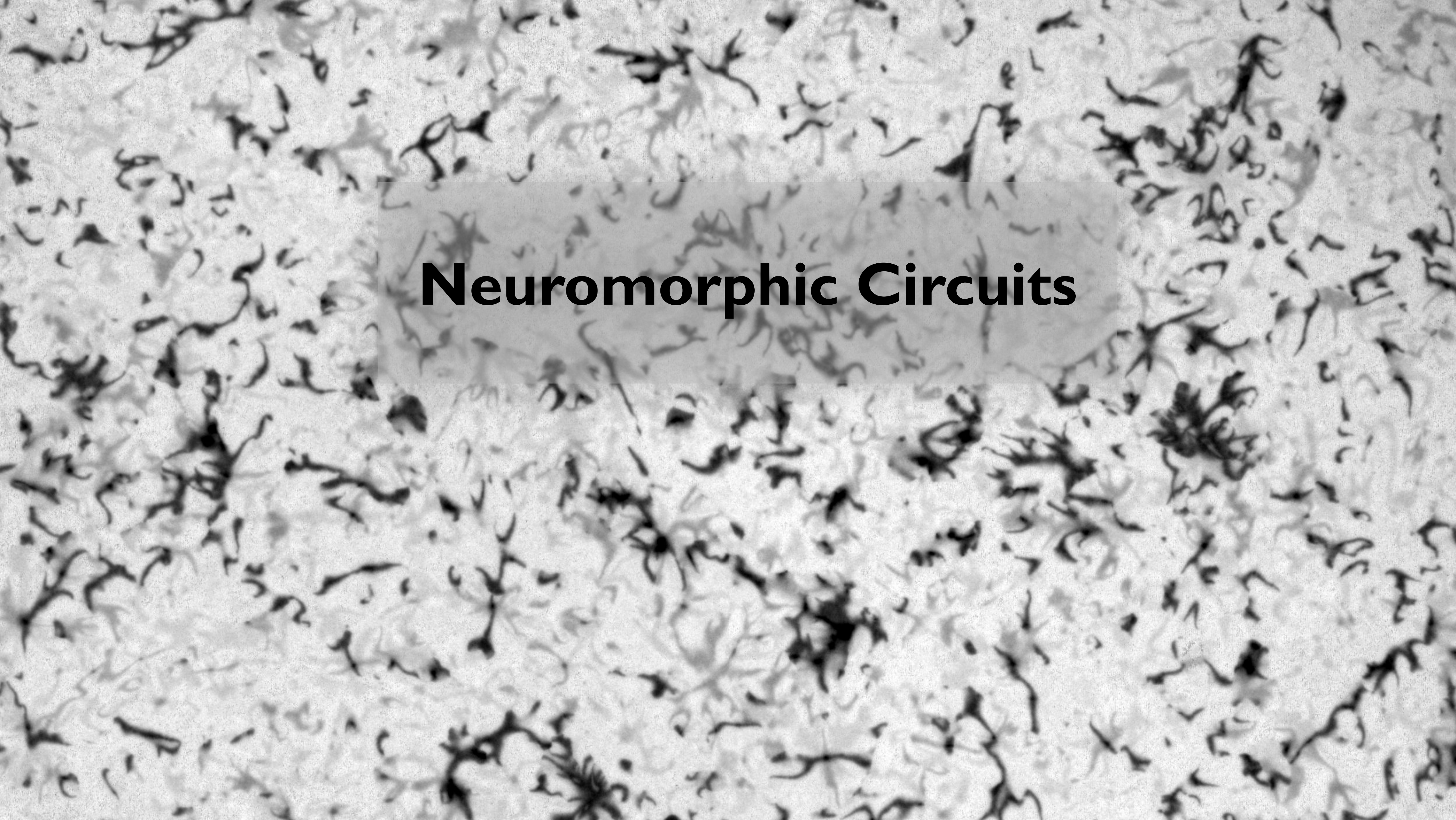




Qingyuan Zhao

Zheng, K., Zhao, Q. Y., et al. "A Superconducting Binary Encoder with Multigate Nanowire Cryotrons." *Nano letters*, *20*(5), (2020) 3553-3559.

Neuromorphic Circuits



Application to Neuromorphic Computing

- **Neuromorphic circuits are likely to require multiple modalities (e.g. flux, light, charge)**
- **Natural fit to spiking characteristic of physical neurons**

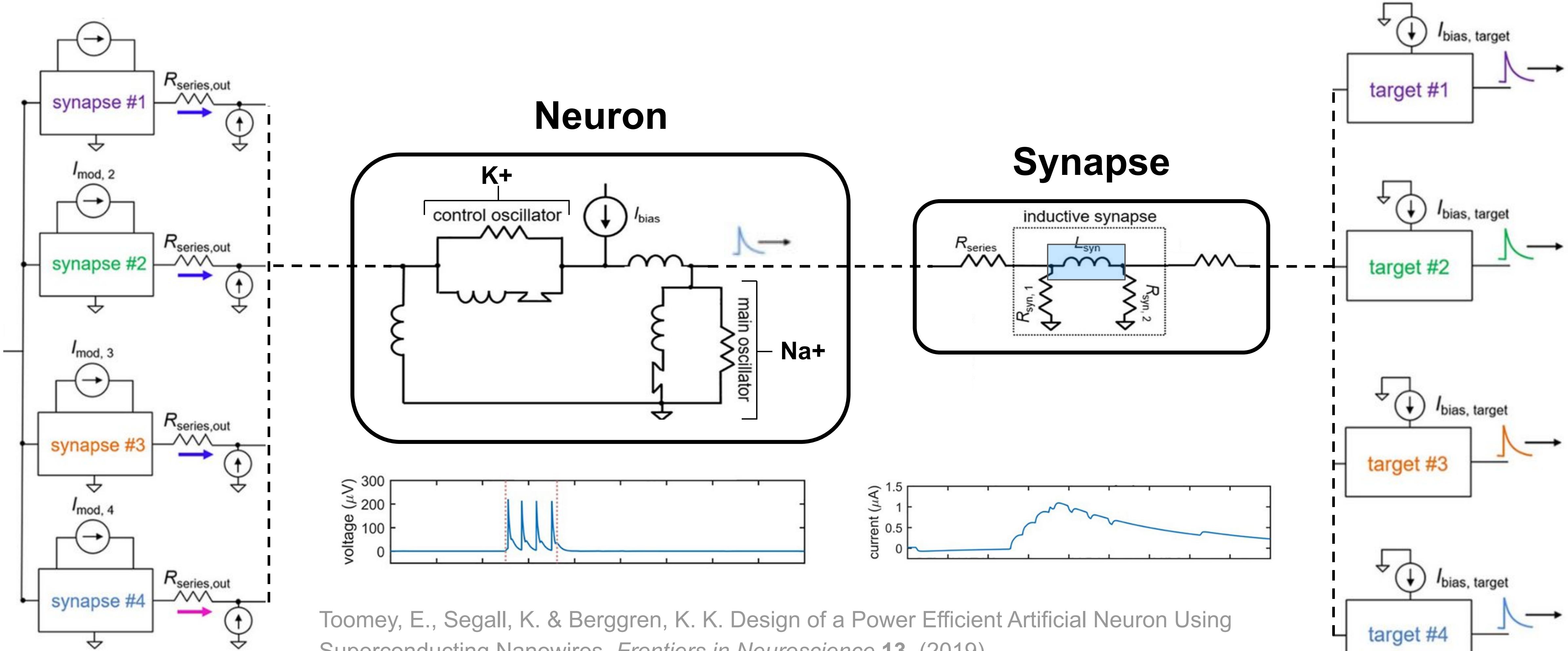
Emily Toomey
Grad student

In Collaboration With

Ken Segall,
Colgate

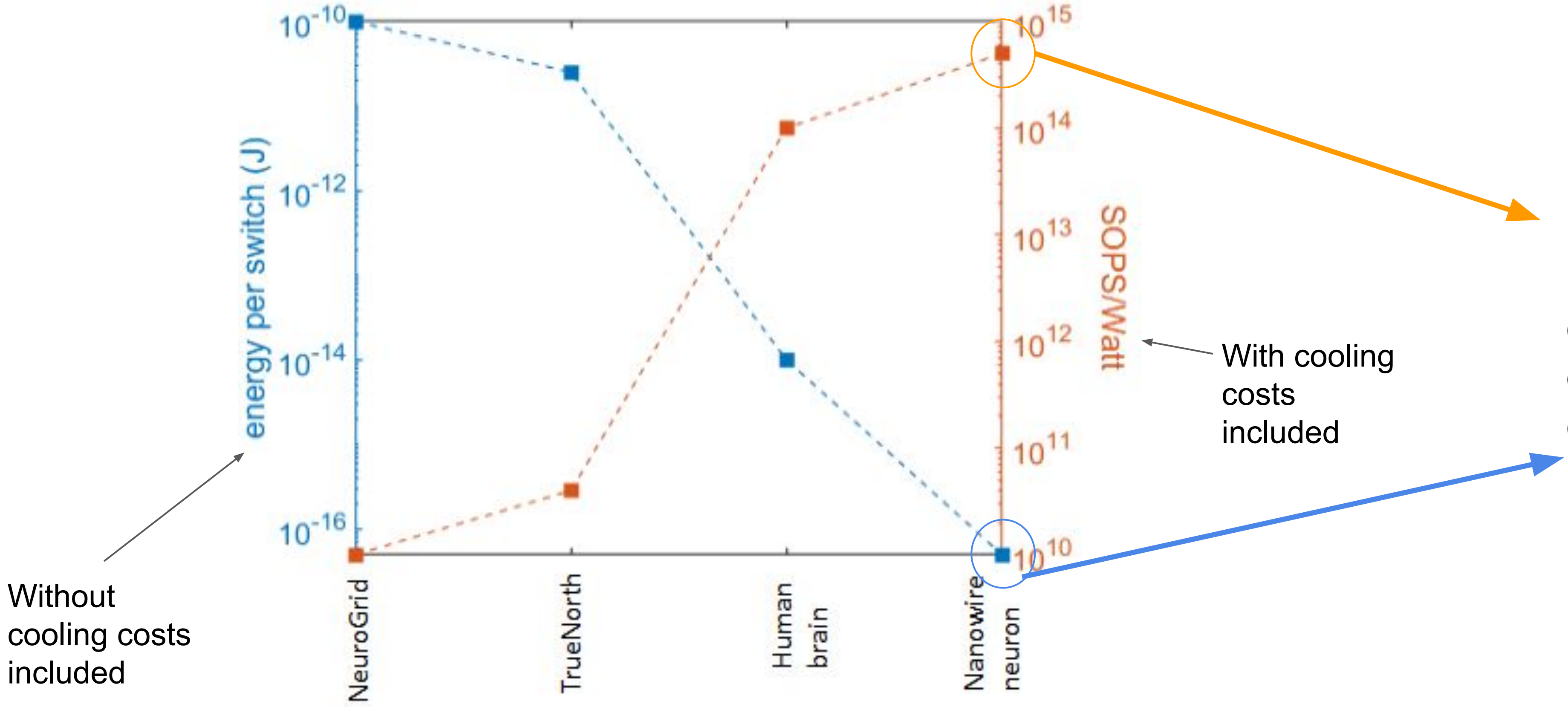
Nancy Lynch,
MIT

Applications to neuromorphic computing



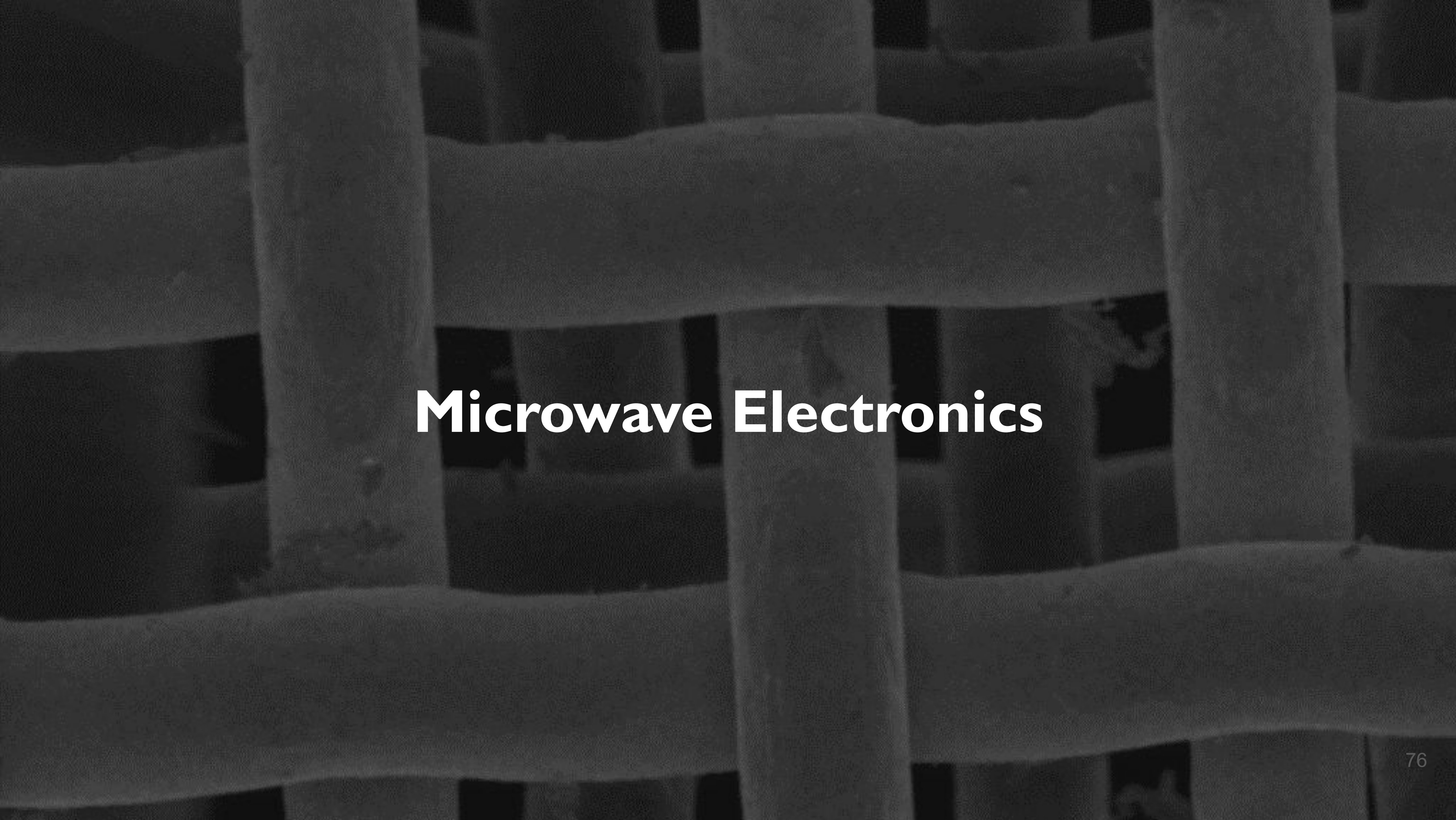
Toomey, E., Segall, K. & Berggren, K. K. Design of a Power Efficient Artificial Neuron Using Superconducting Nanowires. *Frontiers in Neuroscience* **13,** (2019).

Nanowire neuron: energy performance



Disclaimer: These are projections, while the other points on this graph are demonstrations.

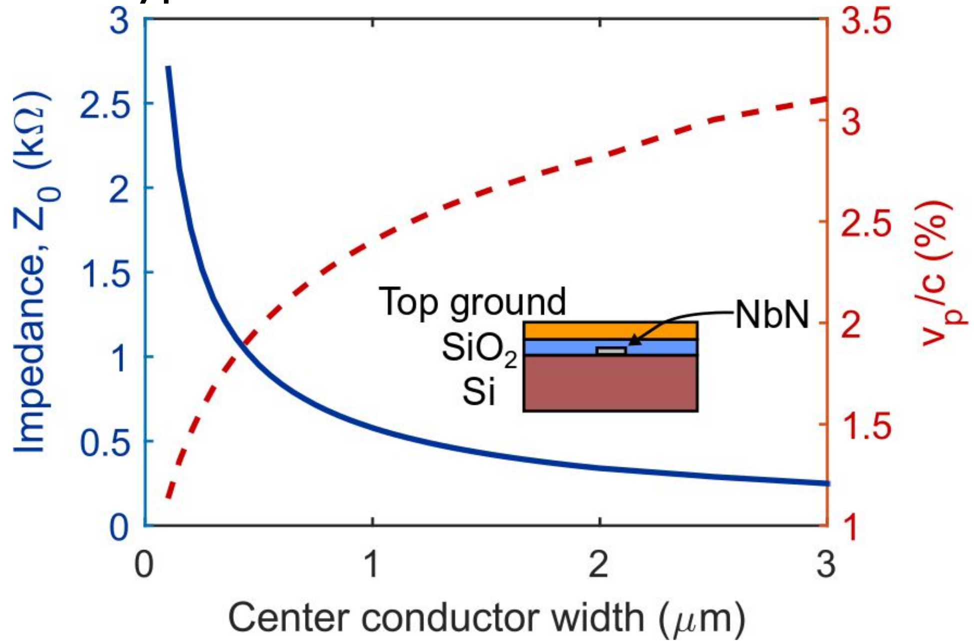
- Projected to have a figure of merit 4 orders of magnitude better than current CMOS architectures
- Additional advantage of no static power dissipation in the interconnects
- JJ neuron projected to have ~ 10^{15} SOPS/Watt

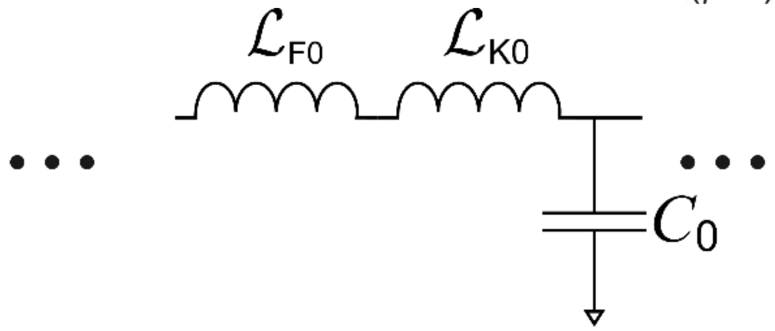


Microwave Electronics

Slow-wave transmission line

A typical nanowire transmission line





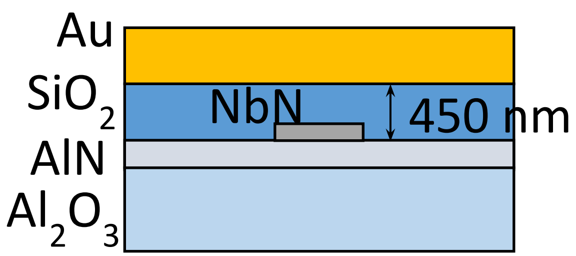
For a ~ 5 nm thick 300 nm wide NbN microstrip,

$\mathcal{L}_{K0} \approx 212\mu_0 \quad \mathcal{L}_{F0} \approx 0.3\mu_0 \quad \mathcal{C}_0 \approx 21\epsilon_0$

Measured group velocities to date

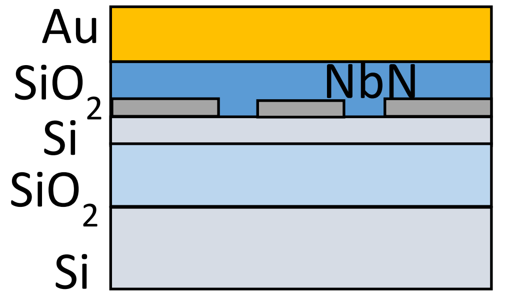
Signal speed ~2%*c* = 6 μm / ps

Zhao et al. Nat. Photonics 11, 247 (2017)



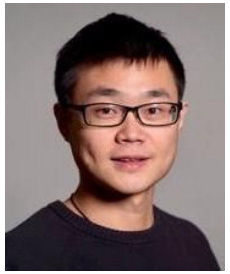
Signal speed 1.6%*c* = 4.8 μm / ps

Zhu et al. Nat. Nanotech. 13, 596 (2018)



Signal speed = 2.7 μm/ps

Zhu et al. (2018), unpublished

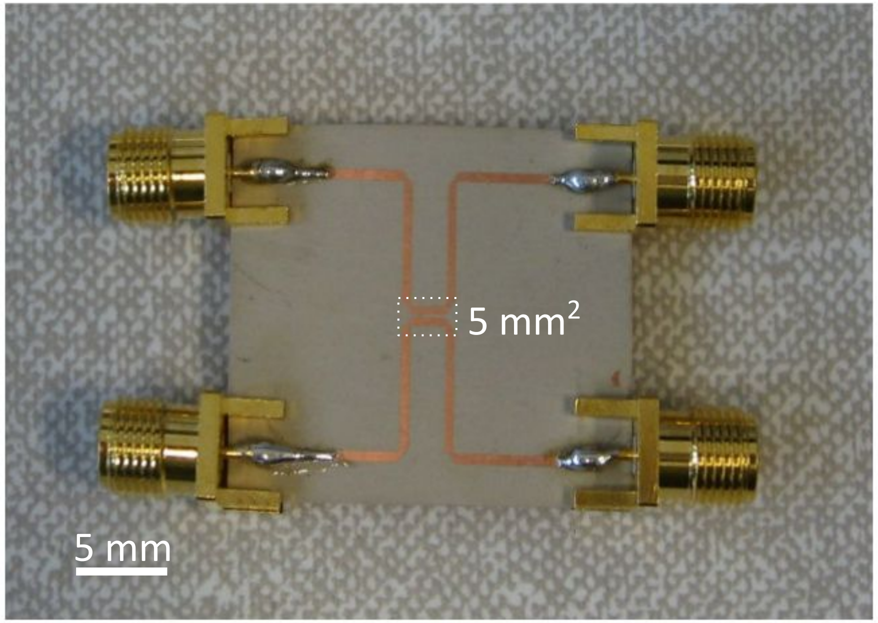


Di Zhu

In collaboration with ***Daniel Santavicca (UNF)***

Extreme footprint reduction

@ 12 GHz - λ = 1 cm



Fauzi, Azahar, and Zairi Ismael Rizman. *Journal of Engineering Science and Technology* 11.3 (2016): 431-442.

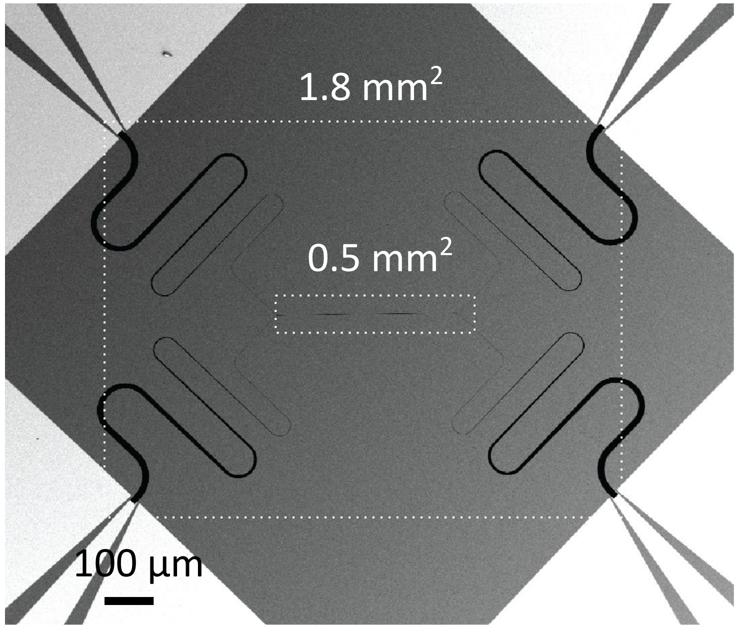
12 GHz microstrip directional coupler (on RO6010)

- backward coupling
- $Z_0 = 50\ \Omega$

Nanowire
Microstrip
Transmission Lines

10× - 100×
footprint reduction

@ 5 GHz - λ = 1 mm



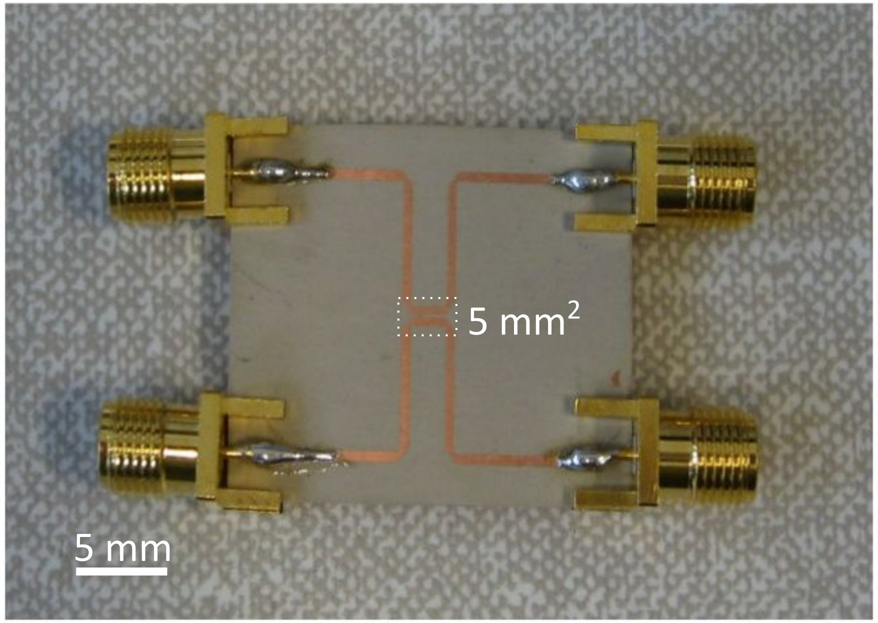
Colangelo, Marco, et al. "Compact and Tunable Forward Coupler Based on High-Impedance Superconducting Nanowires." *Physical Review Applied* 15.2 (2021): 024064.

5 GHz microstrip directional coupler

- forward coupling
- $Z_0 = 1446\ \Omega$

Extreme footprint reduction

@ 12 GHz - λ = 1 cm



Fauzi, Azahar, and Zairi Ismael Rizman. *Journal of Engineering Science and Technology* 11.3 (2016): 431-442.

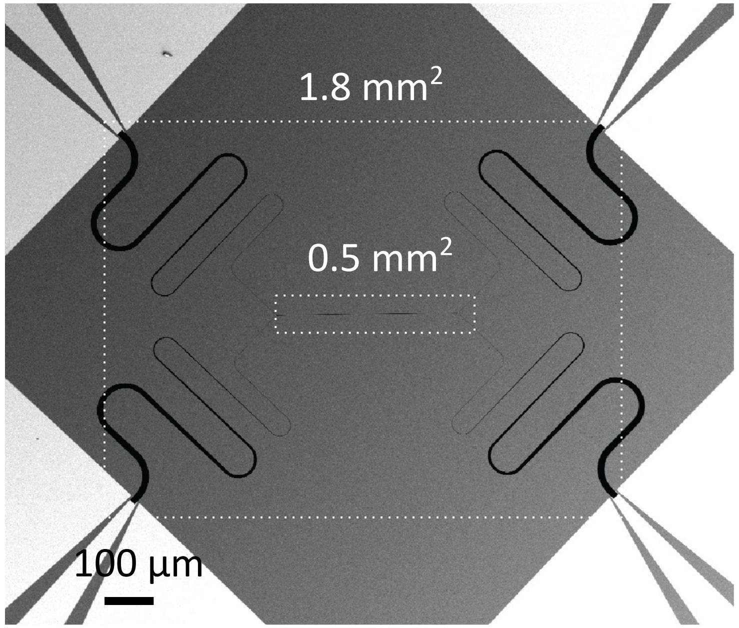
12 GHz microstrip directional coupler (on RO6010)

- backward coupling
- $Z_0 = 50\ \Omega$

Nanowire Microstrip Transmission Lines

10× - 100× footprint reduction

@ 5 GHz - λ = 1 mm

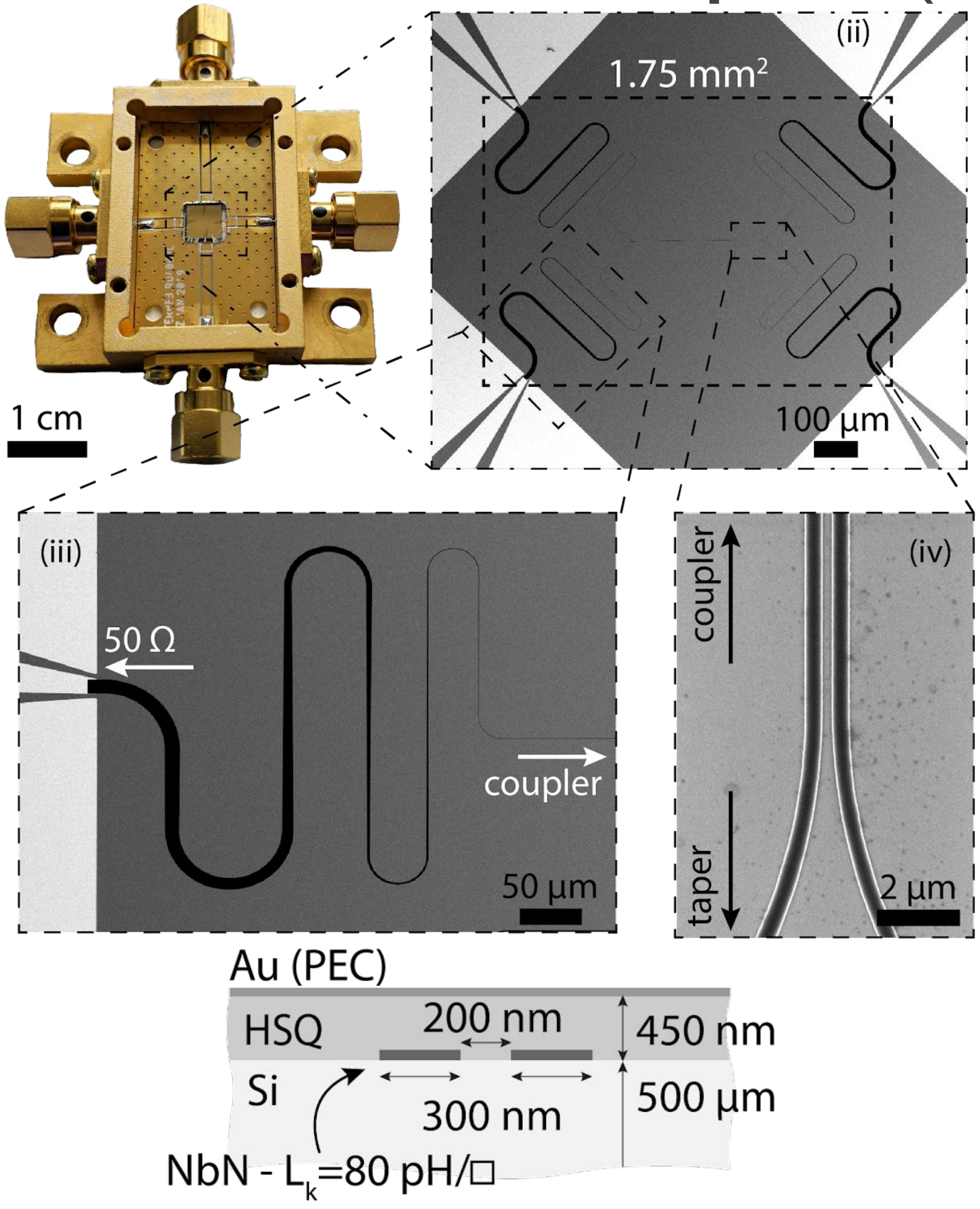


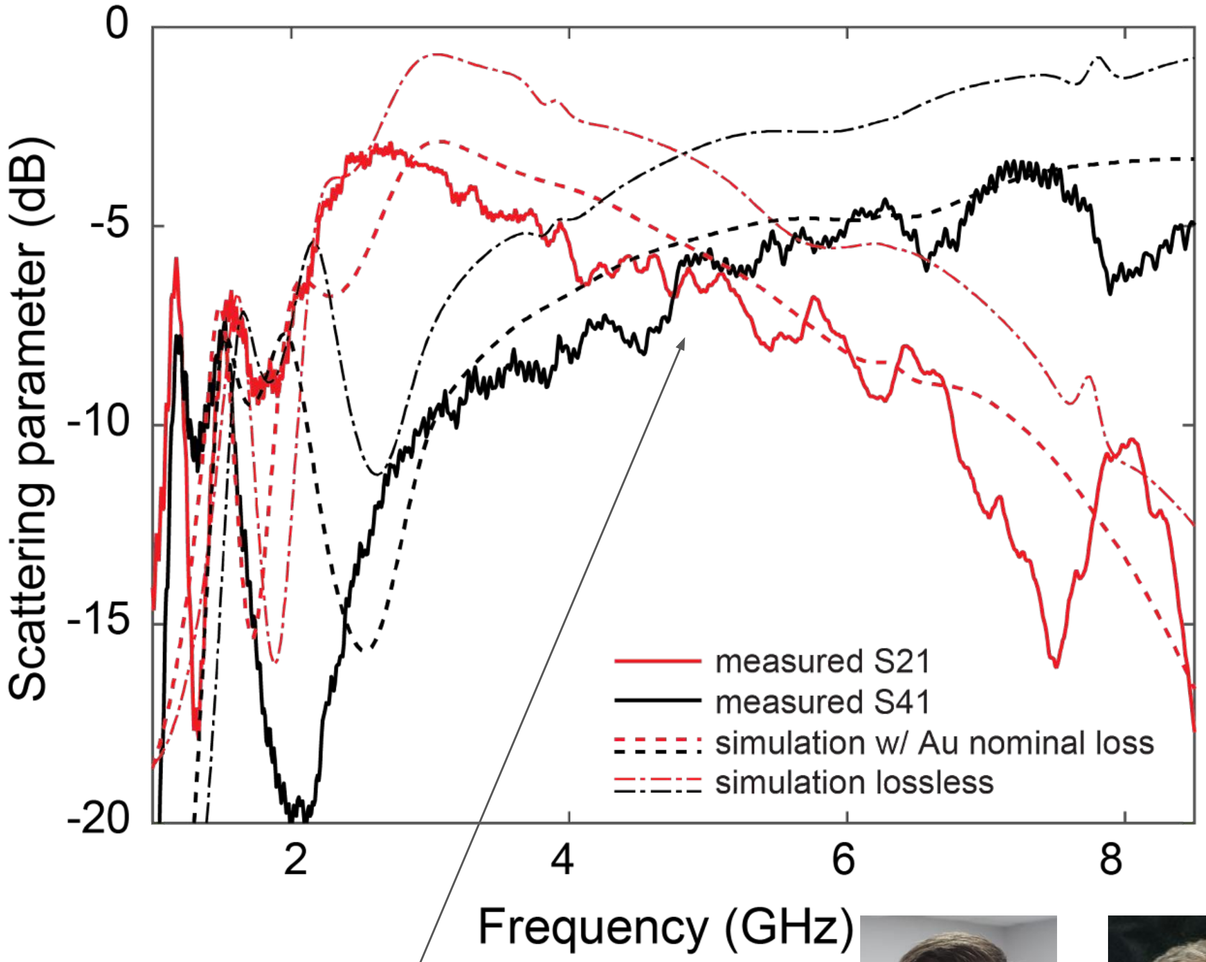
Colangelo, Marco, et al. "Compact and Tunable Forward Coupler Based on High-Impedance Superconducting Nanowires." *Physical Review Applied* 15.2 (2021): 024064.

5 GHz microstrip directional coupler

- forward coupling
- $Z_0 = 1446\ \Omega$

Nanowire coupler (experiment)





50:50 balanced coupling at 4.75 GHz

Colangelo, M., et al. 2021. *Physical Review Applied* 15 (2): 024064.

In collaboration with ***Daniel Santavicca (UNF)*** *and* ***Joshua Bienfang (NIST)***

High-Temp Operation

Potential Future High-Temperature Operation

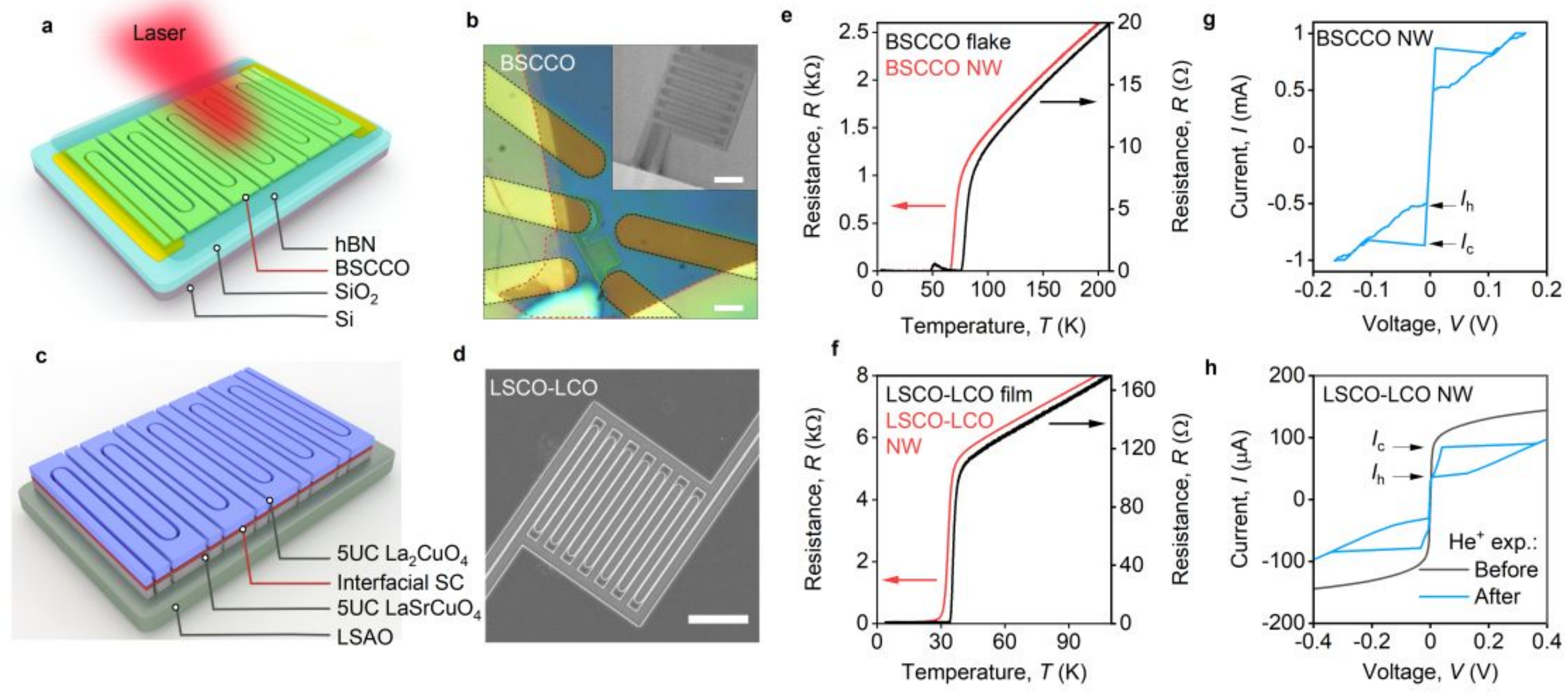


FIG. 1. **High-T_c superconducting nanowires. a,** Schematic of the BSCCO single-photon detector: A relatively thin flake of BSCCO is covered by a much thicker flake of hBN and transferred onto ultra-flat gold contacts. SNW region is defined by a helium beam exposure. **b,** Optical photograph of the BSCCO device. Scale bar is 3 μm. Inset: Example of the SEM image of the BSCCO SNW produced by the He^+ beam exposure (similar but not identical to that from the photograph). The scale bar is 2 μm. **c,** Schematic of the LSCO-LCO single-photon detector: High-T_c two-dimensional superconductor is formed at the interface between the 5 UC of the LCO insulator and the 5 UC of the LSCO metal. 10 nm of chromium-gold was used for contact leads. **d,** An SEM image of a typical LSCO-LCO SNW device. The scale bar is 2 μm. **e-f,** Examples of the $R(T)$ dependencies for BSCCO (e) and LSCO-LCO (f) flake, film and SNWs. **g,** Typical I-V curve for the BSCCO SNWs measured at $T = 3.7$ K. **h,** Typical I-V curves of the LSCO-LCO SNWs measured at $T = 3.7$ K before and after He^+ ion exposure.

Charaev et al. 2022,
arXiv:2208.05674
[cond-mat.supr-con]

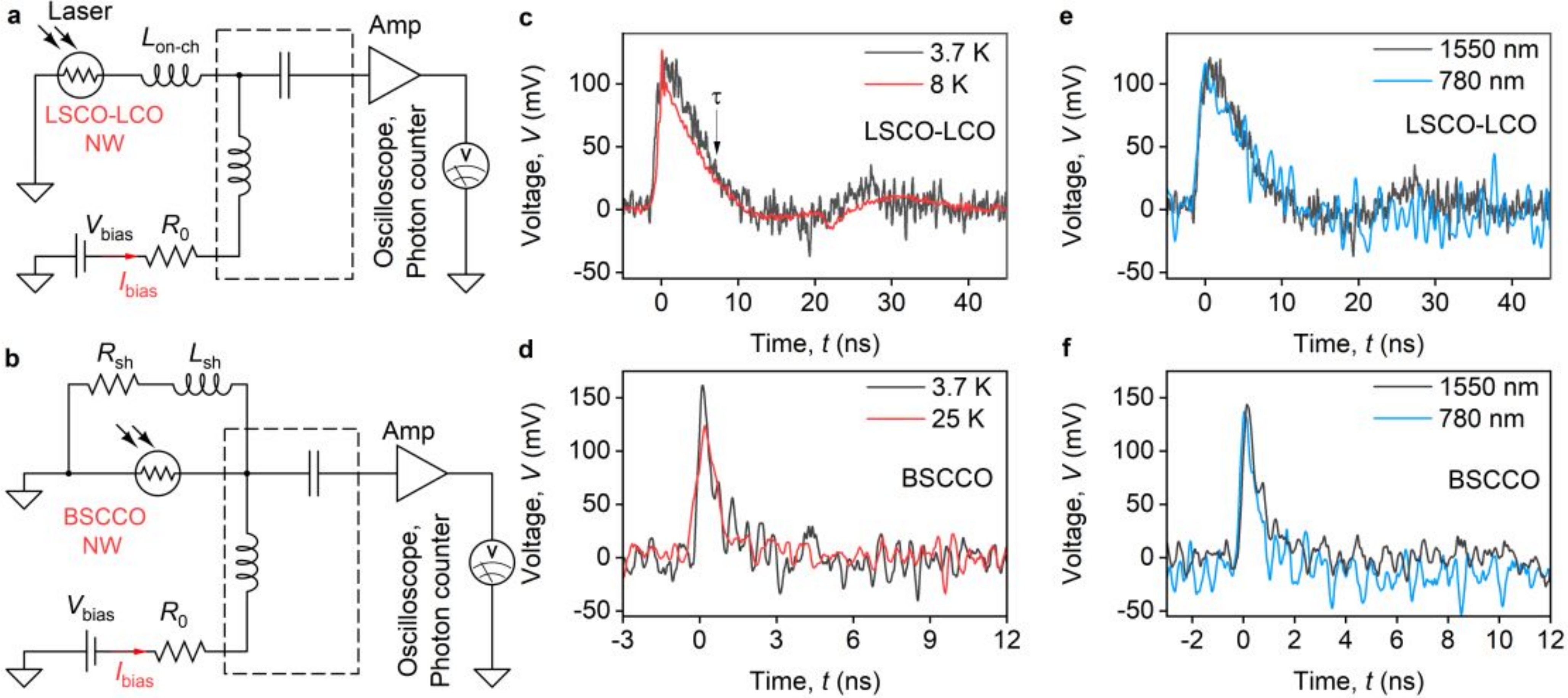


FIG. 2. **Photovoltage generation in cuprate NW detectors.** **a,** The simplified circuit diagram used to measure the photoresponse of the LSCO-LCO SNW detector. The SNW is current-biased by an isolated voltage source connected to the DC port of the bias tee (dashed rectangle) through a resistor, R_0. Incident radiation triggers a voltage spike generating a short pulse that propagates through the AC port of the bias tee to the preamplifier and is read out using an oscilloscope or a photon counter. L_{on-ch} is an on-chip kinetic inductor made out of the LSCO-LCO film. **b,** The simplified circuit diagram used to measure the photoresponse of the BSCCO SNW detector. R_{sh} and L_{sh} are the shunt resistor and the inductor connected in parallel with the BSCCO SNW to prevent it from latching. **c-d,** Photovoltage V_{ph} pulses measured in the LSCO-LCO (c) and BSCCO (d) photodetectors at given T and $\lambda = 1.5\ \mu$m. The devices are biased to the 95% of their critical current for given T. **e-f,** The V_{ph} pulses measured at given λ for the LSCO-LCO (e) and BSCCO (f) devices at $T = 3.7$ K and $T = 16$ K respectively.

Vision & Conclusion

- **Nanowire-Based electronics**
  - Low power, high output impedance
  - Driving more conventional electronics
  - Simple manufacturing

- **Where is this going?**
  - High-temperature (> 20K) electronics for a range of applications (e.g. MgB_2)
  - Exploit microwave behaviors
  - Applications in neuromorphic, reversible, and other alternative computing paradigms
  - Scaling and shunting to speed up devices and lower power

Power Consumption: Rough Analysis

- **Switching energy, compare to Silicon**
  - $E \sim V^2$
  - $V \sim 100\times$ lower →Energy ~ 1e4 lower
  - Cooling penalty ~ 1e3
    - ➪ final advantage ~ 10×
- **Switching energy, compare to RSFQ**
  - $E = \Phi^2 / 2L$
  - $\Phi \sim 100 \times$ larger and $L \sim 100 \times$ larger
    - ➪ final disadvantage ~ 100×
- **V and Φ are scalable, potentially**

Remaining Concerns

- **Realistic models**
- **Reproducible fabrication processes**
  - Can critical current of a wire be controlled?
- **Scalable designs**

Likely Applications

- **Detector readout, where materials are already suitable for nanowire electronics**

- **Memories, where JJs struggle with footprint**

- **Off-chip drivers or memory-line drivers, where JJs struggle with high load impedances and bandwidth requirements are lower**

- **Radiation-sensitive applications (e.g. space, HEP) where dielectric barriers might degrade**

THANK YOU

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  - IARPA, NASA, Skolkovo Inst. of Technology
- Many U.S. and international fellowships

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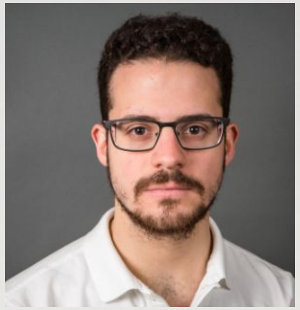

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END OF PRESENTATION

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