CAEN Electronic Instrumentation
Tools for Discovery

Readout chains for Fast Detectors

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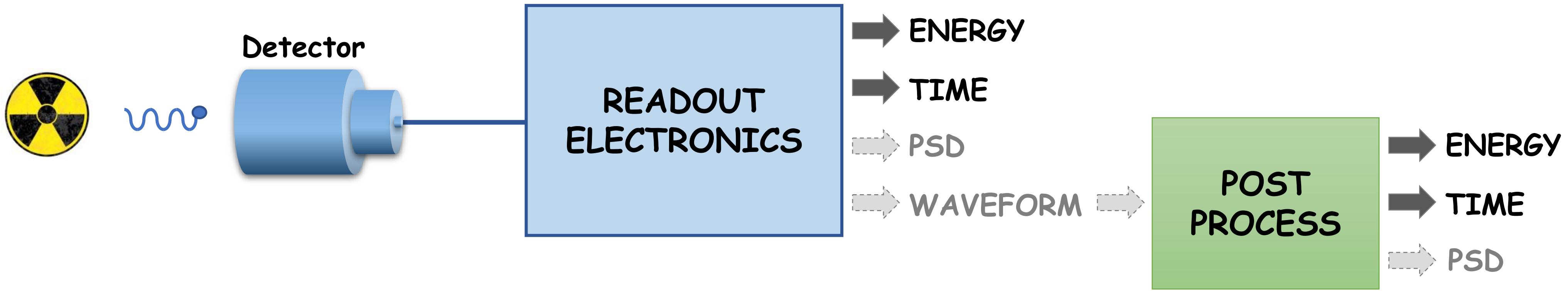
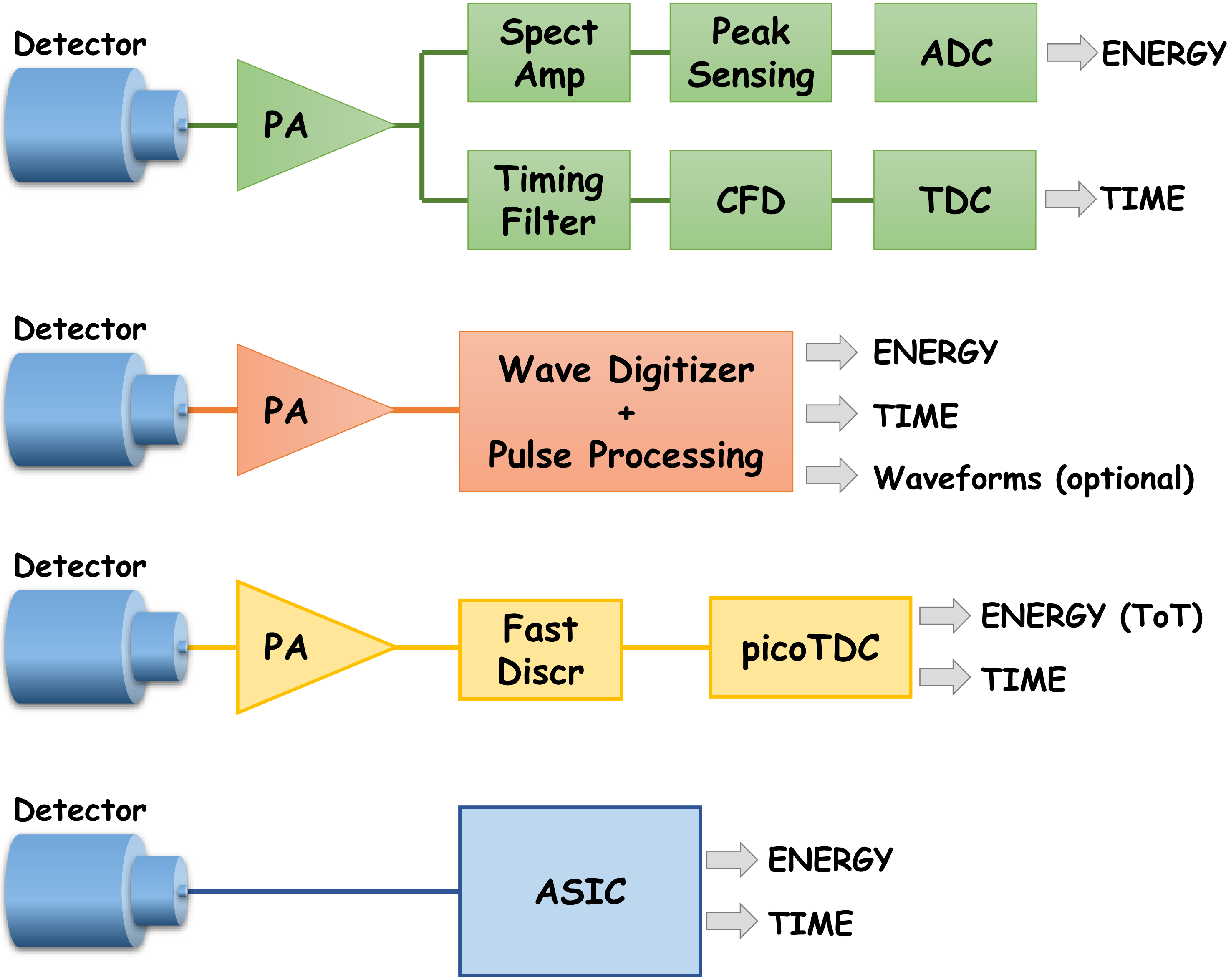
Workshop on Superconducting Electronics and Detectors
JLAB, November 29th, 2022

Detector Readout:

- In most cases, physics experiments require Energy (= charge or amplitude) and Timing, sometimes Pulse Shape
- Analog electronics (including many ASIC chips) provide a direct measurement of Energy and Time, converted to digital by a (slow) ADC
- Waveform digitizers acquire series of raw samples that must be post-processed (either on-line in FPGA or off-line in the software) to extract Energy and Time. Fast detectors => fast ADC (GS/s)

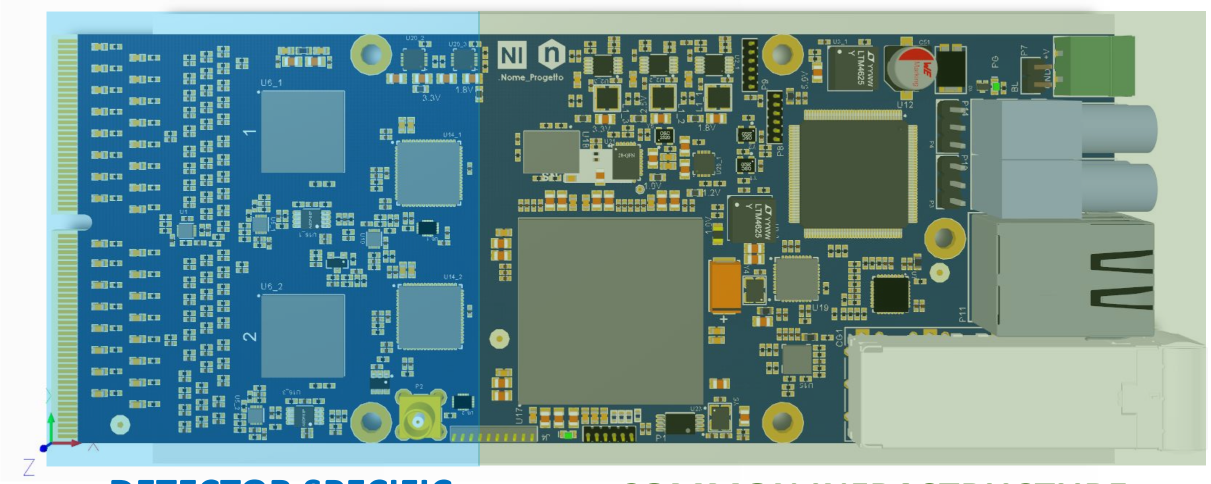


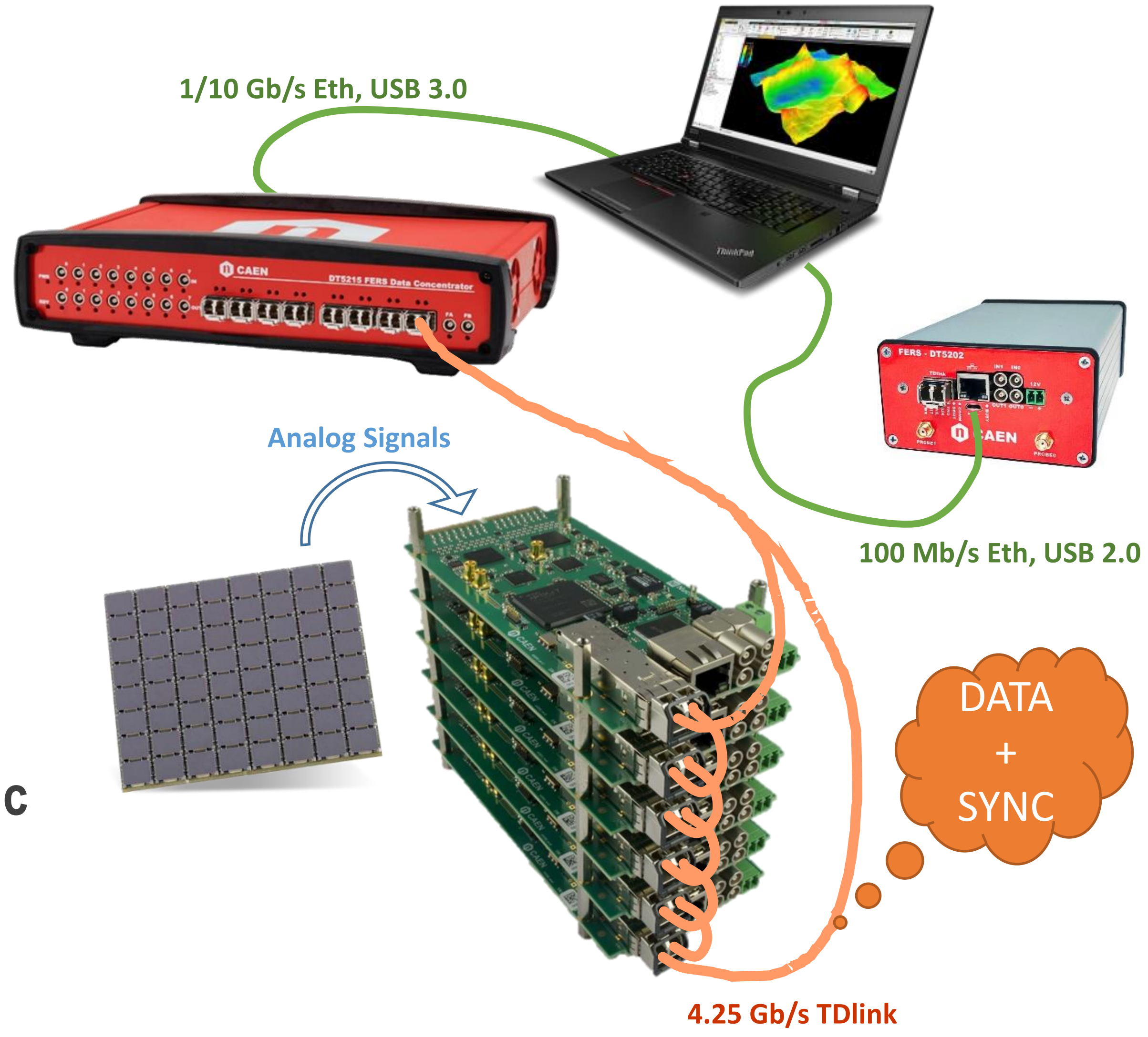
Readout chains



E-Res	T-Res	Cost	Flex	Rate	Notes
☺	☺	☹	☹	☹	• Power hungry • Bulky • Typ. high dead time • Old Stuff!
☺	☹	☹	☺	☺	• DPP algorithm tailored to application (FW upgrade) • fast detectors => high sampling rate => high cost • Wave interpolation • Analog Shaping ???
☹	☺	☺	☹	☺	• Need fast discriminators • Walk correction by ToT • Energy calculation by ToT • Pulse shape dependent => algorithm training
☺	☺	☺	☹	☺ ☹	• Low power, small size • Mounted close to detectors • Low cost but… • Need custom infrastructure • May need ext. ADC/TDC • Specific ASIC => no flexibility

FERS: a scalable readout system

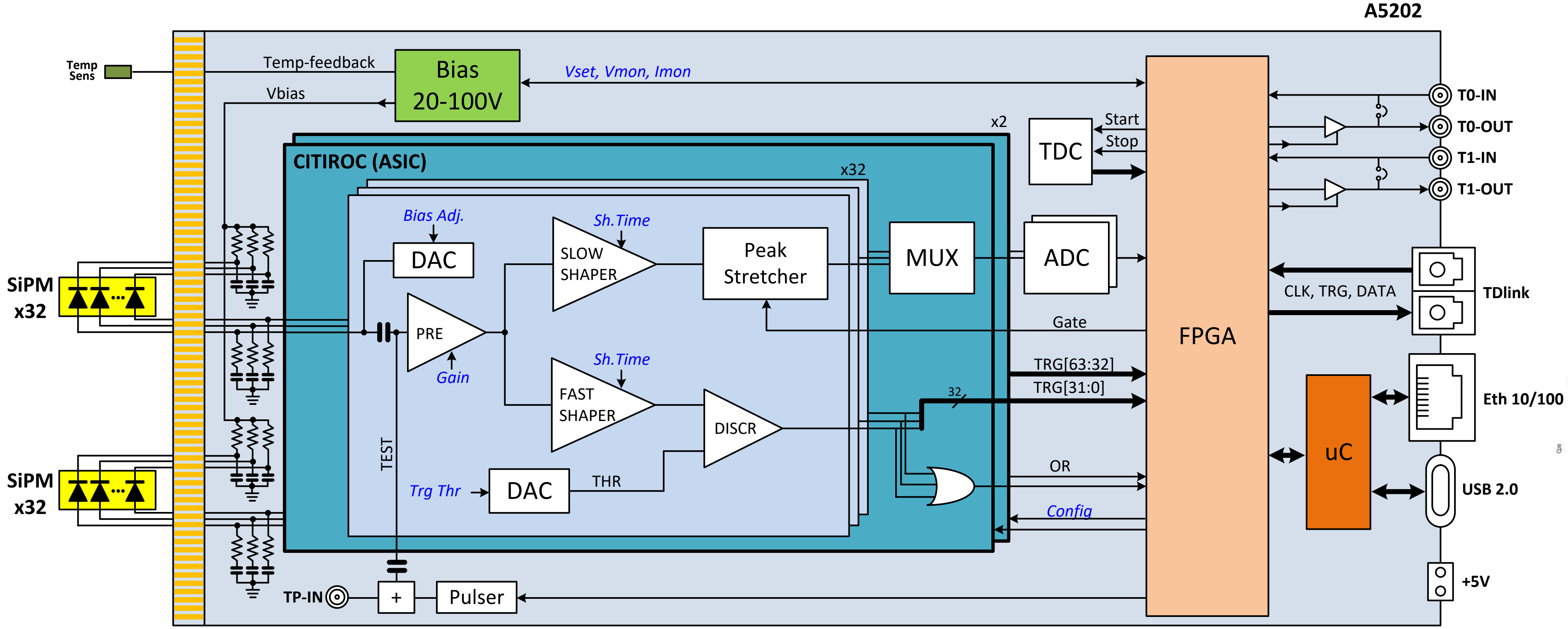


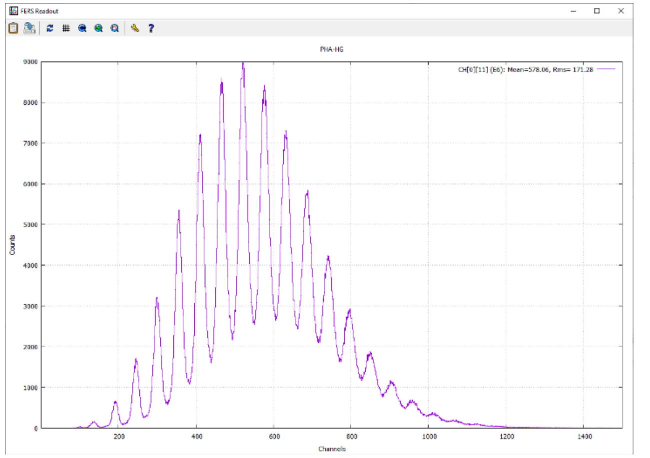


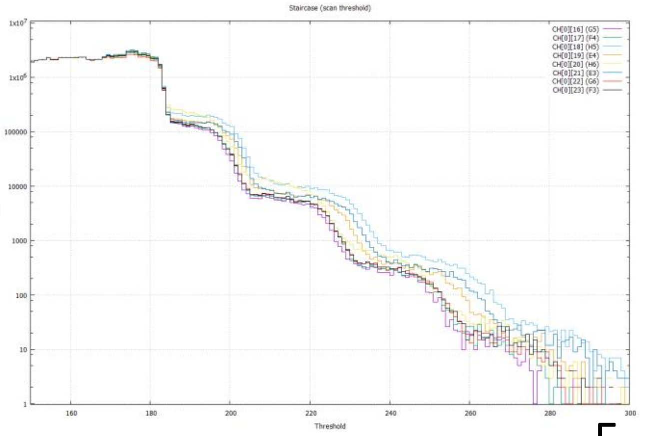
- **FERS:** Front End ASIC + ADC/TDC + Scalable Readout Infrastructure
- Easy **integration** of new ASICs
- **Scalability:** from single stand alone version for evaluation, to 10k/100k channels with same electronics
- **TDL:** daisy chainable optical link protocol with **data+sync**
- **Readout Tree:**
  1 link = 16 FERS units
  1 Concentrator = 8 links = 128 FERS = 8k/16k channels
  Multiple Concentrators for unlimited readout…

FERS A5202: 64 ch SiPM readout

- Based on **Citiroc** ASIC (Weeroc)
- Preamp, Fast shaper + Discrim, Slow shaper + Peak Sensing + Mux ADC
- Programmable gain (up to 600) and shaping time (up to 82.5 ns)
- High Voltage (up to 80 V) for SiPM biasing, with individual adjust
- Acq modes: spectroscopy (PHA), photon counting, timing list mode (ToA + ToT)
- Single photon detection (threshold at 1/3 p.e.)
- Timing resolution = ~0.3 ns RMS



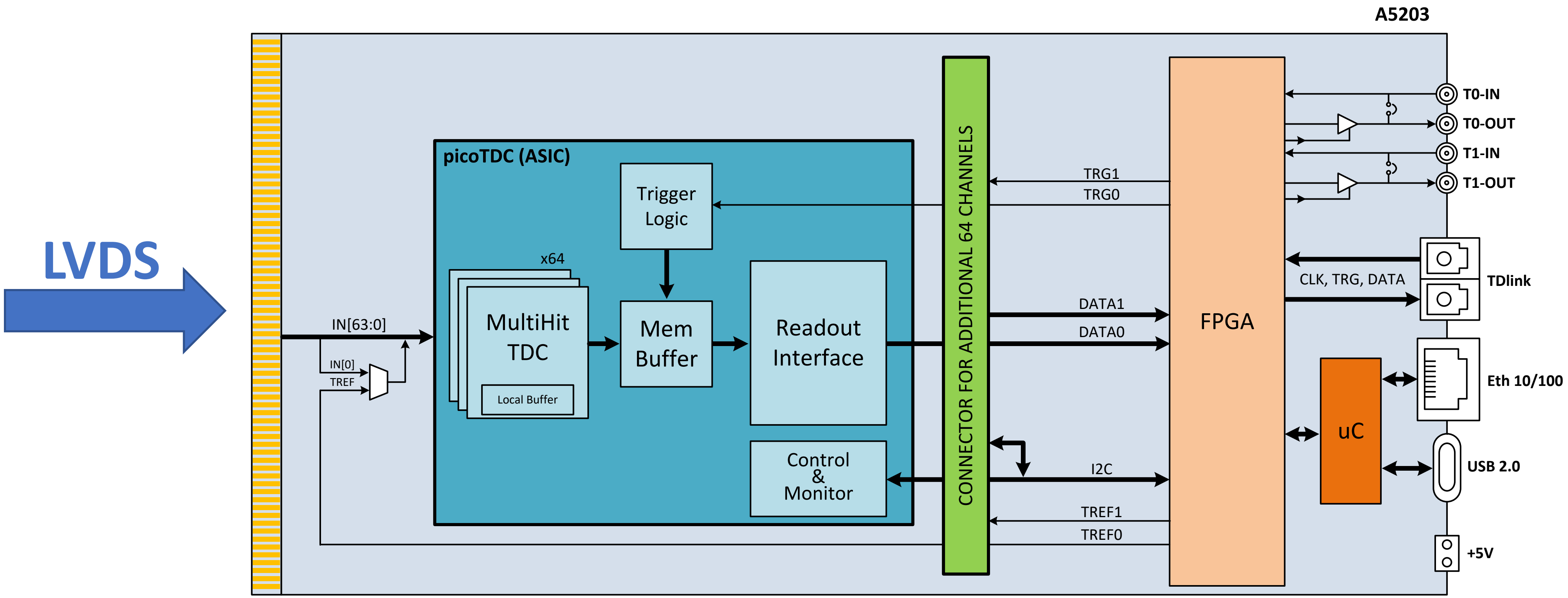




FERS A5203: 64/128 ch TDC (LSB = 3 ps)

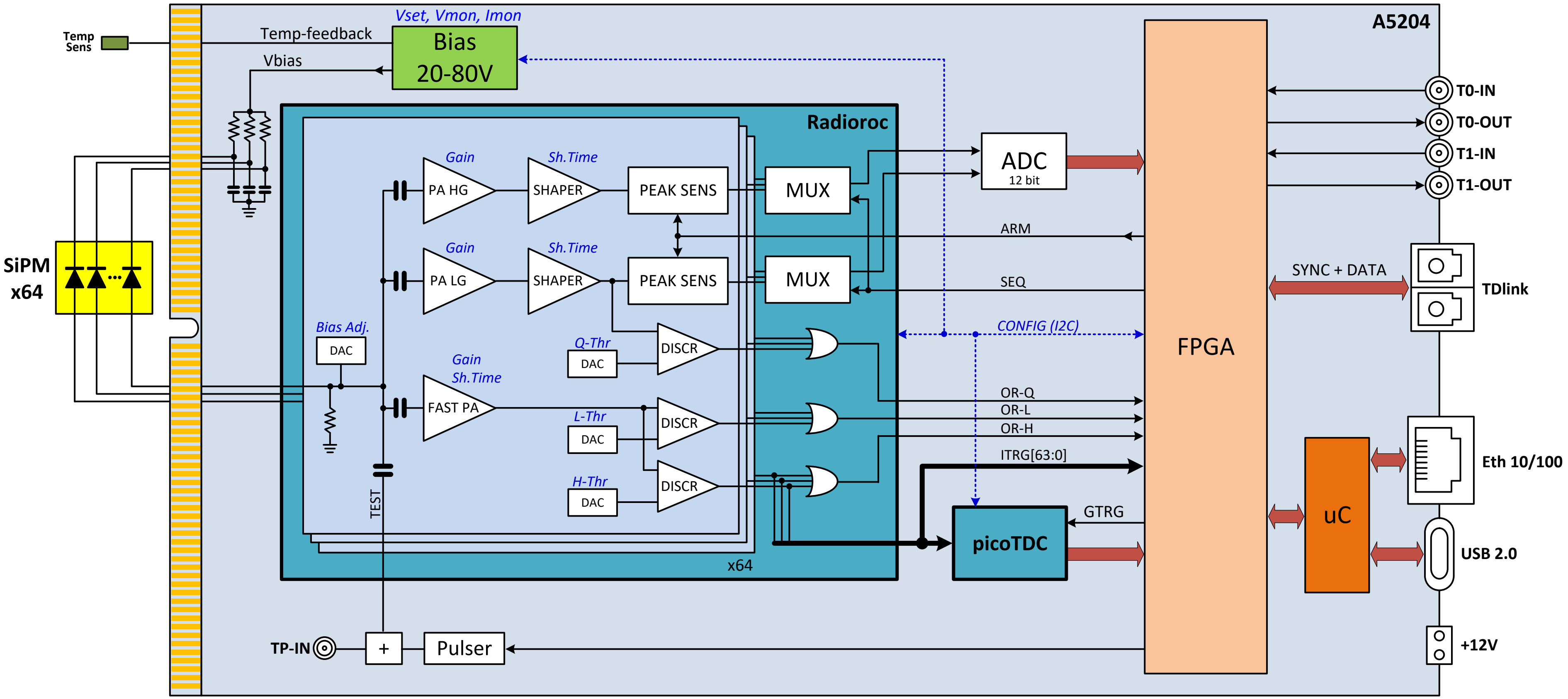
CAEN Tools for Discovery

- Based on **picoTDC** ASIC (CERN)
- Start-Stop timing resolution = ~5 ps RMS (tested with pulser, 0.8 ns rising edge, 1 Vpp)
- Acq. modes: Common Start, Common Stop, Trg. Matching, Streaming
- Leading/Trailing edge or Leading + ToT
- Extension board (A5256) with fast discriminators (16+1 channels)



FERS A5204: 64 ch SiPM Readout with picoTDC

- Based on **Radioroc** (Weeroc) and **picoTDC** (CERN)
- Acq modes: spectroscopy (PHA), photon counting, timing list mode (ToA + ToT)
- Improved timing resolution: 55 ps FWHM on a single p.e.
- Counting rate up to 200 Mcps
- Gain up to 80, Shaping Time up to 1.2 µs



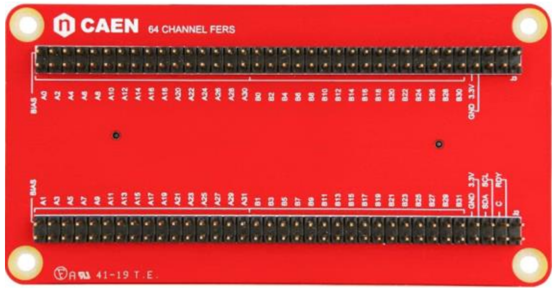
FERS A5205: 64 ch SSD, GEM Readout with picoTDC

- Based on **Psiroc** (Weeroc) and **picoTDC** (CERN)
- Same PCB of A5204
- Best suited for Silicon Strip Detectors (SSD), GEM, PIN Diodes
- Gain: from 0.125 mV/fC up to 4 mV/fC
- Shaping time from 20 ns to 3 µs
- Min trigger threshold = 0,5 fC
- Accepts both Positive and Negative inputs
- Dynamic range up to 5 pC with PHA or 100 pC with ToT
- Timing res = 150 ps RMS @ Q_{IN}=4 fC

- **Linearized ToT allows for high-resolution energy and ps timing, even at high rate and independent channels!**

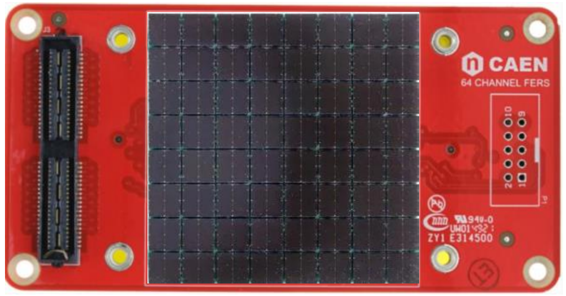
FERS Adapters and Cables

A5250: 2.54 mm Headers



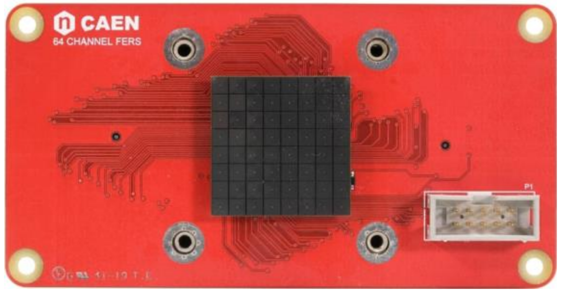
A5260: remotization cable

A5254: OnSemi Array-J Adapter



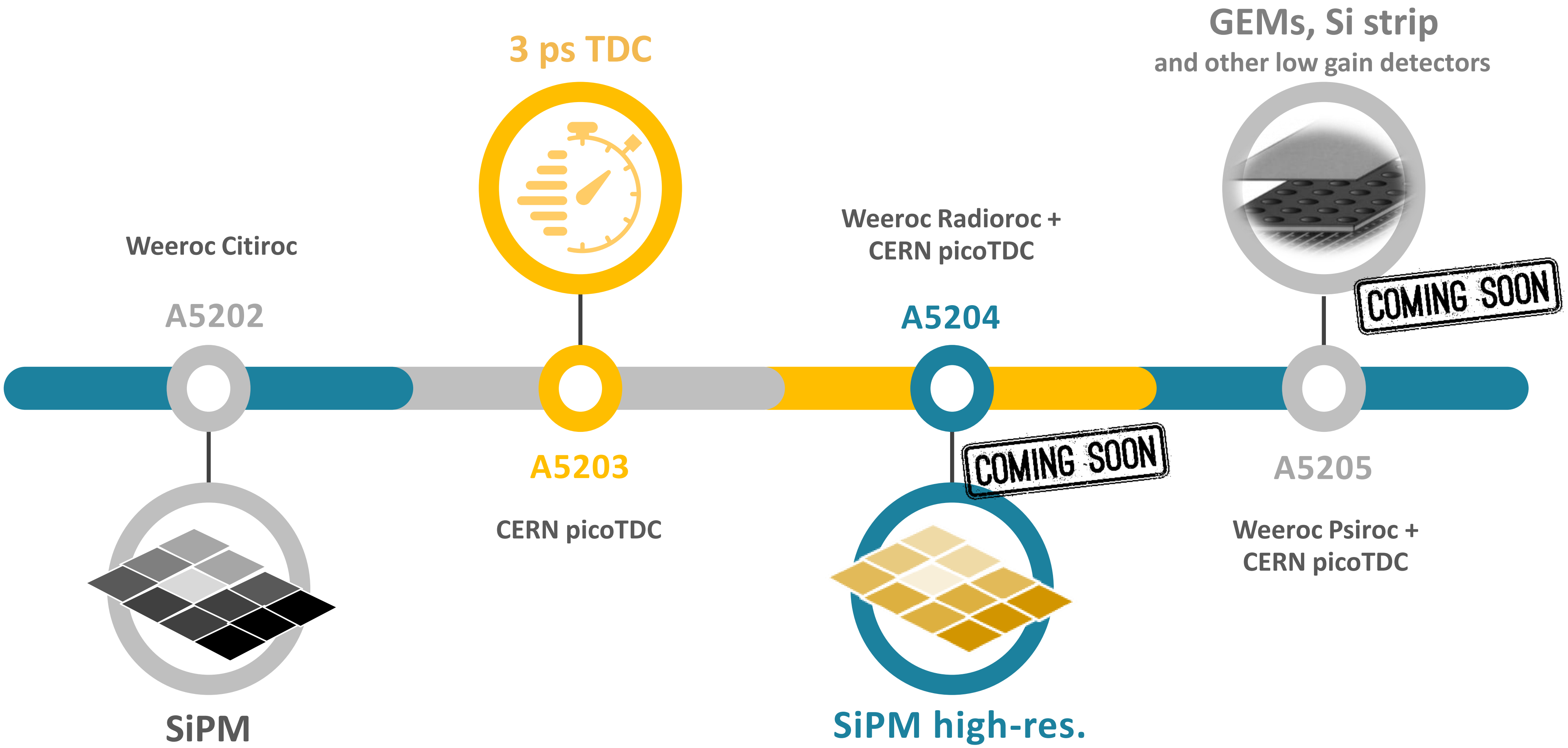
A5253: sparse SiPM cabling

A5251: Hamamatsu MPPC Adapter



A5256: 16+1 Fast Discriminators

FERS roadmap



Candidates for next FERS: SAMPIC (waveform based TDC)

- Developed at CEA/LAL (Paris)
- Best suited for SiPM, Diamond, MCP, APD
- Switched Capacitor Array (64 samples)
- Up to 10 GS/s sampling rate
- Embedded ADC, ~1 µs Conversion Time
- Ping-pong for low dead-time
- Independent channel readout
- Energy by waveform readout or ToT
- 16/32/64 channel eval board available

SAMPIC	
CHANNELS	16
SCA DEPTH	64 cells
SAMPLING RATE	3-8.4 (10.2 for 8 ch) GS/s
BANDWIDTH	1.6 GHz
DYNAMIC RANGE	1 V
ADC RESOLUTION	8-11 bit
CONVERSION TIME	0.2 µs @ 8 bit 1.6 µs @ 11 bit
READOUT TIME	25 + (6.2/sample) ns
SCA NOISE	1.3 mV RMS
TIME RESOLUTION	< 5 ps RMS
POWER CONSUMPTION	180 mW (1.8 V supply)

Candidates for next FERS: Nalu SCA ASICs

- Switched Capacitor Array, up to 2 GS/s
- CAEN-Tech is NALU representative in U.S.

	ASOC V3	AARDVARC V3	AODS V1	HDSOC V1
CHANNELS	4	4-8	1-4	32/64
SCA DEPTH	16K	32K	16K	2K
BANDWIDTH	0.8 GHz	2 GHz	0.5 GHz	1 GHz
TIMING RESOLUTION	35 ps	4-8 ps	<100 ps	<100 ps
SAMPLING RATE	2.4-3.6 GS/s	10-14 GS/s	1-2 GS/s	1-2 GS/s
APPLICATIONS	General Purpose ToF measurement	Accurate timing measurement	High Dynamic range Spare detectors	High Density SiPM readout
FEATURES	Low cost	High Performance High timing resolution	Variable gain stages Flexible serial interface	Internally configurable triggering schemes

Other candidates for next FERS

DRS4

VMM3

SAMPA

TEMPOROC

LIROC

GET

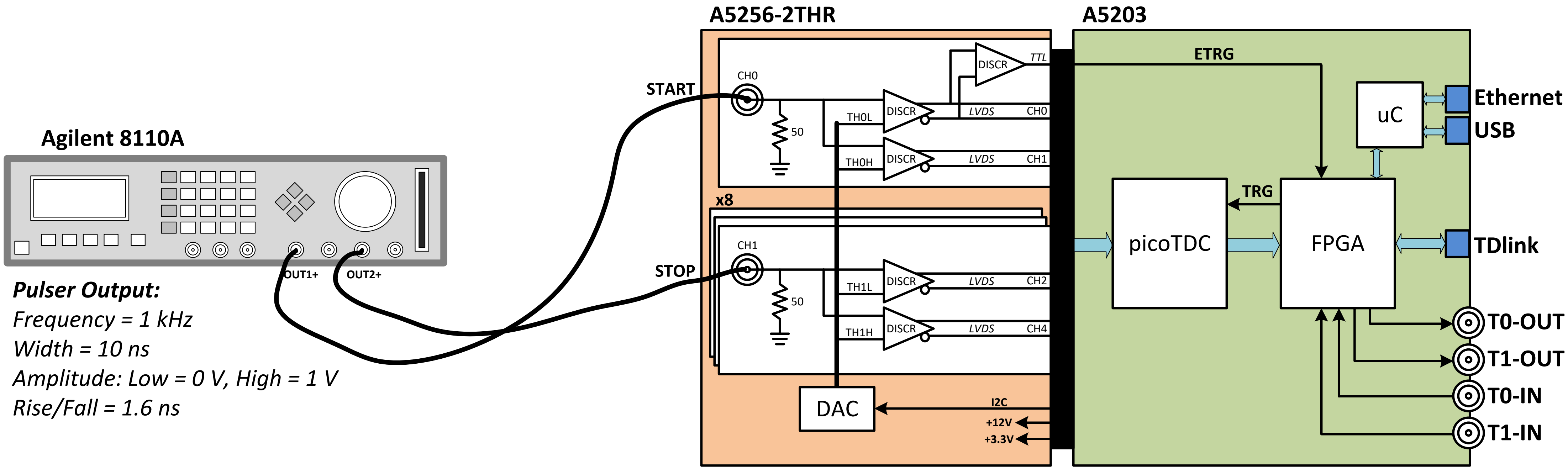
picoTDC: Timing Resolution with fixed amplitude

Setup:

A5203: 64 ch. picoTDC

A5256: 8+1 ch. Dual Threshold Fast Discriminator

A8110A: Dual Pulse Generator



Pulser Output:

Frequency = 1 kHz

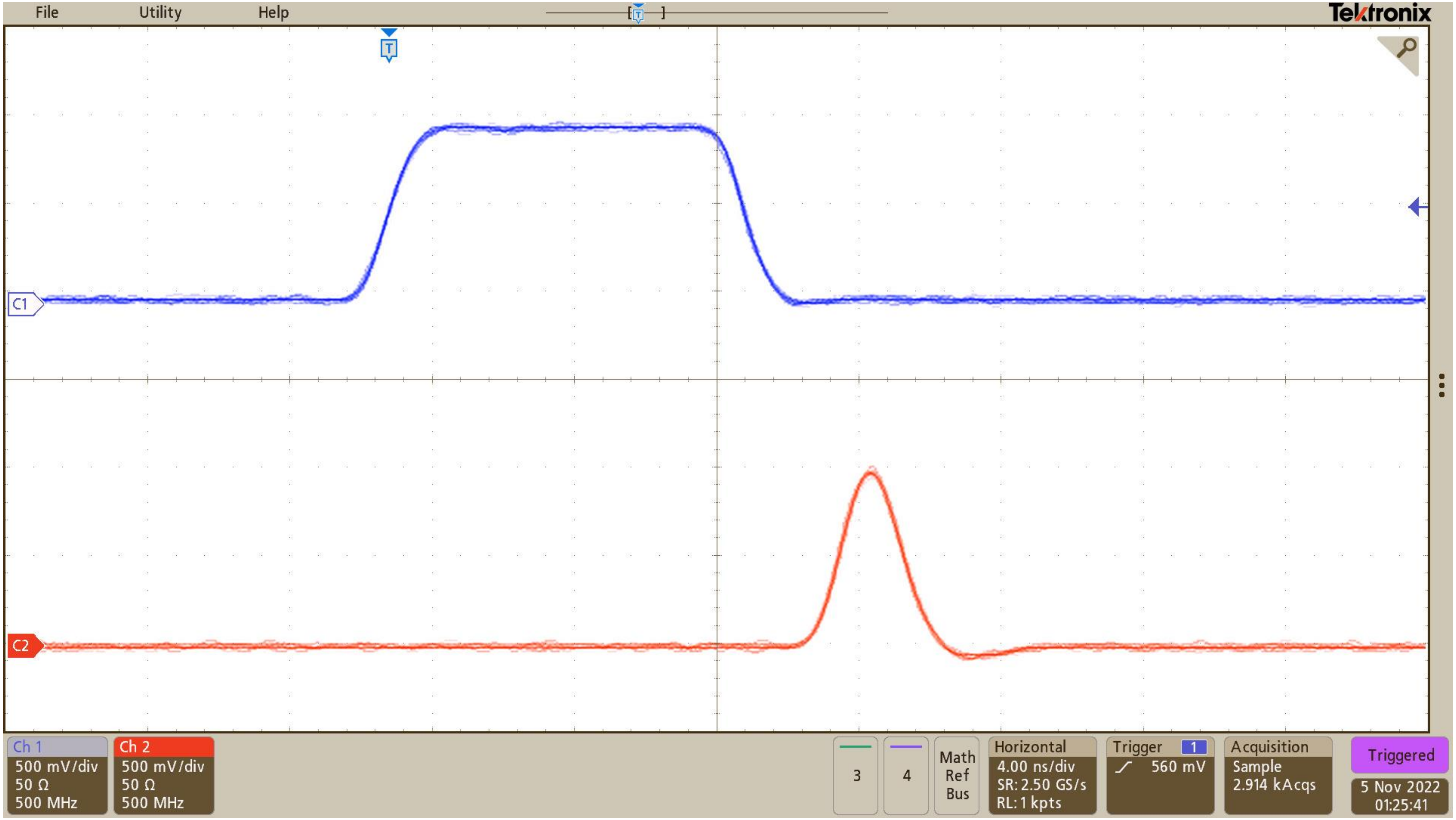
Width = 10 ns

Amplitude: Low = 0 V, High = 1 V

Rise/Fall = 1.6 ns

	Low Thr		High Thr	
	Mean	RMS	Mean	RMS
deltaT (start-stop)	4.7 ns	5 ps	4.9 ns	6 ps
ToT	10.6 ns	6.5 ps	10.2 ns	5.5 ps

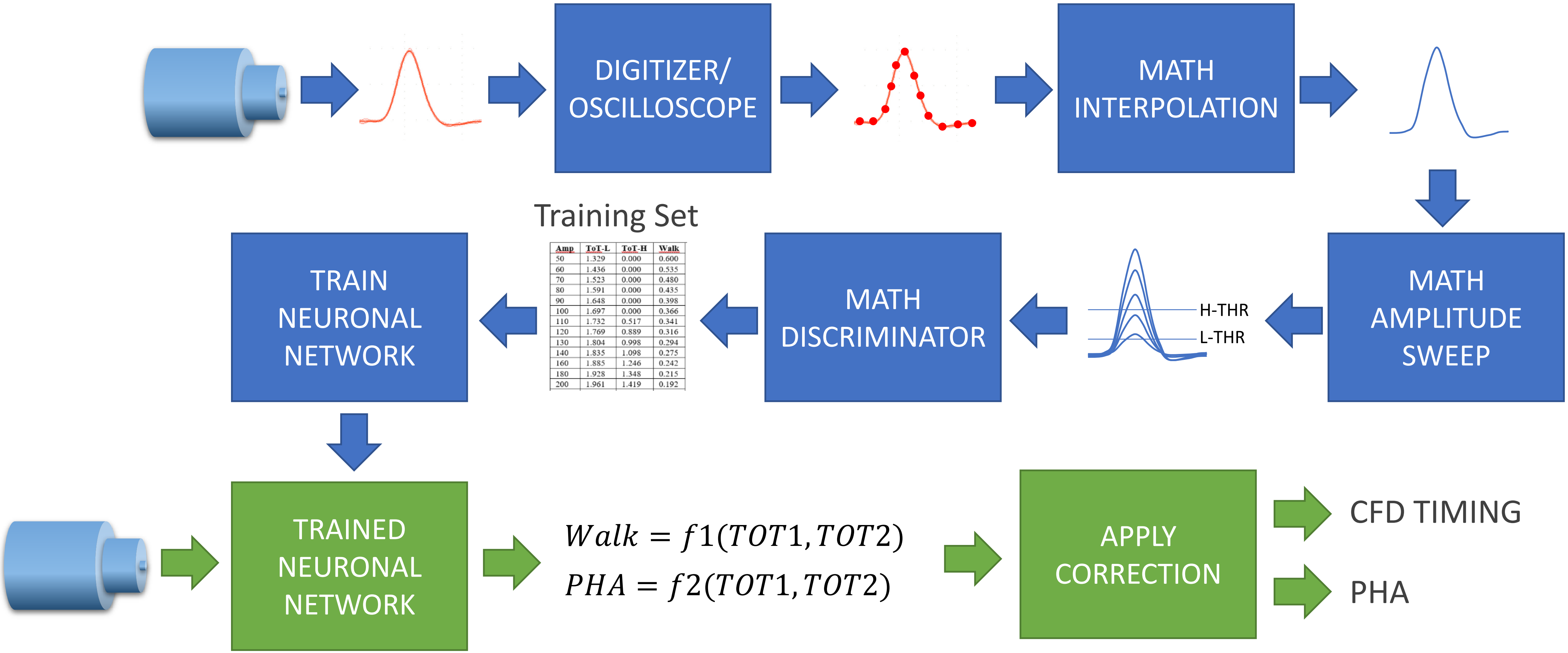
Pulses



File
Utility
Help
Tektronix
C1
C2
Ch 1
500 mV/div
50 Ω
500 MHz
Ch 2
500 mV/div
50 Ω
500 MHz
3
4
Math
Ref
Bus
Horizontal
4.00 ns/div
SR: 2.50 GS/s
RL: 1 kpts
Trigger 1
560 mV
Acquisition
Sample
2.914 kAcqs
Triggered
5 Nov 2022
01:25:41

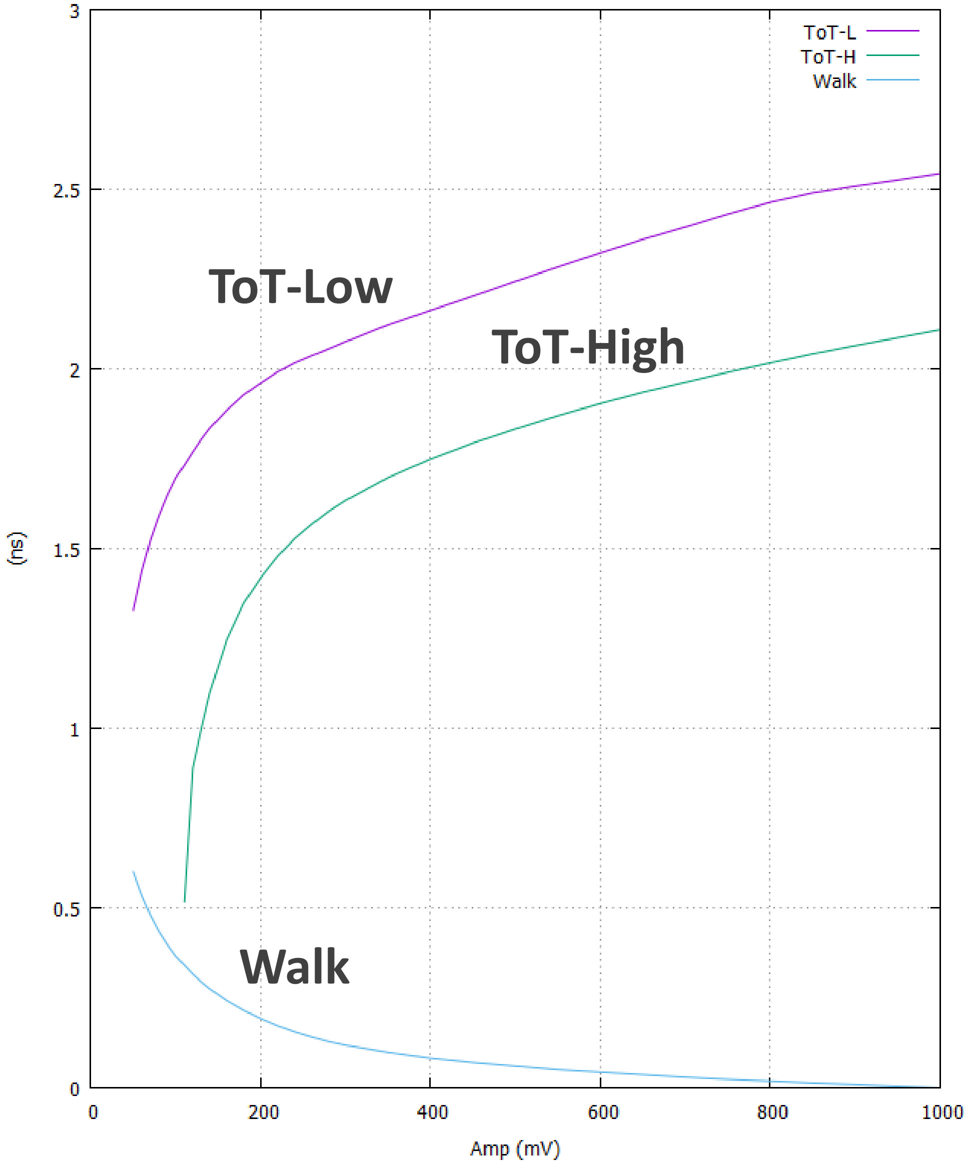
ToT for Walk correction (CFD) and PHA

Need to find an algorithm that estimates Walk (for CFD timing) and Amplitude (for PHA) from the ToT.
Two thresholds (dual ToT) improve resolution at the cost of doubled channels



Amp	ToT-L	ToT-H	Walk
50	1.329	0.000	0.600
60	1.436	0.000	0.535
70	1.523	0.000	0.480
80	1.591	0.000	0.435
90	1.648	0.000	0.398
100	1.697	0.000	0.366
110	1.732	0.517	0.341
120	1.769	0.889	0.316
130	1.804	0.998	0.294
140	1.835	1.098	0.275
160	1.885	1.246	0.242
180	1.928	1.348	0.215
200	1.961	1.419	0.192

$$Walk = f1(TOT1, TOT2)$$
$$PHA = f2(TOT1, TOT2)$$



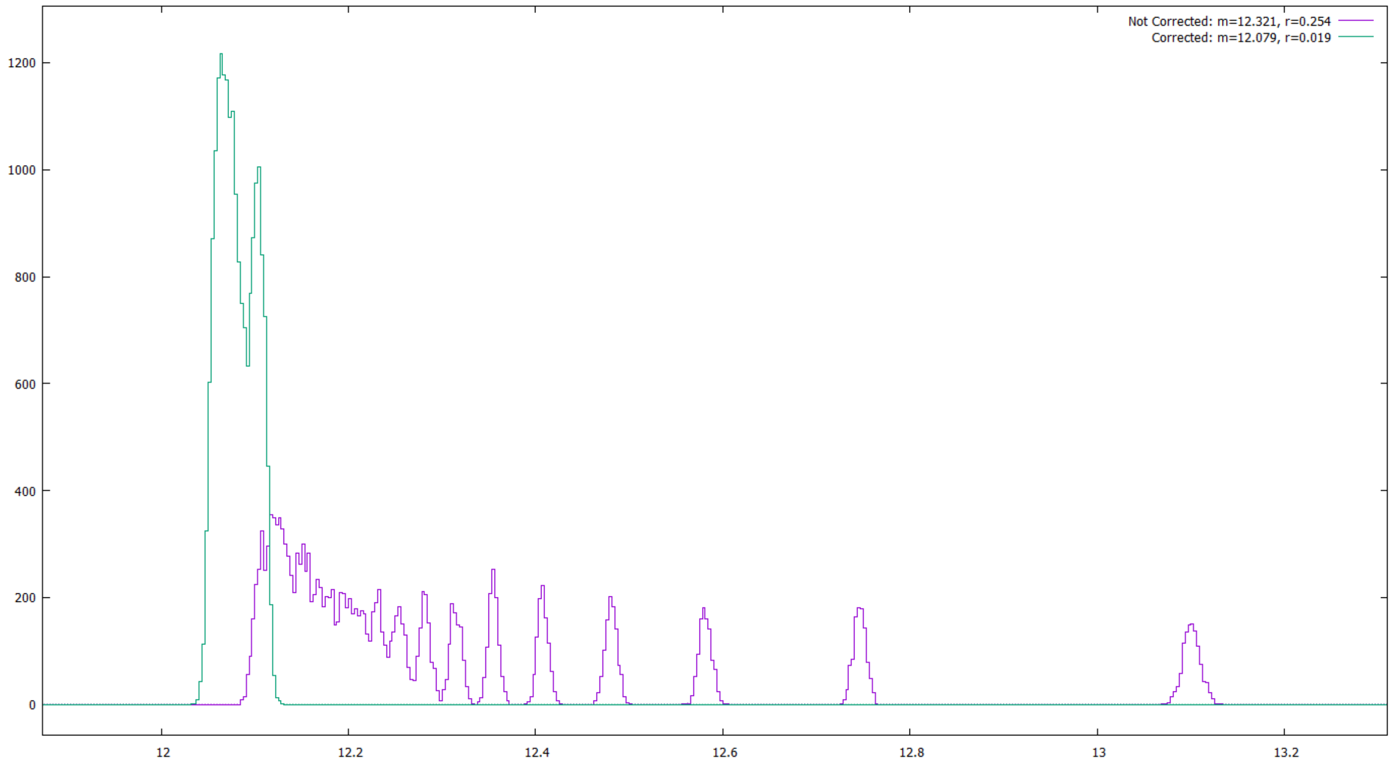
Amplitude Sweep from 50 mV to 1V:

Low Thr. = 30 mV, High Thr. = 300 mV

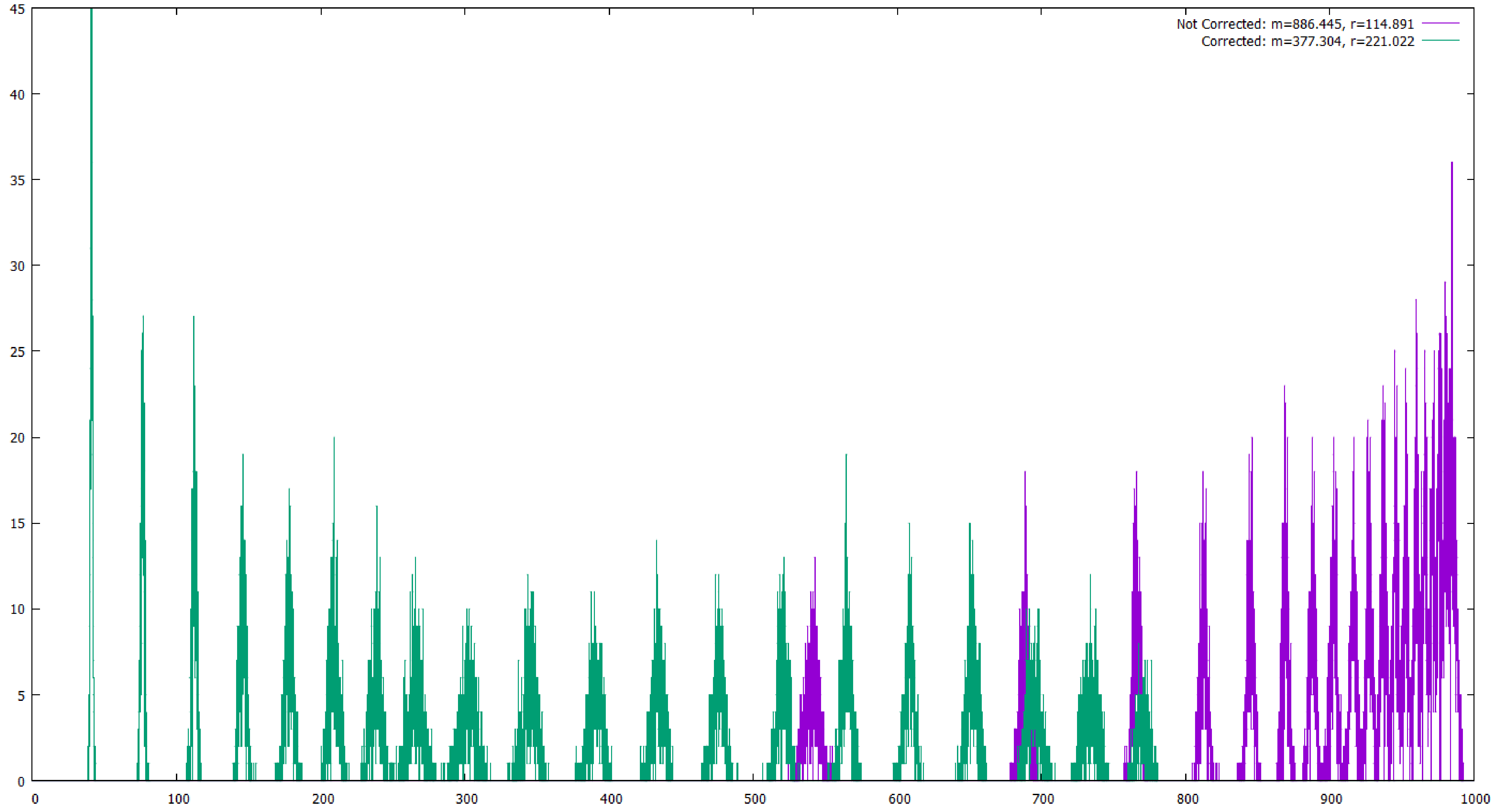
ΔT = 254 ps RMS (no correction)

Use sampled waveform to calculate Walk from ToT

ΔT = 19 ps RMS (after correction)



Amplitude reconstruction by ToT

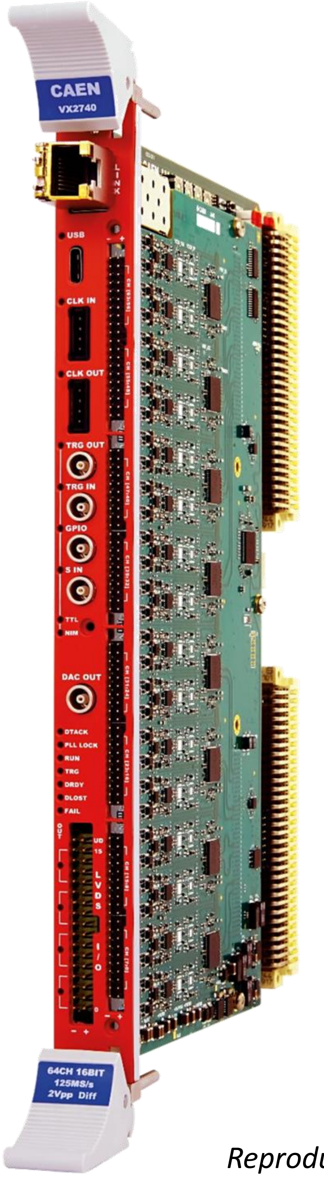


Waveform Digitizers: new series 2.0

CAEN
Tools for Discovery

VX2740/45:
64 ch, 125 MS/s, 16 bit

VX2730:
32 ch, 500 MS/s, 14 bit



- Form factors: VME64X, VME64 and Desktop
- **Inputs and Dynamic Range**:
  - V2740 → 2 V, DIFF or SE
  - V2745 → 40 mV ÷ 4 V (Gain: 0 to 40 dB, 0.5 dB steps), DIFF or SE
  - V2730 → 200 mV ÷ 4 V (Gain: 0 to 26 dB, 1 dB steps, t.b.d.), SE only
- **DC level** adjust (calibrated 16 bit DACs, channel by channel)
- **Readout** interfaces: 1/10 GbE, USB 3.1, Optical Link (up to ~ 300 MB/s)
- **DPP** functionalities: PHA, QDC, PSD, CFD, Zero Suppression
- **Open FPGA** to provide flexibility in the pulse processing algorithm
- Embedded Linux **ARM**

Waveform Digitizers: roadmap

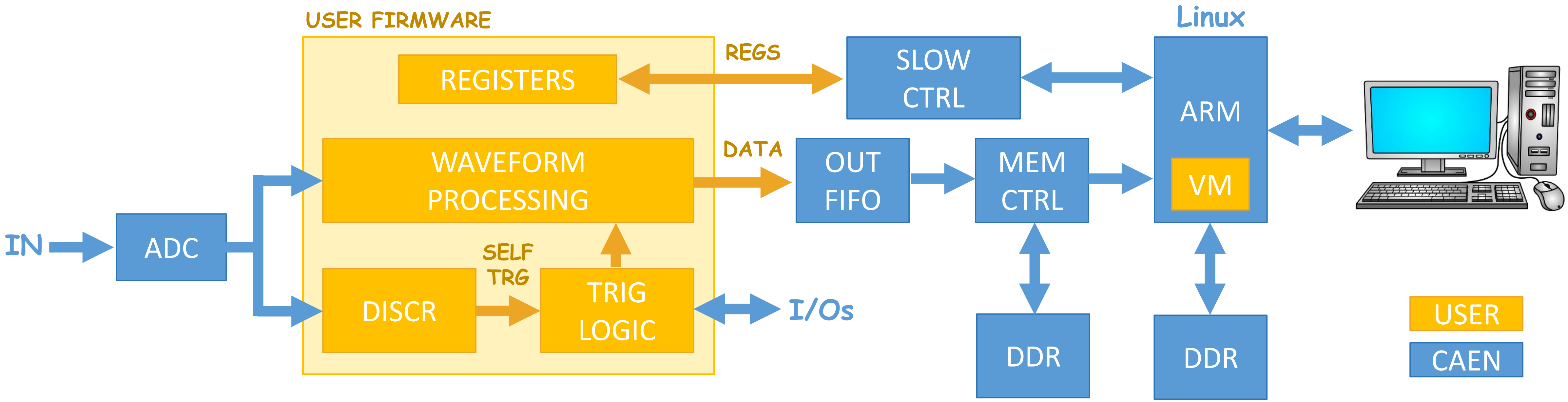
Available	Prototyping…	…2024	
VX2740/45 64 channels 125 MS/s 16 bit	**VX2730/25** 32 channels 500/250 MS/s 14 bit	**VX2751** 16 channels > 1 GS/s 14 bit	**and others…**

We provide infrastructure: ADC data flow, data buffering and transfer, slow control

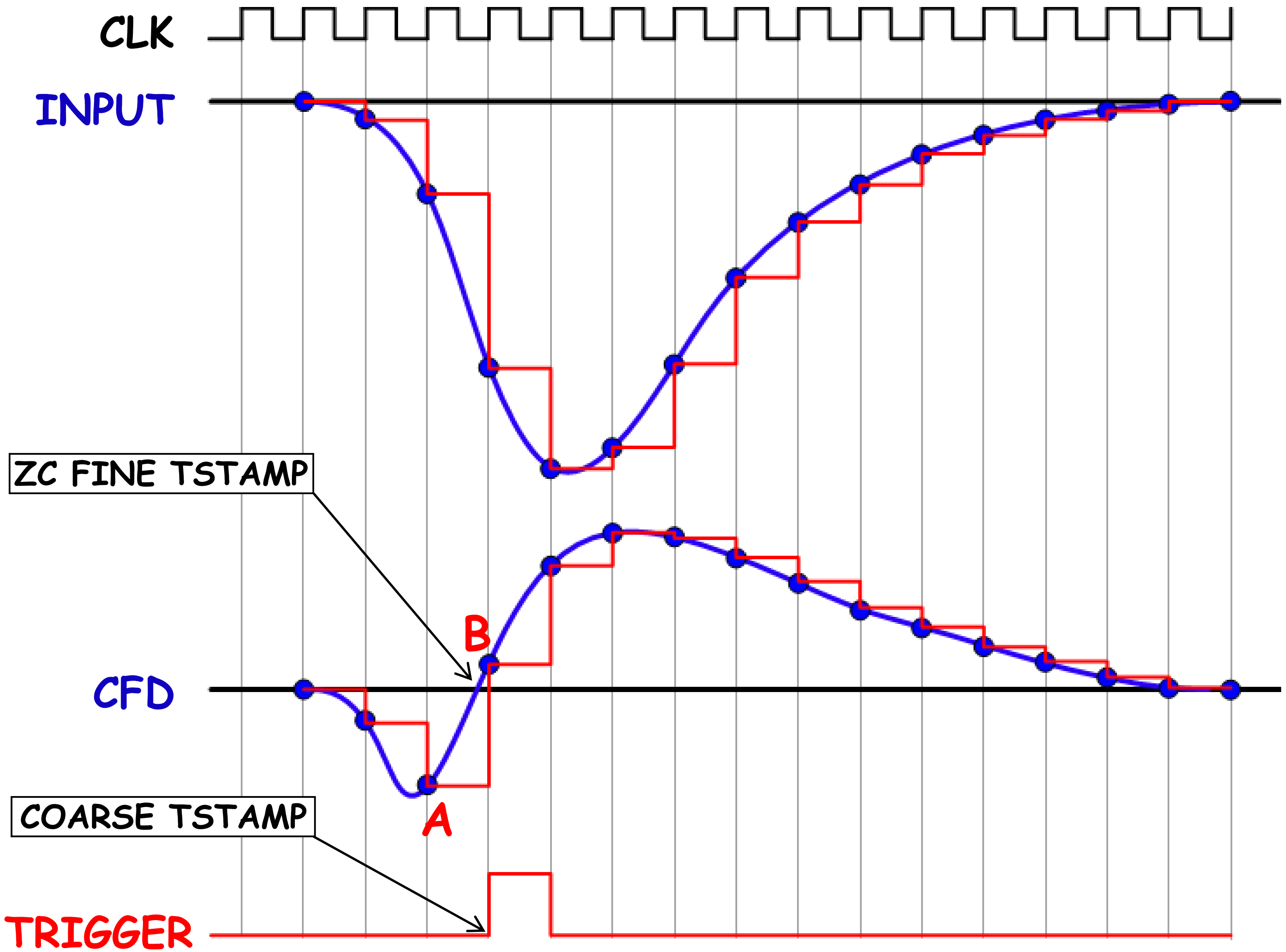
You implement your algorithms for data processing, parameter extraction and trigger logic

Sci-Compiler: graphical FPGA programming tool with precompiled modules (logic, filters, …)

FDK: FW development kit with VHDL templates, simulation models, signal inspection, etc.



Digital CFD with interpolation



digital CFD: same principle as analog

$$CFD_{N+1} = f * S_N - S_{N-D}$$

f = Fraction, D = delay

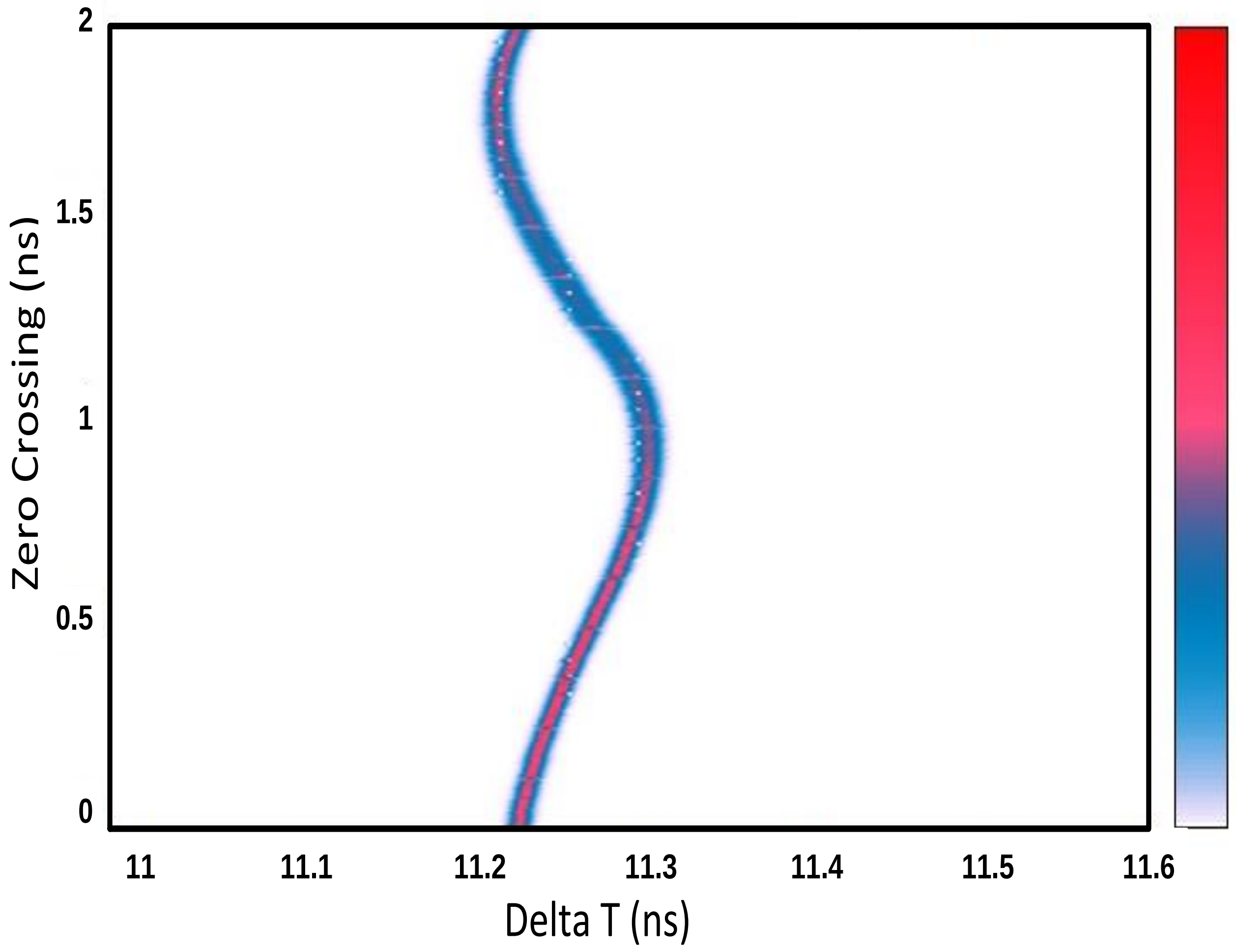
COARSE TSTAMP = T_{CLK} * Clock Counter
FINE TSTAMP = Interpolation between A and B

Linear Interpol.: ZC = T_{CLK} * B/(B-A)
Need 3/5 points on the rising edge to keep the interpolation error low => 5 GS/s for pulses with rising edge = 1ns

Curve fit (e.g. cubic): too complex for on-line FPGA calculation => need waveform readout

ZC correction LUT: increase timing resolution of the linear interpolation. Need algorithm training with real data.

ZC correction LUT



Test with V1730 (500 MS/s, 14 bit)

The linear interpolation between two samples provides the ZC fine time (0 to 2 ns)

Scatter plot: X = measured ΔT, Y = ZC fine time

The interpolation error generates a predictable **pattern**!

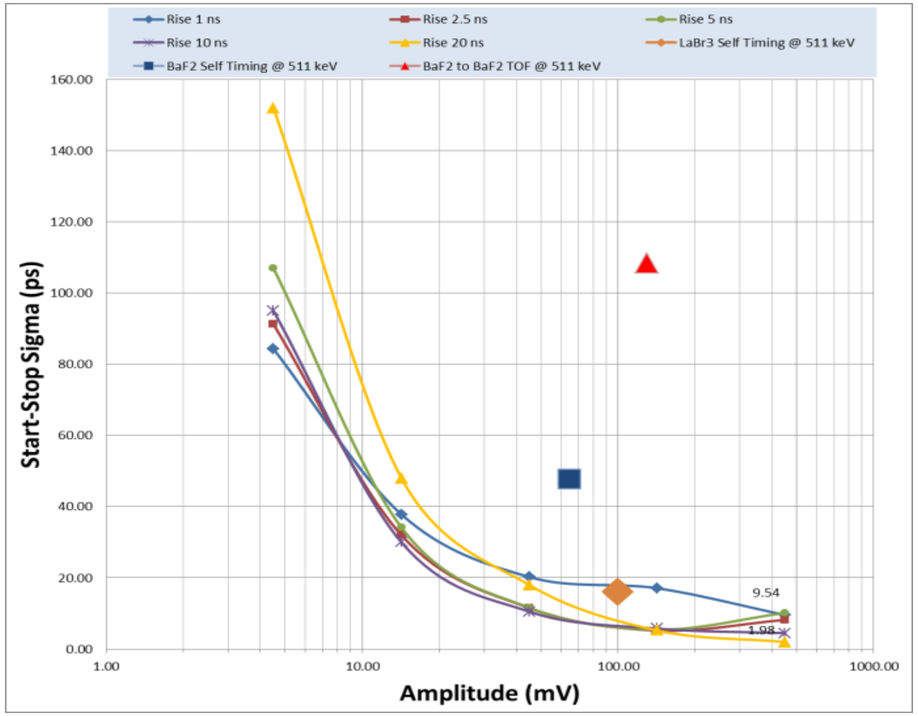
A correction LUT can be created to compensate for the interpolation error

Need calibration run with real pulses to fill the LUT

Test Results with V1730: 500 MS/s, 14 bit digitizer

CAEN Tools for Discovery

Test	Rise Time	Amplitude	ZC corr	Start-Stop Resolution	
				RMS	FWHM
Pulse Generator	1 ns	450 mV	✓	9.5 ps	22 ps
Pulse Generator	5 ns	450 mV	✓	10.1 ps	24 ps
Pulse Generator	20 ns	450 mV	✓	1.9 ps	4.5 ps
BaF_2 to BaF_2	1.3 ns	130 mV	✓	120 ps	280 ps
BaF_2 to BaF_2	*1.3 ns*	*130 mV*	✗	*538 ps*	*1.3 ns*
BaF_2 to $LaBr_3$	1.3/15 ns	130/200 mV	✓	186 ps	437 ps
NaI to NaI	20 ns	100 mV	✓	1.02 ns	2.40 ns



Single Detector Resolution				
Detector Type	Size	PMT	T_{RES} (FWHM)	Notes
BaF_2	1"	H3378-51	200 ps	
$LaBr_3$	2"	R6231	~ 400 ps	extrapolated from BaF_2 to $LaBr_3$ Timing
NaI (Tl)	2"	ETL 9266	1.7 ns	


Thank you
for your
attention
Any question/curiosity?