Cryogenics ASICs at Fermilab

Davide Braga
on behalf of the ASIC Department

Growth of IC design over 3 decades

DOE HEP builds and operates among the most difficult and biggest projects with the most complex detectors in science.

These experiments operate in **extreme environments** which require robust custom microelectronics with long-term reliability over decades

Since 1980's

Ionizing radiation
>1 Grad (1000x higher than outer space)
Extreme flux for single event upsets
- Collider Experiments (FCC, HL LHC)

Since 2010's

Cryogenic electronics (77K – 100K)
- Neutrino experiments (DUNE), Dark matter experiments (Skipper CCDs)

Since 2019

Deep Cryogenic electronics (~ 4K)
- Dark matter experiments (Cryogenic detectors e.g. SNSPDs, TES etc.), Quantum Information Science

Superconducting electronics (~100 mK)
- Quantum Information Science (TWPAs, JPAs for ADMX)

New 2022

Fermilab

Structure and Partnerships

University Partnerships

(ECE departments)

- Northwestern U.
- Columbia U.
- Purdue U.
- Washington U.
- UIC, UIUC
- University of Washington
- Stonybrook University
- EPFL
- and several other physics departments

Industry Partnerships

- Microsoft
- Global Foundries
- Synopsys
- Siemens
- Skywater
- Flex logix
- Caporus Technologies
- Nhanced
- Qolab
- other SBIR companies ….

ASIC PMG

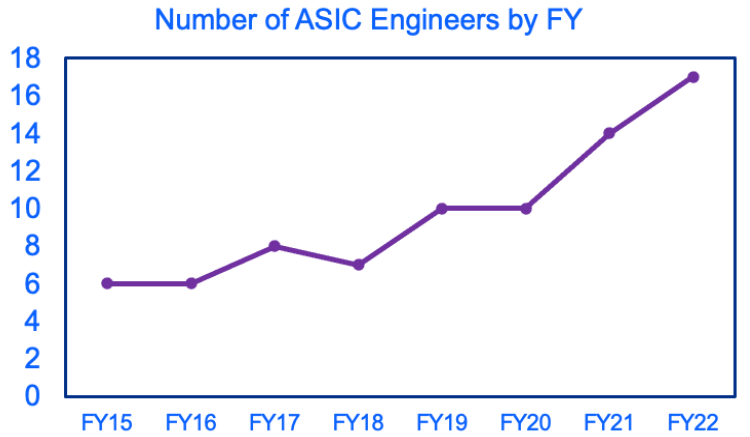
ASIC Groups

- Quantum and Analog Cryoelectronics
- Advanced Digital and Verification
- Ultrafast timing and Cross-cutting initiatives
- Testing and Tool support

- 19 ASIC designers (2 JA) + *1 open position*
- 1 PhD, 1 MS EECS student (Northwestern University)
- 1 scientist, 2 Application Physicist
- 1 test engineer, 1 engineering associate

Started ASIC Design Associate program for post BS, MS or PhD students in 2021 (3-6 months training program)

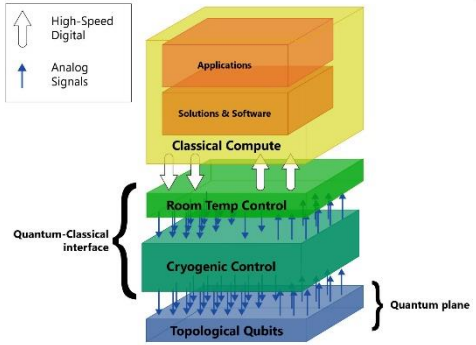
- 5 interns in 2021 (Carnegie Mellon, U. Toronto, Northwestern University)
- 4 interns (Stanford, Purdue U., U. Toronto, UTA)– HIRING 2 more interns in 2022



ASIC Design at Fermilab

FQI (HEP/ ASCR/DOD/NASA)

SCD (HEP / ASCR)

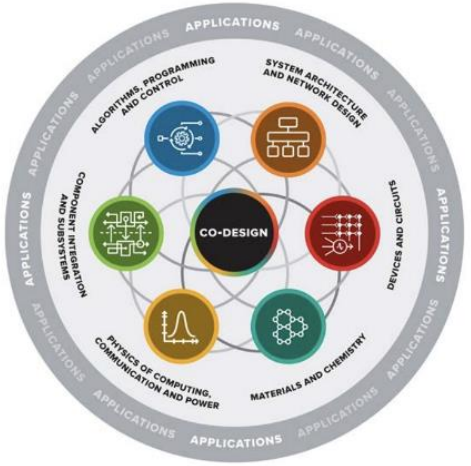


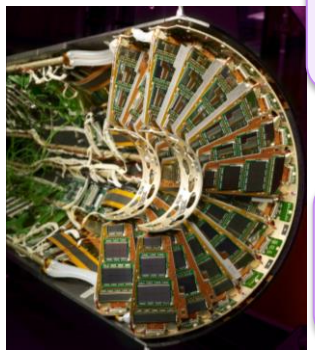
Quantum

Artificial Intelligence

OPTT

Technology Transfer





ND

HEP

PPD

Microelectronics Codesign

PPD, FQI, SCD, AD, etc. (HEP/BES/ASCR/NP/FES)

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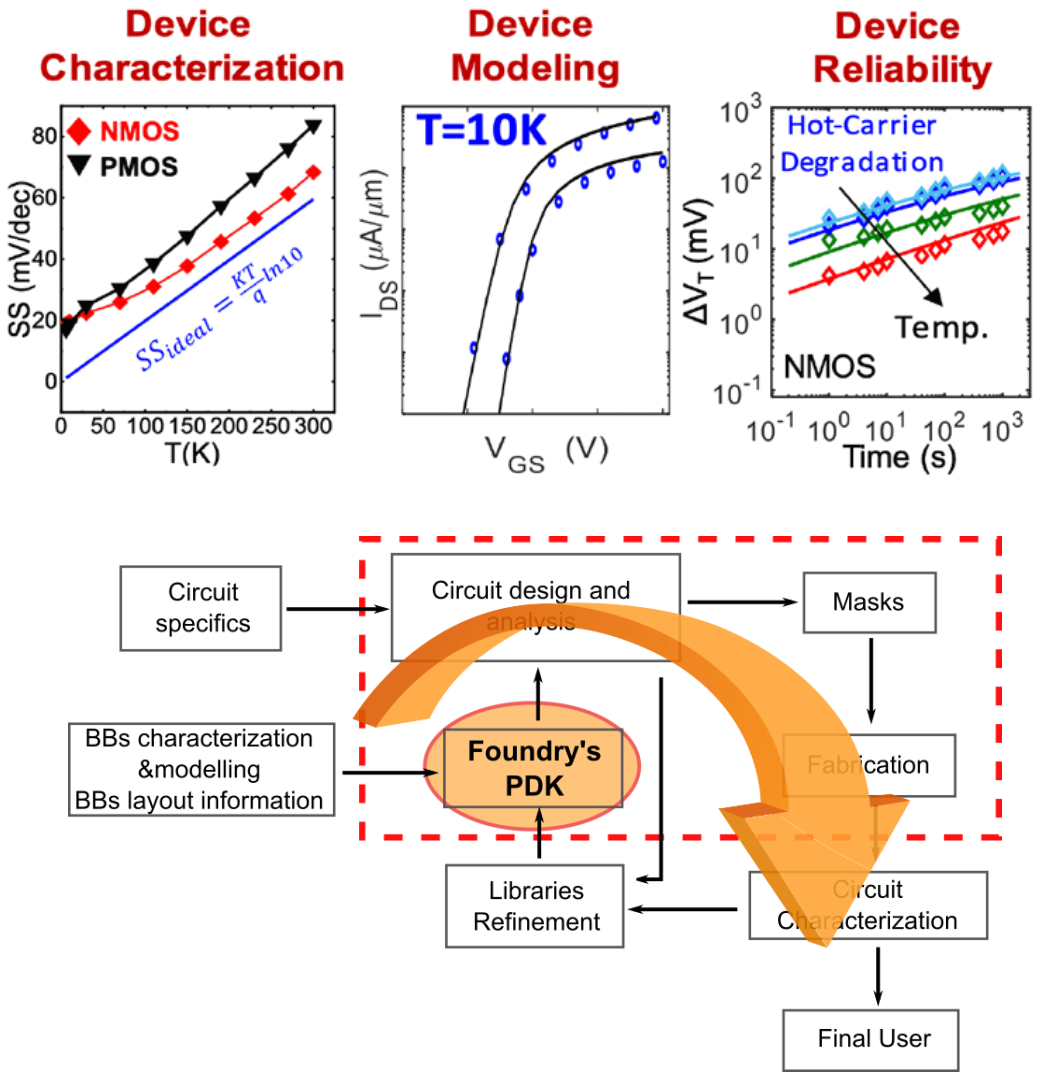
Support ASIC design community for extreme environment

- Extreme environment PDK development (collaboration with Foundries and CAD Tool companies)
- Modelling radiation tolerance / cryogenic behavior of the semiconductor process
- Develop SEE mitigation approaches

- Previously 65 nm: up to 1 Grad / 77K
- Current focus:

  GF 22 FDX below 4K;

  TSMC 28 HPC+ beyond 1 Grad



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Relevant expertise

- Radiation hardness techniques and processes
- Fast timing
- Photonics/electronics integration (collaboration with University of Washington)
- Edge Computing
- 3D integration

Cryo CMOS technologies and modeling

CMOS at cryogenic temperature

- Carrier freezeout avoided in modern CMOS processes (<160nm)
- Higher mobility
- Higher Threshold voltage
- Higher subthreshold slope
- at low VDS, the subthreshold region of the MOSFET transfer characteristics exhibits peaks and valleys due to Coulomb Blockade
- Mismatch increases
- Leakage drastically reduces
- Substrate can becomes floating

GF 22FDX Fully Depleted Silicon-on-Insulator

- **Advantages: Multi-technology platform**

  LDFET: Asymmetric high voltage transistors: Max Vds = 7V; Max Vgs = 2V

  BOXFET: Symmetric high voltage transistors: Max Vds = 5.5V; Max Vgs = 5.5V

  EGFETs: 1.8V transistors with additional back gate control

  FETs: 0.8V transistors with additional back gate control (HVT, NVT, LVT, SLVT) (excellent cryogenic performance)

  High density memory: SRAMs (0.5V option) / eMRAMs

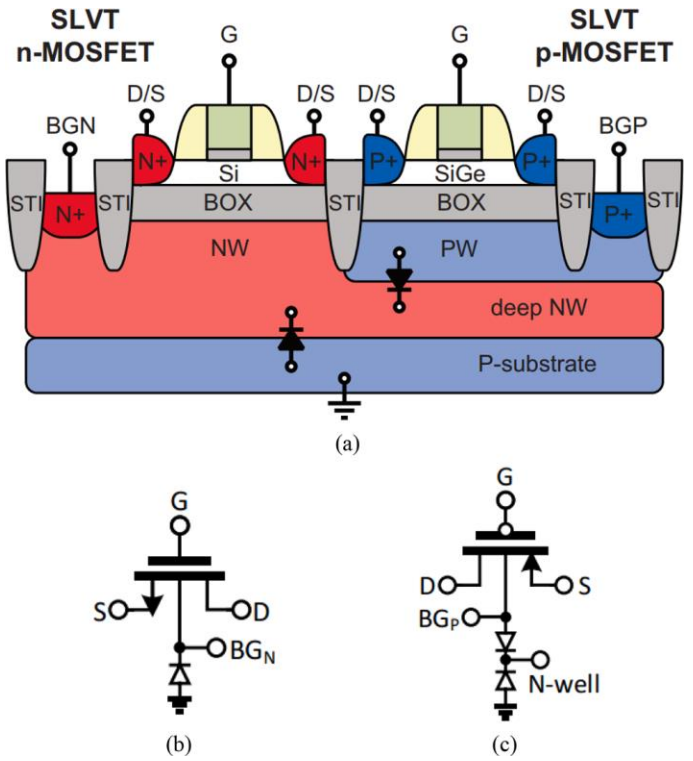
  Digital Power supply scaling 0.8V --> below 400mV: ULP- ultra low power performance

- **Performance/Power ratio:**

  Up to 50% more performance

  Up to 70% lower power

  (NOTE: All data as compared to bulk 22nm CMOS process)



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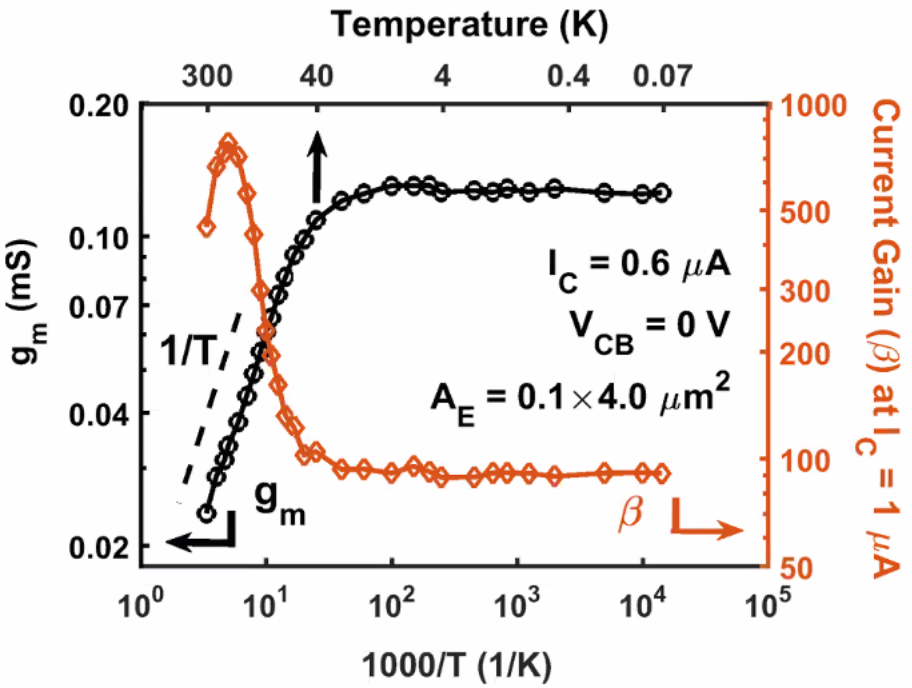
SiGe Heterojunction Bipolar Transistors (HBTs) at cryogenic temperatures

- Unlike conventional bipolar transistors, when cooled SiGe HBTs exhibit **improved frequency response, current gain, noise, bandwidth, output conductance and other performance metrics**.
- **BiCMOS** (SiGe HBT + Si CMOS) platform **ideal mixed-signal technology** that marries high-performance SiGe HBTs for analog, RF, and microwave circuits, with Si CMOS to support highly-integrated system functionality.

- Fabricated on large wafers (300 mm) at **high yield** and **low cost** using conventional silicon processing techniques and silicon economy-of-scale.
- SiGe HBTs cooled to temperatures as low at 70 mK demonstrated operability for a variety of interesting circuit designs (gain of 2000 at 100 mK at only a few µW dissipation).
- At sub-K, the amplification principle becomes fundamentally quantum mechanical in nature, as tunneling becomes the dominant transport mechanism. **Constant operation across temperature below ~7K**.



H. Ying et al., "Operation of SiGe HBTs Down to 70 mK," in IEEE Electron Device Letters, vol. 38, no. 1, pp. 12-15, Jan. 2017.

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Transistor Models and Library Development for Radiation Hardness

Collaboration with CERN (65 nm)

Transistor models

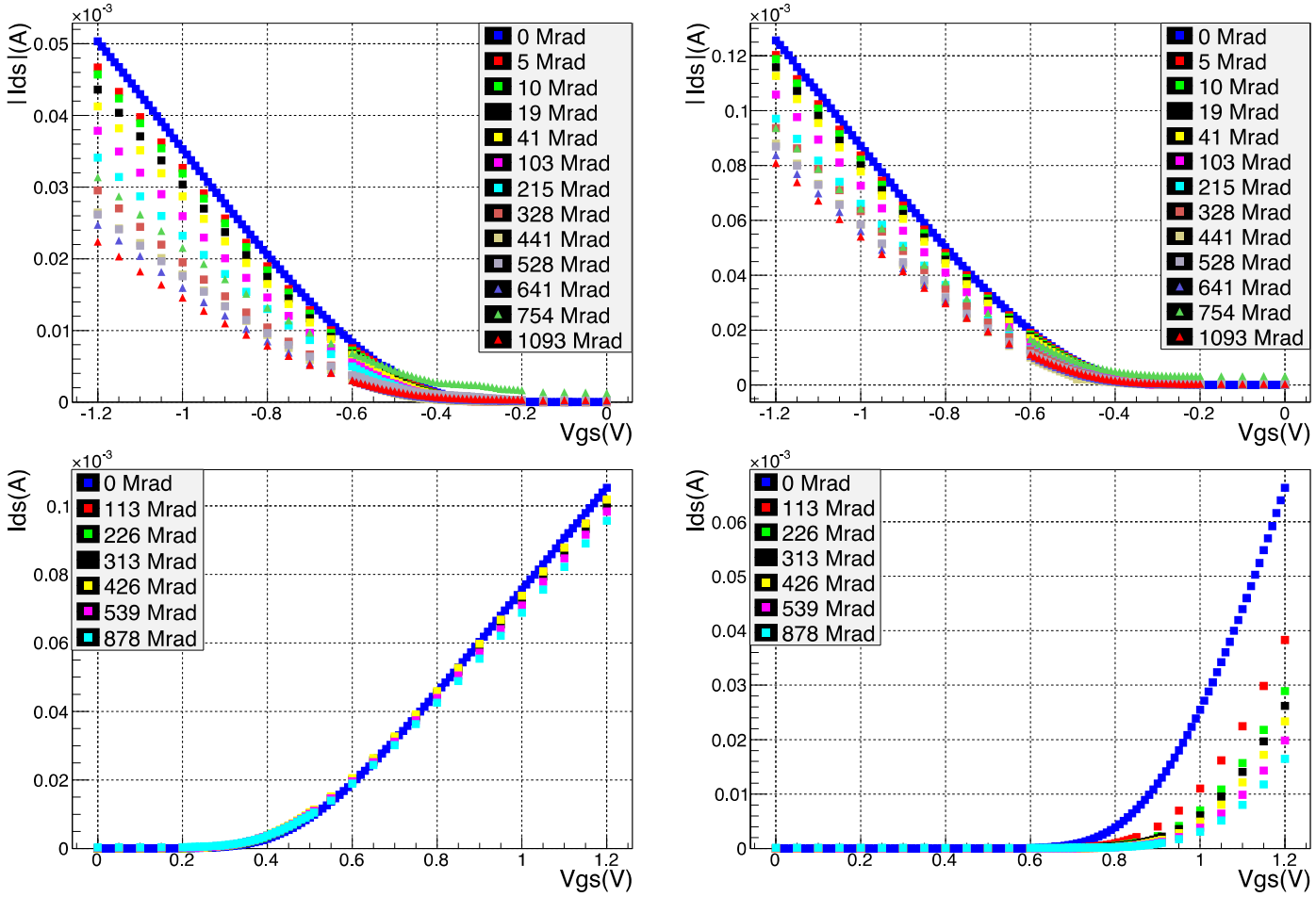
Irradiation up to 1 Grad for various transistor sizes

Standard Cell Libraries

6 libraries @ 500Mrad, T= -30 & 25

9 track normal VT

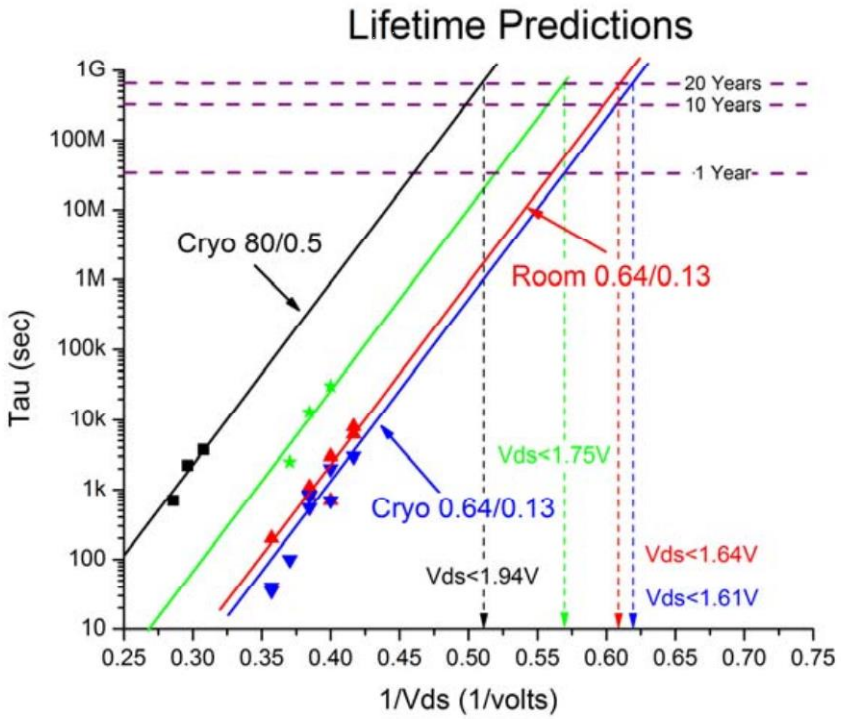
12 track low VT



Transistor characteristic curves for PMOS (top) and NMOS (bottom)

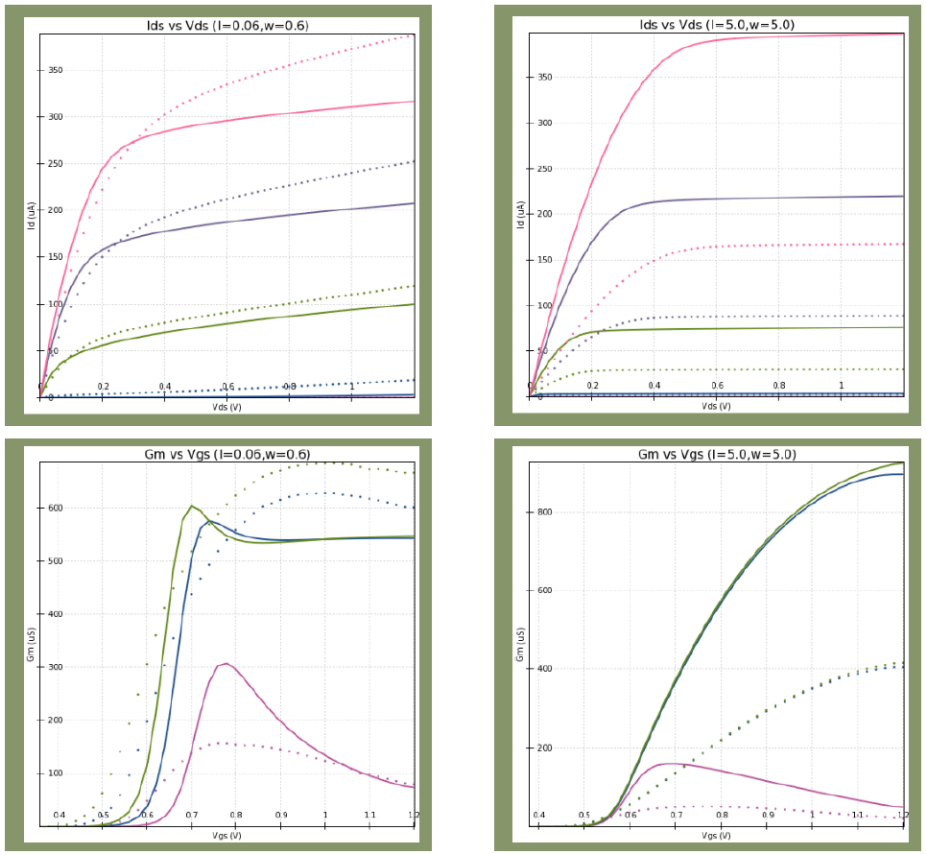
Lifetime Studies and Library Development for LAr (89K)

- Lifetime studies to determine **Hot Carrier Effect** degradation
- Characterized and modelled transistors operating at 89K;
- Created **custom standard cell library** (~230 gates), compatible with P&R, to avoid hot-carrier degradation;
- Creation of timing and power files for custom library, essential for static timing analysis and complex digital designs.



Example of Spice model simulation with foundry models vs. measured data:
Points: measurement (= custom models)
Lines: foundry models extrapolated at 89K

W/L=0.6/0.06 W/L=5/5



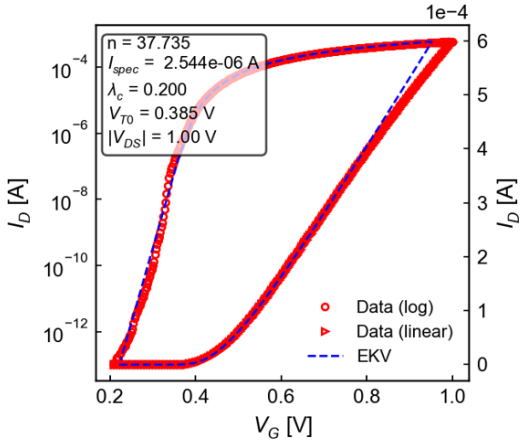
SC electronics and cryo-CMOS modeling and extraction

- Collaboration with EPFL for measuring and cryo EKV model for analog design
- Development of test structure for RF/low-freq noise characterization of transistor

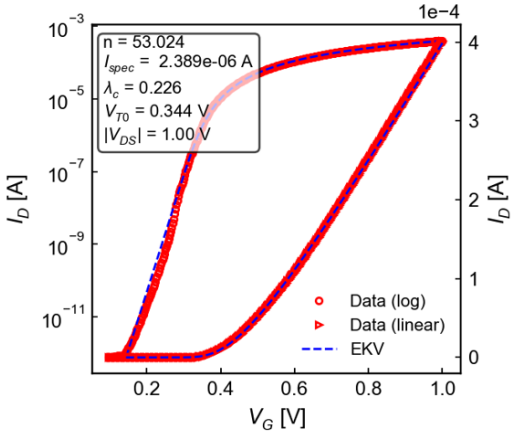
EPFL **Simplified EKV modeling for 22FDX at 3 K**

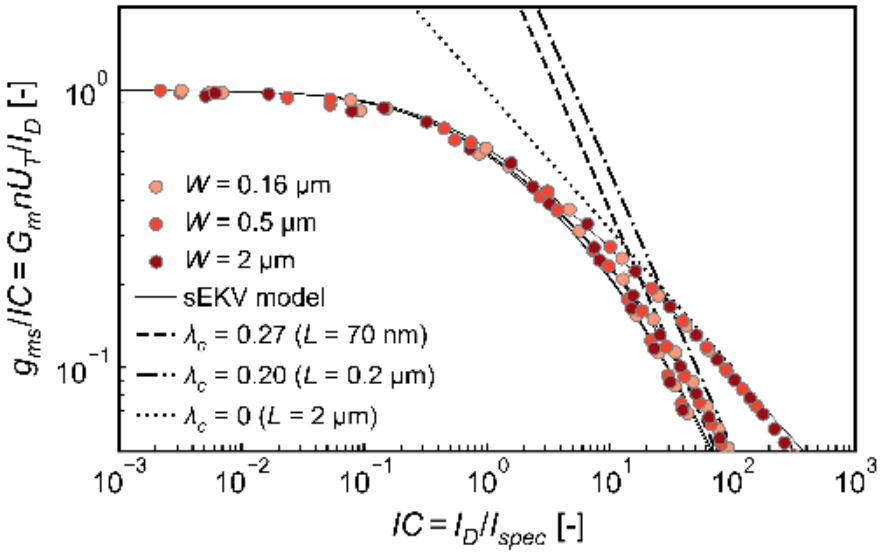
Hung-Chi Han

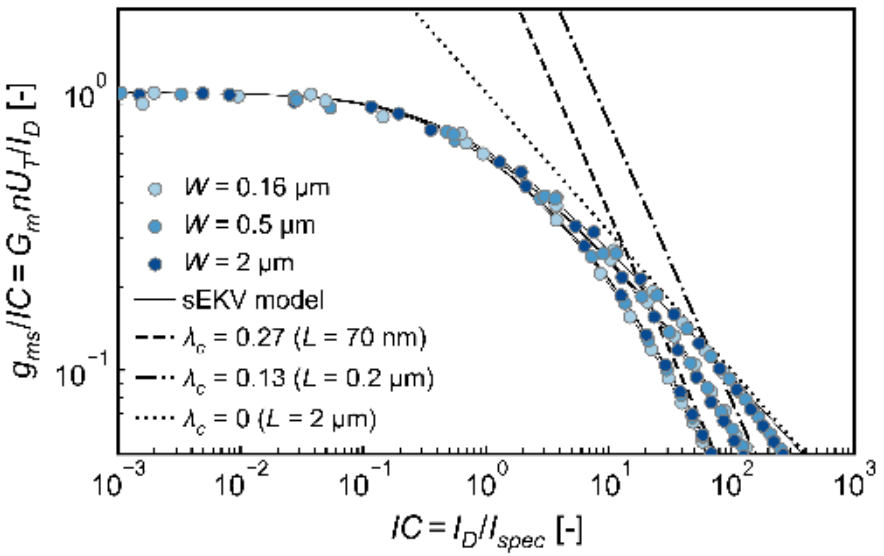
FDSOI, nMOS
L = 18 nm
W = 500 nm



FDSOI, pMOS
L = 18 nm
W = 500 nm







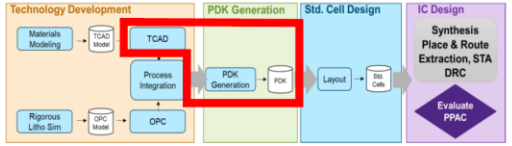
The normalized transconductance efficiency with the application of simplified EKV model on EG FDSOI devices at room temperature; (left) nMOS, (right) pMOS.

SC electronics and cryo-CMOS modeling and extraction

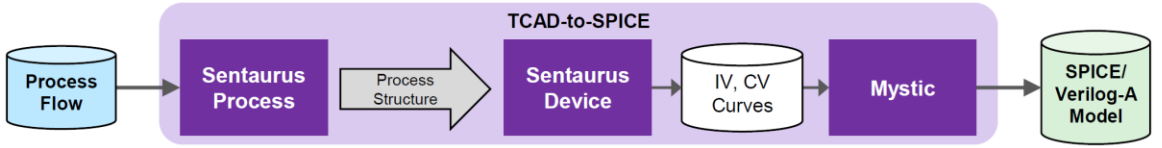
In collaboration with **Synopsys:**

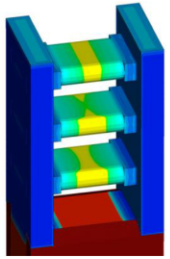
- SC electronics models (MIT, FNAL)
- cryoCMOS models (FNAL)

TCAD-To-SPICE Sub-Flow Extracts SPICE Model From TCAD Before Wafers Are Available

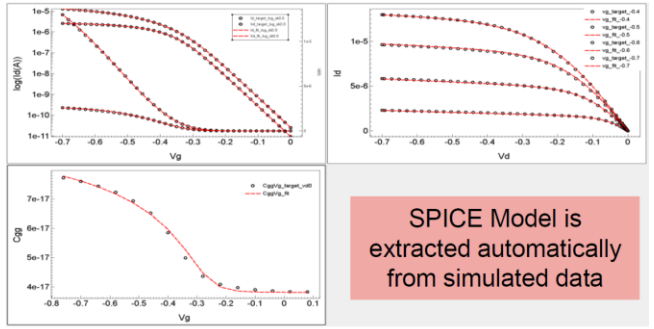


Mystic extracts SPICE or Verilog-A compact model from Sentaurus Device Output





Transistor Structure Simulated in TCAD

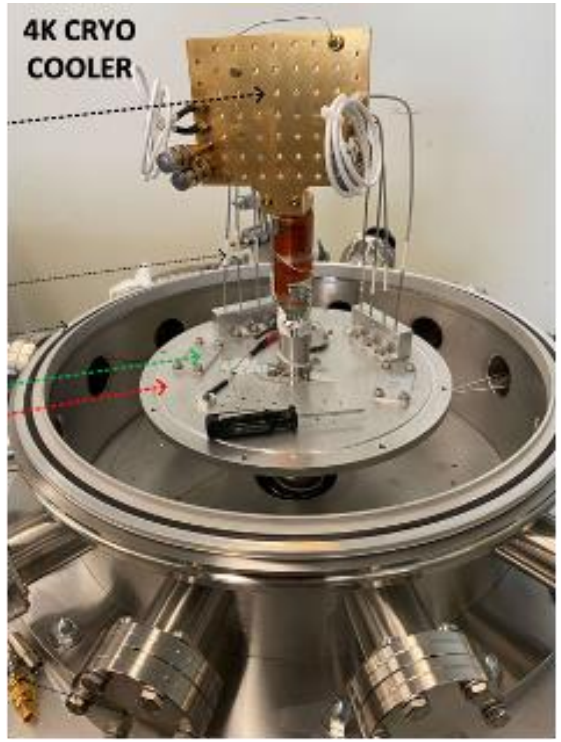


SPICE Model is extracted automatically from simulated data

```
#if "@type@" == "nMOS"
.subckt mos5n d g s b l=@lgate@ nfin=3

.param rgc      =0
.param rgc_fin  =rgc*rgc_en
.param rsc      =0
.param rsc_fin  =rsc*rsc_en
.param rdc      =0
.param rdc_fin  =rdc*rdc_en


rd      d       d_i     rdc_fin
rs      s       s_i     rsc_fin
rg      g       g_i     rgc_fin

mos d_i g_i s_i b mosmod l=l nfin=nfin
.model mosmod nmos
+ DEVTYPE=1
+ EASUB = 4.0727
+ NI0SUB = 1.1055e16
+ BG0SUB = 1.1242
+ NC0SUB = 2.9951e25
+ EOT = 1.2E-9
+ PHIG = 4
+ RDSW = 0
+ RDSWMIN = 100
+ CDSCD = 1e-10
+ VSAT = 100000
+ VSAT1 = 100000
+ U0 = 0.02
+ UA = 1.0
+ PDIBL2 = 1e-4
+ PCLM = 1e-10
+ PCLMG = 0.0
```

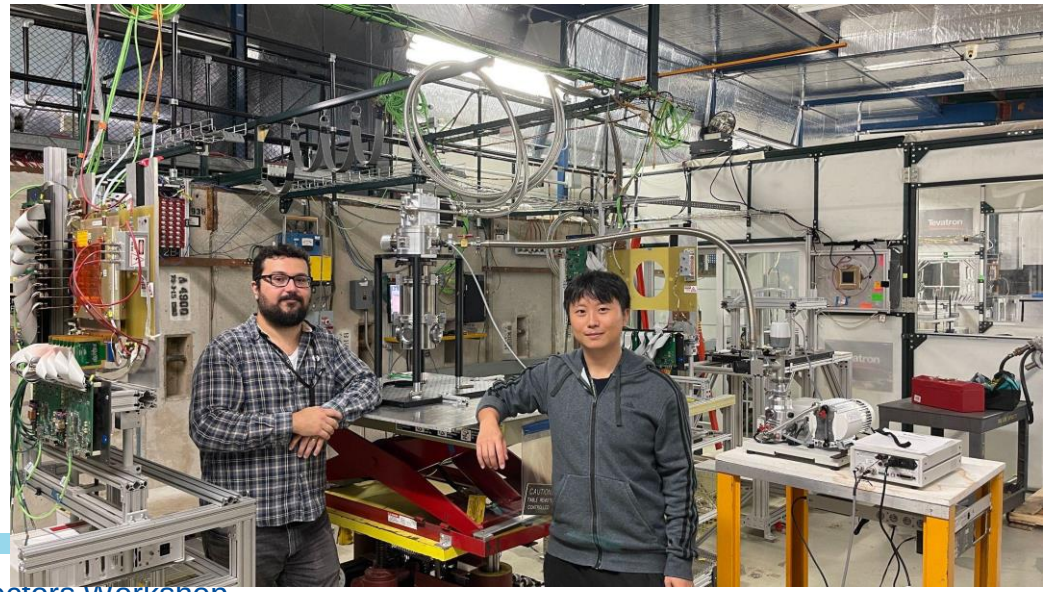
Cryogenic ASIC testing

4K cryocooler with custom large cold finger



Collaboration with ANL (W. Armstrong) for cold operation in test beam and irradiation area at FNAL

→ Radiation hardness + cryogenic operation



LAr readout electronics (89K) and Skipper CCD Readout (~100K)

DUNE front end electronics for LAr TPC

Front-End Mother Board (FEMB)

LArASIC

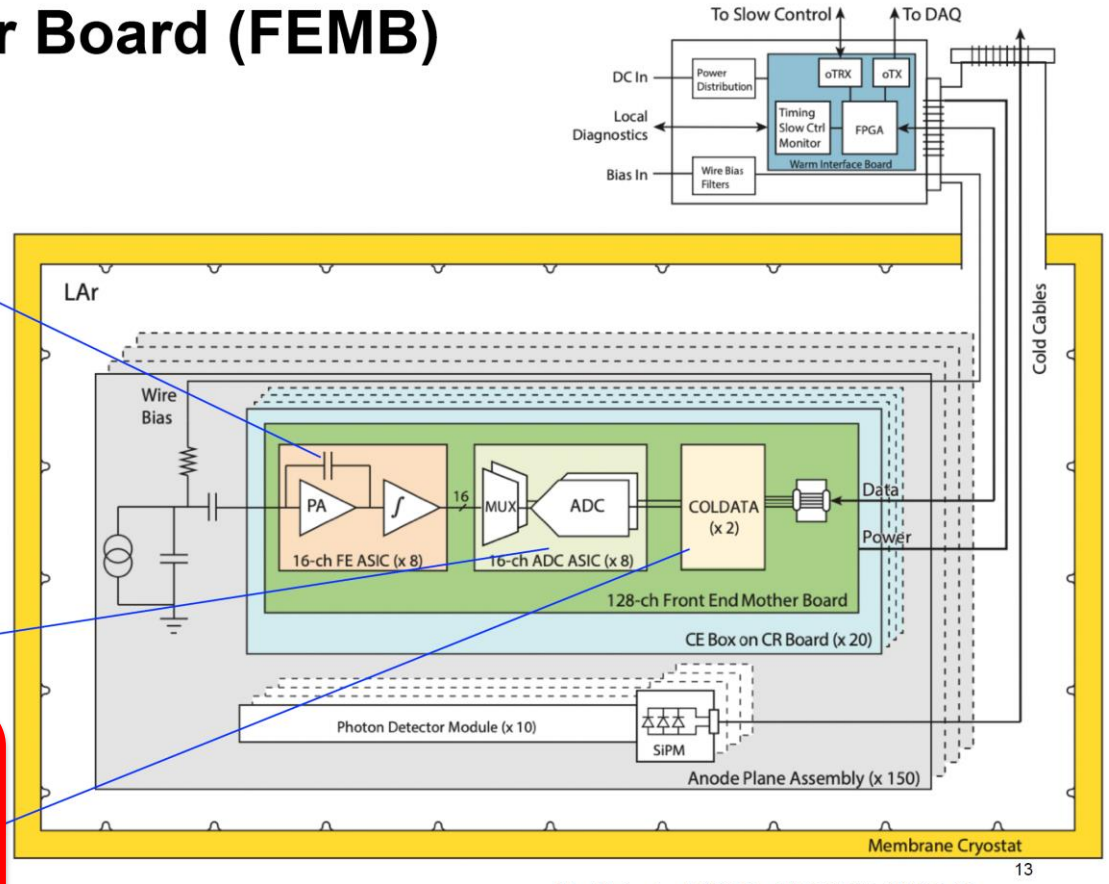
16 channels, pulse amplification and shaping ASIC; 4 gains 4.7 to 25 mV/fC; 4 peaking times 0.5, 1, 2, 3 us; 2 baselines;

ColdADC

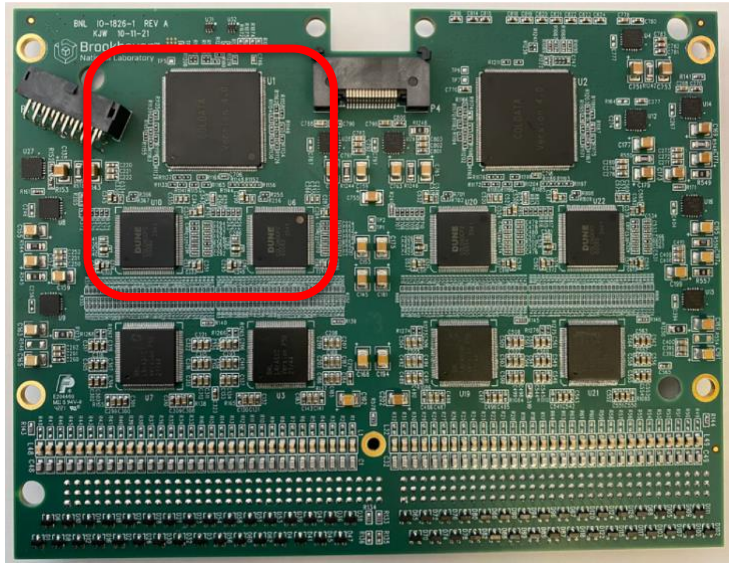
16 channels 14 bit ADC ASIC with digitized rate ~ 2MHz; pipelined ADCs operating at 16 MHz.

COLDATA

64 channels, data merging, control and communication ASIC; two 1.25 Gbps links



B. Abi *et al* 2020 *JINST* **15** T08010



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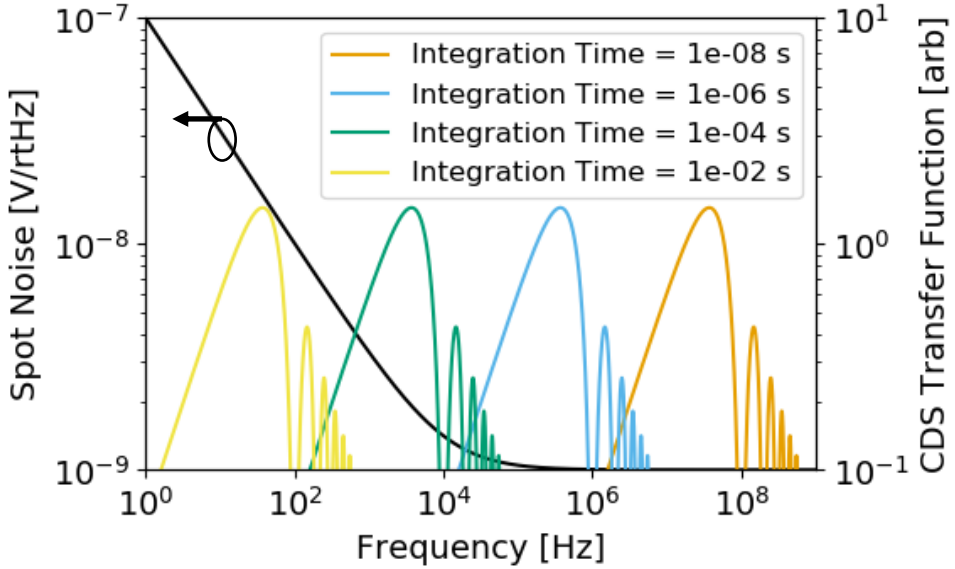
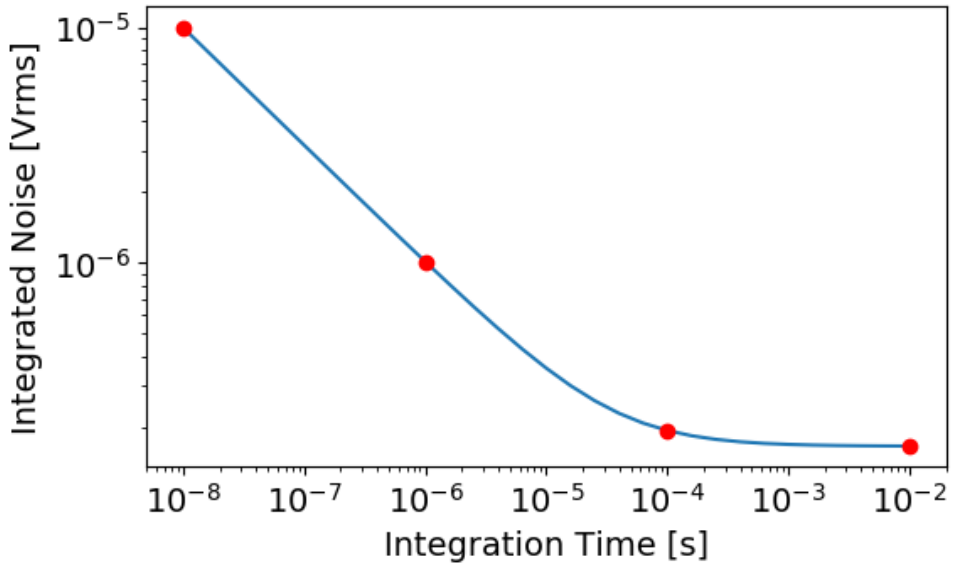
CCDs for Low Noise Imaging

- CCDs have long been the main choice for low noise scientific imaging
- The low noise has been enabled by a combination of integrating the readout for long periods and using correlated double sampling (CDS) [1]
  - Unfortunately, 1/f noise means that there was a limit to the effectiveness of this approach
  - Long integration moved the content of interest to lower and lower frequencies
  - The spreading out of the CDS sampling points reduced the filtering of flicker noise





[1] White et al., "Characterization of Surface Channel CCD Image Arrays at Low Light Levels."

The Skipper-CCD Principle

- What if instead of one long sample, we took many short ones?
- Avoid shifting to 1/f-dominated region.
- Samples are still uncorrelated; reduce noise as $\sqrt{N}$.
- **Integrated noise << 1 e- is possible!**

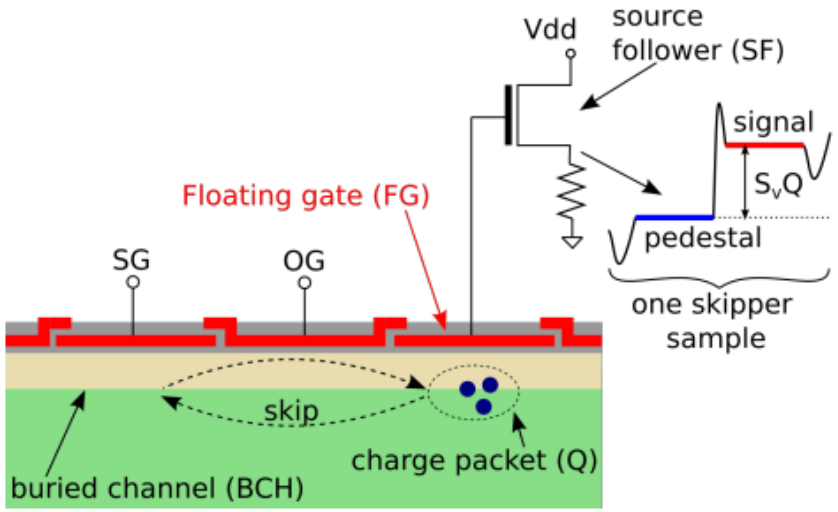
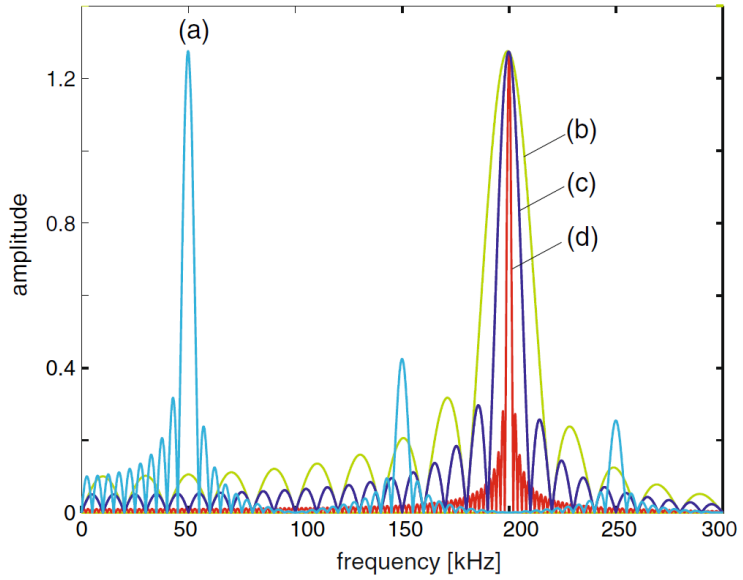
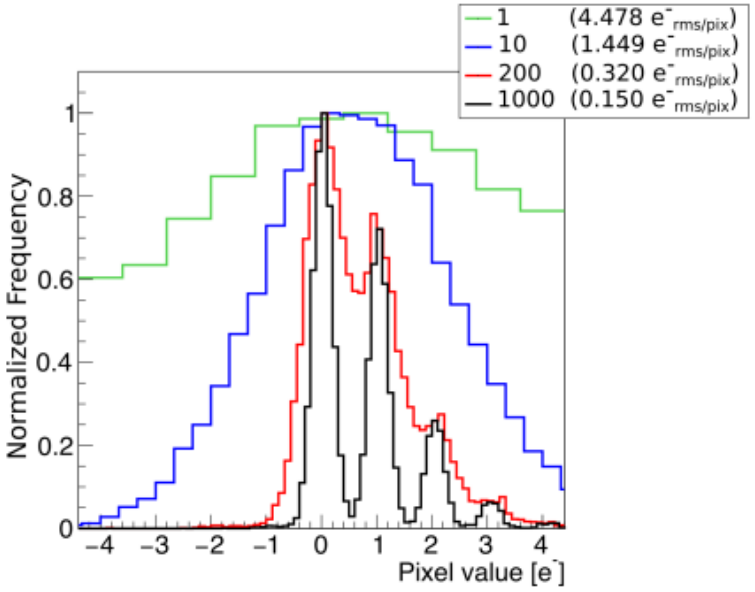


Fig. 8 Frequency response of the Skipper readout system for $T_S = 10\ \mu$s and $N = 10$ (**a**) and for $T_S = 2.5\ \mu$s and $N = 10$ (**b**), $N = 20$ (**c**) and $N = 100$ (**d**)





Images from Moroni, et al. [7]

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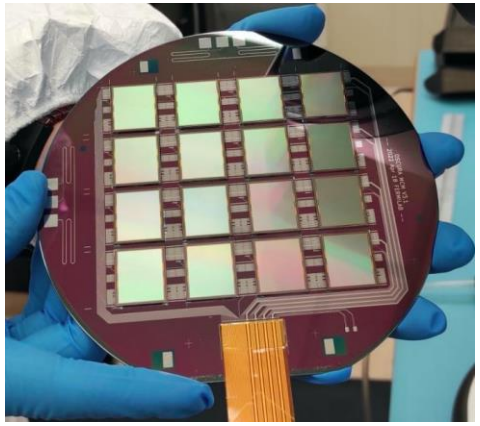
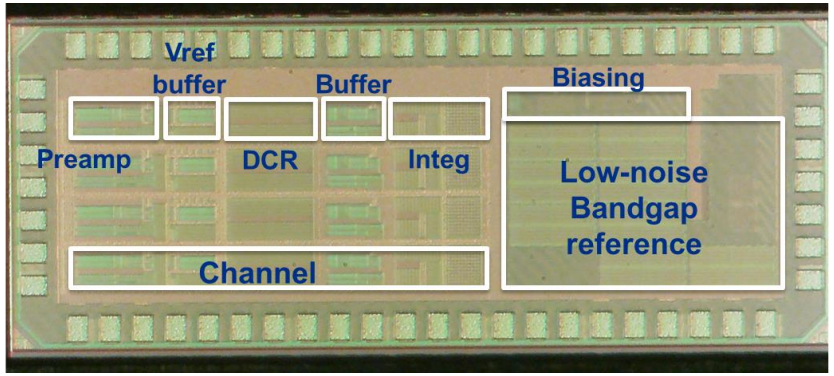
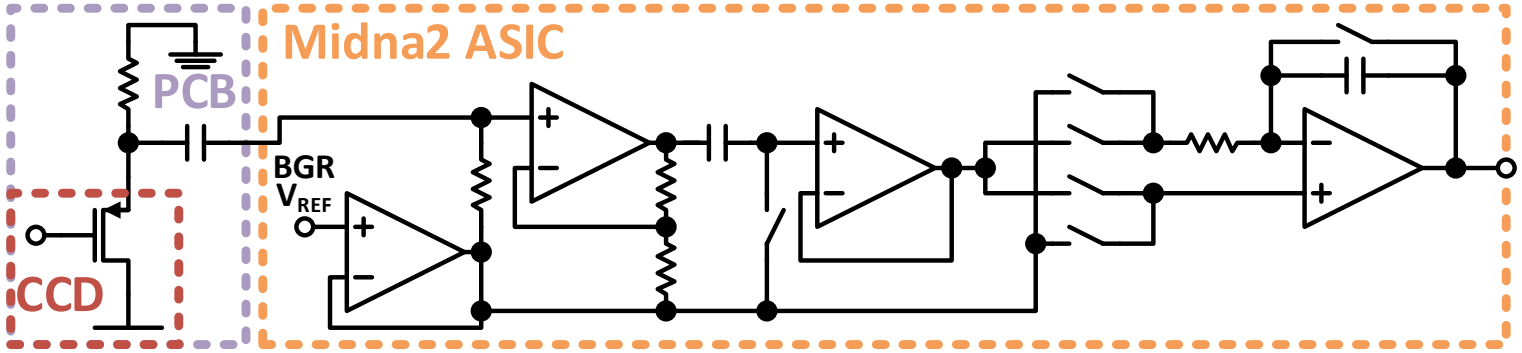
MIDNA: Sub-electron skipper-CCD readout with multi-channel cryogenic low-noise readout ASICs



- OSCURA 10kg dark matter detector (28Gpixel, 24K channels)

- 65nm CMOS, operates at roomT and 84K
- 2.5 mm x 1 mm
- Four analog channels
- On chip low-noise bandgap reference and biasing
- Sub-e^- read noise from channel at 10 µs integration times
- < 6 nV/√Hz input referred noise at 10 kHz
- 3000 e^- dynamic range
- High linearity, R^2-1 = -8.5e-7
- Cryogenic operation down to 84 Kelvin
- Selectable gain
- 4.2 mW per channel





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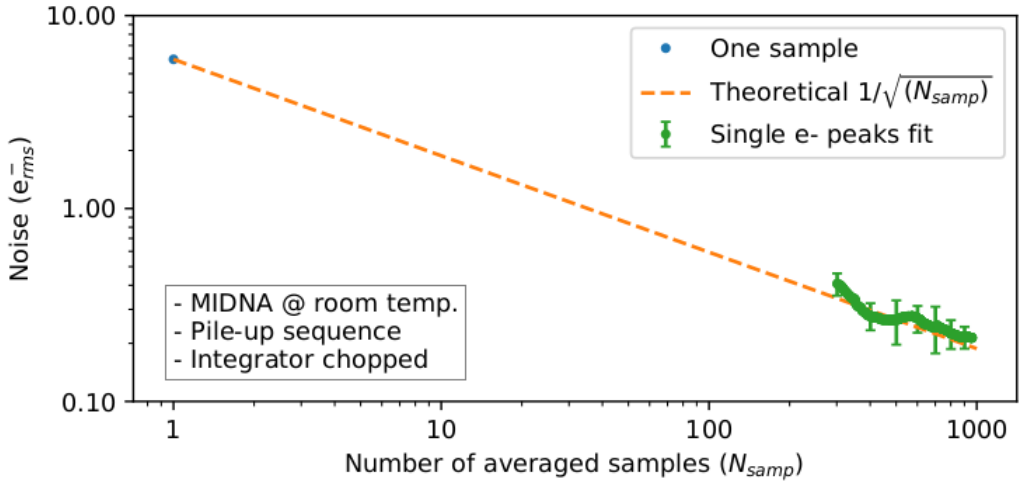
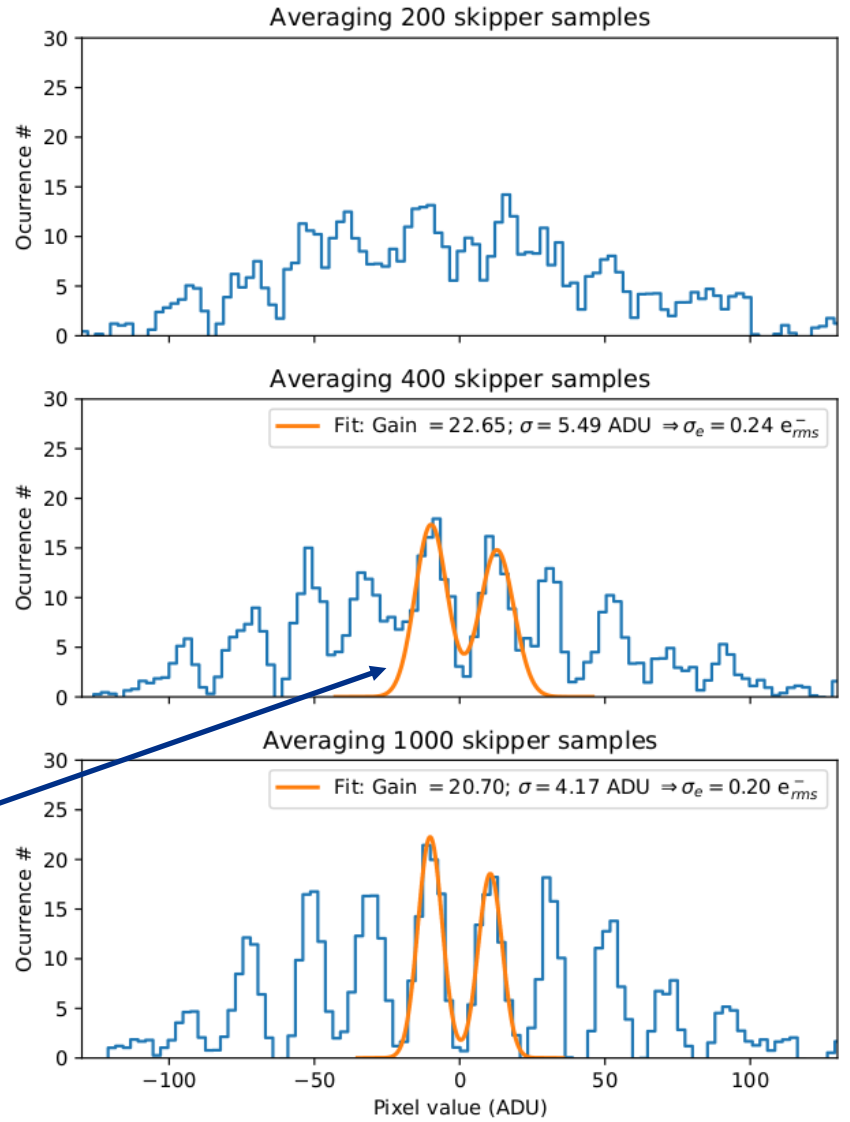
MIDNA 1 Achieves Sub-electron CCD Readout Noise

- Even with MIDNA at room temperature, sub-electron readout noise was achieved
- Noise is dominated by the CCD
- 0.2 e-rms achieved with 1000 piled up reads

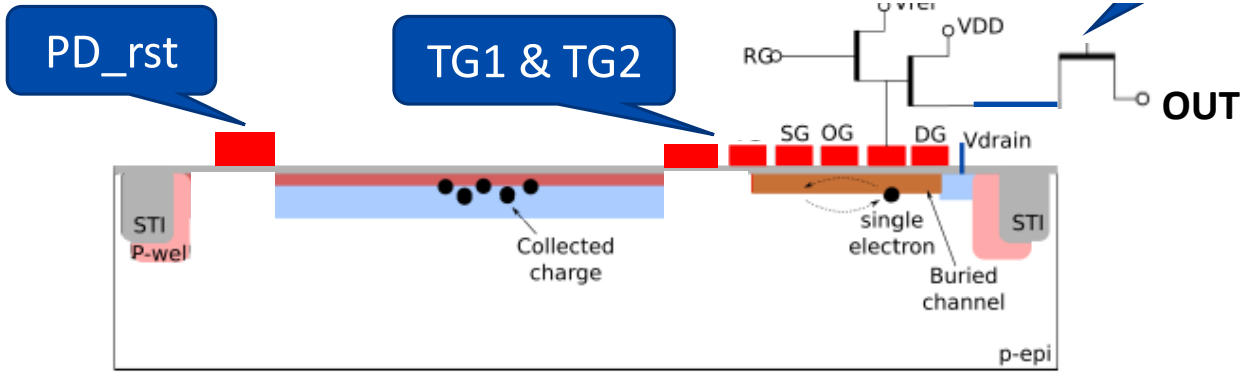


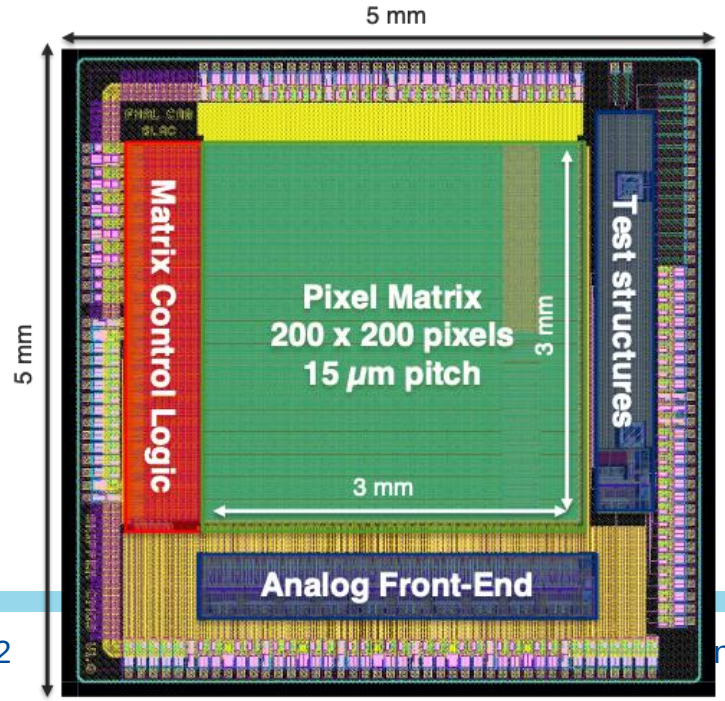
Separation of single electron peaks visible even at 400 reads

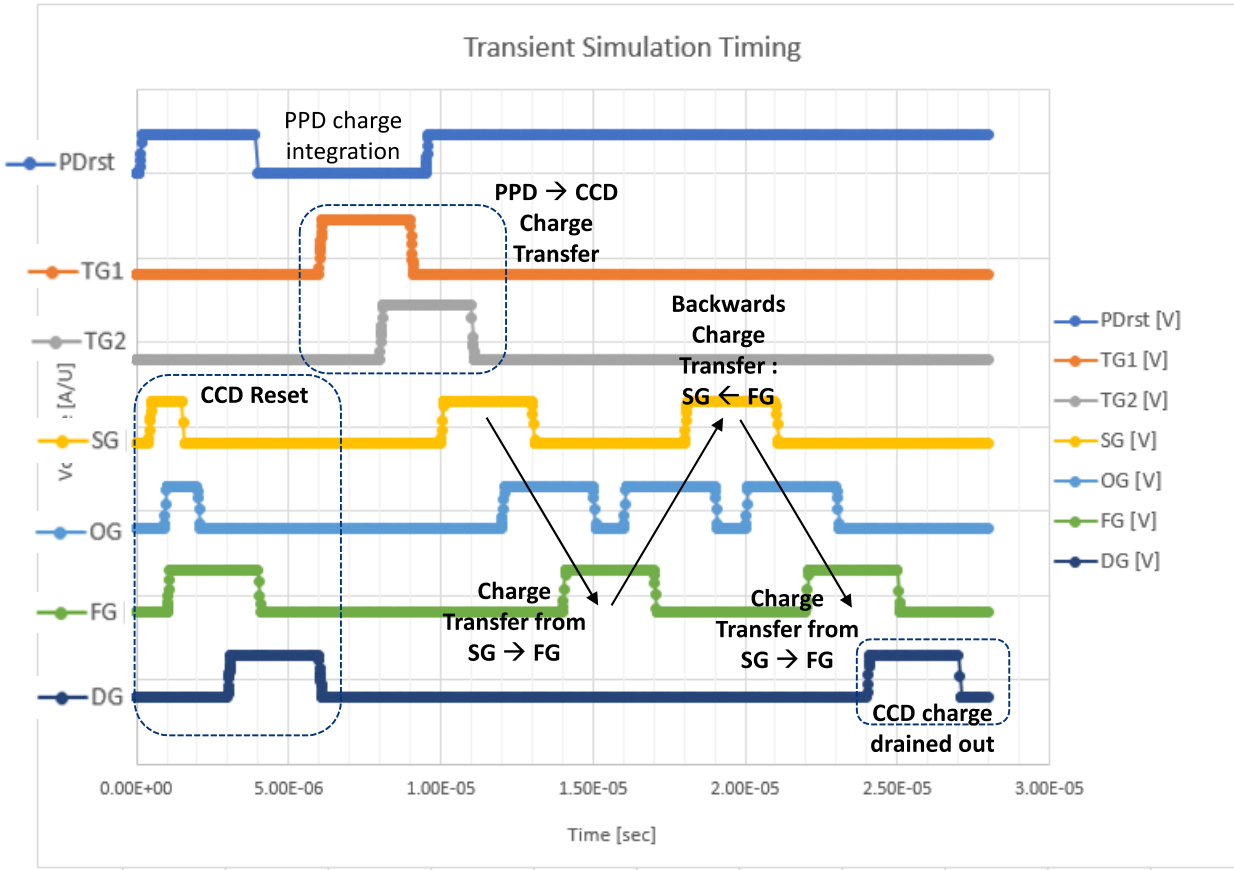


Skipper CCD-in-CMOS

- Utilize a commercial 180nm CMOS Image Sensor process for lower noise performance (Collaboration with SLAC and Tower Semiconductor)
- Noise of a pinned photodiode (0.7e-)
- With 10 averages we hope to achieve ~0.2e- noise at 1µs per read

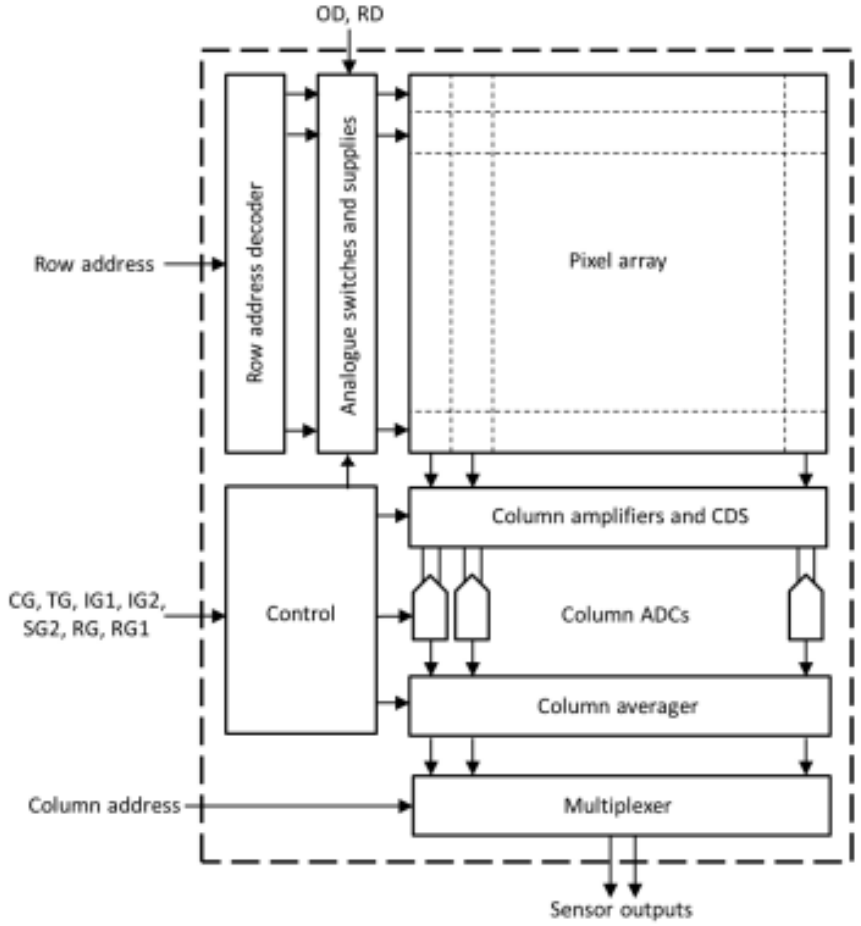






SPROCKET: Skipper CCD-in-CMOS Parallel Read-Out Circuit

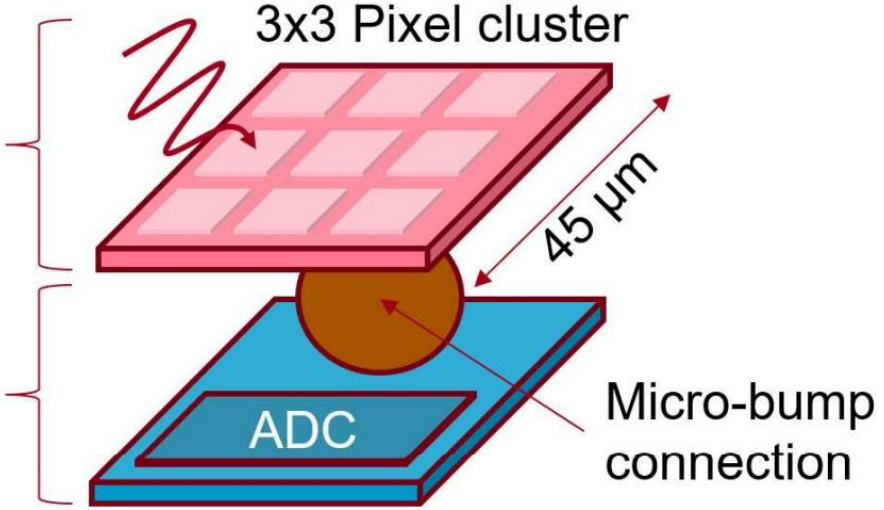
Monolithic, Column-Parallel



Hybrid, Per-Pixel

Skipper ASIC:
- Pixel matrix with skipper functionality

Readout ASIC:
- ADCs
- Real-time data processing
- Fast I/Os



Per-Pixel readout offers $\approx O(n)$ speedup, but at a cost:

Severely constrained power and layout area for the front-end and ADC circuits.

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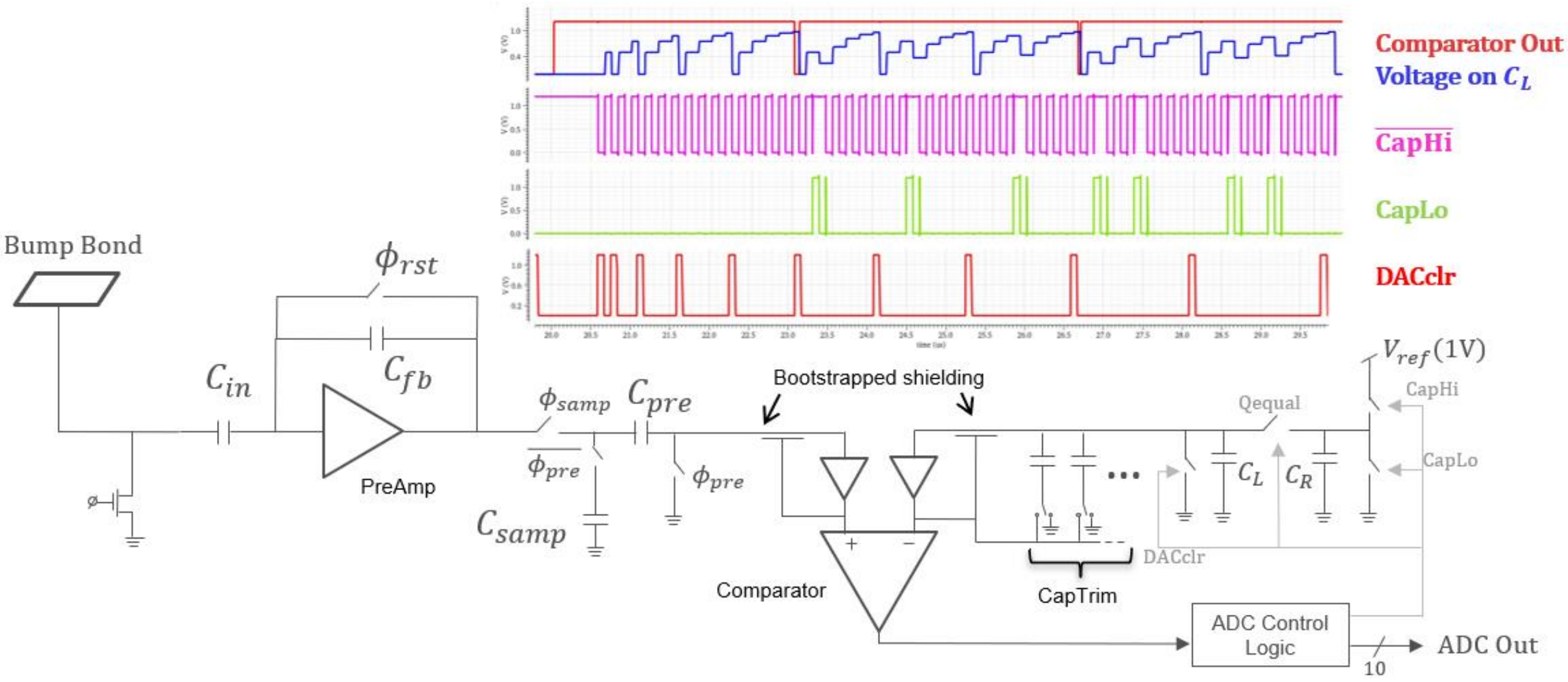
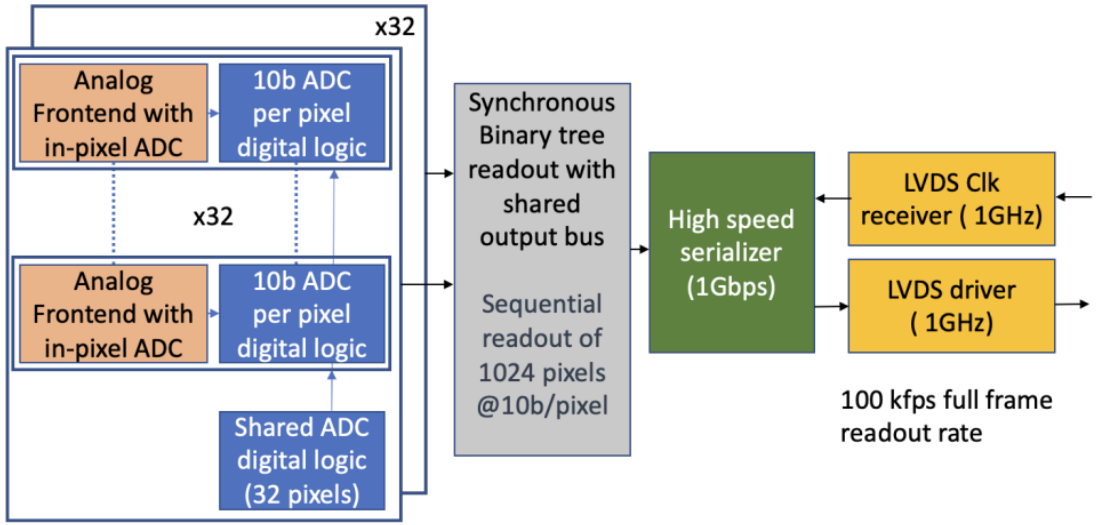
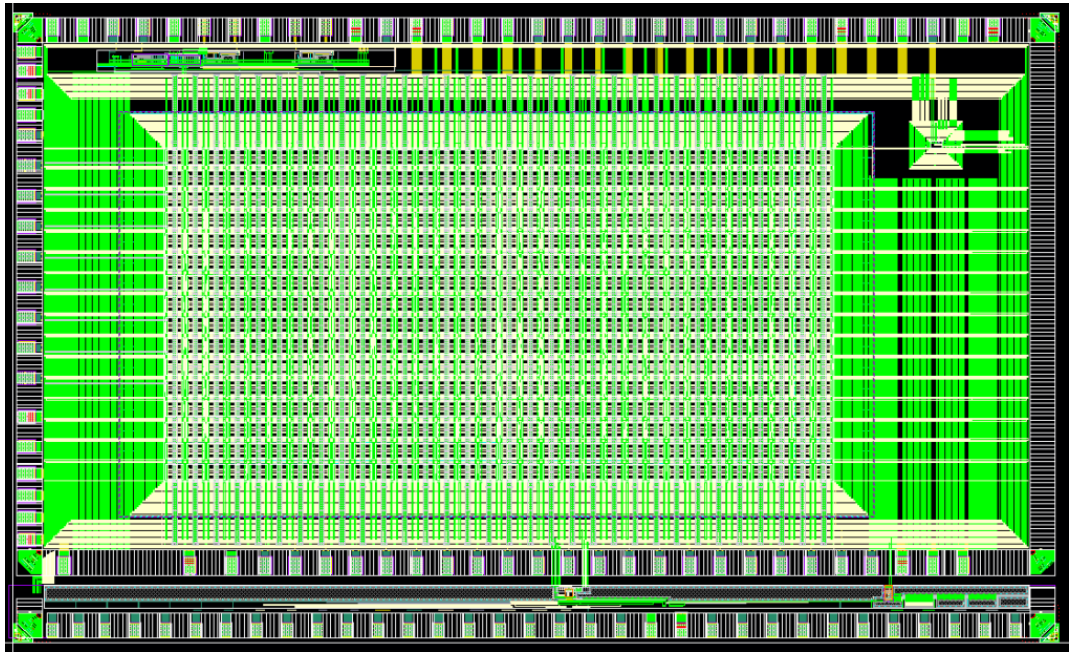
In-pixel compact ADC



Fermilab

- Cryogenic Readout IC for Skipper-CCD
- 100 KSPS in-Pixel ADC

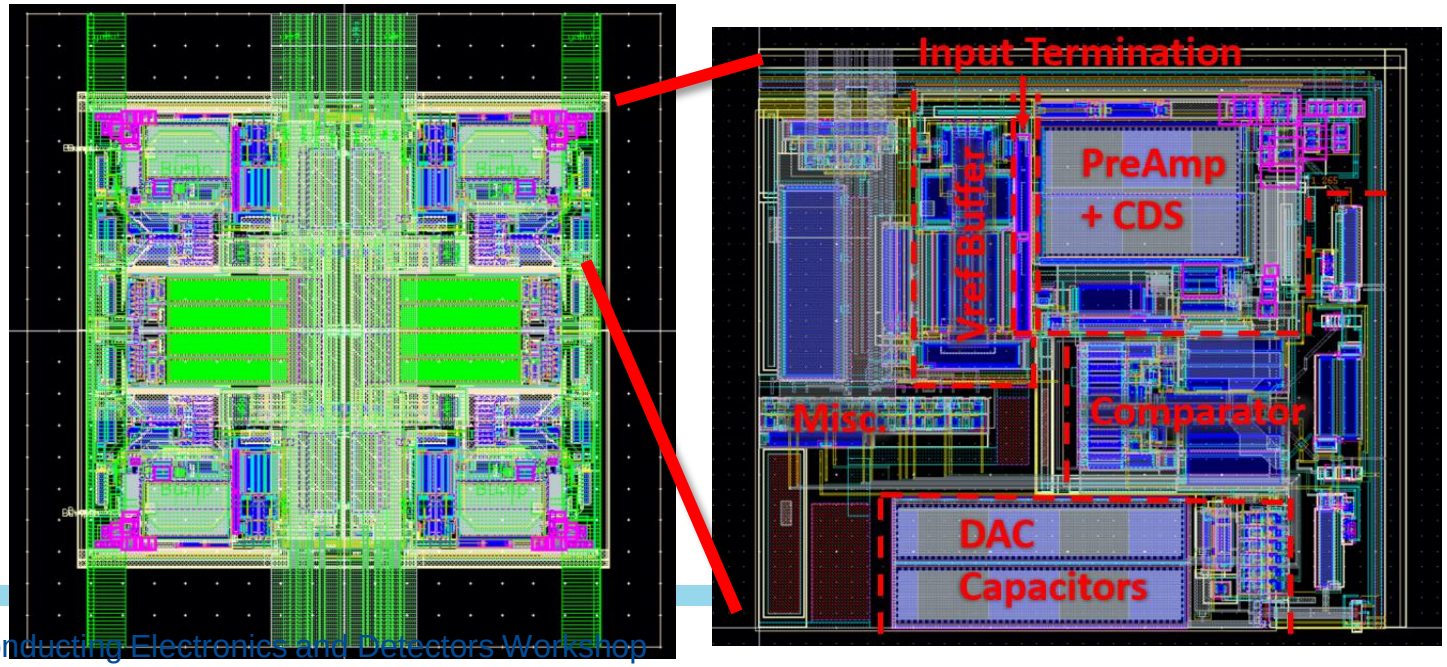




10b * 100 kHz * 1 MPix = 1 Tbps!

Data compression is important:

- Zero-suppression
- PCA
- ML-based Autoencoder



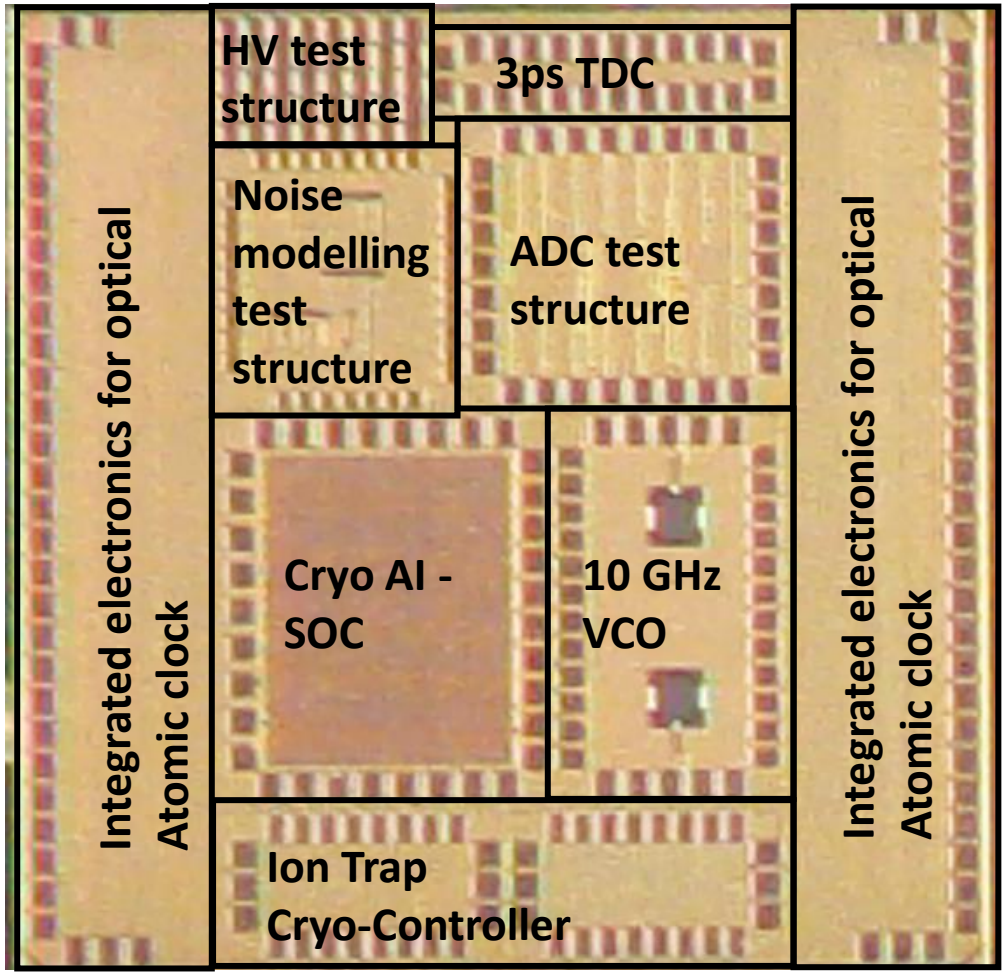
Cryo ASICs at 4K

3x3mm 22nm Fermilab tape out (Nov 2021)

Deep cryogenic electronics on advanced technology nodes (GF 22 FDX)

- Cryogenic **modelling** for development of 4K process design kit for GF 22 FDX with EPFL, Synopsys & GF
- **Quantum Science center** (National Quantum Initiative center led by ORNL)

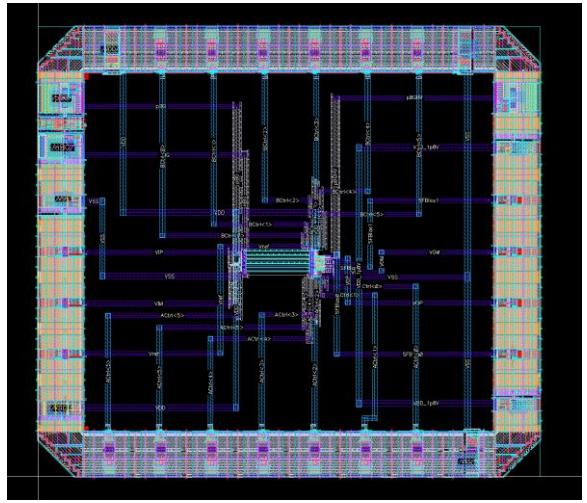
  Ion trap based Quantum Simulator: Cryoelectronics Controller – Low noise, high speed, high voltage DACs
- Compact Optical Atomic Clocks: Room temperature, integrated control **Joint DOE-DOD project** with MIT LL
- High speed cryogenic ADCs at 4K with **Industry**
- **Precision timing** for SNSPD detectors



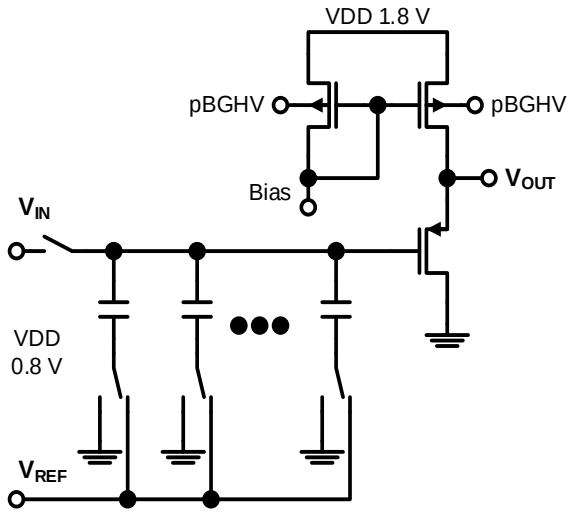
Fermilab

Capacitive DAC test structure for high-speed ADC

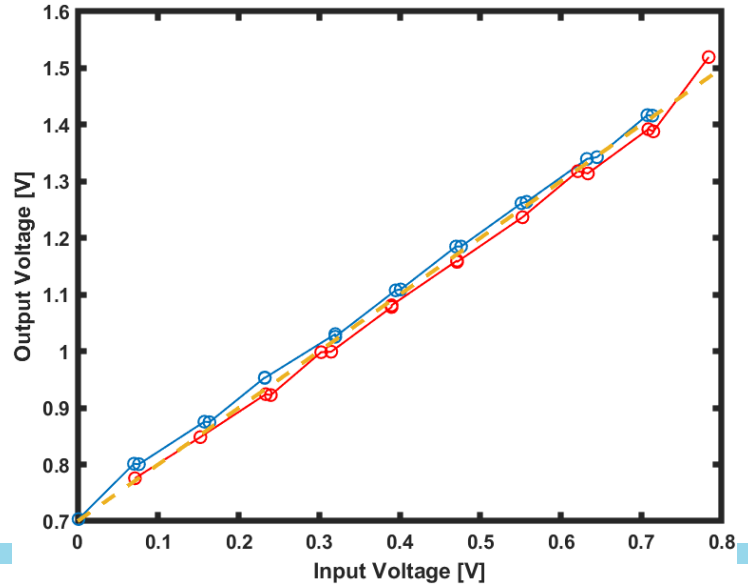
- Joint development with Microsoft Quantum, Sydney
- The chip is fully functional and performed as expected
- The transfer function shows the source followers worked as intended
- The control bits provide binary scaled adjustments of the held voltage
- The bootstrapped switch works very quickly to charge the sample capacitors



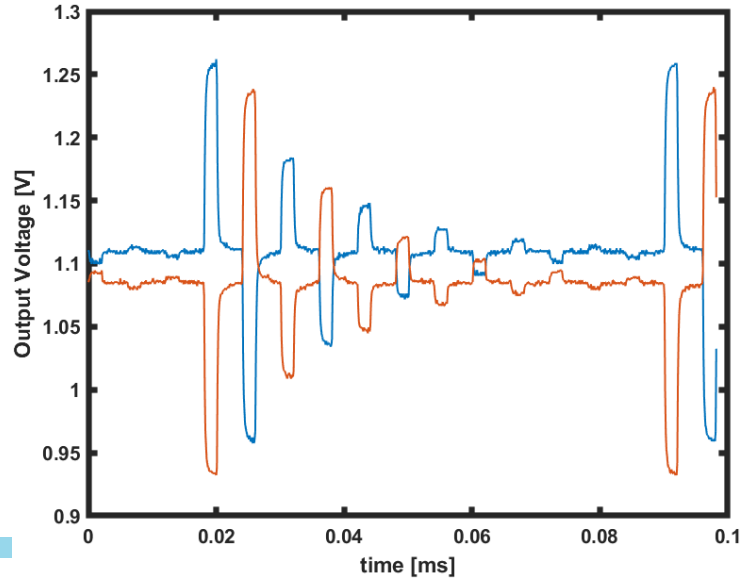
MMTC Simplified Schematic



MMTC Transfer Function

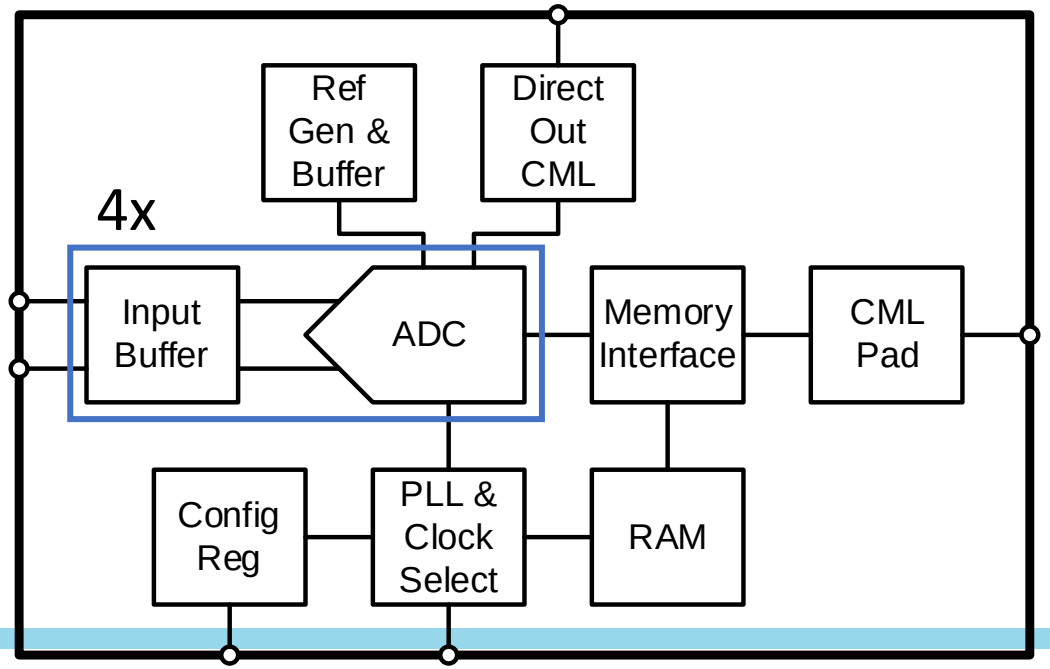


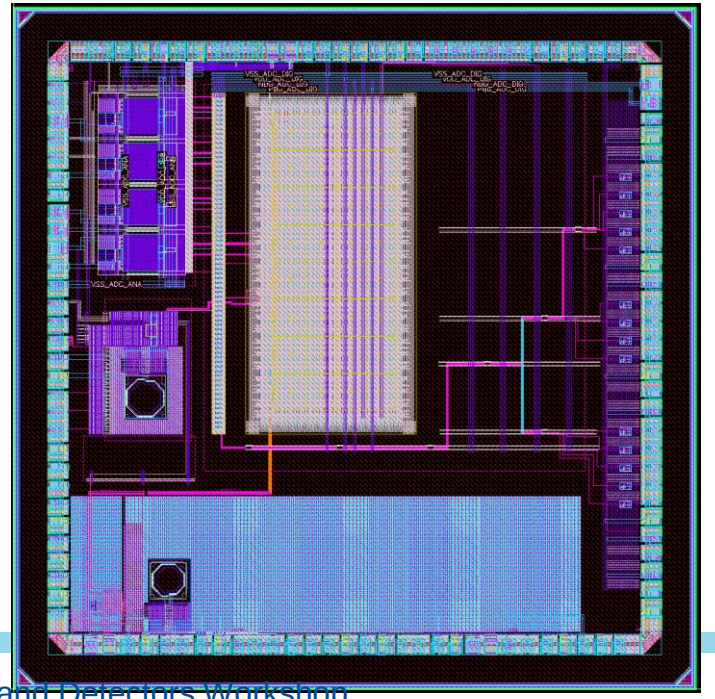
MMTC Control Bit Testing



Michigan Chip towards 10 GSPS ADC with 12b resolution operating at 4K

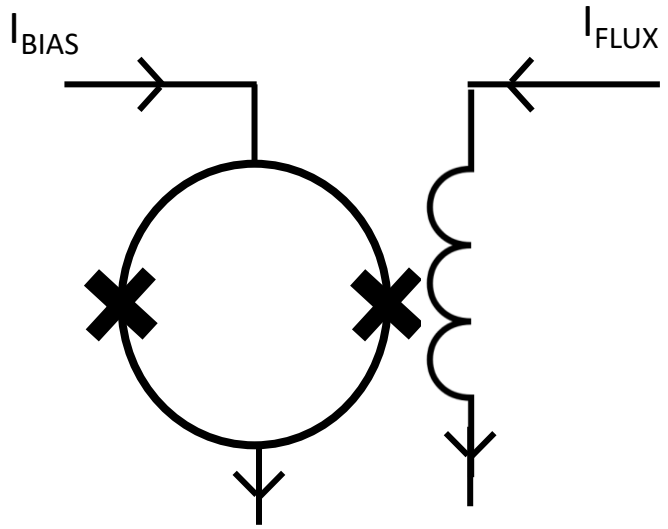
- The tapeout of the Michigan ASIC was a key milestone for the effort
- It includes four full sub-ADCs, input buffering, reference generation, full prototype PLL, clock generation alternatives, digital interface, and digital sample storage
- The first major chip collaboration with Microsoft with multiple contributors
- Low power ADC for quantum readout





Cryo DAC for current biasing

- Fully thermometric Current switching DACs designed for SQUID biasing
- Separate current DACs required for SQUID current bias and flux bias
- $\approx$ 40 % variation observed in SQUID
- Low power consumption to stay within limited power budget ($\approx$ 1 W at 4 K)
- Low current noise to maximise readout fidelity and avoid decoherence



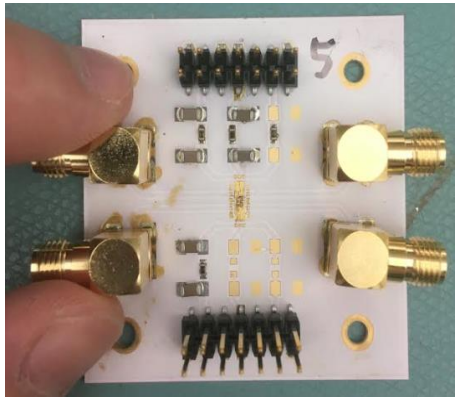
Specification	DAC 1	DAC 2
Maximum Current	2 mA	120 μA
Resolution	8 bits ($\approx$ 7.8 μA step)	6 bits ($\approx$ 2 μA step)
Maximum Power Consumption	$\approx$ 200 μW	$\approx$ 12 μW
Settling Time	$< 100\ ns$	$< 100\ ns$
Output noise @10 Hz	$< 1\ \mathrm{nA}/\sqrt{Hz}$	$< 300\ \mathrm{pA}/\sqrt{Hz}$
Output noise @10 MHz	$< 200\ \mathrm{pA}/\sqrt{Hz}$	$< 50\ \mathrm{pA}/\sqrt{Hz}$

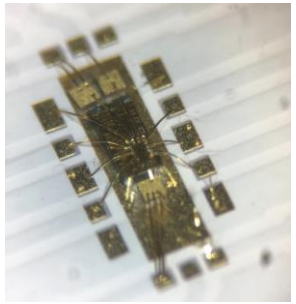
ASICs for SNSPD readout

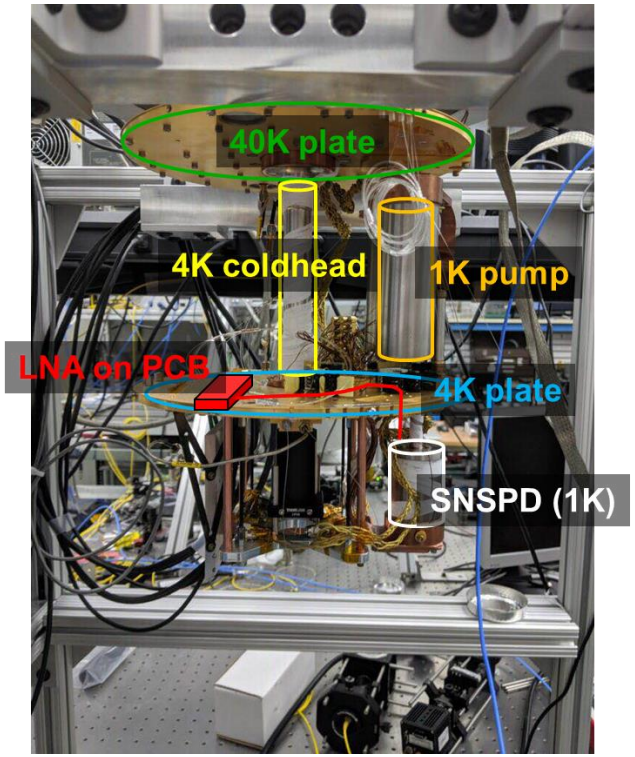
NECQST: Novel Electronics for Cryogenic Quantum Sensors Technology

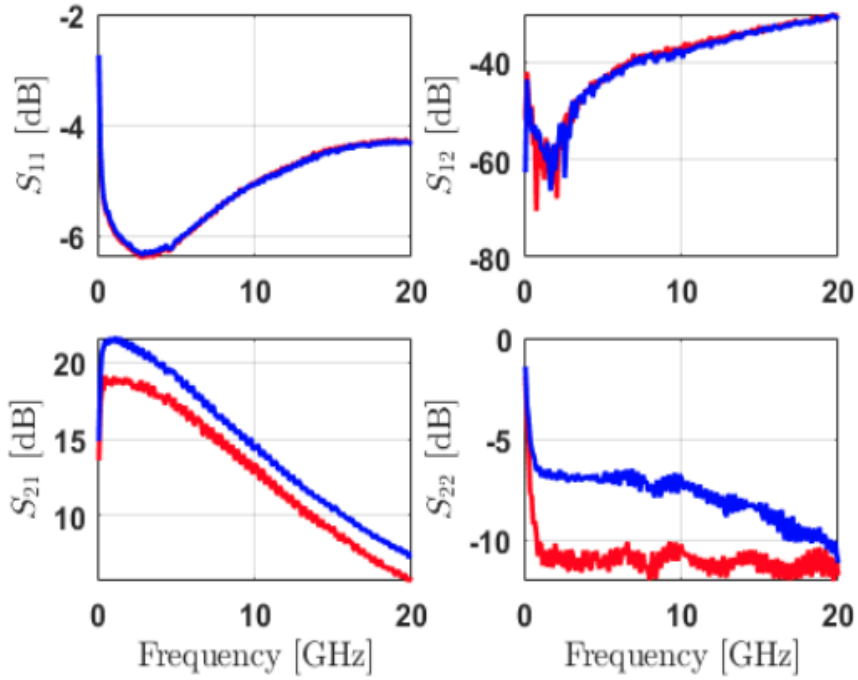
- Cryogenic (4K) SiGe HBT Low-Noise Amplifier (LNA), optimized for low-jitter low-power readout of Superconducting Nanowire Single Photon Detectors (SNSPDs).

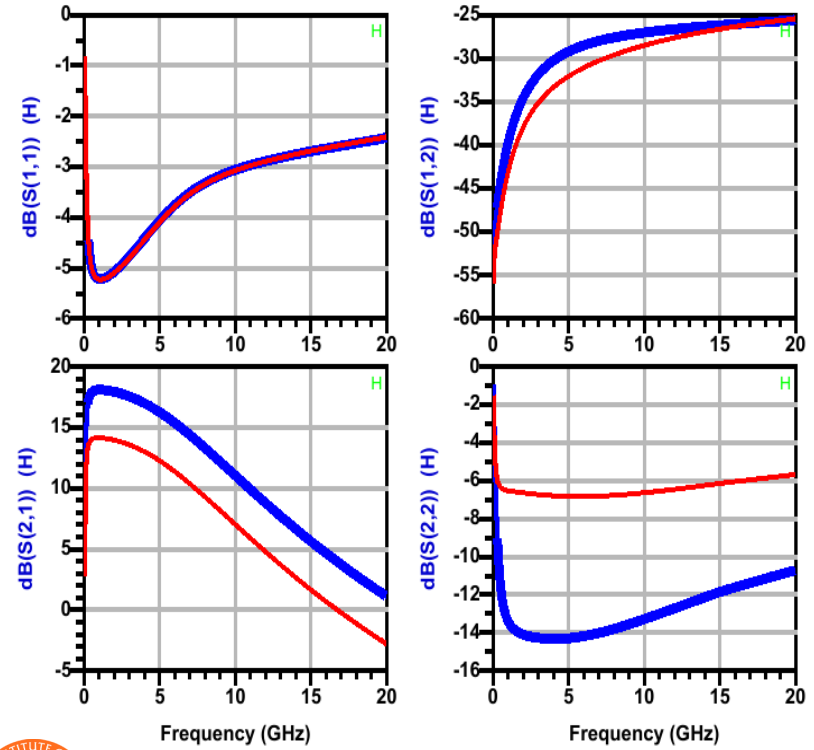
- Chip results without SNSPD are promising (some limitation in current test setup). Waiting for measurements with SNSPD





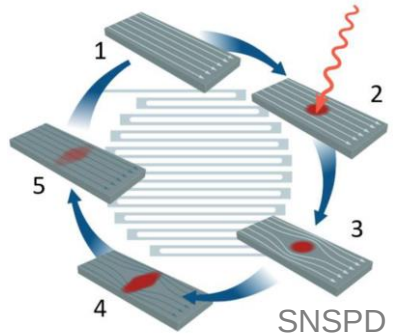






Fermilab Georgia Institute of Technology JPL Jet Propulsion Laboratory California Institute of Technology

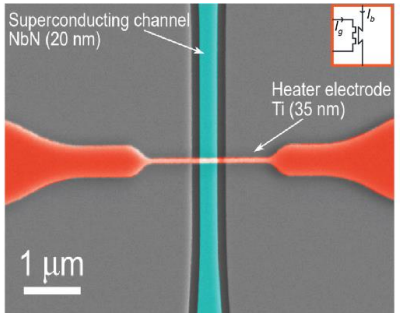
DOE Microelectronics Co-Design Research: "Hybrid Cryogenic Detector Architectures for Sensing and Edge Computing enabled by new Fabrication Processes"



SNSPD

Advancement of two complementary classes of cryogenic state-of-the-art single-photon and particle detectors:

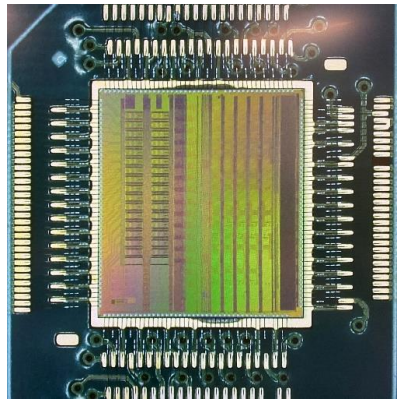
- the **Skipper CCD-in-CMOS** silicon detector
- a **hybrid detector platform based on superconducting nanowires**



xTrons

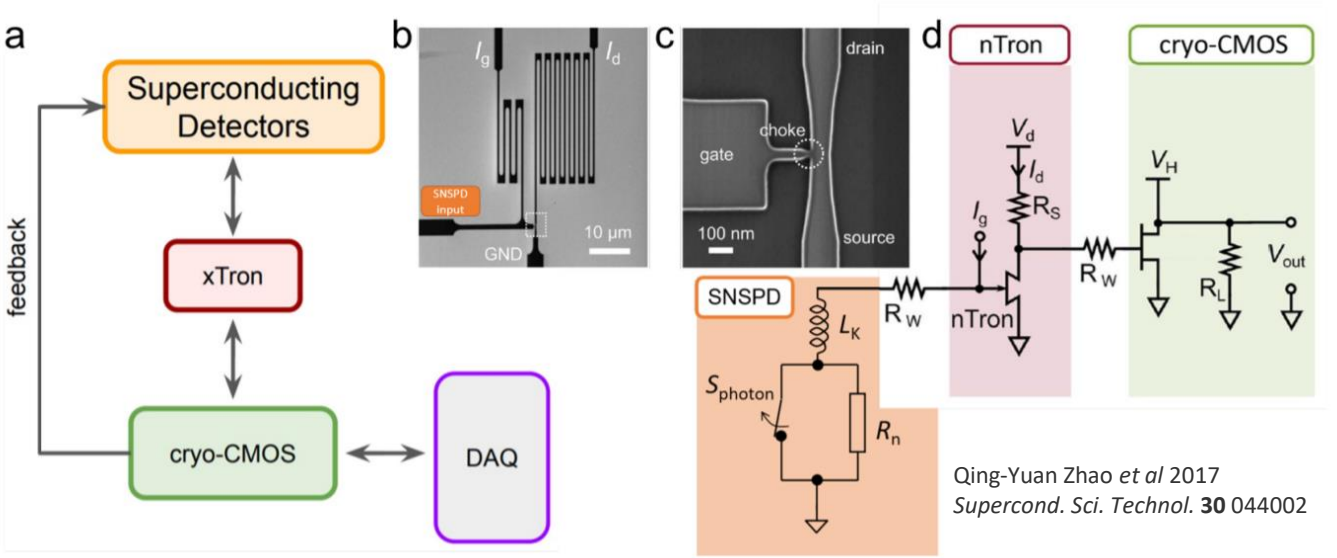
Development and co-design of:

- advanced **fabrication and integration techniques**
- novel optimized **hybrid readout architectures**
- cryo-ASICs and cryotron-based superconducting electronics for **integrated sensing** and data reduction at source, through **feature extraction** and **edge computing**.


cryoASIC

Fermilab Argonne NATIONAL LABORATORY SLAC NATIONAL ACCELERATOR LABORATORY NIST MIT JPL Jet Propulsion Laboratory California Institute of Technology SYNOPSYS® Fermilab

Hybrid nanowire-based superconducting detector platform



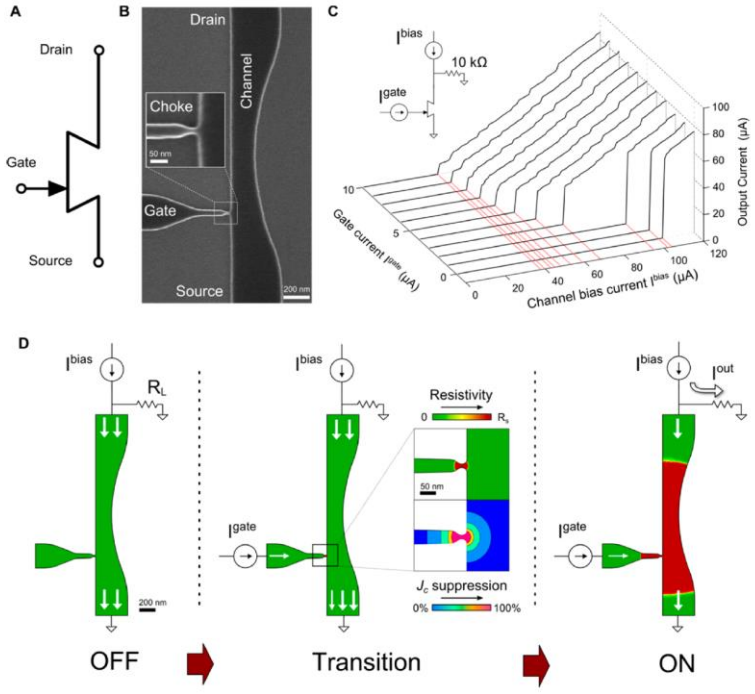
Qing-Yuan Zhao *et al* 2017
Supercond. Sci. Technol. **30** 044002

Hybrid architecture for cryogenic detectors, based on the co-design of:
1 – superconducting sensor (SNSPD),
2 – nanocryotron-based superconducting electronics (xTRON),
3 – cryoCMOS ASIC in nanometer scale (22nm FDX).

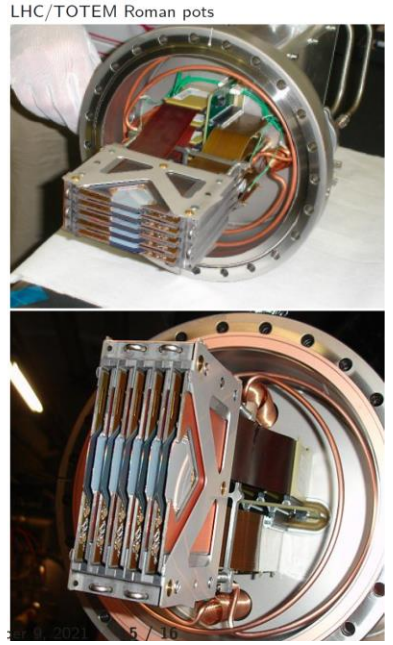
- develop the technology required for overall integration at cryogenic temperatures (Matt Shaw – JPL)
- SC and cryo-CMOS modeling and extraction (Synopsys, EPFL)

Goal: scalable, large count detector with edge computing and integrated sensing

Device-circuits-system codesign will concurrently enable large channel count, power optimization, impedance matching, edge compute and feature extraction, and data processing



Superconducting Nanowires Detectors



As PHOTON DETECTORS:

- Highest performing detectors available for time-correlated single photon counting from the deep UV to the mid-infrared
- Demonstrated detection efficiencies as high as 98% at 1550 nm
- Timing jitter below 3 ps
- Effectively zero dark count rates
- Intrinsic photon number resolution
- Maximum count rates exceeding 1 Gcps in arrays

Exploited for photon detection (classical and quantum optics and communication)

As PARTICLE DETECTORS:

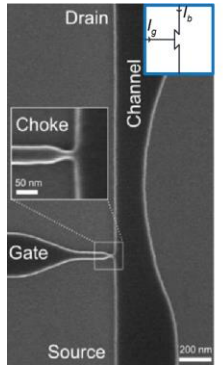
- Can have high segmentation (~10um “pixels”)
- Can be truly edgeless detector (important for beam monitoring)
- Operation in high magnetic field (5T)
- Radiation hardness to be investigated at Fermilab test beam facility

Unique capabilities for far-forward detectors that operate close to the beam (high T, high radiation, high segmentation)

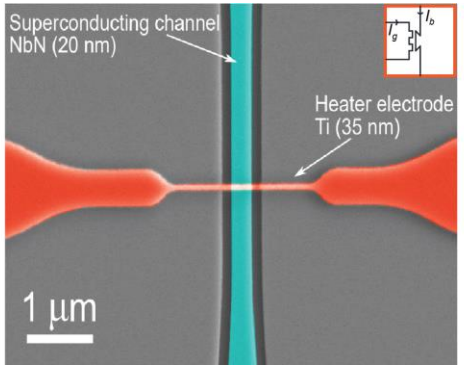
Superconducting Integration (Matt Shaw, JPL)

- Caltech/JPL to develop a nanofabrication process which will enable indium bump bonding of SNSPD focal planes to interposer structures,
- Evaluate the limits of ultra-high-density cryogenic microwave interconnects,
- and perform interface tests between SNSPD devices and digital readout electronics developed at FNAL and MIT.

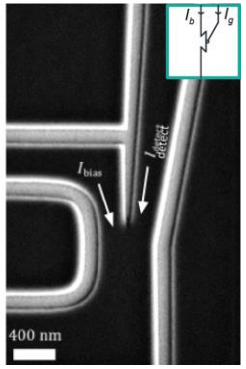
Nanocryotrons (MIT, K.Berggren)



nTron



hTron

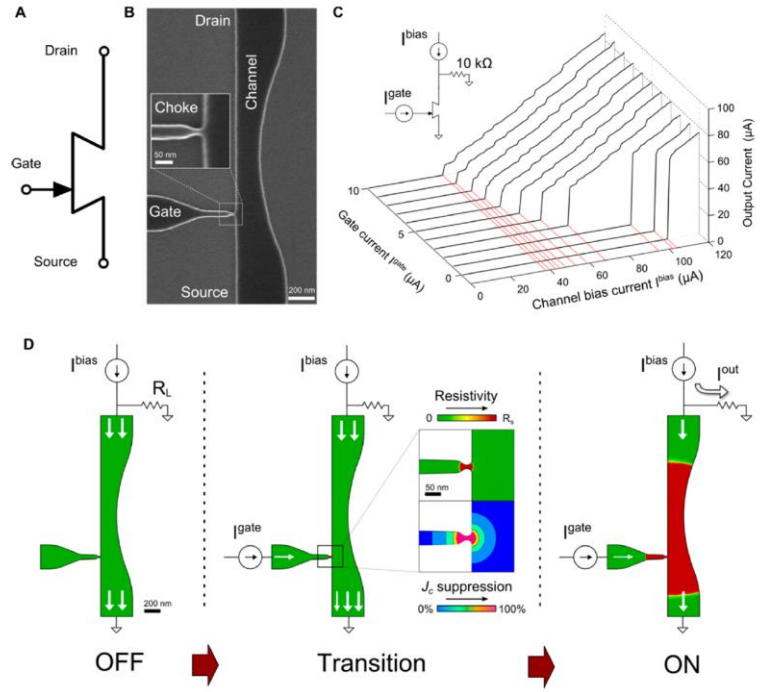


yTron

- Family of devices based on superconducting nanowires
- Could thus be monolithically integrated with the nanowire sensor
- Can be configured to operate as comparators, logic gates, signal level shifters, memories, shift registers…
- Impedance matching drive high-impedance loads and drive following cryoCMOS stage

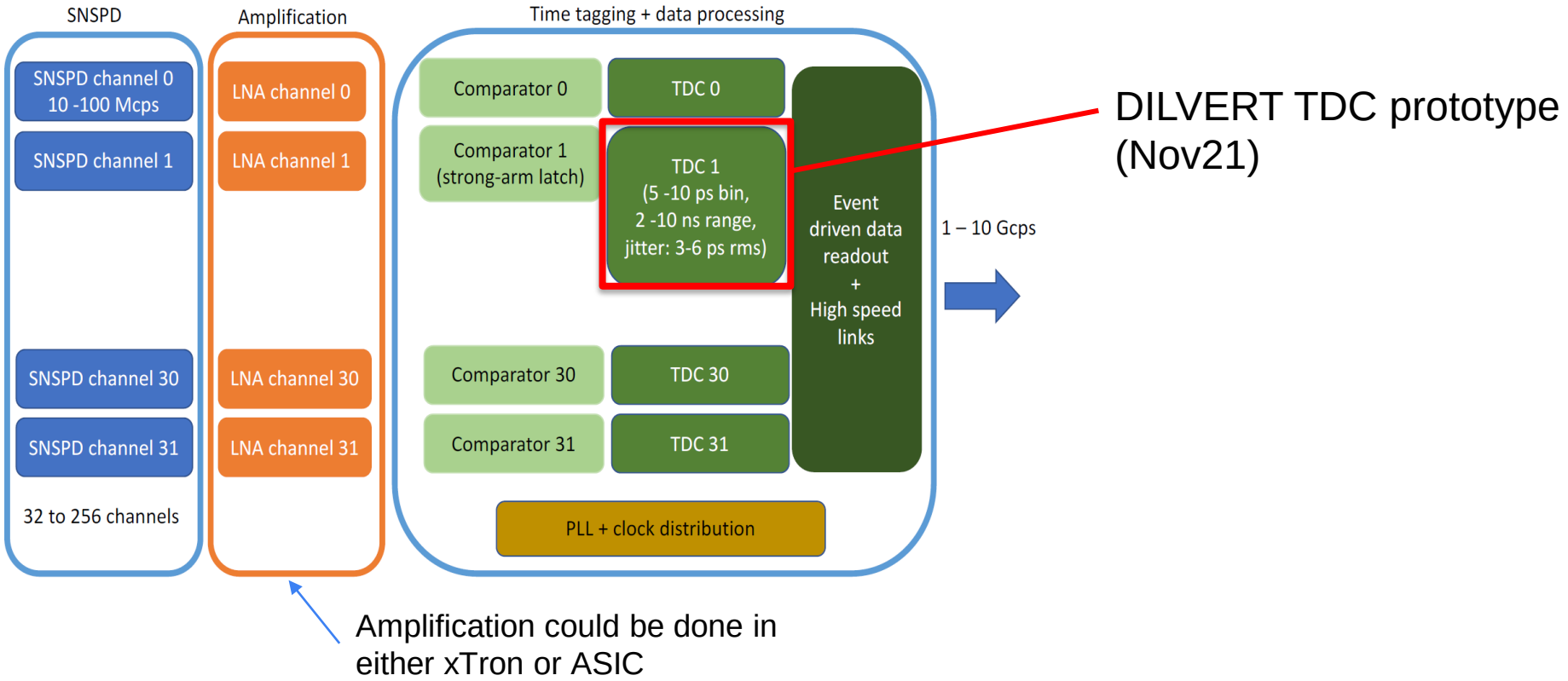
→ Ideally suited for feature extraction and data reduction at the edge

- Evaluating radiation hardness (fabrication and architecture) and optimal energy budgeting
- Developing increasingly complex circuits as well as work on yield

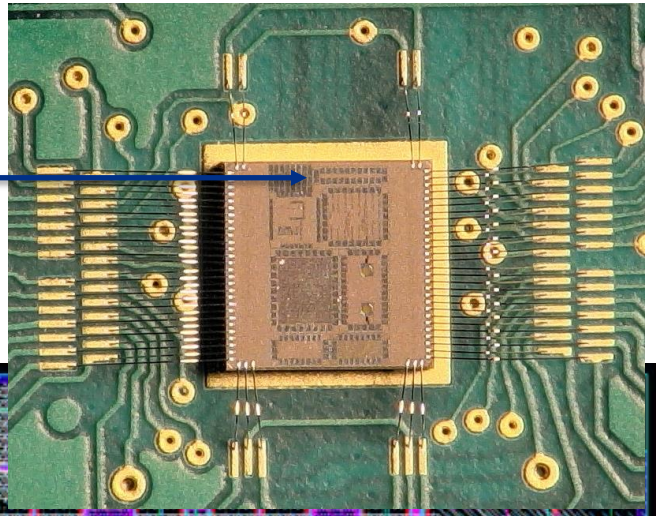


CryoCMOS ASIC

- Operation at <4K demonstrated in modern, state-of-the-art commercial processes (no special processing)
- Leverage low power, high performance ASICs for signal conditioning, time-tagging, data concentrator/edge computing, and serialization/readout



Test Chip 11/2021



≈ 250 µm

≈ 1000 µm

≈ 20 µm

[DILVERT_digital]

≈ 150 µm

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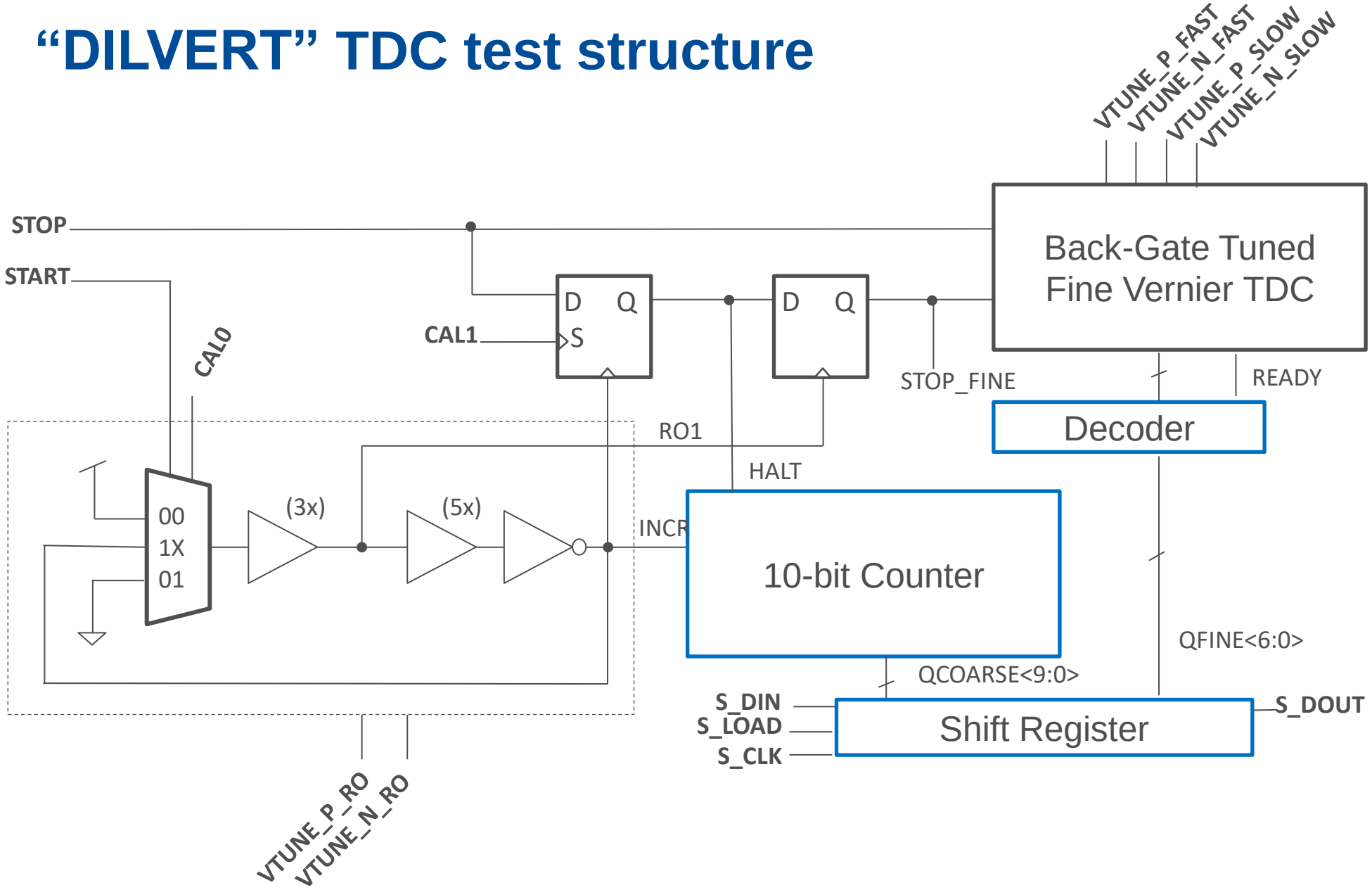
“DILVERT” TDC test structure

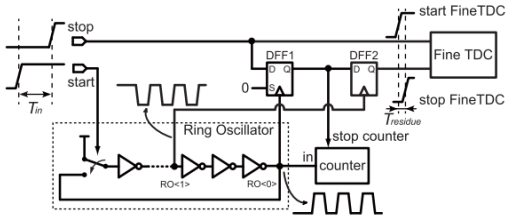


Total Pins: 22

- 6 analog inputs
- 7 digital inputs
- 3 digital outputs
- 6 power pins

Not Shown:

* RO1, HALT, INCR, and STOP_FINE are mux’d to **two** digital outputs with the select done by 4 shift register bits.
* RESET pin



Enomoto et al. [2]

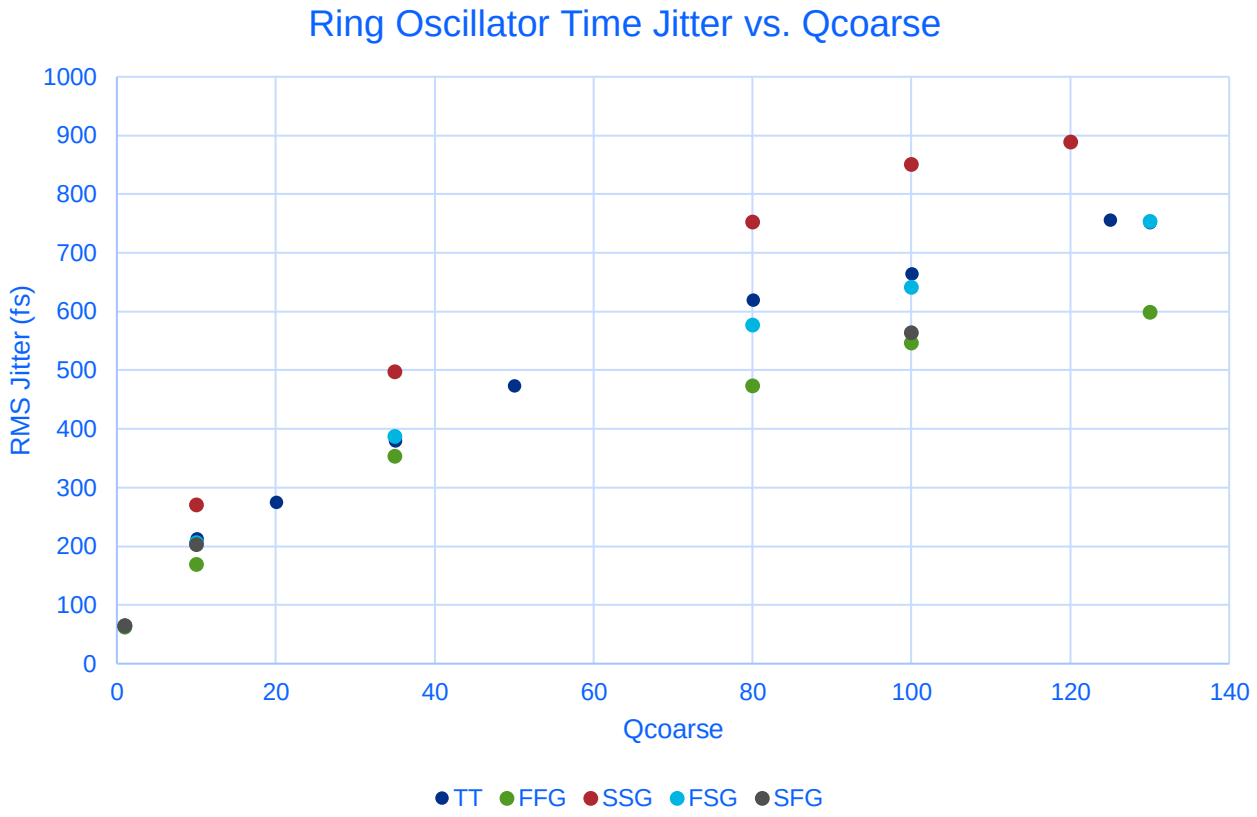
Fermilab

Simulation Results: TDC Jitter vs T_{in}

$$\sigma_{jitt} = \sigma_{tp} \times \sqrt{N_{stage} \times 2} \times \sqrt{Q_{coarse}}$$
$$= \kappa_{jitt} \sqrt{Q_{coarse}}$$

Assuming that maximum allowable jitter is approximately ½ LSB:

Corner:	TT	FF	SS	FS	SF
κ_{jitt} [fs]	66.18	55.9	80.7	65.0	61.7
$\sigma_{jitt(max)}$ [fs]	1.3	1.0	1.8	1.4	1.2
$Q_{coarse(max)}$	385	320	497	463	378
Dynamic Range [ns]	**55.4**	40.2	83.7	68.5	53.1



State of the Art

	Chen ‘17	Sesta ’18	Enomoto ‘19	Palaniappan ‘19	Khaki ‘21	Lee ‘21	**DILVERT (sim) ’21**
Architecture	ΔΣ TDC	Counter + Vernier Delay Line	Counter + Pulse-Shrink Delay Line	Cap Boost Vernier Delay Line	ΔΣ TDC w/ GSRO	SAR TDC	Counter + Vernier Delay Line
Process	65nm	0.35 μm	0.18 μm	180 nm	40nm FPGA	130nm	22nm SOI
Resolution	0.48 ps	7 ps	2.0 ps	1.74 ps	0.18 ps	6.6 ps	2.7 ps
Dynamic Range	-	80 ns	120 ns	0.112 ns	4.5 ns	1.7 ns *	55.4 ns
Power	3 mW	-	18 mW	0.217 mW	9.24 mW	0.504 mW	0.5 mW
Rate	-	20 MS/s *	3.3 MS/s	50 MS/s	1600 MS/s	10 MS/s	100 MS/s
FoM	-	-	3.33	0.30	2.71	0.51	41.04

$$FoM = \frac{[\text{Dynamic Range in ns}]}{[\text{Power in mW}][\text{Resolution in ps}]}$$

* = calculated from available data

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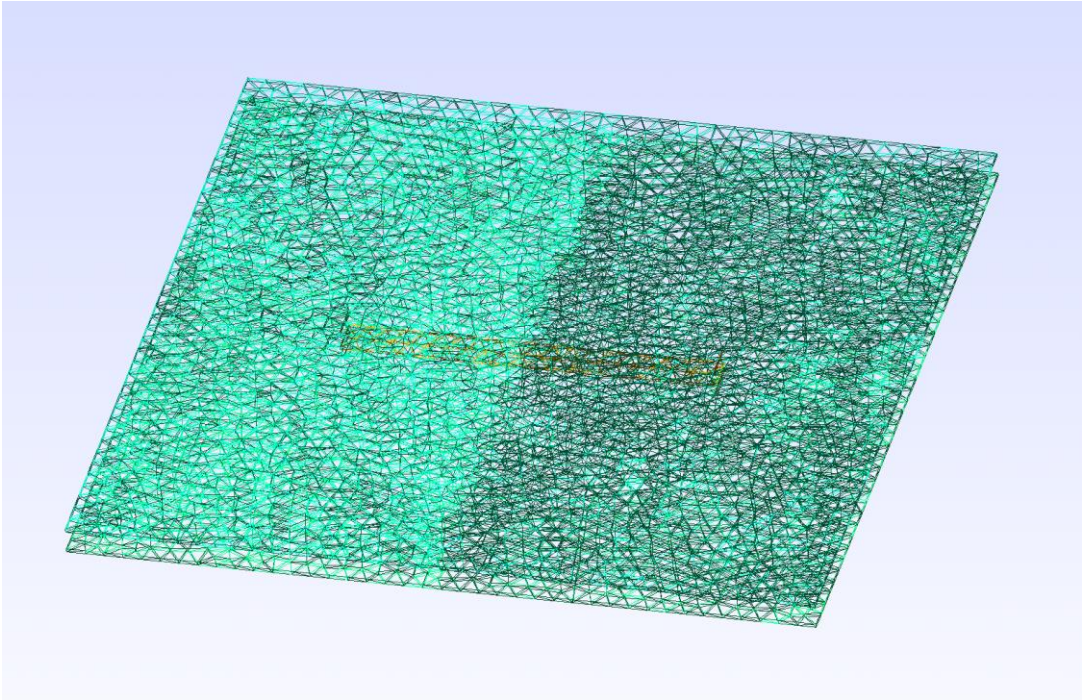
Superconducting Electronics

PDK and Tools

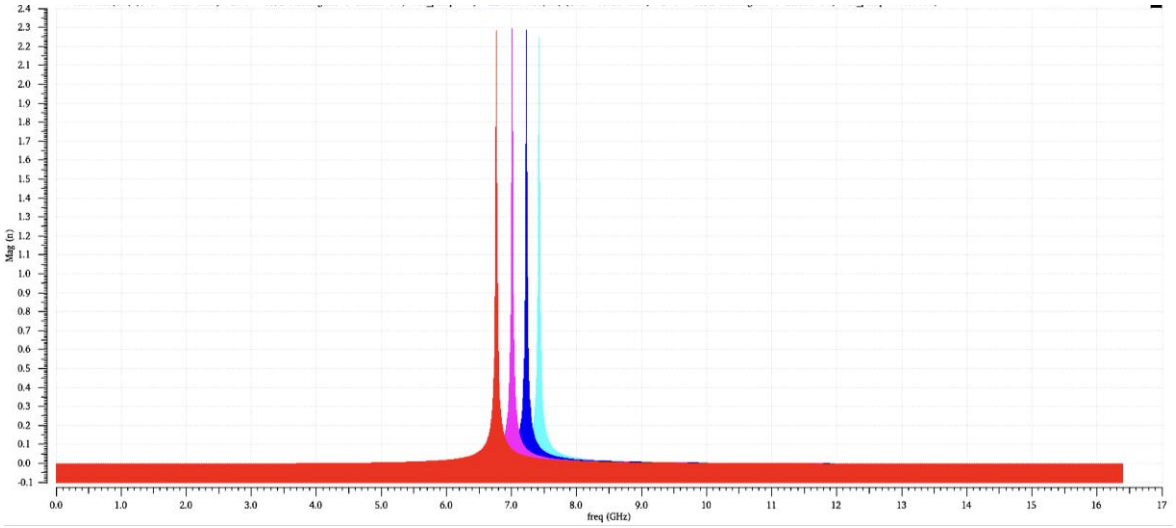
- MIT-LL SFQ5ee Superconducting Process
- LVS and DRC decks compatible with existing toolset at Fermilab
- InductEx EM Solver has support for SFQ5ee



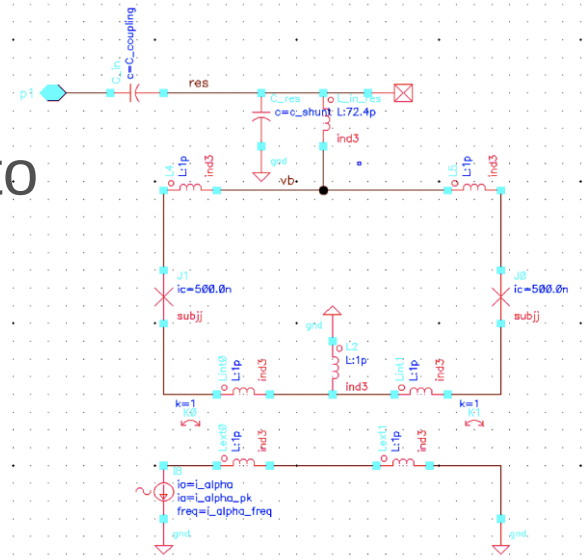
Mesh of EM test structure

Superconducting Amplifiers

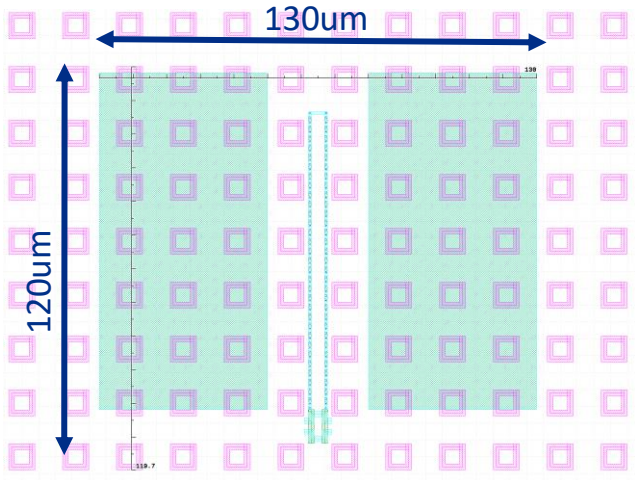
- TWPAs and JPAs for ADMX-BREAD using a super conducting fab at MIT-LL
- Collaborating with Washington University at St. Louis
- Established design flow for Josephson Parametric Amplifiers (JPA)
- Using JPA design flow as a foundation to study Traveling-Wave Parametric Amplifiers (TWPA)
- Layout of compact JPA using MIT LL SFQ5ee PDK



JPA Simulation



JPA Schematic



JPA Layout

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AI-on-chip : To solve the HEP data challenge

AI-on-chip: data processing at source

Hardware - software codesign, driven by edge compute: Processing data at source, real-time feedback and control.

- **1st AI-on-Chip for HEP**: Radhard, Low-power, Low-latency Autoencoder - **Tested and working well !!!!**

  ECON-T for HG CAL **(7-20x data compression: 48 pixel,** Inference every 25 ns**).** Established design methodology.

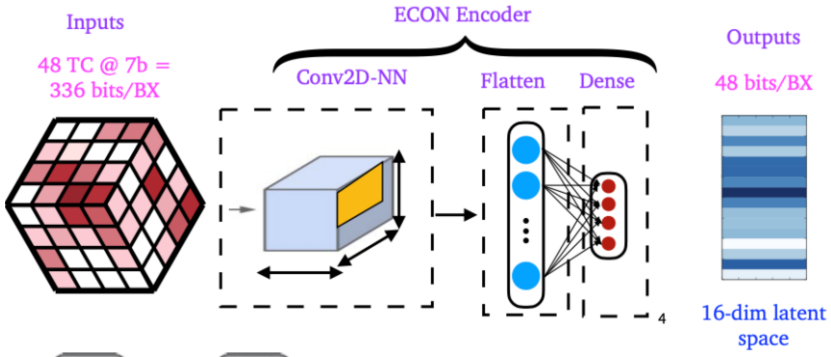
  Working with Siemens/ Mentor Graphics for integrating hls4ml with Catapult HLS

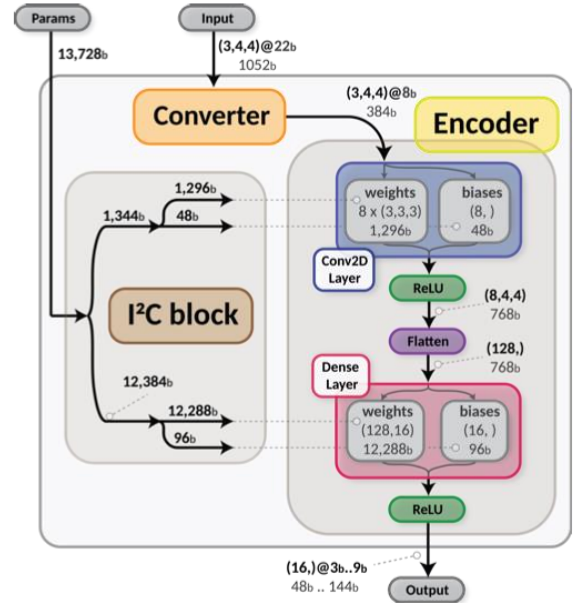
- AI-in-Pixel: **Data processing at source**

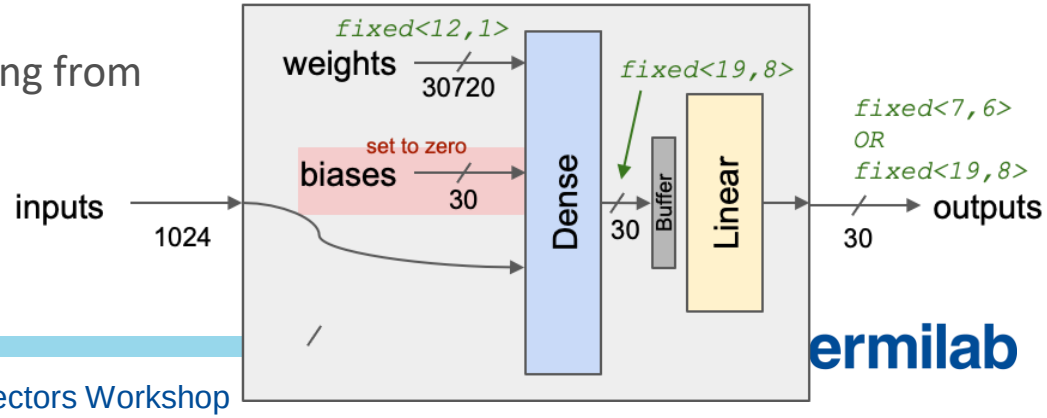
  In-pixel PCA vs. Autoencoder **(30x - 80x data reduction: 1024 pixel)**

  Algorithm utilizes the extremely redundant data structure to achieve a high compression ratio while maintaining good image reconstruction capability

  Establishing new design flow to overcome implementation challenges arising from routing congestion







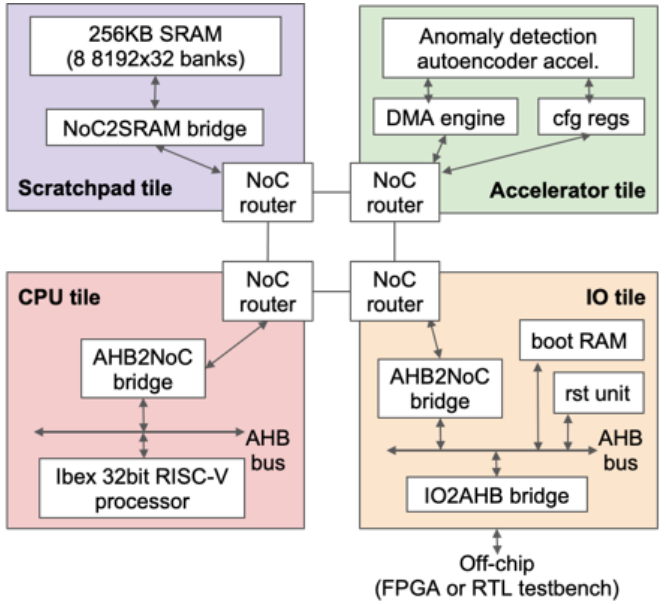
ermilab

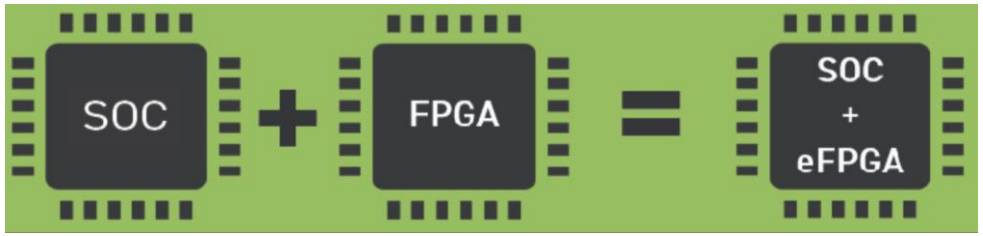
Reconfigurable Edge AI – Solve the HEP data challenge

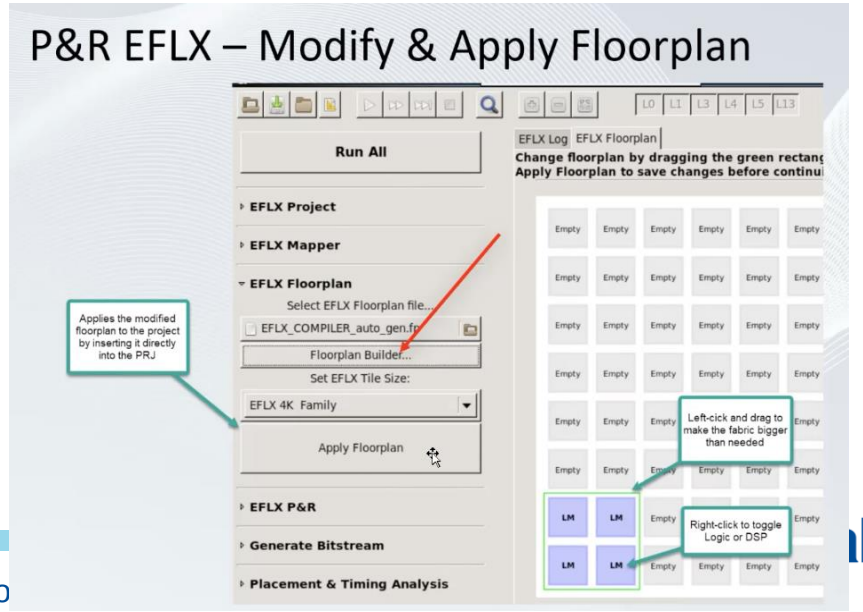
- Collaboration with Columbia U. & Northwestern U.
- Edge AI: Combining two established open-source platforms (ESP and HLS4ML) into a new system-level design flow to build and program a System on chip

  In the modular tile-based architecture, we integrated a low-power 32-bit RISC-V microcontroller (Ibex), 200KB SRAM-based memory, and a neural-network accelerator for anomaly detection utilizing a network-on-chip.

- Embedding FPGAs on detector: Radhard/ cryogenic eFPGA on-chip – with Flex Logix (22nm / 28nm). Establishing design flow and investigating extreme environment performance







Thank you!