



Insights on frontend organization and specifications

(very EIC Detector-1 oriented)

Irakli Mandjavidze

*Irfu, CEA Saclay
Gif-sur-Yvette, 91191
France*

Streaming Readout X

JLAB, May 17-19, 2022



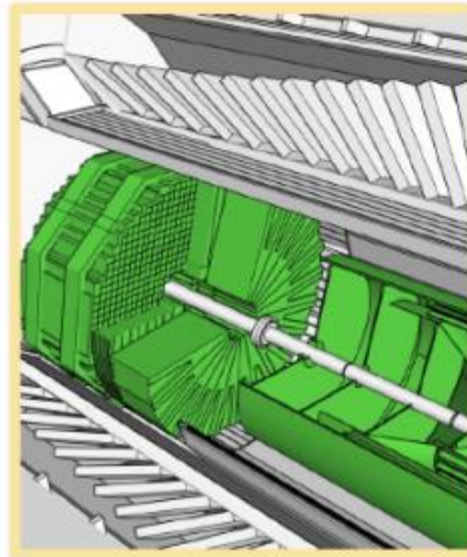
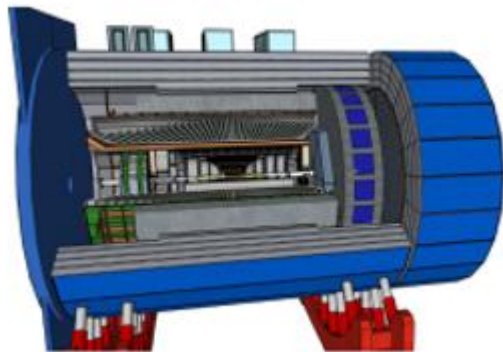
Outlook

- Frontend organization
- Timing & clock
- Power / slow control / monitoring
- Run control
- Data
- Integration
- Summary

Rather questions than answers from a designer who needs to build a frontend for EIC detector

EIC Detector

- Diversity of technologies



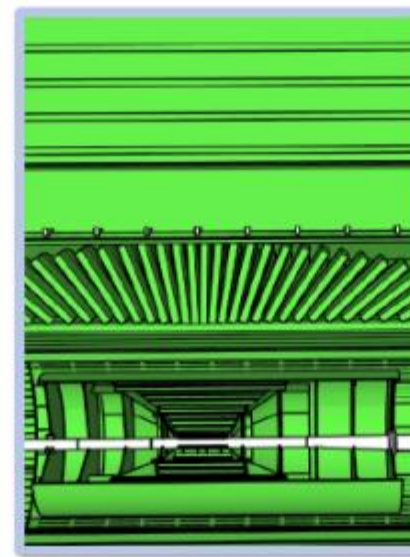
Backward Endcap

Tracking:

- ITS3 MAPS Si discs (x4)
- AC-LGAD

PID:

- mRICH
- AC-LGAD TOF
- PbWO₄ EM Calorimeter (EEMC)



Barrel

Tracking:

- ITS3 MAPS Si (vertex x3; sagitta x2)
- μRWell outer layer (x2)
- AC-LGAD (before hpDIRC)
- μRWell (after hpDIRC)

h-PID:

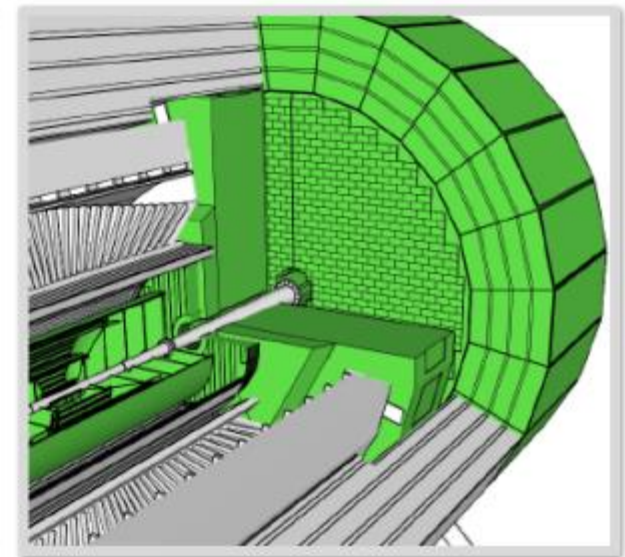
- AC-LGAD TOF
- hpDIRC

Electron ID:

- SciGlass EM Cal (BEMC)

Hadron calorimetry:

- Outer Fe/Sc Calorimeter (oHCAL)
- Instrumented frame (iHCAL)



Forward Endcap

Tracking:

- ITS3 MAPS Si discs (x5)
- AC-LGAD

PID:

- dRICH
- AC-LGAD TOF

Calorimetry:

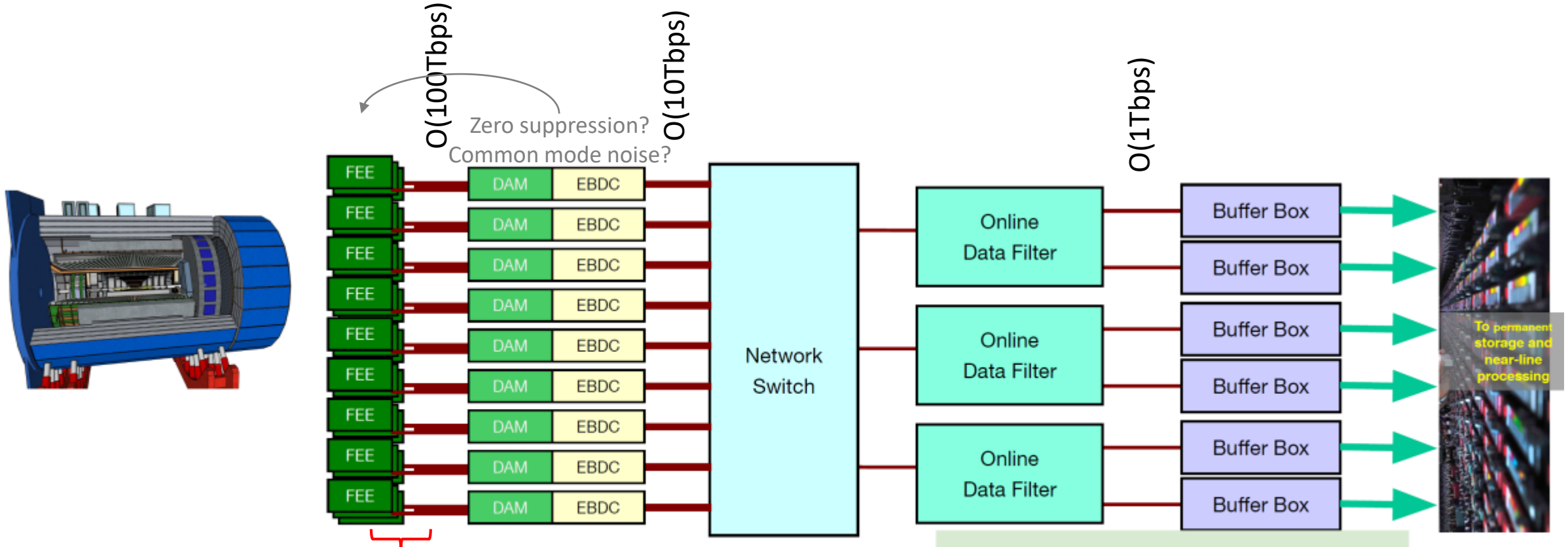
- Pb/ScFi shashlik (FEMC)
- Longitudinally separated hadronic calorimeter (LHFCAL)



O(20 million) electronics channels

EIC Detector

- Uniform streaming DAQ



Uniformization happens here

Subject of this presentation



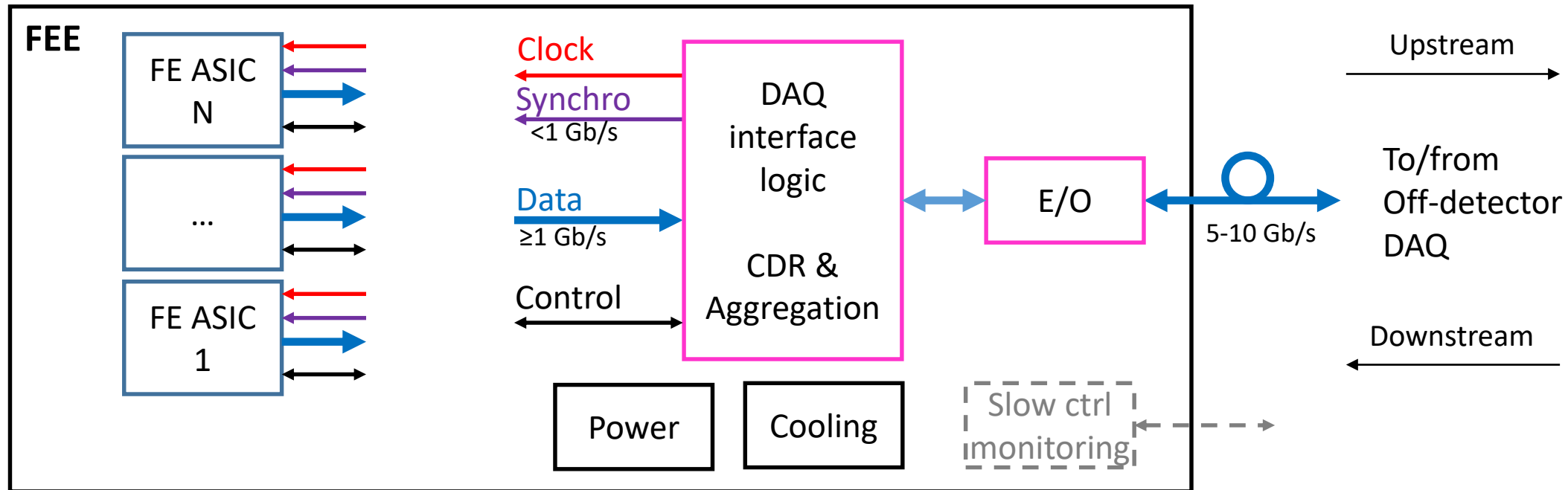
FEE = Front End Electronics
 DAM = Data Aggregation Module
 EBDC = Event Buffer / Data Compressor



Frontend electronics

- A popular organization of recent years

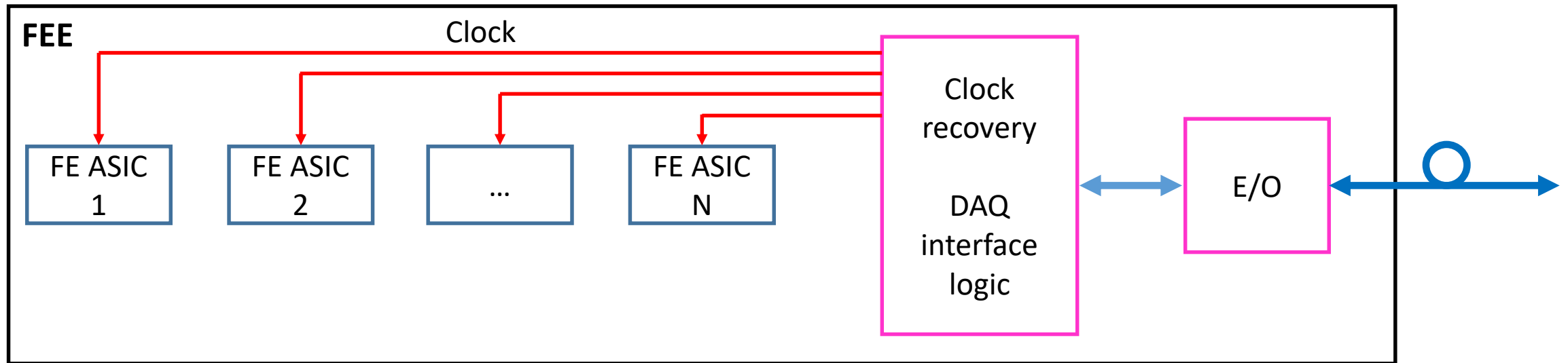
- A bi-directional optical link for clock, synchronization (run control), data, configuration
 - Also for slow-control and monitoring, at least partially
- Obviously detector-family specific frontend chip
- Common e/o interface



- DAQ interface logic: how common can it be to a majority of sub-detectors, if not to all?
 - Like the IpGBT ASIC for the LHC experiments (coupled with e/o VTRX+)
 - Or if implemented in FPGA, with a common framework and sub-detector specific modules

A centralized effort within the EIC project for DAQ interface and link?

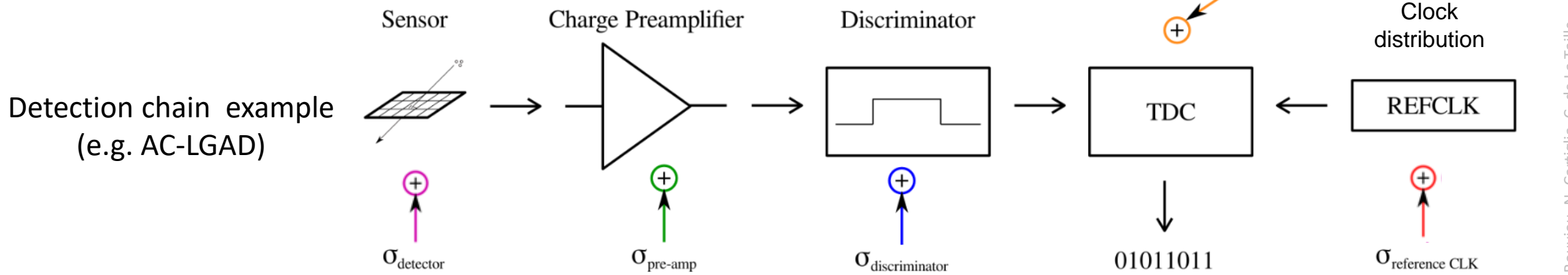
Clock distribution and timing





About timing and clock distribution

- Clock quality is only one part in long list of contributions determining resulting timing precision
 - Quadratic sum of contributions



$$\sigma_t^2 = \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2 + ([TDC]_{RMS})^2 + ([CLK]_{RMS})^2$$

Example timing figures are approximates

→ For large signals: 25ps 15ps ≈0 15ps 10ps

- Marginal improvement pushing clock quality to 5ps RMS jitter

→ For small signals: major contribution from sensor / preamplifier / discriminator

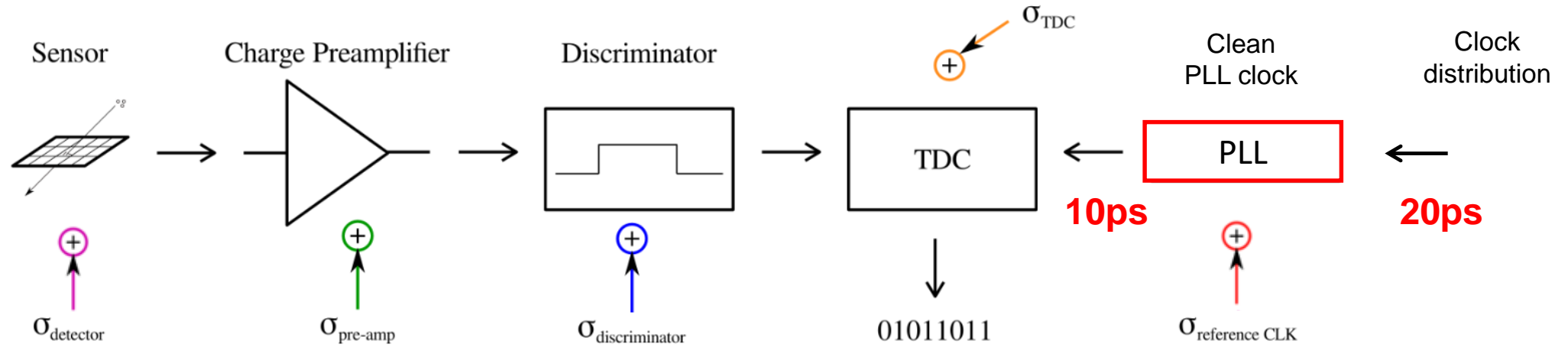
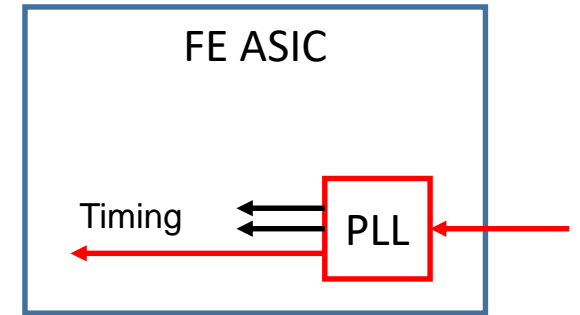
Precision clock distribution is extremely complex: do not over-constraint requirements

© Lukas Perktold, F. Bouyjou, N. Cartiglia, C. de La Taille, ...

About timing and clock distribution

- FE ASICs with jitter cleaner PLLs

- Generation of internal clocks including the one used for measurements
- Common for precision timing ASICs

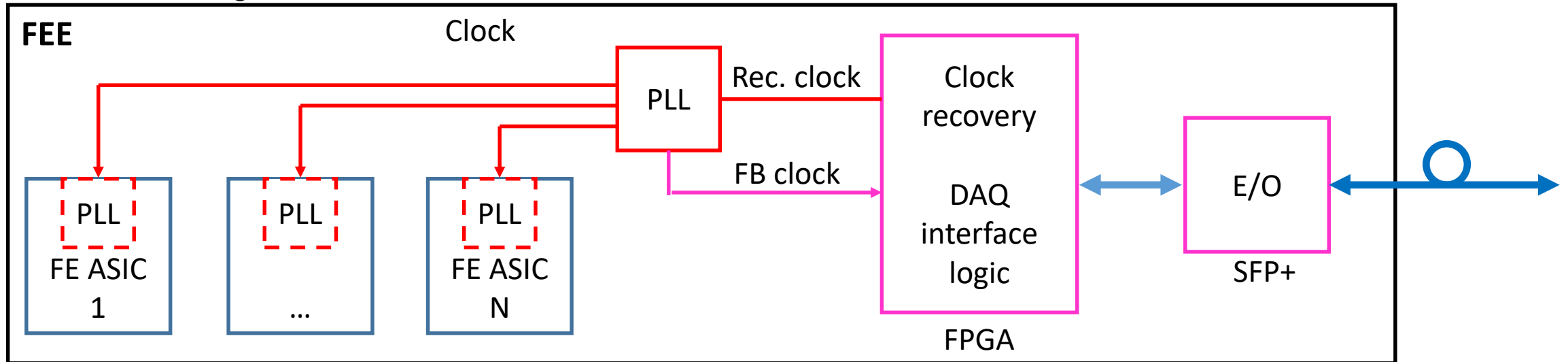


Requirements on clock distribution system may be somewhat relaxed

About timing and clock distribution

- Frontend clock distribution with COTS components

→ Assuming low radiation level allows their use



- The quality of recovered by FPGA clock may not be enough for precision timing measurements

→ To be compared to the IpGBT performance: <4ps RMS jitter for 40 MHz recovered clock

- The use of an on-board jitter cleaner PLL is a common practice

→ SEU may cause phase shifts which are slow to recover, e.g. $O(10 \mu s)$

- Recovered clock must have the same phase as the distributed one

- Attention to power and environmental stability

→ Power modulation impact on clock jitter (RMS): $O(\text{few ps}) / \text{mV}$

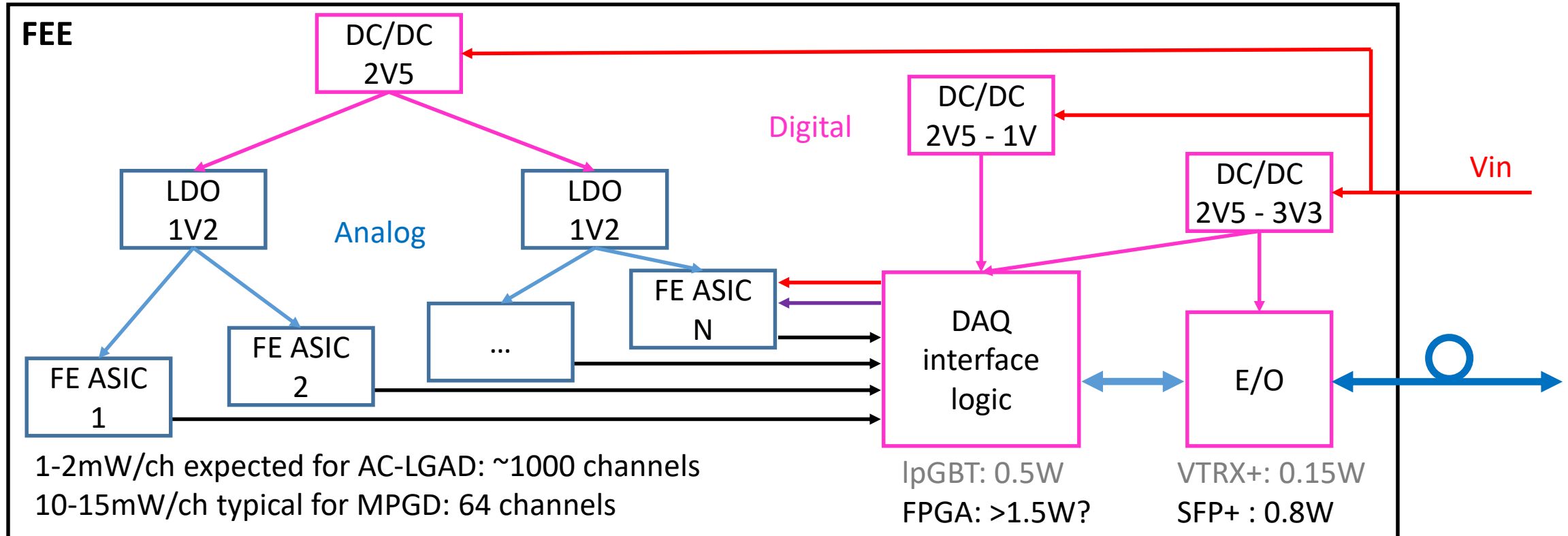


Power and slow control



Frontend power distribution

- 1.5 T magnetic field requires efficient power regulation
 - High efficiency DC/DC converter for digital power
 - LDO regulators for analog circuitry



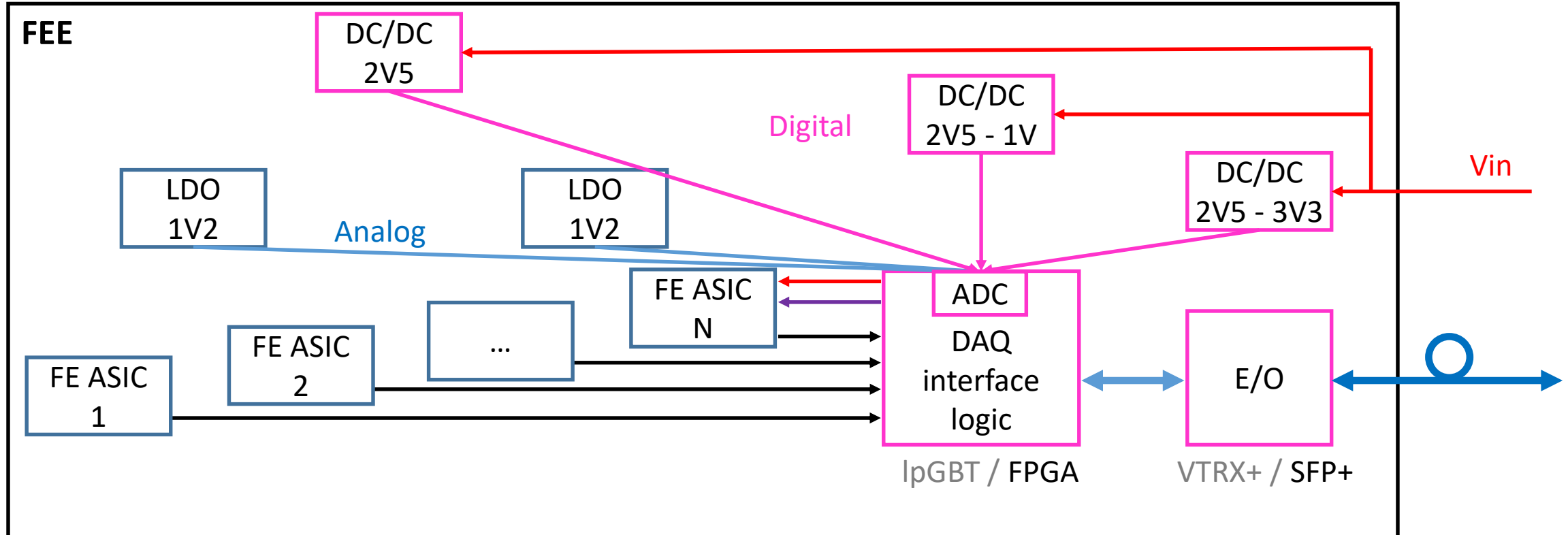
Common effort for magnetic field (and low radiation) tolerant power supply components?

Common effort to an uniform power distribution (and cooling) scheme?



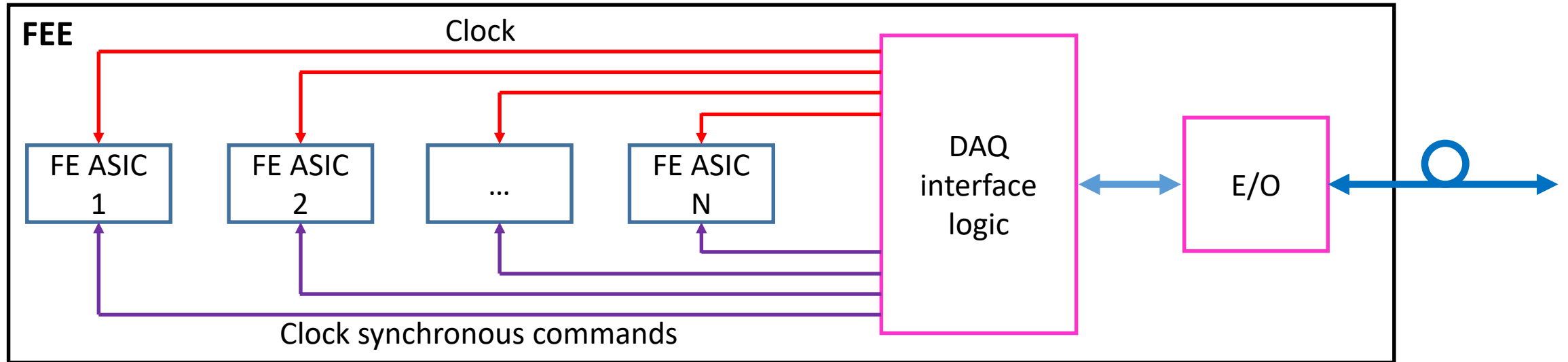
Frontend slow control and monitoring

- Part of the backend-fronted data flow over the bi-directional optical link
→ Embedded ADC to monitor on-board generated voltages, current, temperature



- An alternative of some kind field-bus and on-board micro-controller?
→ Possibility to detect corruption due to radiation and to reboot frontend (firmware)

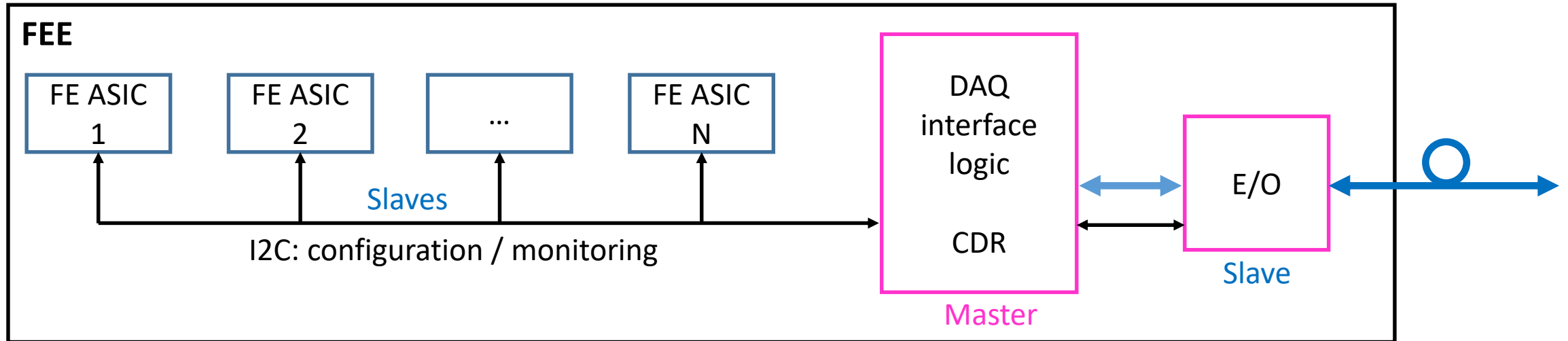
Run control



Frontend run control

- Run configuration

- A bi-directional frontend / backend link conveys I2C (SPI) protocol
- Several I2C chains may be needed if “N” is large
 - There is a companion GBT-SCA chip developed by CERN



- Avoid interoperability surprises

- Slaves are implemented by ASIC designers within different sub-detector groups
- Master is implemented by a (central) group

- An alternative of some kind field-bus and on-board micro-controller?

- Possibility to detect corruption due to radiation and to reboot frontend (firmware)



Frontend run control

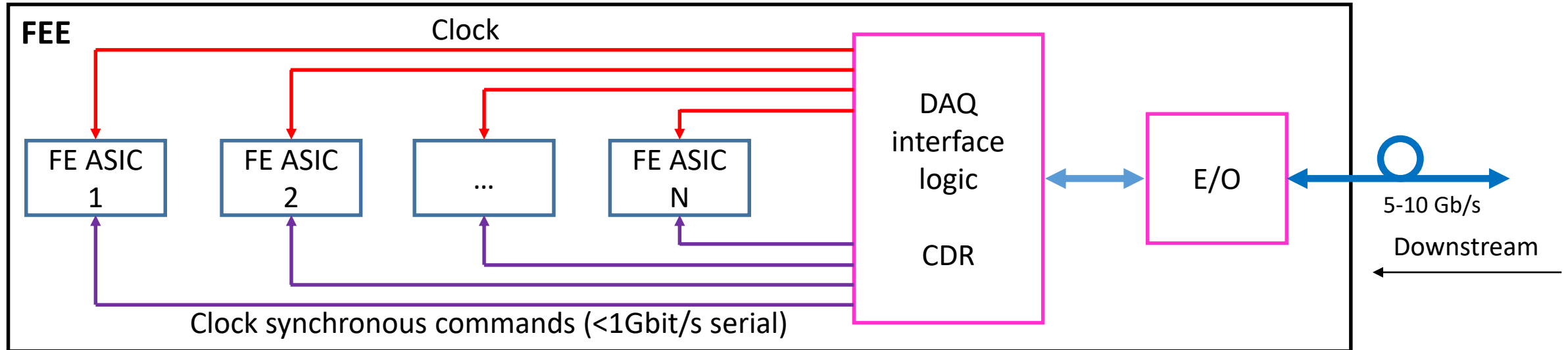
- Run control

- Clock synchronous commands

- Bx clock phase recover
- ReSync, Start / Stop, ...

- Synchronization of frontends at BX level – $O(\text{ns})$

- This is different from precision timing synchronization – $O(10\text{ps})$



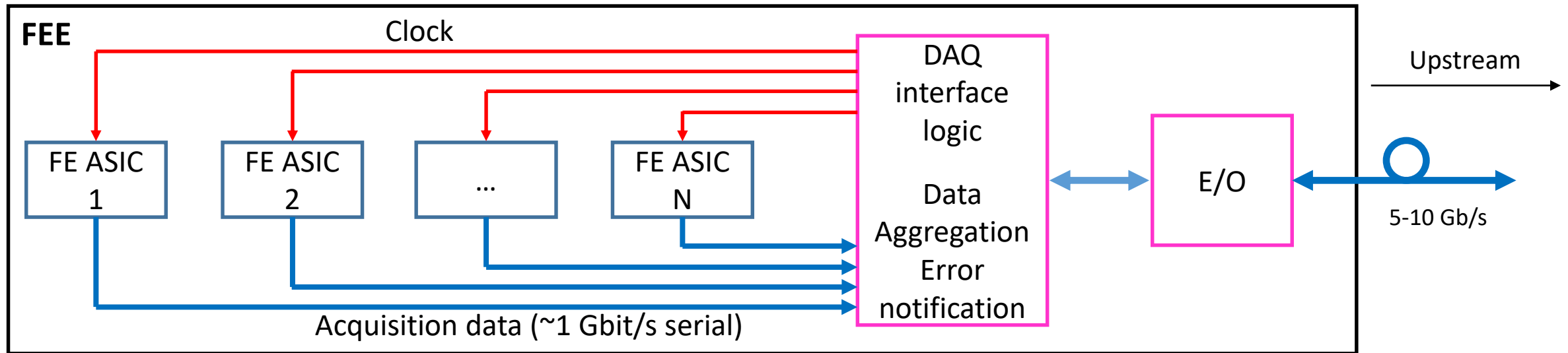
- A set of common broadcast synchronous commands

- Sub-detector specific multicast commands, e.g. calibration sequences, pedestal measurements

In opposite direction, from FE to DAQ, fast pass for error notifications is needed



Data



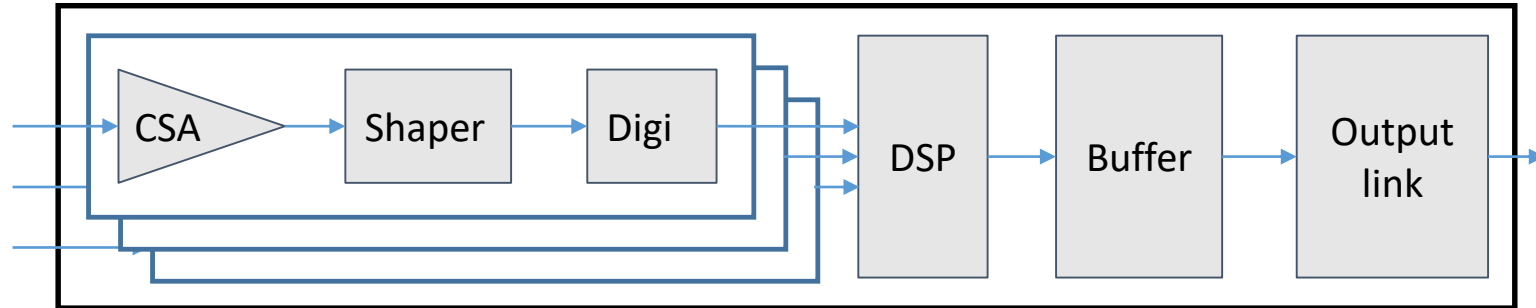
Example of a multi-channel ASIC for MPGD tracker

- FEE based on multi-channel MPGD ASICs

→ Compatible with streaming readout

→ Typical characteristics

- Gain: 10 down to 4 mV/fC
- Peaking time: 75 to 300 ns
- Detector capacitance: up to 400 pF
- 10-12 bit ADC; 10-20 ns timing



→ On-chip zero suppression

- Possibly with **common mode noise subtraction**
- **Peak finding ZS**: amplitude, time and ToT
- **Sampling ZS**: signal shape around ToT
- “Region of interest” ZS: if a strip exceeds a high threshold, forced or lower threshold reading of its neighbors

- ASICs

→ 64-channel **peak finding** VMM3a

→ 32-channel **sampling** Sampa

→ Next generation 64-channel **sampling** Salsa

- On-going initiative of Brazilian institutes (Sampa) and Irfu (AGET, Dream)
- See for example: <https://indico.cern.ch/event/1040996/contributions/4402636/>



MPGD ASIC data rate: ZS and common mode noise

- Assume a 64-channel sampling ASIC with 12-bit sample per channel
- Full readout of the ASIC - no ZS
 - 50 MSPS: 50 Gbit/s (including 20% overhead)
Not a realistic option: ZS is needed
- Coherent noise subtraction
 - Based on dedicated CMN channels in ASIC not connected to detector
 - Evaluates noise in chip / board but not coming from detector (and detector interconnect – e.g. cables)
 - Based on group of channels connected to consecutive detector strips
 - External to chip in streaming readout: **move 25-50 Gbit/s data out of chip**
 - External to chip in triggered readout: **doable**
 - If needed, perform coherent noise removal on chip prior to ZS

What about *in-situ* detector studies when full readout is necessary?

At low frequency with a dedicated “trigger” command? In a pre-scale mode?

Should not be overlooked when building the DAQ system



MPGD FEE data rate: **sampling readout**

- Sampling ASIC with 12-bit sample per channel
- Signal shape ZS
→ 500 ns readout window when signal is above threshold

- 64-channel ASIC (e.g. Salsa) and 512-channel FEE with 8 ASICs

Channel rate kHz	Sampling MSPS	Number of samples	64-chanel ASIC Mbit/s	512-chanel FEE Gbit/s	Remarks
2 (physics)	50	25	46	0.4	5-10 Gbit/s aggregation link unjustified
10 (safety)			230	1.9	5 Gbit/s aggregation link is enough
50 (Clas12)			1 150	9.5	20 Gbit/s aggregation link needed

- 32-channel (Sampa) based 256-channel FEE
→ 5-10 Gbit/s link can be justified for 50 kHz channel hit rates
 - See in backup



MPGD FEE data rate: **peak-finding readout**

- Peak-finding ASIC
- ZS with time-amplitude readout
 - Assume 12-bit timing, 8-bit ToT and 12-bit amplitude
- 64-channel ASIC (e.g. VMM3a) and 512-channel FEE with 8 ASICs
 - Or a new development

Channel rate kHz	64-chanel ASIC Mbit/s	512-chanel FEB Gbit/s	Remarks
2 (physics)	5	0.04	5-10 Gbit/s aggregation link unjustified
10 (safety)	25	0.2	
50 (Clas12)	125	1	2 Gbit/s aggregation link is enough

- Knowledge of channel occupancies (physics, background, noise) is important to optimize aggregation

Is it acceptable to have an important number of high rate links frankly underused?

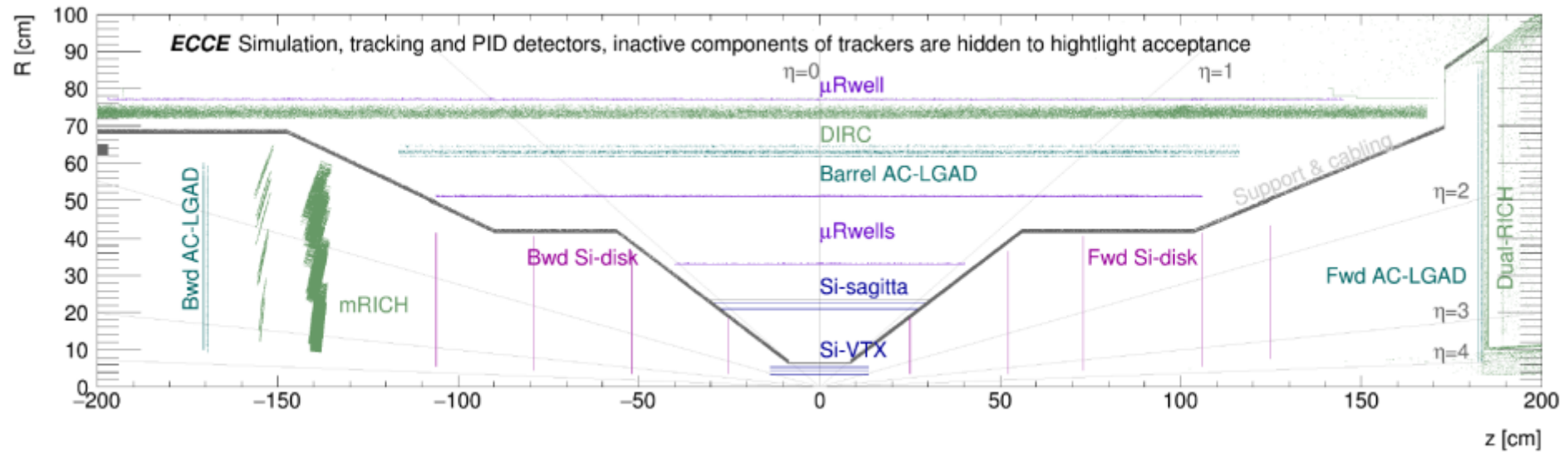
e.g. power, cost

Is it worth to complicate system adjusting link speeds?

e.g. 2-stage aggregation, cost



Integration





An MPGD tracker

- A 4-layer ~66k-channel cylindrical Micromegas barrel tracker studied for Athena

→ Scarce space for electronics even if placed in the cracks on both sides

- Readout link
- LV, HV, gas
- Cooling

→ Magnetic field

→ Material budget restrictions

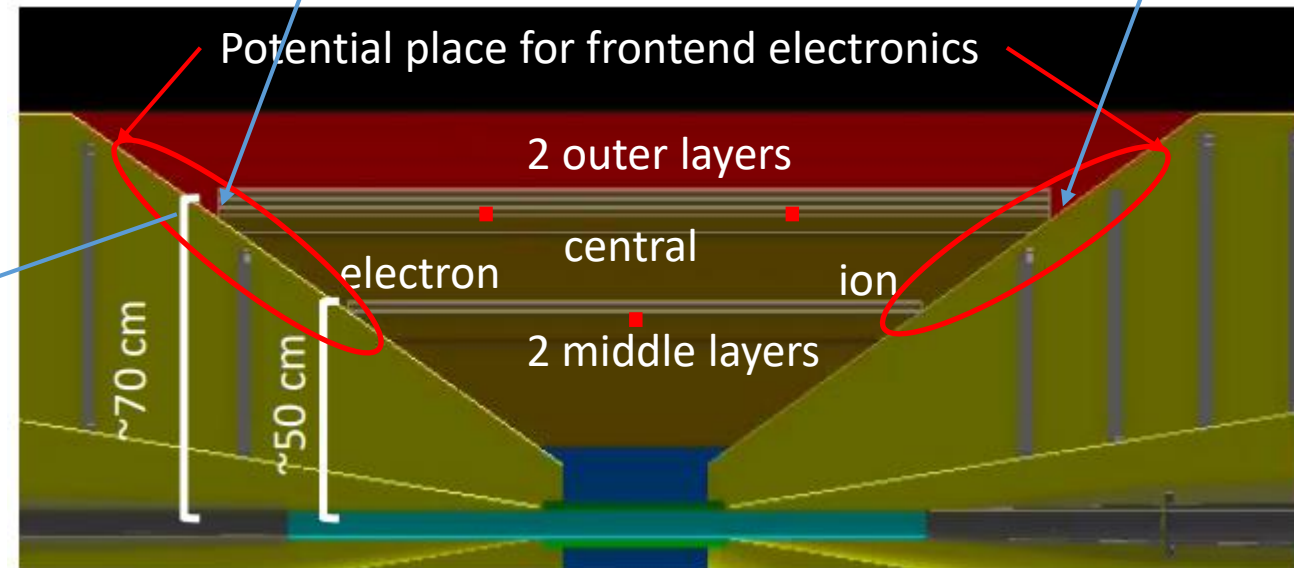
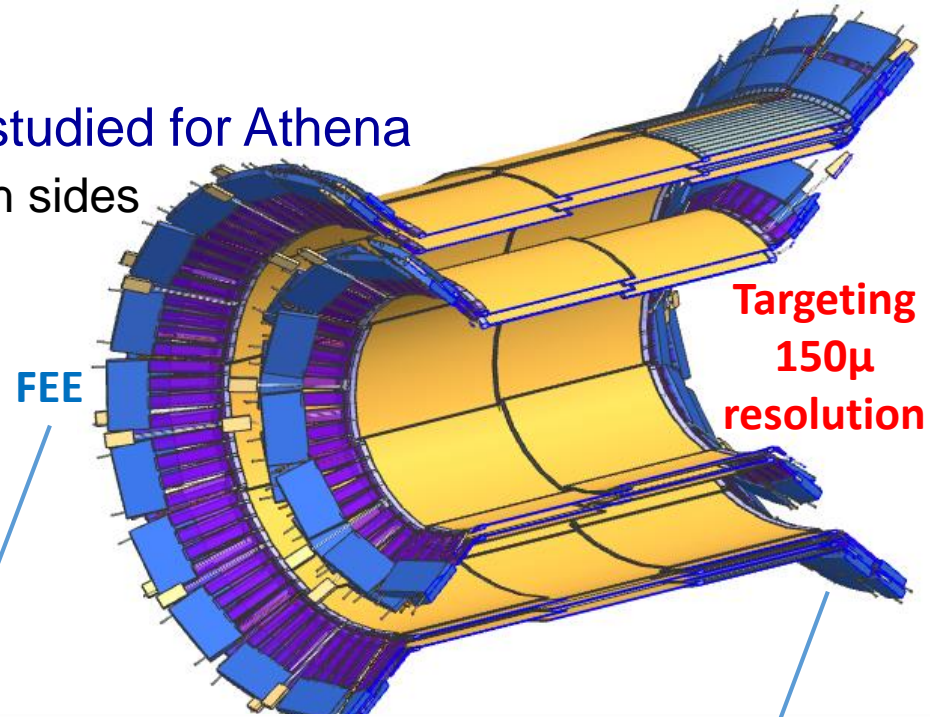
- Impact on cooling

→ Radiation?

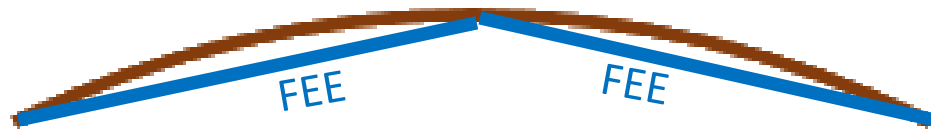
- FEE length determined by detector geometry

→ Must contain enough chips to read the region

- Single row of ASICs – closest to detector
- Simplify interconnect



Elementary detection tile

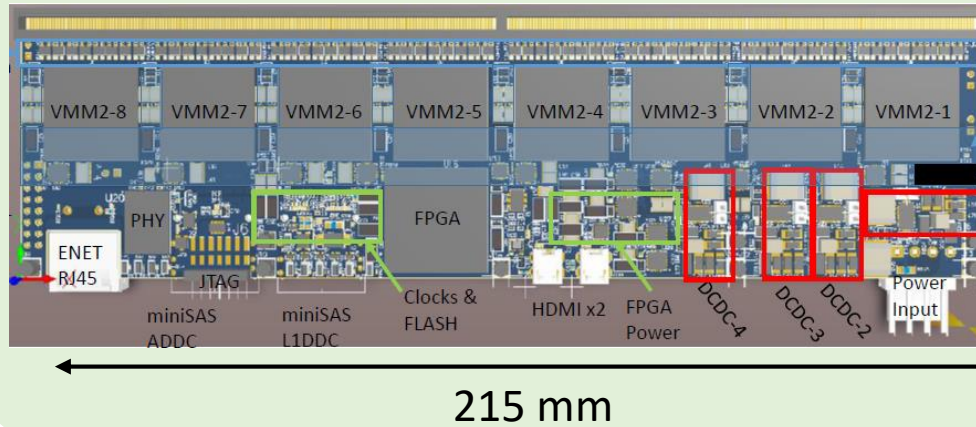


FEE constructions that could fit

- A 4-layer ~66k-channel Micromegas barrel tracker studied for Athena

- 64-channel ASIC
- 132 units of 512-channel FEE
- 225 mm to fit 8 ASICs

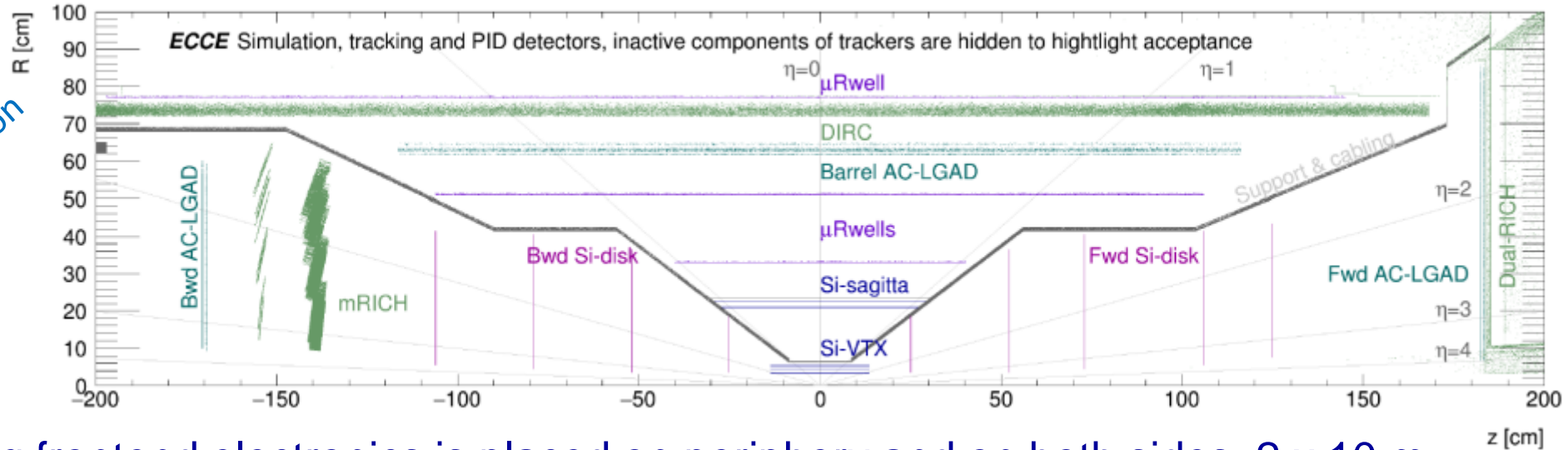
Illustration: Atlas FEM8 prototype
512 channels: with 8 VMM3a: 215 x ~60



- Detector-FEE connectivity with modest 0.8 mm pitch could fit
- 32-channel (Sampa) based 256-channel FEE fits too (backup)
- Looks encouraging, but...

Example of integration challenge

- ... 280k-channel 3-layer μ RWell cylindrical tracker in the same volume targeting 50μ resolution



Still under definition

- Assuming frontend electronics is placed on periphery and on both sides: $2 \times 10 \text{ m}$

- 64-channel VMM: $21 \text{ mm} \times 21 \text{ mm}$ package

→ 4.5K chips required

→ 768 chips can be placed in a single row

- Even less denser for 32-channel (Sampa) based 256-channel FEE (backup)

→ Multi-layer FE stack with several rows of ASICs?

Place for electronics and services is scarce – collaboration of subsystems to share it



Summary

- Frontend electronics specifications
 - Sub-detector: interface, S/N, dynamic range, saturation, timing, channels, data, environment, mechanics
 - Sub-detector responsibility (e.g. some hints for MPGD in backup)
 - Common: data aggregation, clock and command distribution, configuration, monitoring, protocols
 - Led by a central DAQ group
- Protocol / format definition
 - Transport layer: common to most (all?) sub-detectors
 - Application layer: data, synchro commands, errors: all sub-system comply
- Clock distribution
 - Do not over-constraint – it is not easy
 - Experience with CERN developments
 - e.g. TCLINK IP: Timing Compensated Link
- Common efforts welcome (needed, required)
 - DAQ interface logic and optical bidirectional link
 - COTS components validation for magnetic field and radiation
 - Power regulators
 - FPGAs, optical transceivers, PLLs
 - Components within the HEP community
 - e.g. DC-DC and linear regulators, precision clock fan-out, IP blocks

Central DAQ group in close collaboration with sub-detectors?

eRD104 – Silicon service reduction



Backup

Some links

- Xilinx, Device Reliability Report

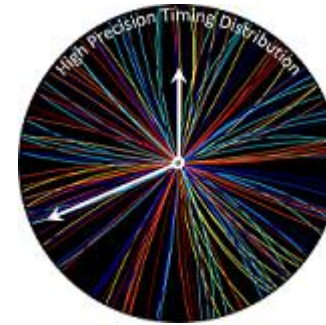
→ <https://docs.xilinx.com/v/u/en-US/ug116>

→ Single event upsets, among others



- High Precision Timing, CERN

→ <https://ep-ese.web.cern.ch/project/high-precision-timing>



- Versatile Link, CERN

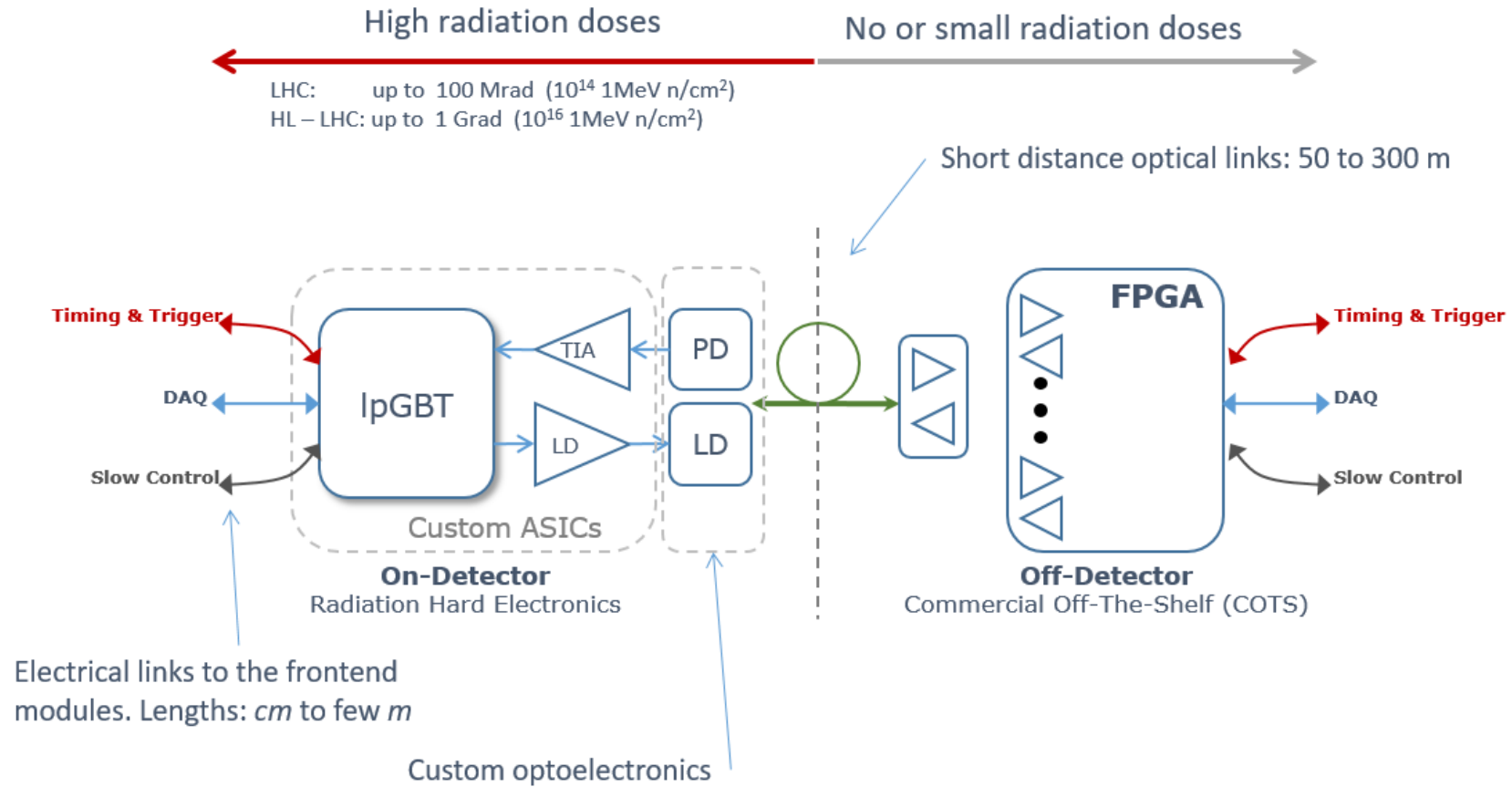
→ <https://espace.cern.ch/project-versatile-link/public/default.aspx>





Versatile link @ CERN

IpGBT Link Architecture



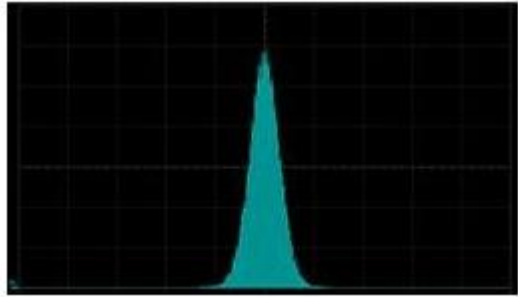


Clock

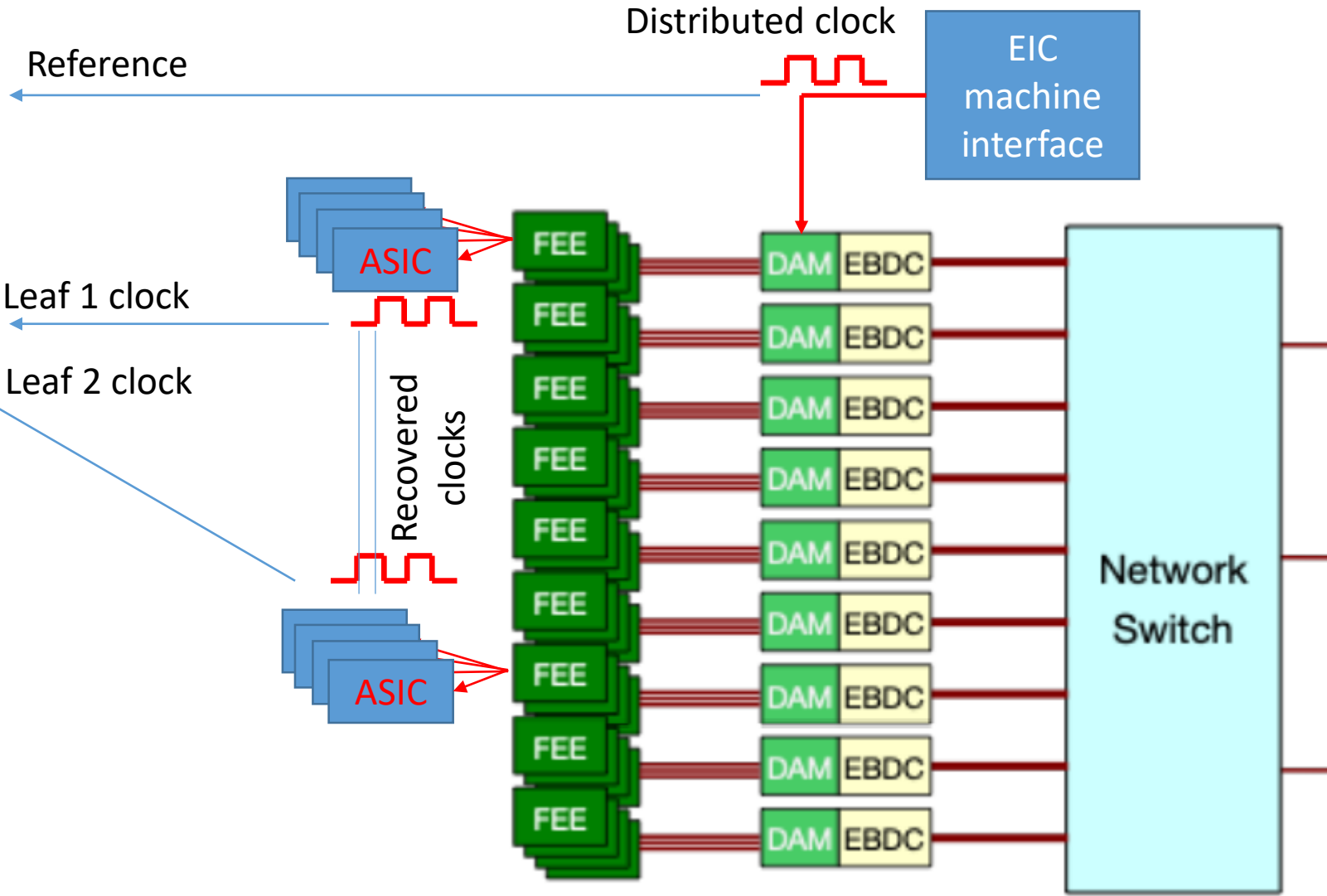


Precision clock distribution

High speed scope



Leaf TIE jitter
Leaf to leaf jitter
Leaf to reference jitter
RMS: **xxx** ps



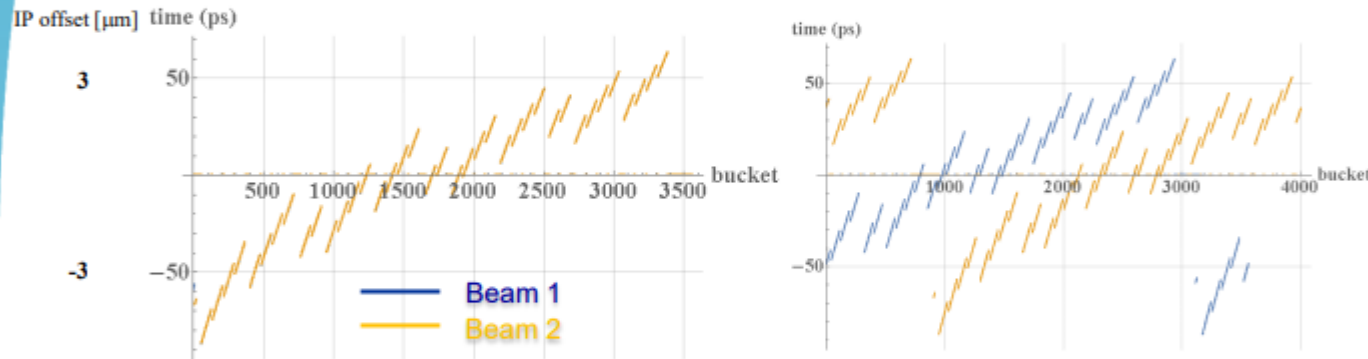
Different means to compensate high, middle and low frequency phase variations of clocks on different leaves



Expected bunch crossing phase change @ HL-LHC

Other features

- In order to operate at double current as compared to LHC with the available klystron power we will have to operate in the so-called “full detuning mode” the main 400 MHz RF system → **Modulation of the bunch arrival time over the machine turn $\sim \pm 70$ ps**



IP1/5 – symmetric for symmetric filling patterns

IP2/8 – asymmetric even for symmetric filling patterns

- modulation of the transverse position** of the collision point at **IP1-5** in the crossing plane and **modulation of the longitudinal position** of the collision point in **IP2-8** ($\sim \pm 1$ cm) → $\sim 1\%$ lumi. modulation

2016
Can this be calibrated out?

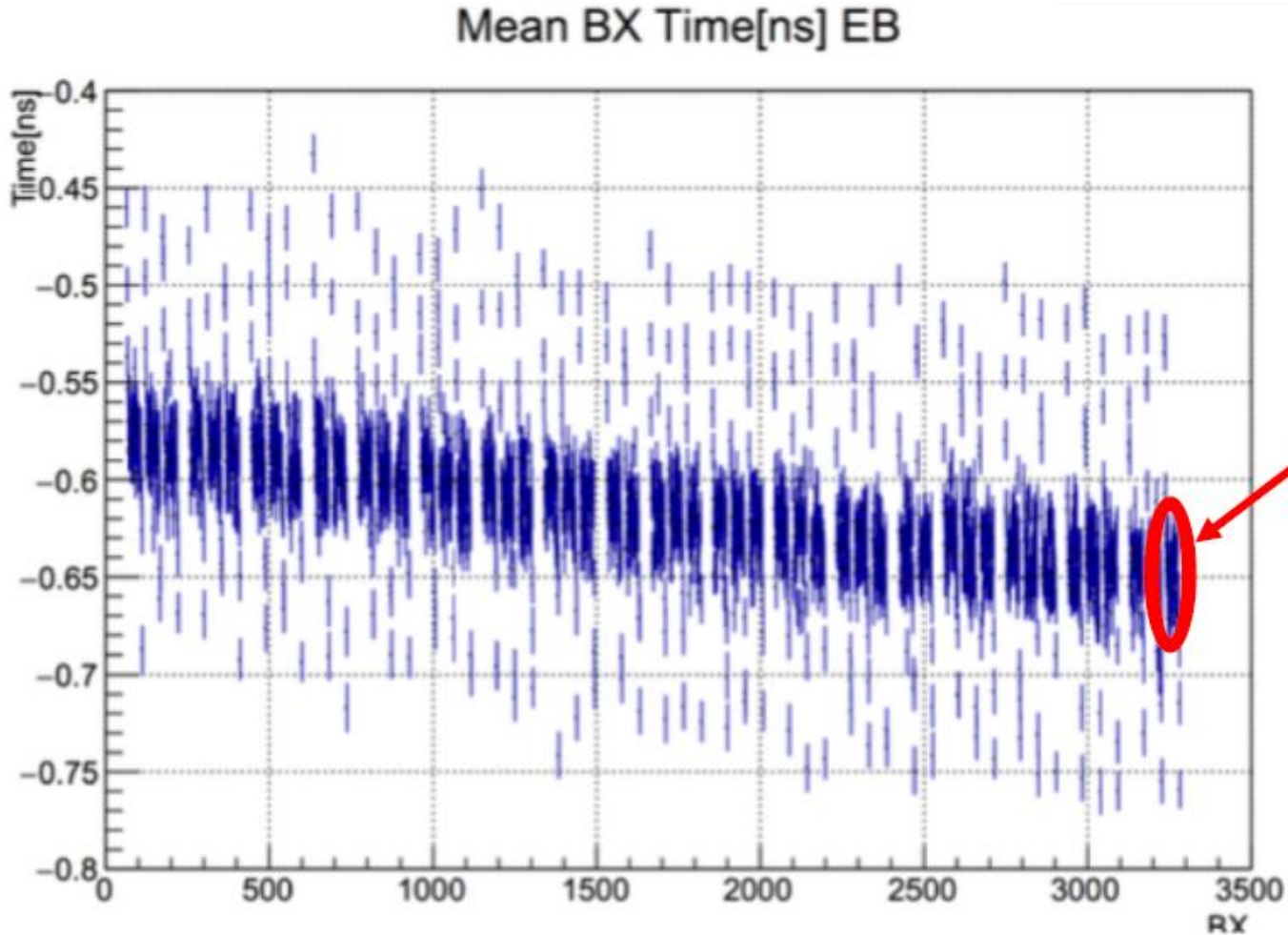


G. Arduini, R. Tomas - 3rd ECFA HL-LHC Meeting

10



Bunch crossing phase change measured in with CMS ECAL data



- Data derived from ECAL
– Extracted from a 4 hour run from 11h00 to 15h00)

This correspond to the fact that
The phase is proportional to the
Mean current in a turn

$\langle I \rangle_{\text{turn}}$

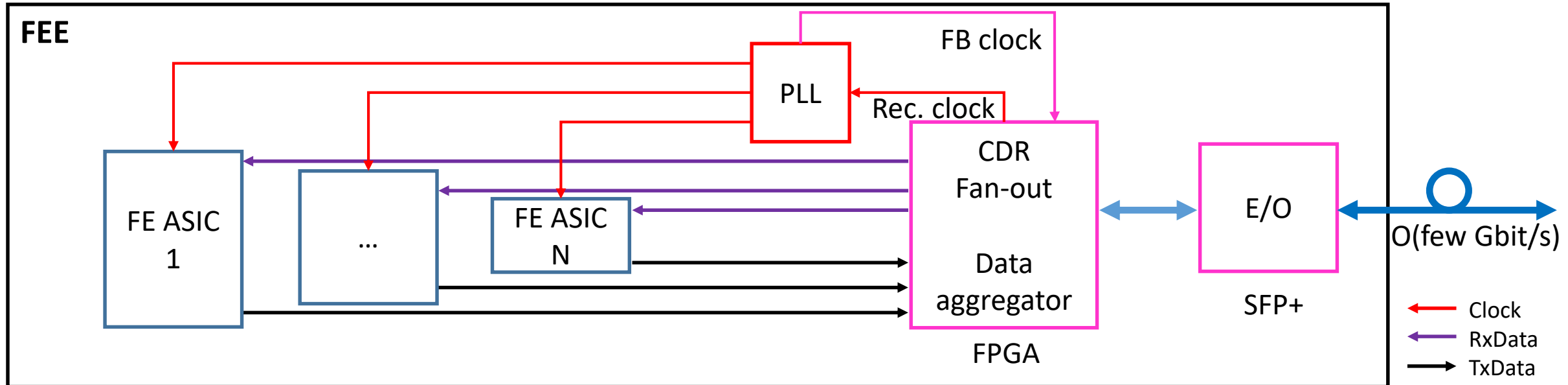
This gives 5 ps for 4 hour

2017
Can this be calibrated out?

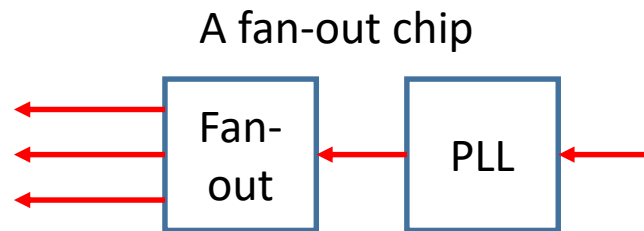


Embedded precision clock distribution

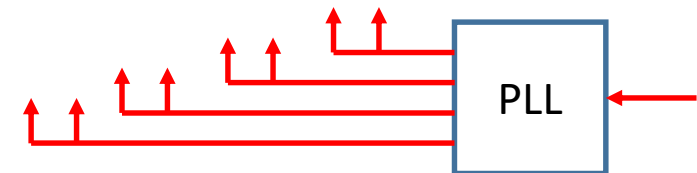
- Use of an external PLL to clean-up recovered by FPGA clock
→ Assuming low radiation level allows its use



- If PLL does not have enough outputs use either:



- A small size multi-drop topology (e.g. 2)

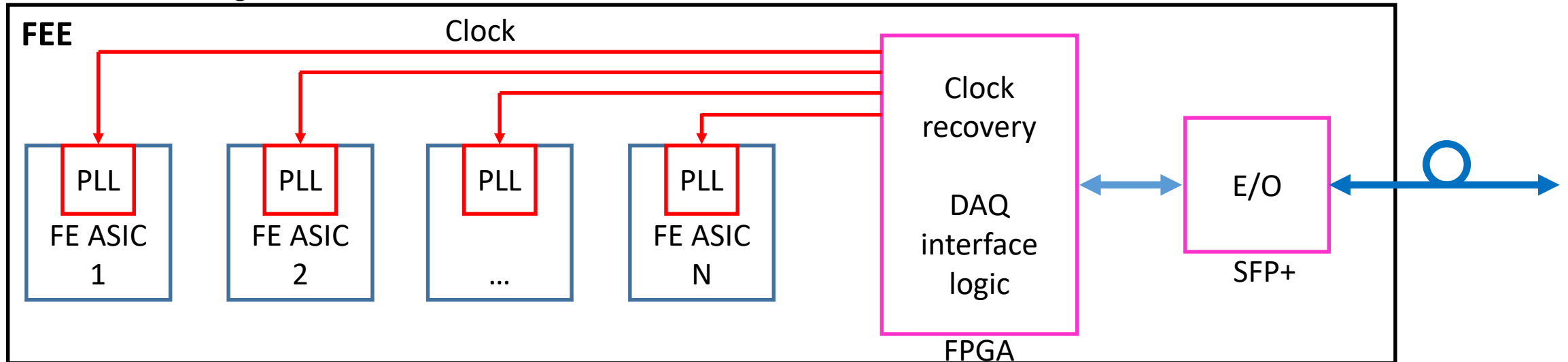


- Make sure clock phase adjustment is possible to decode RxData in the ASICs

About timing and clock distribution

- Frontend clock distribution with COTS components

→ Assuming low radiation level allows their use



- The quality of recovered by FPGA clock may not be enough for precision timing measurements

→ To be compared to the IpGBT performance: <4ps RMS jitter for 40 MHz recovered clock

- Jitter cleaner PLL embedded in ASICs

- Attention to power and environmental stability

→ Power modulation impact on clock jitter (RMS): O(few ps) / mV



Data



MPGD FEE data rate: **sampling readout**

- Sampling ASIC with 12-bit sample per channel
- Signal shape ZS
→ 500 ns readout window when signal is above threshold

- Existing 32-channel ASIC (e.g. Sampa) and 256-channel FEE with 8 ASICs

Channel rate kHz	Sampling MSPS	Number of samples	32-chanel ASIC Mbit/s	256-chanel FEE Gbit/s	Remarks
2 (physics)	20	10	19	0.16	5-10 Gbit/s aggregation link unjustified
10 (safety)			92	0.75	
50 (Clas12)			460	3.7	

- New development: 64-channel ASIC and 512-channel FEE with 8 ASICs

Channel rate kHz	Sampling MSPS	Number of samples	64-chanel ASIC Mbit/s	512-chanel FEE Gbit/s	Remarks
2 (physics)	50	25	46	0.4	5-10 Gbit/s aggregation link unjustified
10 (safety)			230	1.9	5 Gbit/s aggregation link is enough
50 (Clas12)			1 150	9.5	20 Gbit/s aggregation link needed



Integration



Athena Micromegas tracker: FEE constructions that could fit

- A 4-layer ~66k-channel Micromegas barrel tracker studied for Athena

- 32-channel ASIC
- 264 units of 256-channel FEE
- 150 mm to fit 8 ASICs

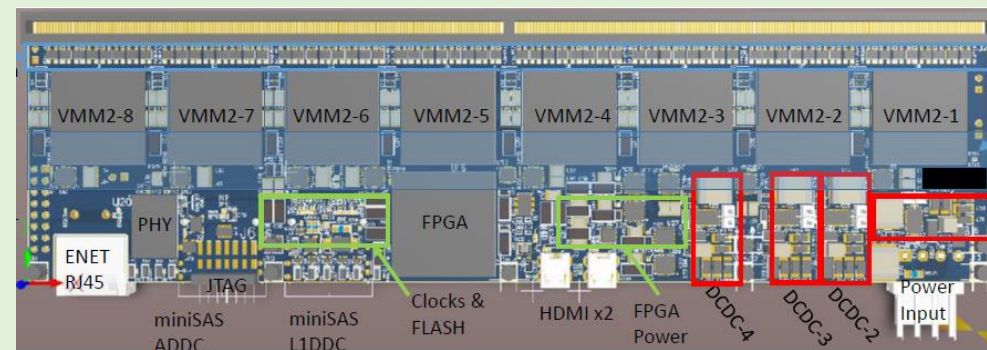
Illustration: fragment of sPhenix TPC FEE
256 channels: 8 Sampas: 140 x 140



140 mm

- 64-channel ASIC
- 132 units of 512-channel FEE
- 225 mm to fit 8 ASICs

Illustration: Atlas FEM8 prototype
512 channels: with 8 VMM3a: 215 x ~60



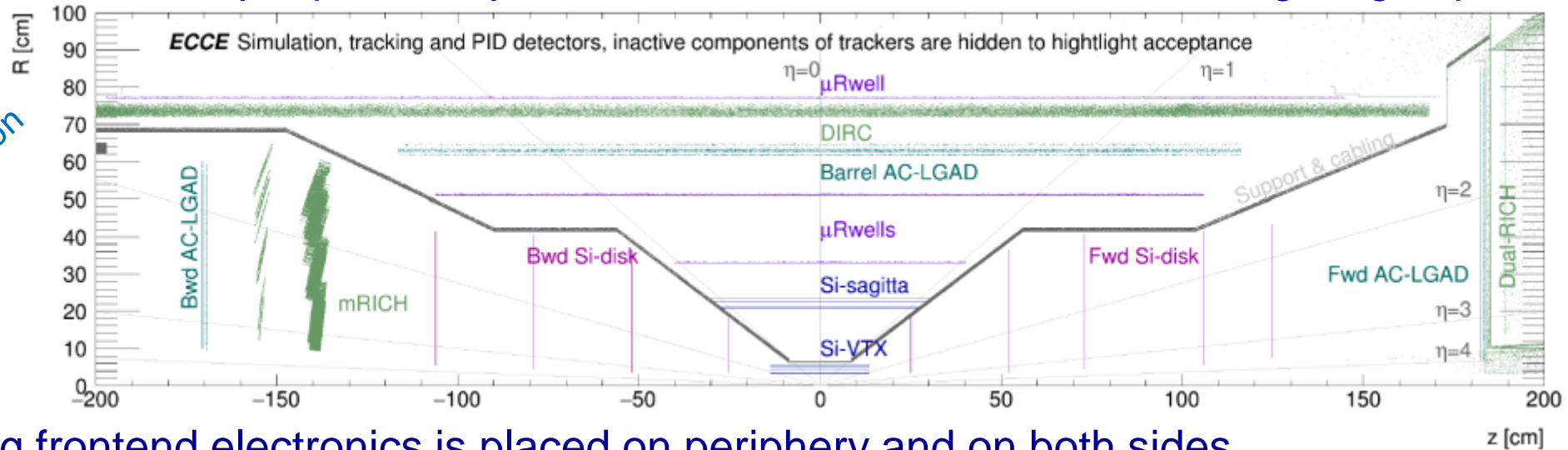
215 mm

- Detector-FEE connectivity with modest 0.8 mm pitch could fit



Example of integration challenge

- ... 280k-channel 3-layer μ RWell cylindrical tracker in the same volume targeting 50 μ resolution



Still under definition

- Assuming frontend electronics is placed on periphery and on both sides

→ 2 x 10 m of total periphery

- 32-channel Sampa

→ 15 mm x 15 mm package

→ 9K chips required

→ 1.1K chips can be placed in a single row

■ 35K channels

- 64-channel VMM

→ 21 mm x 21 mm package

→ 4.5K chips required

→ 768 chips can be placed in a single row

■ 48K channels

→ Multi-layer FE stack with several rows of FE ASICs?

Place for electronics and services is scarce – collaboration of subsystems to share it

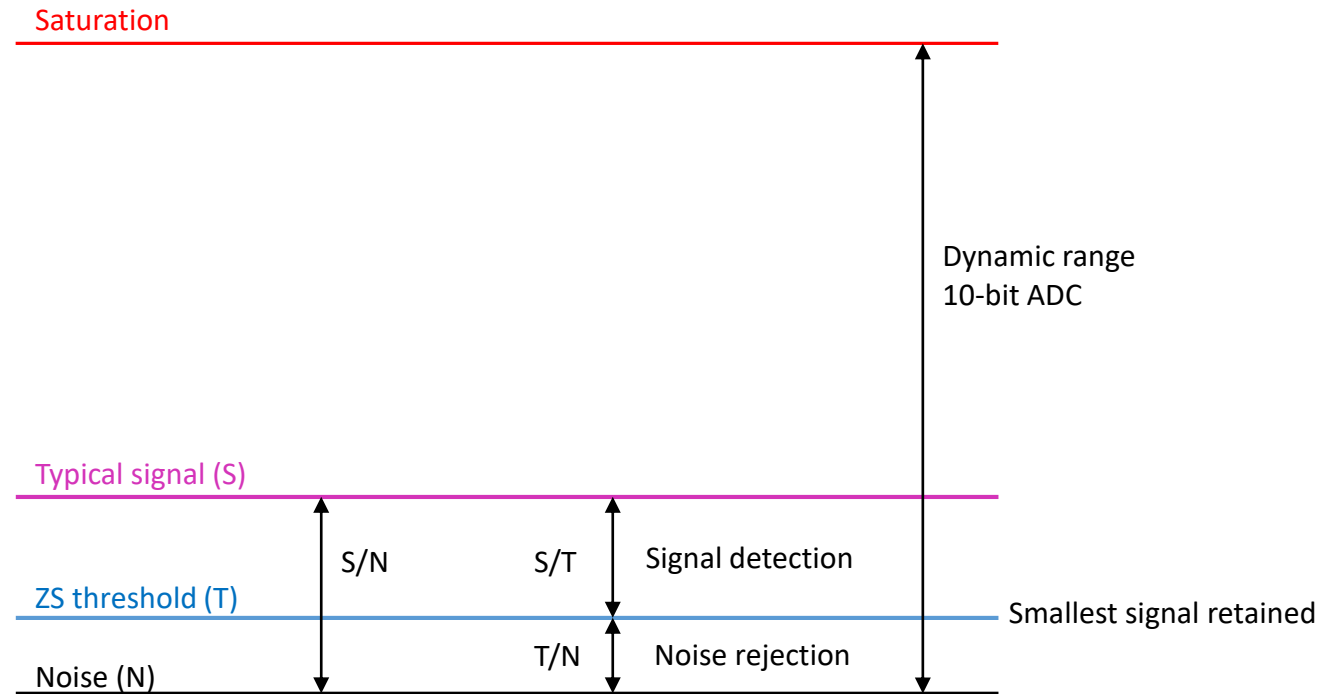


MPGD ↔ ASIC interface
Determining working point
A non-EIC related example



Finding a working point for an MPGD detector

- Effect of ASIC dynamic range and detector gain
- Asses saturation probability and charge measuring accuracy
 - Take into account charge transfers in detector and towards CSA

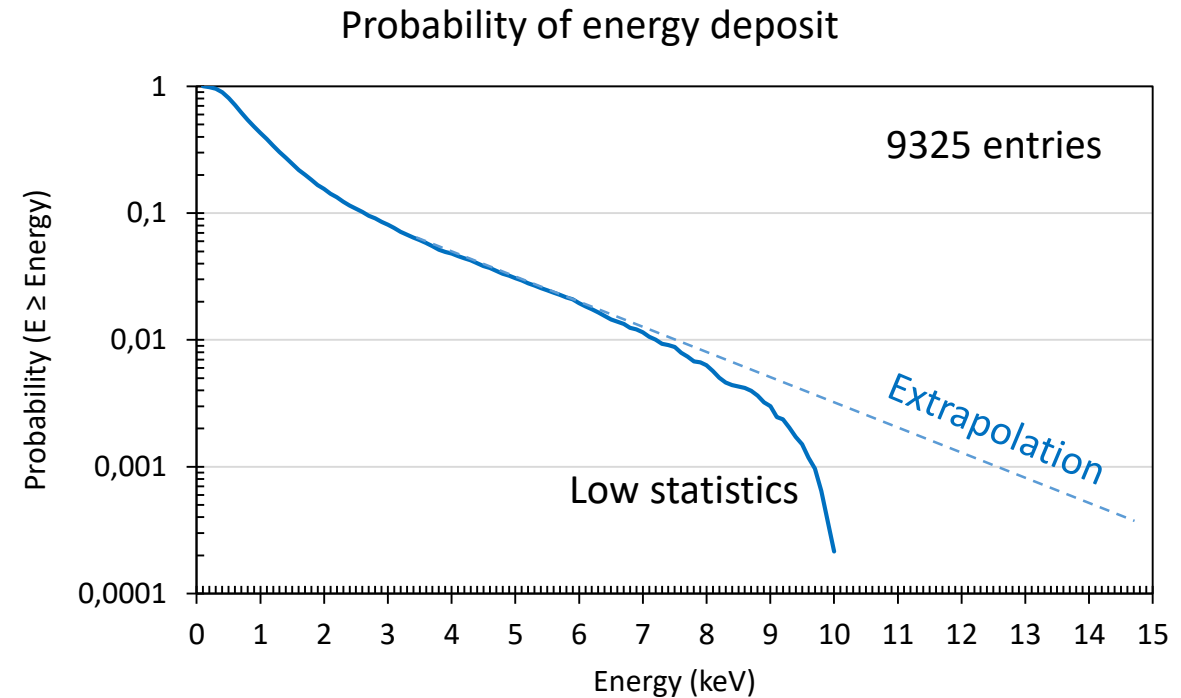


- Choice of dynamic range and detector gain
 - Tradeoff between measurement accuracy and saturation probability



Finding a working point: A detector example

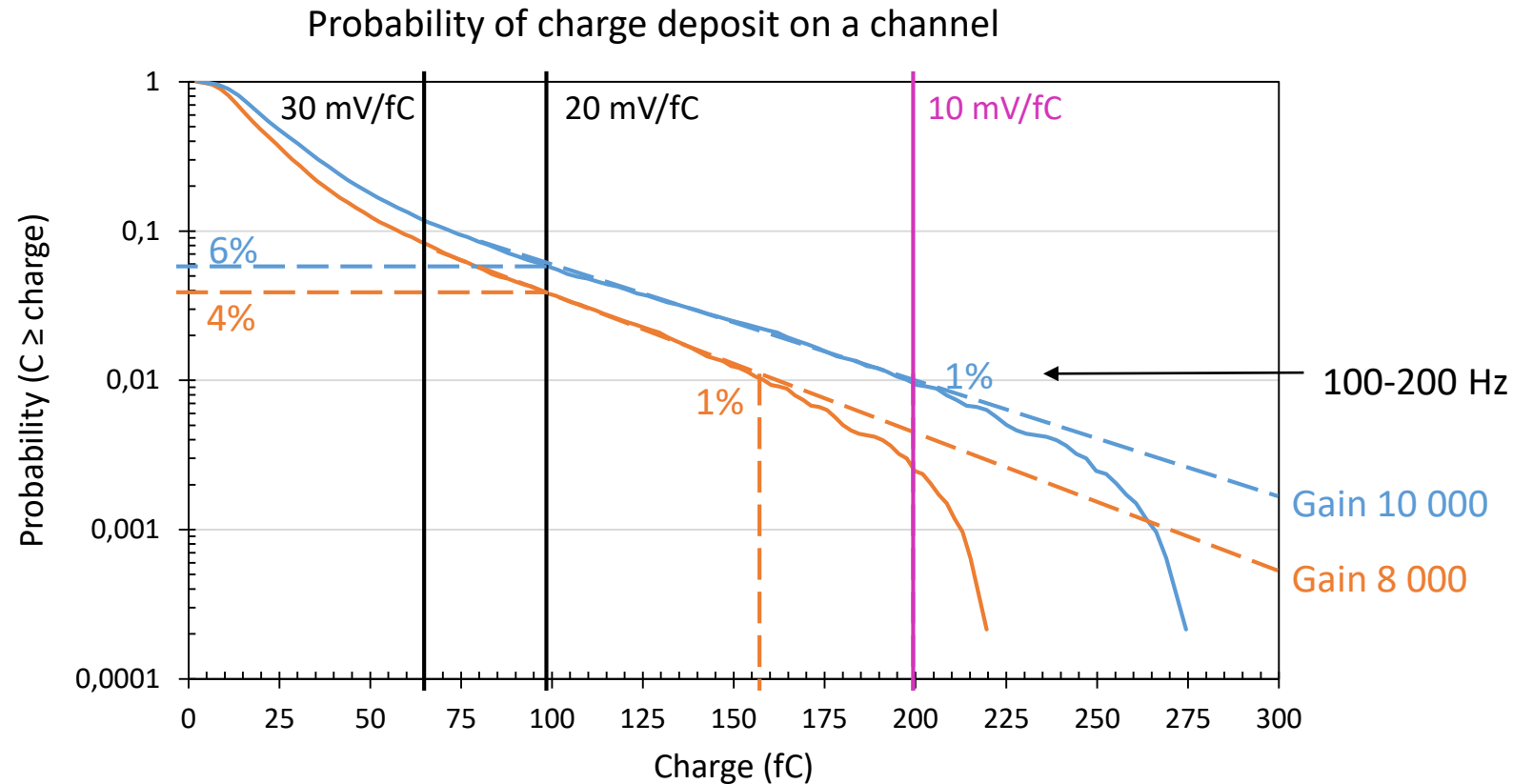
- Typical signal: ~500 eV
 - Ionization energy: 27 eV
 - Primary electrons: ~18.5



- Cluster size: ~5 strips
 - Strip with max energy: 65% of cluster energy - hypothesis
- Detector capacitance: 150 – 200 pF
 - Charge transfer to front end electronics: ~80%
- Strip hit rate: 10-20 kHz

Finding a working point: Detector gain impact on a CSA

- Assume detector gain within 8 000 - 10 000 range



- 20 mV/fC: 100 fC range might be overrun in ~5% cases
 - Is there a problem to saturate CSA with 2 times higher charge at ~200 Hz
 - What is the level of saturation when real problems start
- 10 mV/fC range looks comfortable



Finding a working point: Signal to noise

- Assumptions

- ENC @ 160 ns peaking time: 3.5 ke for 150-200 fC input capacitance
- Strip with max energy: **65%** of cluster energy
- Charge collection efficiency: 75%

Detector gain	Signal @ CSA ke – fC	S/N	VFE gain mV / fC	Signal ADC bin
8 000	68.6 – 11.0	19.6	30	150
			20	100
			10	50
			4	20
10 000	85.8 – 13.7	24.5	30	190
			20	130
			10	64
			4	26

- In case S/N= \sim 20 is not enough, higher detector gain will be needed
 - With a potential risk of more frequent saturations



Finding a working point: Threshold to noise

- ENC of 3.5 ke^- for 150-200 fC input capacitance

Detector gain	Signal @ CSA $\text{ke}^- - \text{fC}$	S/N	T/N	E_{MIN}/E %
8 000	68.6 – 11.0	19.6	4	13
10 000	85.8 – 13.7	24.5		10.5

- @ T/N=4, if a strip sees $< 14 \text{ ke}^-$ (11-13% of signal energy), it will be suppressed
 - Need to study charge distribution within clusters to assess the consequences
- Is it possible / interesting to perform a kind of “region of interest” ZS on-line?
 - If a strip exceeds high threshold, forced or lower threshold reading of its neighbors

- Min detectable signal at T/N = 4 level

Min signal	30 mV/fC 66 fC	20 mV/fC 100 fC	10 mV/fC 200 fC	4 mV/fC 500 fC
ADC bin	35	23	12	5

→ 20 mV/fC is sure, 10 mV/fC looks comfortable

- Study T/N = 5 (or even 6) cases