Global Timing Specifications and Fast Control System for EIC detector

Outline ● Discussion on the specification ● Possible hardware for realization

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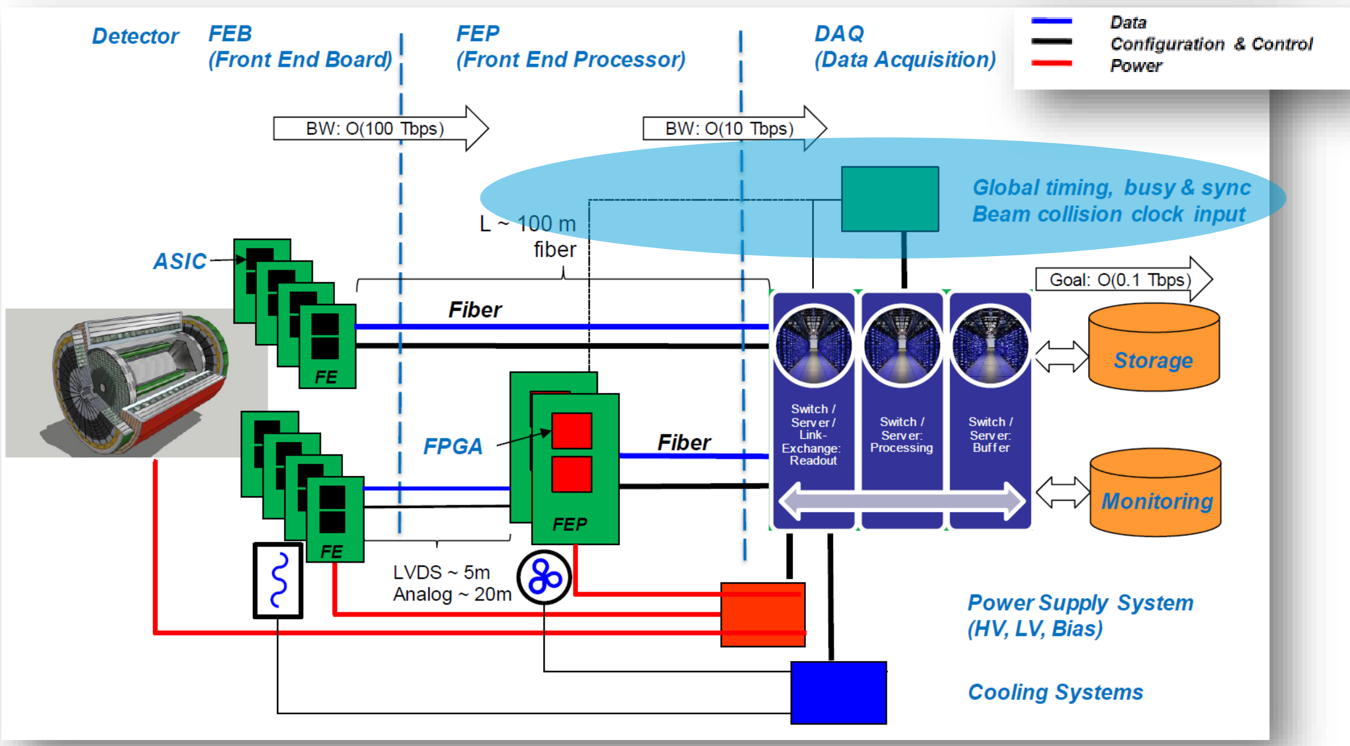
Thanks to discussion with many colleagues and partly based on discussion of the past 9 SRO workshops

Introduction

- Fast control systems, for control/feedback/sync that is at <O(10us) level
  - Distinct from slow control
  - Require routes of fixed timing constraints
- Fast controls topics:
  - Beam crossing counter
  - Precision timing distribution
  - Synchronization and fast control bits
  - Time bucketing
  - Busy feedback and flow control



Ref: EIC-CDR

A discussion: Specification on fast control

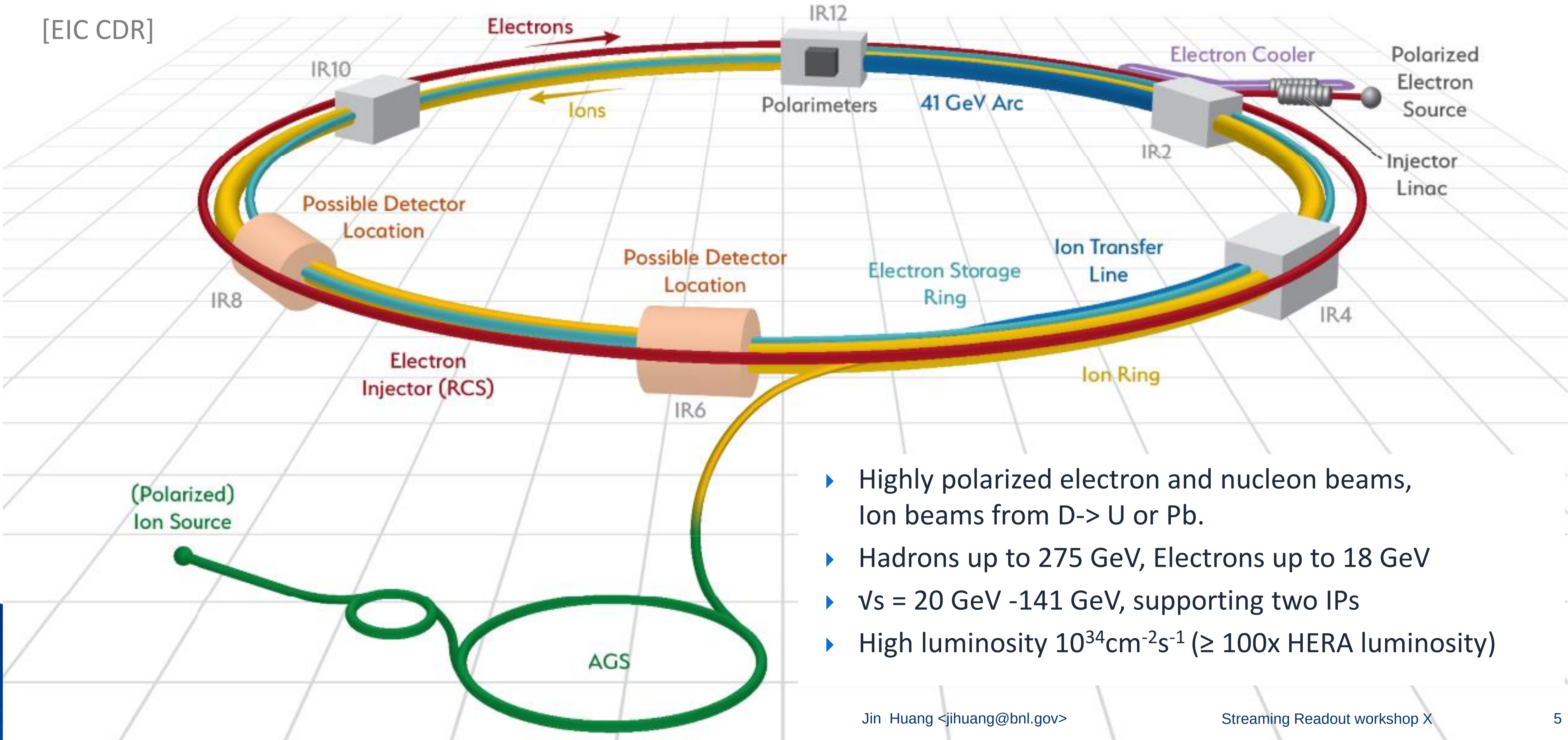
- Beam crossing counter
- Precision timing distribution
- Synchronization and fast control bits
- Time bucketing
- Busy feedback and flow control

Synchronization to beam crossing

- For a collider experiment, absolute time is not directly useful (e.g picoseconds count to some reference time)
  - ms would be sufficient for calibration tracing
- What matters is relative time:
  - Hit correlation between detectors at bunch separation O(10ns) , time of flight clock distribution uncertainty requirement at O(10ps)
  - Correlation of detector hit with the origin of the beam bunch crossing at O(10ns) →
- Why tagging streaming hits with beam bunch crossing (98.5Mhz)
  - Necessity to trace back to physical quantity that could change between neighboring bunches: spin state, luminosity, polarization, etc.
  - “Free” boost of precision from 10ns counter to 100ps bunch interaction time

Beams of the EIC

[EIC CDR]



- Highly polarized electron and nucleon beams, Ion beams from D-> U or Pb.
- Hadrons up to 275 GeV, Electrons up to 18 GeV
- √s = 20 GeV -141 GeV, supporting two IPs
- High luminosity $10^{34}cm^{-2}s^{-1}$ (≥ 100x HERA luminosity)

EIC beam crossing clock features

- 1260 RF bunch, 98.5254 MHz beam crossing clock
  - In a friendly range for many FPGA-optical transceivers base clock: e.g. 6Gbps transmit 8Byte per beam clock
  - E.g. sPHENIX beam clock was envisioned to transmit at 56.4 or 112.8MHz (56.4 was final choice)
  - Upstream signals: beam clock, revolution tick tag bunch zero
- Clock signal originating from accelerator RF source
  - High precision clock source for operation of RF cavities (rebuilding RHIC 28 MHz RF cavities as 24.5 MHz resonators), which in turn defines the bunch in time
  - High precision clock signal routed through the accelerator site, installed for sPHENIX operation
- EIC beam clock has fixed frequency without ramp variation [EIC CDR sec 3.3.2]:
  - Electron beam does not change frequency during acceleration
  - Hadron beam change *orbit* to match electron beam frequency
  - Simplification compared with hadron colliders:
    - RHIC (9.34-9.38 MHz) and LHC (40.078422 to 40.078970 MHz), tricky configuration for transceiver and PLLs
  - Caveat: possibility of change of frequency operation poitn for low sqrt-s EIC operation, TBD

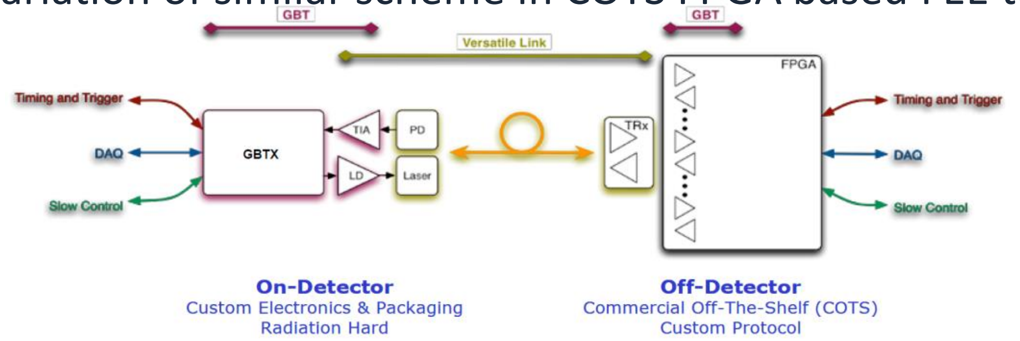
EIC beam crossing counter

- Given the use of beam clock, the beam crossing counter and its harmonics can be conveniently used for detector hit synchronization
- Global timing system should maintain a master beam crossing counter
  - For example, 64bit integer: never roll over in lifetime of EIC (6k years)
  - Indexing for event, run period, calibration validation periods
- Sync the subsystem and their FEEs to the beam crossing counter
  - *Minimal requirement*: front end maintain a (shorter) beam clock counter, synchronized to master clock counter (with fixed offset) at initialization with a fast signal (Clock START).
  - *More robust practice*: broadcast of a section of beam clock counter (20-40 bits) to FEE and directly embed into hit data

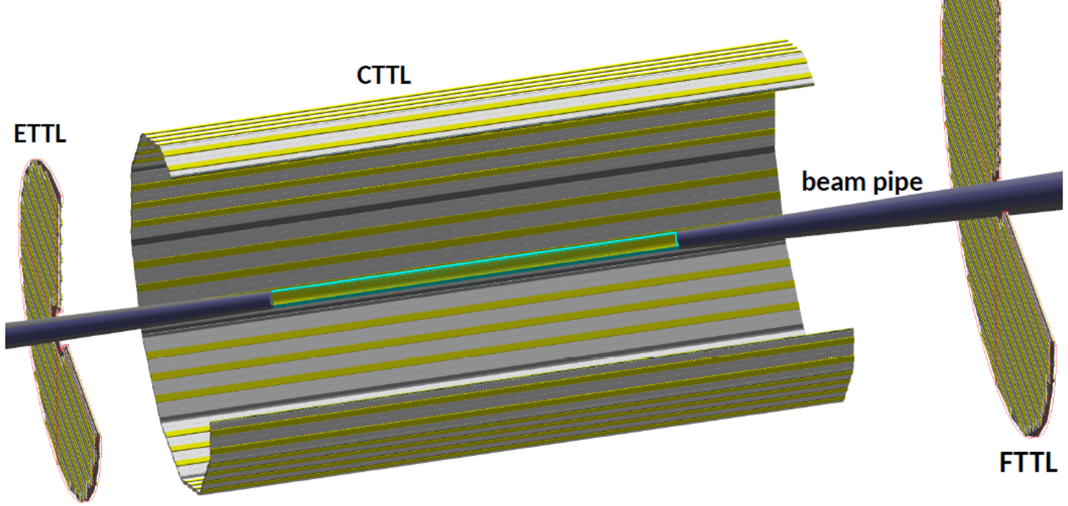
Precision specification for clock distribution

- Most subsystem: it would be sufficient to use clock recovered from optical link that run at harmonics of beam clock
  - Stabilized beam clock with PLL
  - Just need to be stable enough to maintain link: O(<10)ps stability, with caveat of larger uncertainty between components of a large system →
- One significant exception is high precision TOF both used in ATHENA and ECCE:
  - AC-LGAD tracker and beam line det. of dT~30ps
  - Require stable clock distribution to O(10)ps
  - For TOF, we could consider a dedicated clock signal, PLL, and clock signal splitting tree

Embedded clock in GBTx [GBT manual]
Variation of similar scheme in COTS FPGA based FEE too



ECCE TOF PID system [ECCE proposal]



Synchronization and fast control bits

More information can be broadcasted synchronized tagging bits to clocks: e.g. 6Gbps transmit 8 Byte per beam clock

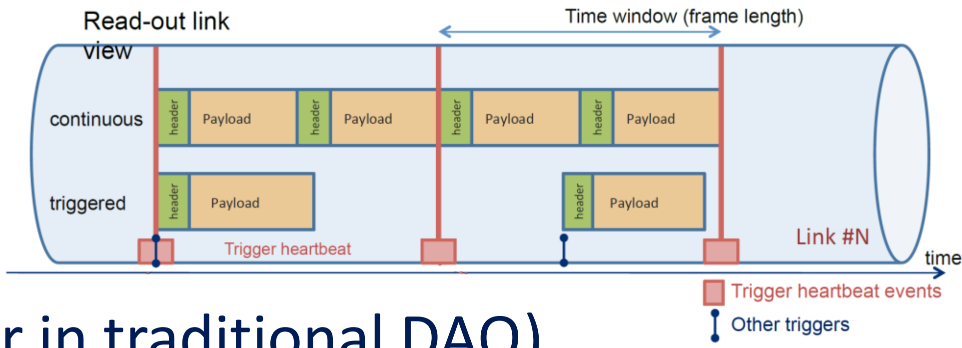
- Calibration, e.g. fire laser calibration during abort gap
- FEE clock counter restarts
- Trigger or data stream throttle (high background contingency)
- Hit time-bucketing (next section)
- Methods: mode Bits

Example: sPHENIX clock data embedding at 6x 9.4MHz beam clock, 12Byte/beam clock [sPHENIX TDR, M. Purschke]

clock count		0	1	2	3	4	5
bits 0-7	mode bits/BCO	mode bits	BCO bits 0-7	BCO bits 8-15	BCO bits 16-23	BCO bits 24-31	BCO bits 32-39
bit 8	beam clock	1	0	0	0	0	0
bit 9	LVL1 accept	X	0	0	0	0	0
bit 10	endat0	X	X	X	X	X	X
bit 11	endat1	X	X	X	X	X	X
bit 12	modebit en.	1	0	0	0	0	0
bits 13-15		3 user bits	0	1	2	3	4

Time bucketing

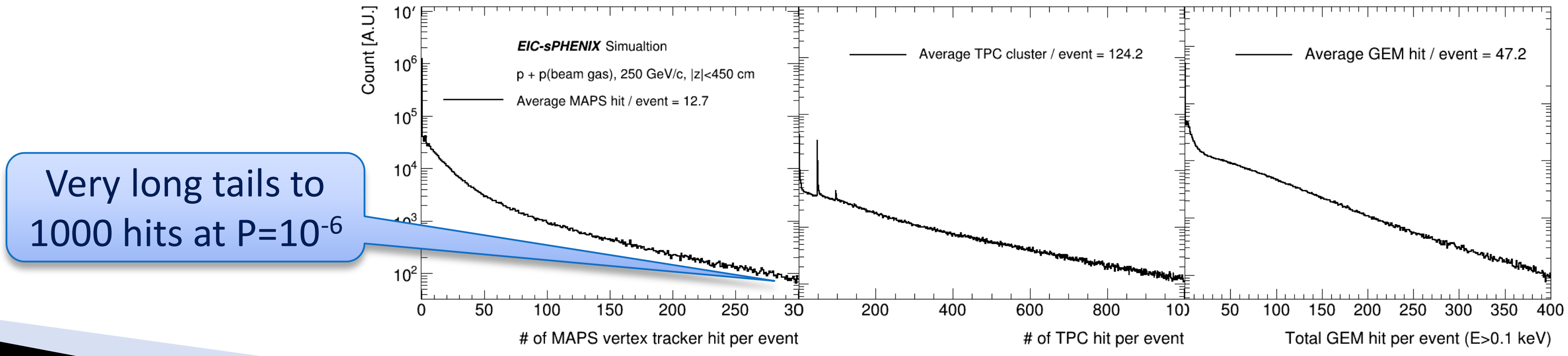
Example:
ALICE heartbeat frame
O(20)ms [ALICE-TDR-019]



- Hit grouping in time period (instead of event trigger in traditional DAQ)
  - Used by many streaming system: e.g. heartbeat frame in ALICE, time slice in CBM
  - Efficient time encoding, i.e. each hit do not need to encode full beam clock counter, just relative counter inside a time bucket
  - For downstream processing, data can be processed and combined in chunks of 1-2 time bucket to obtain a complete set of event; unit for bookkeeping (calib/QA)
  - Easier handling in simulation sample preparation
- For EIC, we could *consider* a time frame of
  - 2^16 = 65536 beam crossings
  - 0.7ms in absolute time
  - At top luminosity, containing about 300 collisions and 30 beam gas interactions
  - Convenient size of 8MB of raw zero-suppressed collision signal data + background data load

Busy feedback and flow control

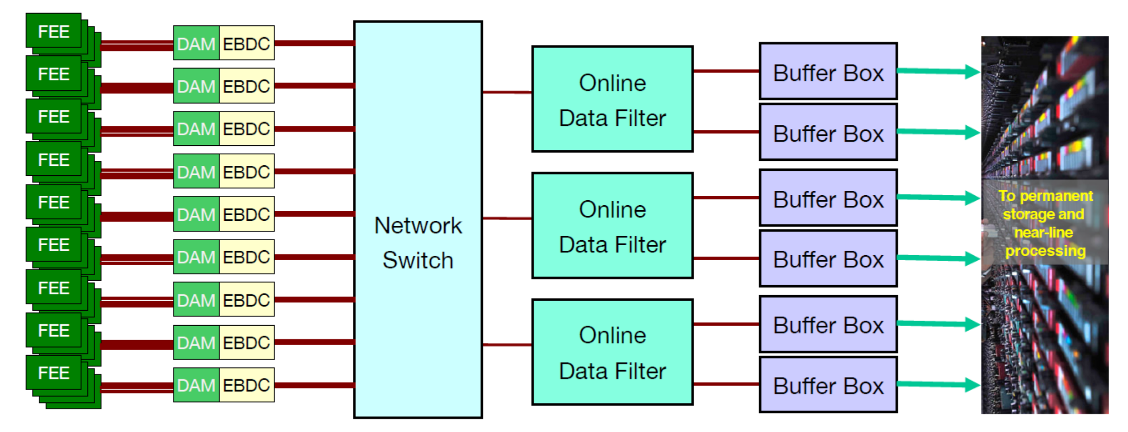
- Event at small probability, readout congestion may happen
  - There is chances of very high multiplicity events or collection of events, background splash, etc.
  - Collision in shared resources, e.g. network routing, CPU cycles
- For readout, important to not to drop events with a bias (particular important for EIC sys. ctrl.)
  - Always readout current event
  - So, analysis do not carry rare bias, e.g. low efficiency for high multiplicity events
- One common solutions:
  - buffers with high water mark in readout pipeline agreggators
  - Send busy signal, fast enough O(10) us to stop the data taking of the whole experiment for the coming (non-biased) events. Clear the buffer processing → Dedicated feedback lines (fiber, copper)



Hardware realization the system

- With a focus on hardware today

Envisioned system in EIC proposals



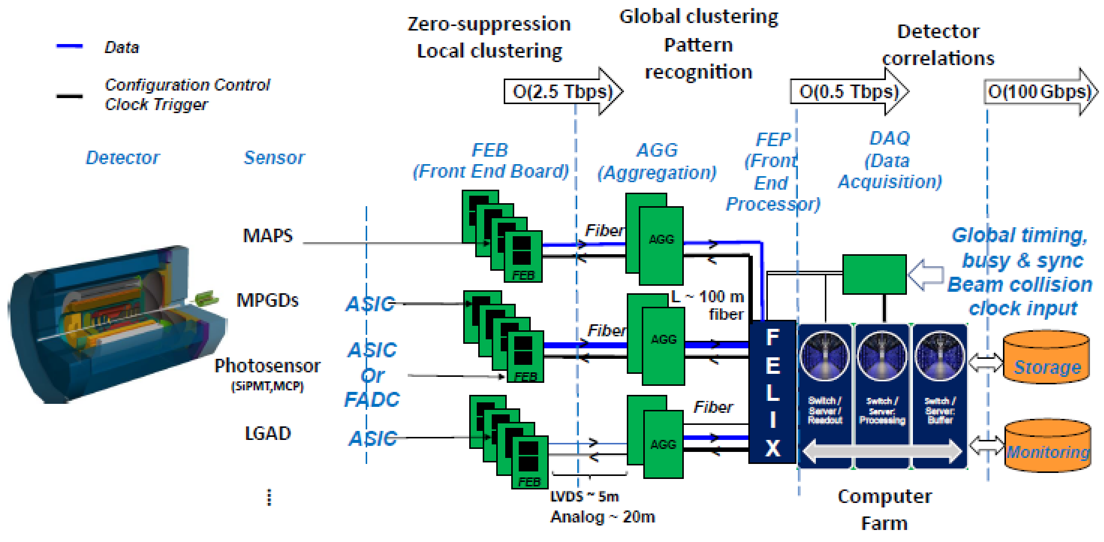


Figure 2.16: Overview of the ATHENA DAQ architecture.

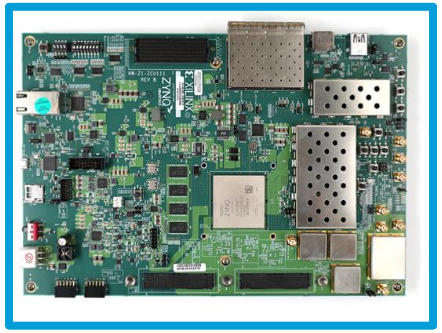
ECCE DAQ architecture
[proposal, Talk by M. Purschke]

ATHENA DAQ architecture
[proposal, Talk by J. Landgraf]

sPHENIX-related streaming readout electronics

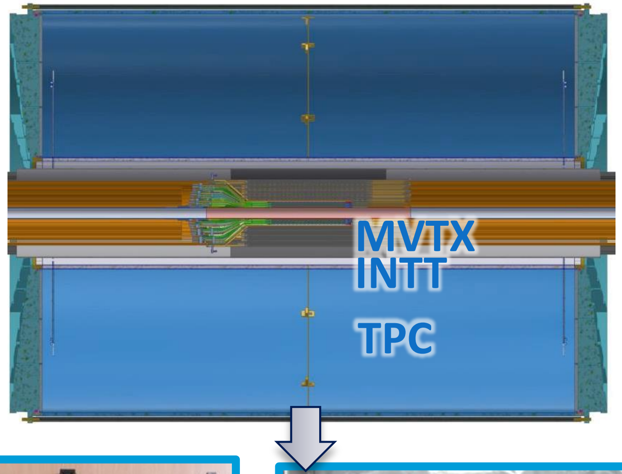
Associated test projects

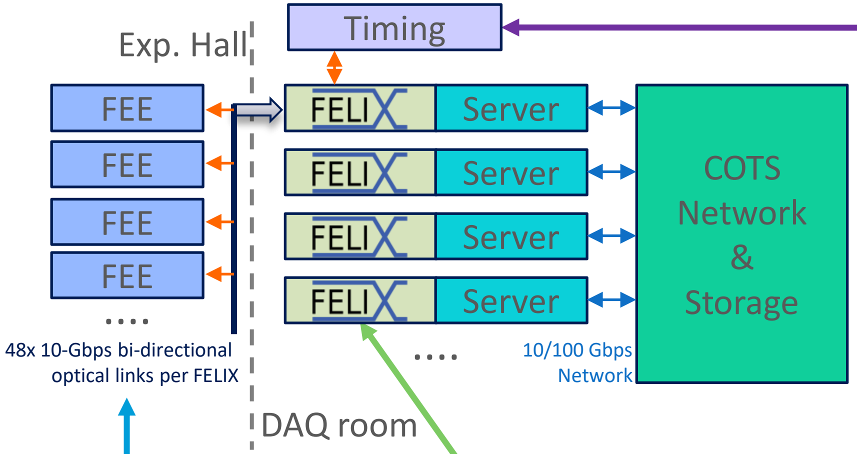
Precision timing digitizer
DRS4GlO (SBIR/LDRD)



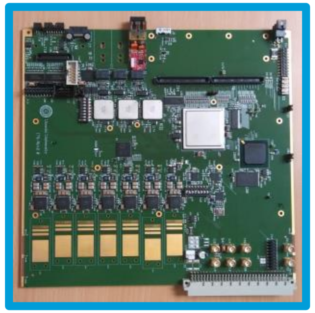
High density multiplexer+ ADC
RFSoC Digitizer (LDRD)

sPHENIX streaming DAQ for tracker



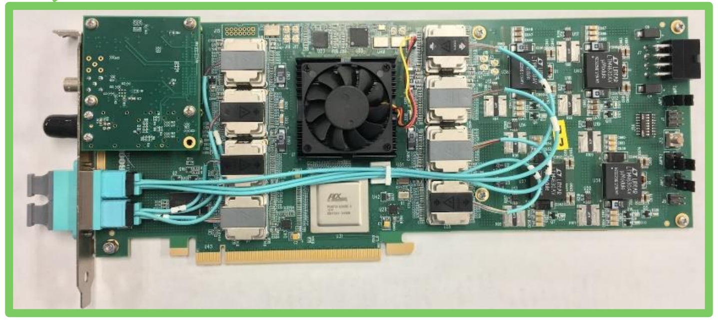


Global Timing Module (NSLS II/sPHENIX)
Receiving from RHIC RF low glitter clock source



MVTX RU, 200M ch　INTT ROC, 400k ch
ALPIDE (ALICE/sPHENIX), FPHX (PHENIX)

TPC FEE, 160k ch
SAMPAv5 (ALICE/sPHENIX)

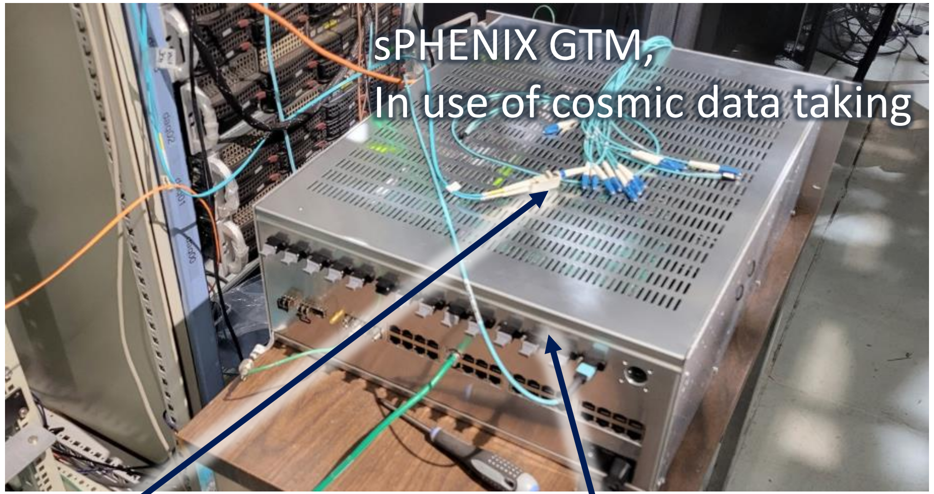


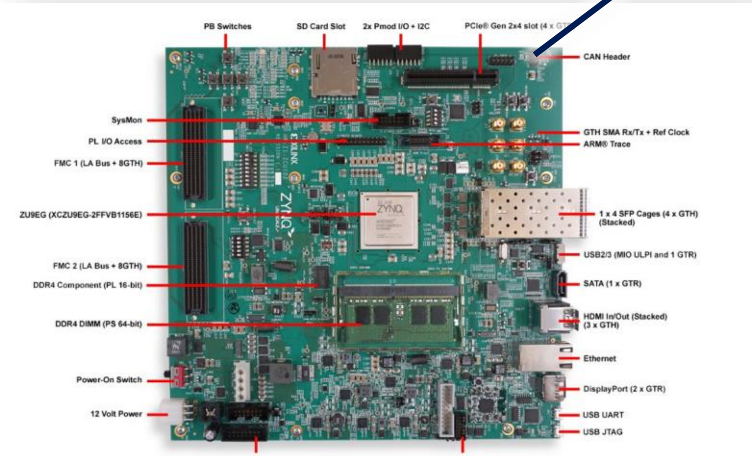
BNL-712 / FELIX v2 x38 (ATLAS/sPHENIX)

FELIX Ref: 10.1109/tim.2019.2947972
Similar role as PICe40 in LHCb [R. Aaij's talk]

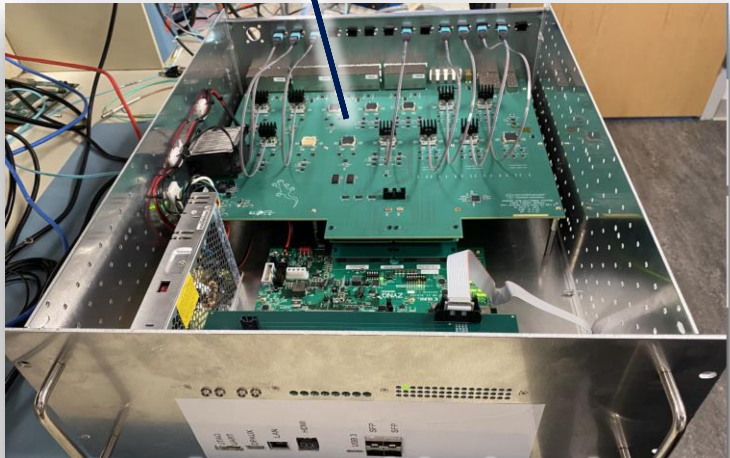
sPHENIX global timing module (GTM)

- ZCU102-based + fanout board
  - Receive the accelerator RF bucket clock and revolution tick
  - Maintain master clock counter
  - Broadcast sync and clock to all subsystems via fiber links
  - Receive busy feedback
- See also talk
  M. Purschke, A. Camsonne





Generic FPGA board (ZCU102)



\+ custom fan out + delay board

FPGA-PCIe interface

- Dedicated transceiver to allow receive timing and fast control channel and provide busy feedback
- Jitter cleaner (next slides)
- Send clock and control to FEE via optical links
  - GBT family ASIC
  - Custom SFP+ link encoding clock + data
- As EIC version of FELIX-like device develops, EIC could benefit from a large pool of current FELIX (712v2) for large scale testing after the sPHENIX operation concludes

FELIX in develop [FLX-181, H. Xu SRO IX]

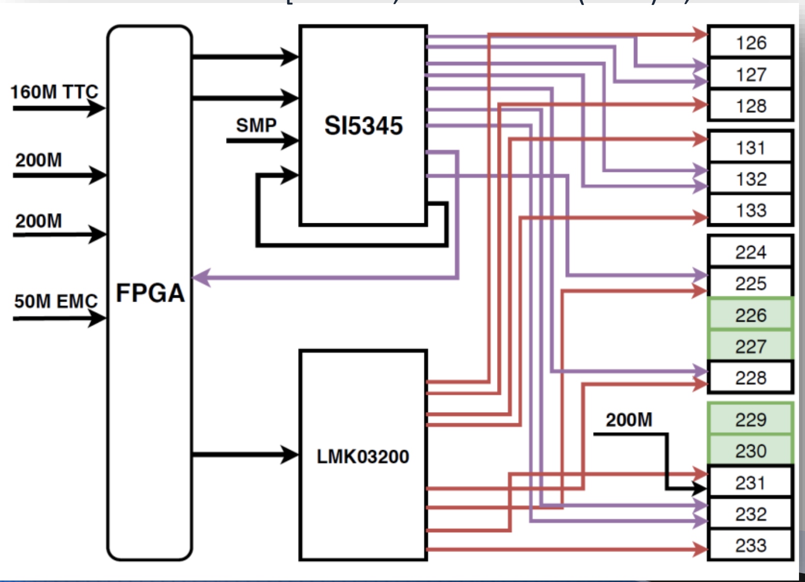
FELIX 712v2, ATLAS Phase-1/sPHENIX production

PCIe40, LHCb/ALICE, [N. Neufeld]

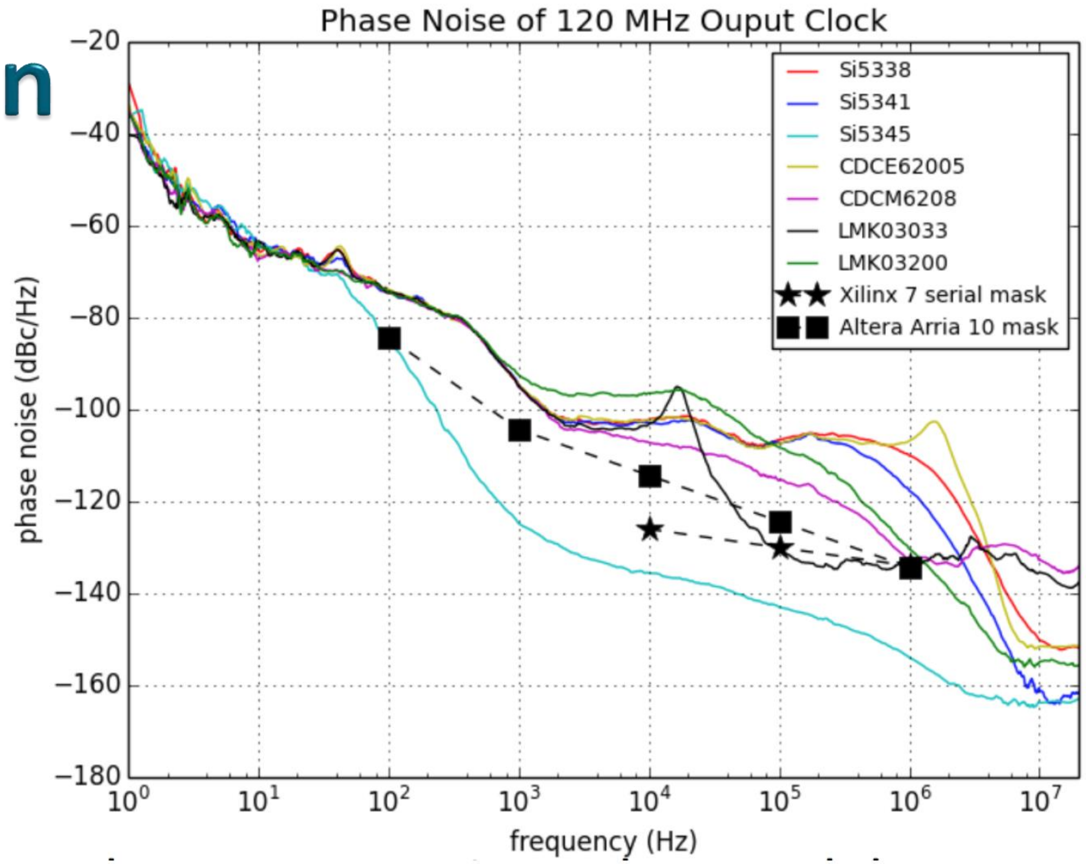
Clock distribution precision

- FELIX is designed with clock jitter to provide stable clock to FEE
- Precise enough for robust transceiver lock, ps-level at 10kHz-1MHz in current part selection
- Caveat is sync over many FELIX's clock over many detector components and all frequency ranges, e.g AC-LGAD TOF and beam line detector.
  - Contribute to the uncertainty of TOF measurement, 20-30 ps total uncertainty
  - Therefore, ToF should consider a dedicated precision clock distribution, monitoring and calibration

FELIX v712 clock tree [K. Chen, IEEE TIM. 69 (2019) 7, 4569-4577]



[K. Chen, ATLAS Phase-I FELIX Design Review]



Device	SI5338	SI5345	SI5341
Jitter (ps)	8.58	0.09	6.39
Device	CDCM6208	LMK03200	LMK03033
Jitter (ps)	2.06	5.91	2.74
Device	CDCE62005		
Jitter (ps)	8.61		

The jitter from 10 kHz to 1 MHz

Summary for Global Timing Specifications

- Timing tag: follow and tag hits with beam crossing counter
- Clock precision: maintain stable link, which is sufficient for most detector
  - TOF may require dedicated clock distribution to control variation: 10 ps
- Fast control: provide additional bits in sync to beam clock for fast control in timing system
- Hit grouping: time bucketing hits, e.g. 2^{16} crossing wide / 0.6ms
- Provide fast O(1)us busy feedback and flow control

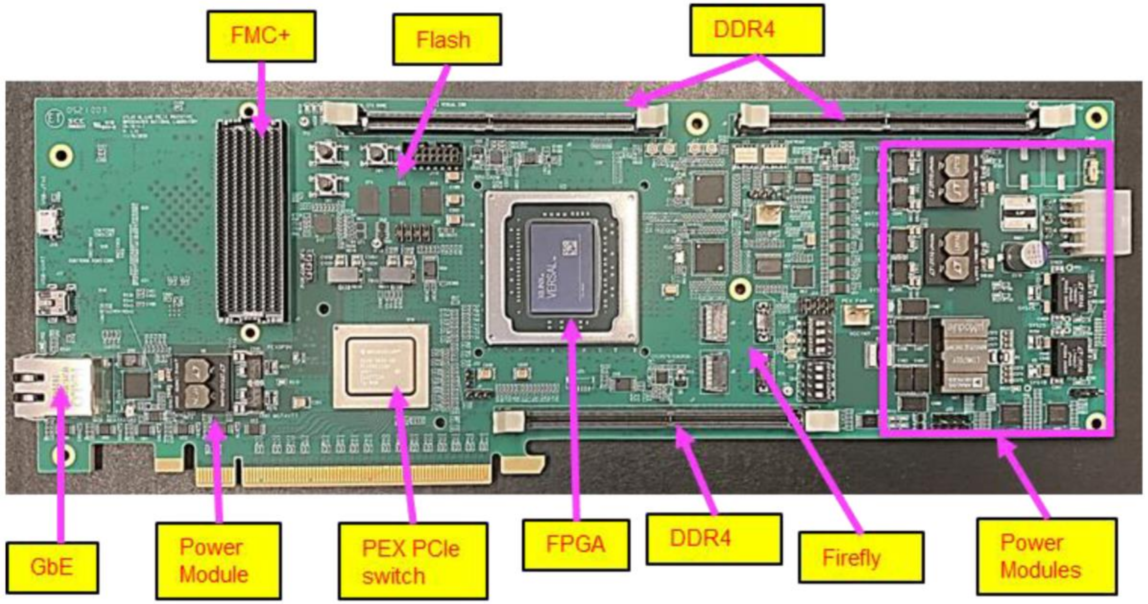
Discussions Please!

Extra information

FELIX for ATLAS Phase-2 Upgrade

FPGA: Xilinx Versal XCVM1802

- High speed optical links
  - 12 x FE-Links: 1 pair of Samtec Firefly 25Gb/s 12-ch modules
  - 16 GTY links @ 25Gb/s on FMC+
- Dual PCIe Gen4 x 8, up to 256 GT/s
  - 16 x GTY links
- 3 x Mini-UDIMM DDR4 Modules
  - Accessible by both PL and PS through NoC
- FMC+ mezzanine card
  - 34 x differential pairs from XPIO banks
  - 16 x GTY links
- Peripherals:
  - Micro SD 3.0 and QSPI flash for system boot
  - USB - I2C/UART
  - GbE RJ45



Picture of assembled FLX-181

Status of FLX-181

Hardware

- Three boards have been produced for firmware development
  - One is being used for ATLAS firmware development at Nikhef
  - One is being used for DUNE firmware development at CERN
  - One is kept at BNL for hardware and firmware development

Firmware

- PCIe Gen4x16 has been developed
- 24 channel GBT mode is being implemented

Photo of FLX-181 with 25Gbps FireFly FMC+

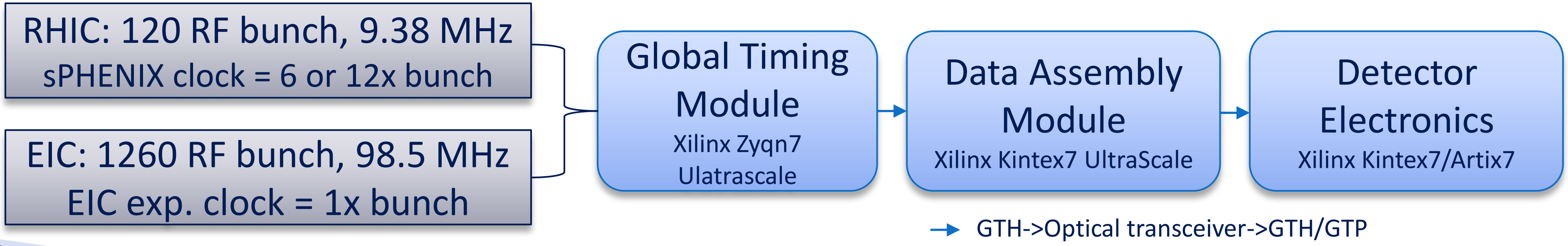
Development Plan

- FLX-182
  - Schematics design is done. Layout design will be finished by March 2022.
  - FLX-182 will be available in summer 2022 for firmware development.

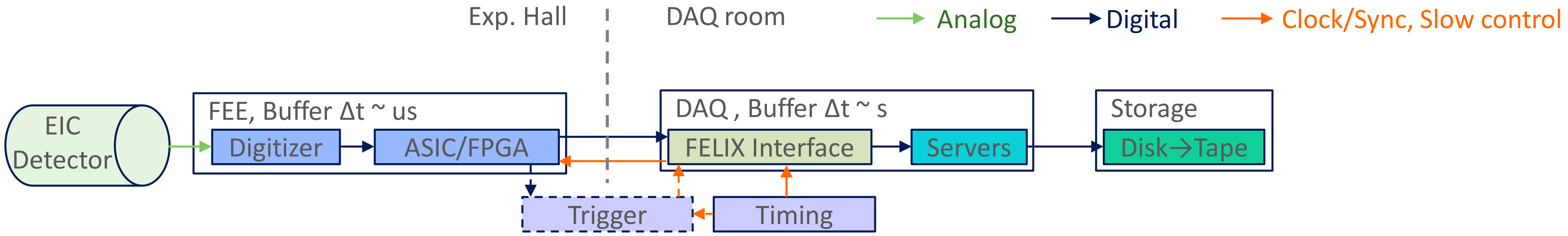
- 48-ch FELIX
  - FPGA: Versal Premium
  - Transceivers: Up to 100+ GTYP/GTM
  - PCIe Gen 5 up to 16 lanes
  - Design will start in Q4 of 2022, first board is expected to be available in Q3 2023.

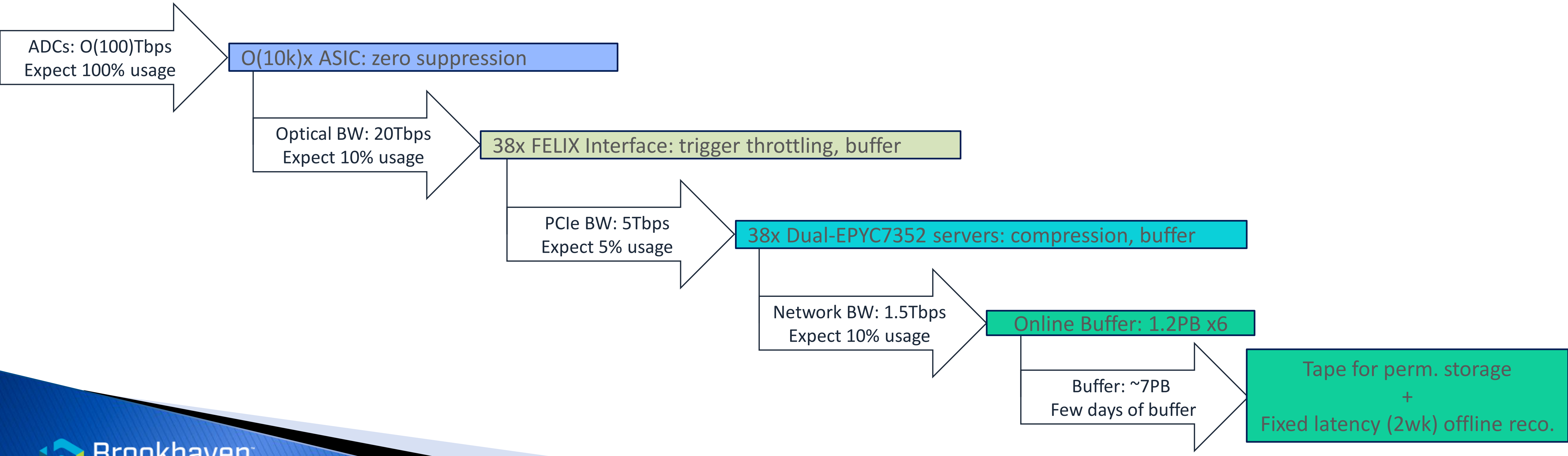
Timing and synchronization

- Precision timing is relative (e.g. ToF, TPC, coincidence), with exception that we need to know which bunch is colliding
- Therefore, collider experiment DAQ and FEE usually sync to beam bunch RF/collision clock
  - Then we need to be able to handle variation in beam clock. EIC clock variation seems simpler than RHIC (no ramp, weaker energy dependence), but design still on going
- EIC RF : modifying or rebuilding RHIC 28 MHz RF cavities as 24.5 MHz resonators
  - In discussion with RHIC RF group on testing sPHENIX timing distribution chain at RF clock source
- Timing system also collect/distribute busy, to ensure loss is uncorrelated with event type



sPHENIX Streaming data flow





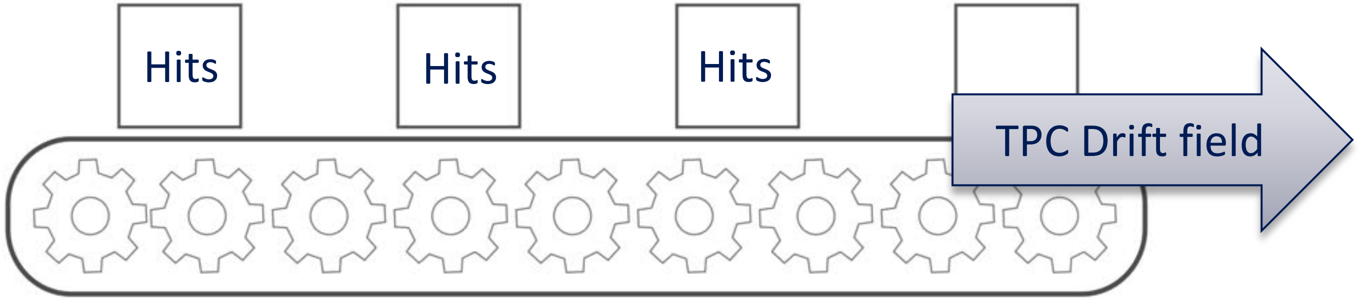
Streaming readout status at sPHENIX

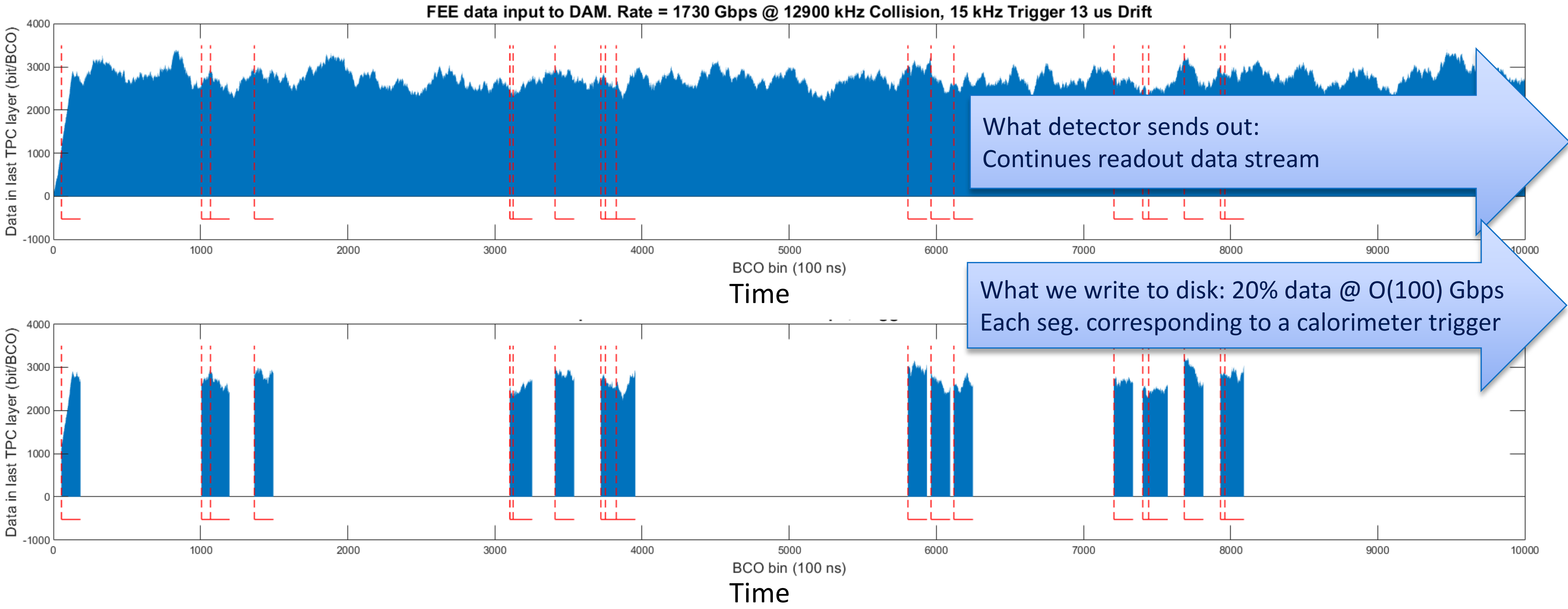
- All three sPHENIX tracking detector uses streaming readout
- Developed plan to take streaming data for heavy flavor physics program (next slides), commended by RHIC PAC.
- Completed construction of sPHENIX FELIX DAQ interface (~50) and procurement of DAQ servers, network infrastructure and online disk buffers
- Data taking start in 2023!

RHIC PAC 2020 report

> We commend sPHENIX for developing the continuous streaming readout option for the detector, which increases the amount of data that can be collected in Run-24 by orders of magnitude. In particular in the sector of open heavy flavor, this technique will give access to a set of qualitatively novel measurements that would otherwise not be accessible. Given the tight timeline for completing the RHIC physics program before construction of the EIC begins, this is a tremendous and highly welcome achievement.

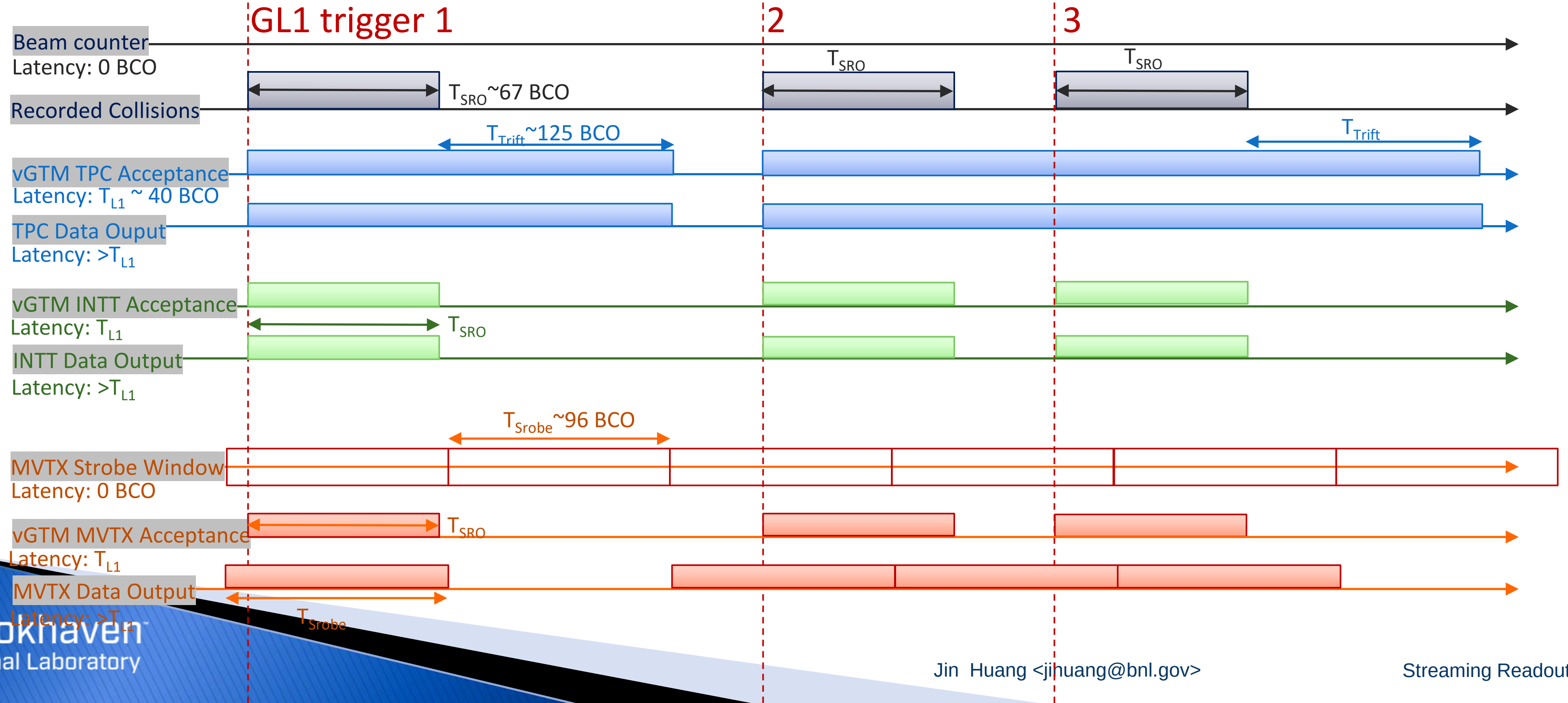
TPC data stream in sPHENIX triggered DAQ





SRO-Mode1-Simple [Recommended]

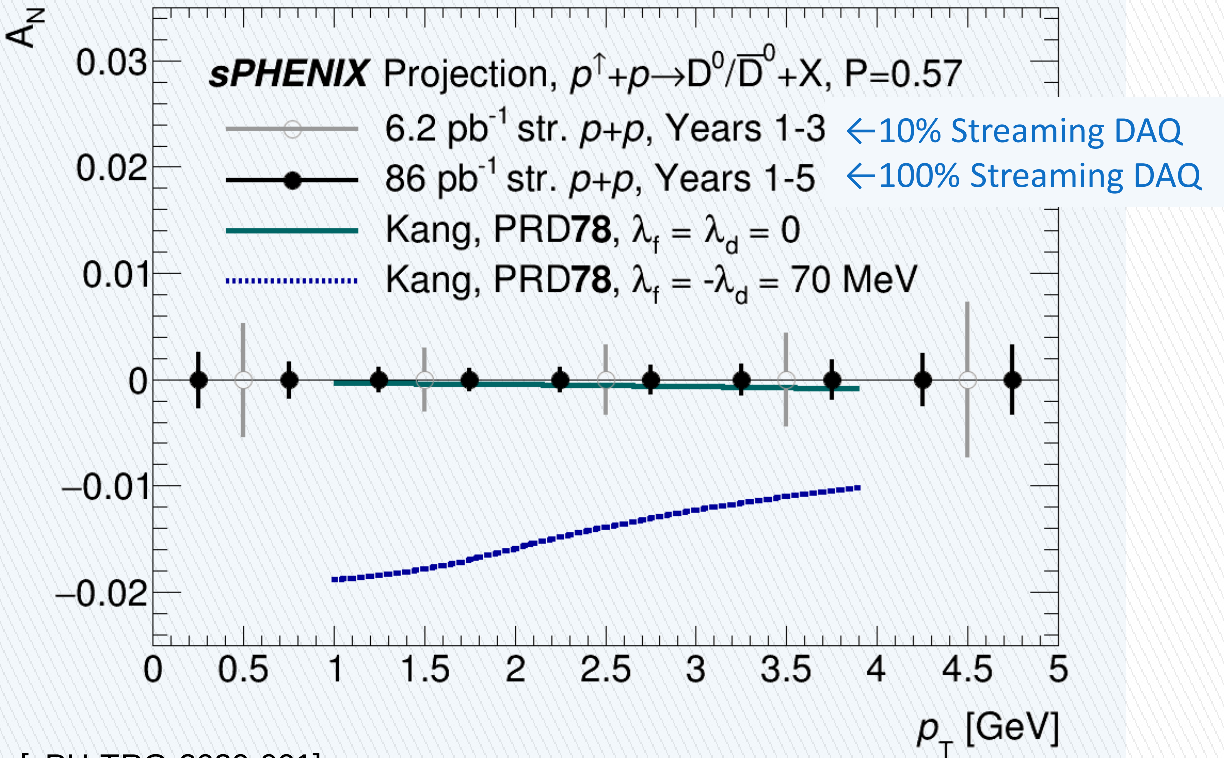
Simply prolong L1-Acceptance signal to each subsystem, from 1 BCO to T_{SRO}~67 beam crossings (~7us or 10% SRO data)
→ x500 increase of hard-to-trigger p+p sample
→ at cost only 50% increase in data vol. (by piggy back on long TPC readout window of 13us)



Streaming-DAQ enabled scientific connection: e.g. gluon dynamics via heavy flavor A_N

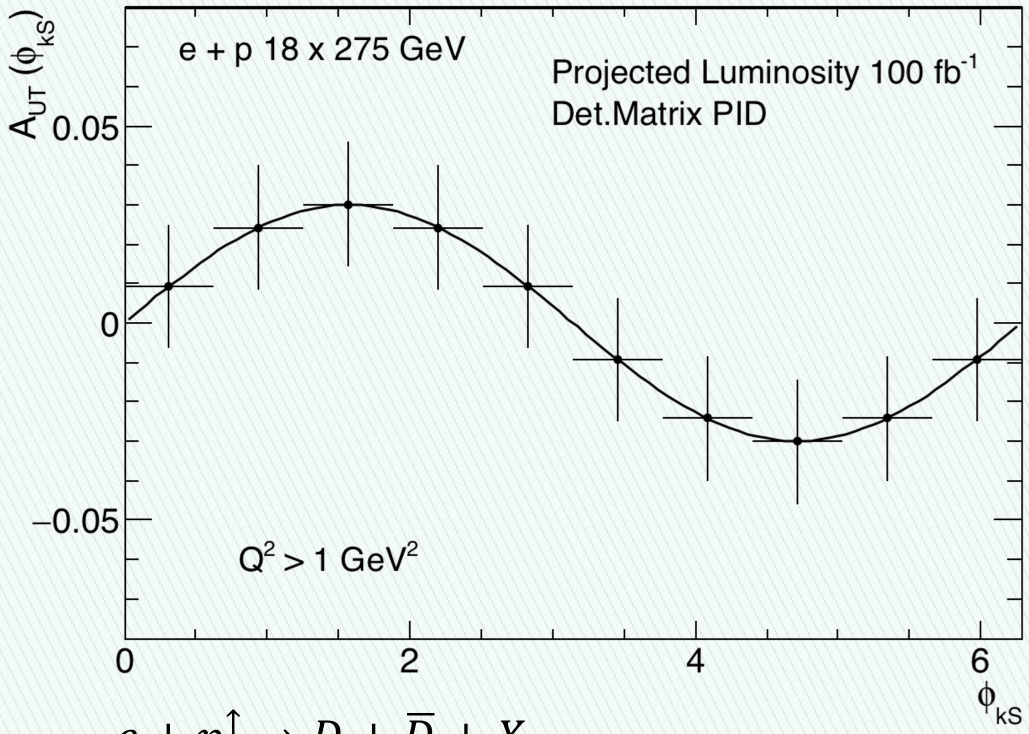
Universality test on gluon Sievers

sPHENIX D^0 trans. spin asymmetry, $A_N \rightarrow$ Gluon Sievers via tri-g cor.



[sPH-TRG-2020-001]
Model: 10.1103/PhysRevD.78.114013

EIC SIDIS D^0 transverse spin asymmetry → Gluon Sievers



$e + p^{\uparrow} \rightarrow D + \overline{D} + X$

[CNFS HF@EIC workshop, Nov 4-6, 2020]

EIC: unique collider
→ unique real-time system challenges

	EIC	RHIC	LHC → HL-LHC
Collision species	$\vec{e}+\vec{p}, \vec{e}+A$	$\vec{p}+\vec{p}/A, A+A$	$p+p/A, A+A$
Top x-N C.M. energy	140 GeV	510 GeV	13 TeV
Bunch spacing	10 ns	100 ns	25 ns
Peak x-N luminosity	10^{34} cm^{-2} s^{-1}	10^{32} cm^{-2} s^{-1}	10^{34} → 10^{35} cm^{-2} s^{-1}
x-N cross section	**50 µb**	**40 mb**	**80 mb**
Top collision rate	500 kHz	10 MHz	1-6 GHz
$dN_{ch}/d\eta$ in p+p/e+p	0.1-Few	~3	~6
Charged particle rate	**4M N_{ch}/s**	**60M N_{ch}/s**	**30G+ N_{ch}/s**

- EIC luminosity is high, but collision cross section is small ($\propto \alpha_{EM}^2$) → low collision rate
- But events are precious and have diverse topology → hard to trigger on all process
- Background and systematic control is crucial → avoiding a trigger bias

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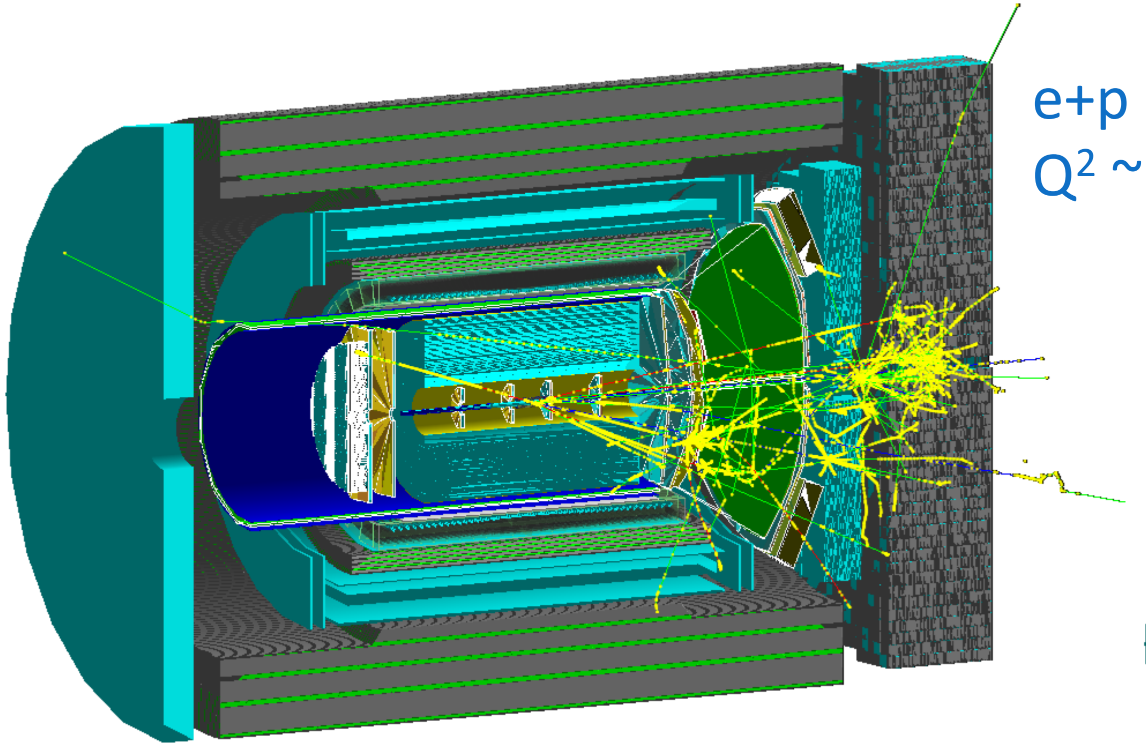
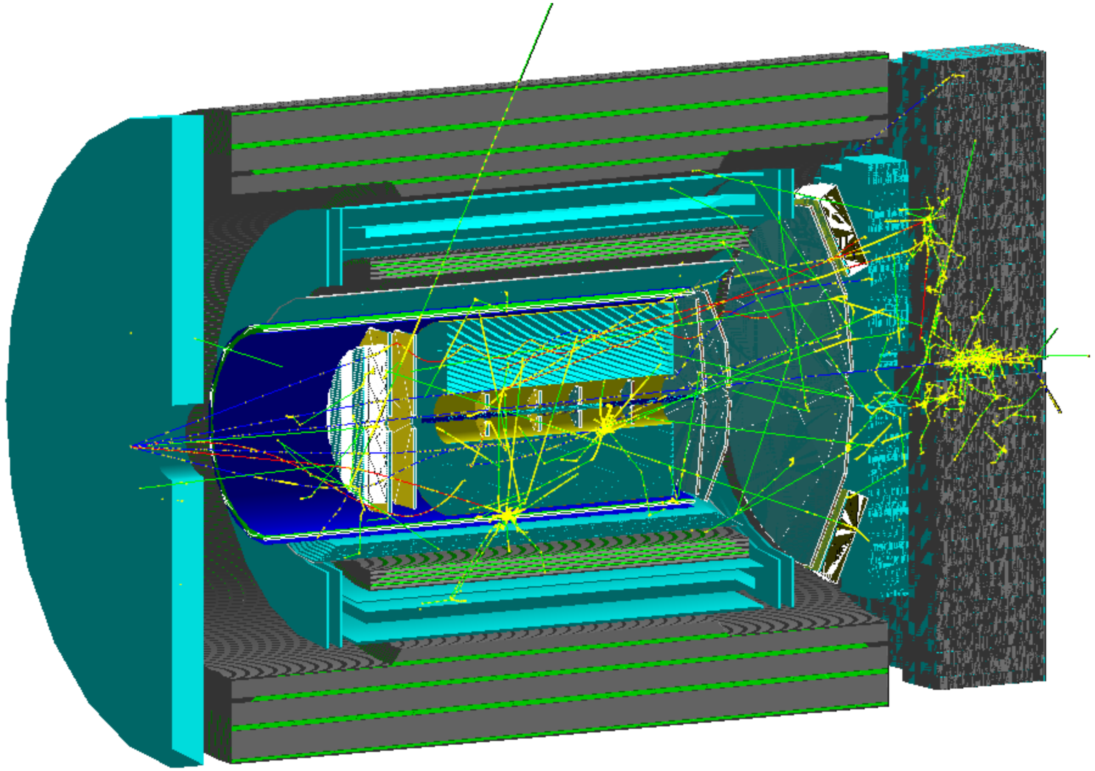
EIC DAQ in Fun4All-EIC simulation

Refs: EIC CDR, sPH-cQCD-2018-001: https://indico.bnl.gov/event/5283/



e+p DIS 18+275 GeV/c
$Q^2 \sim 100\ (GeV/c)^2$



Beam gas event
p + p(gas), 275 GeV/c
at z=-4 m

Data Rate

MAPS silicon tracker

Raw data: 16-24 bit / MAPS hit (3-layer ALPIDE model)

TPC

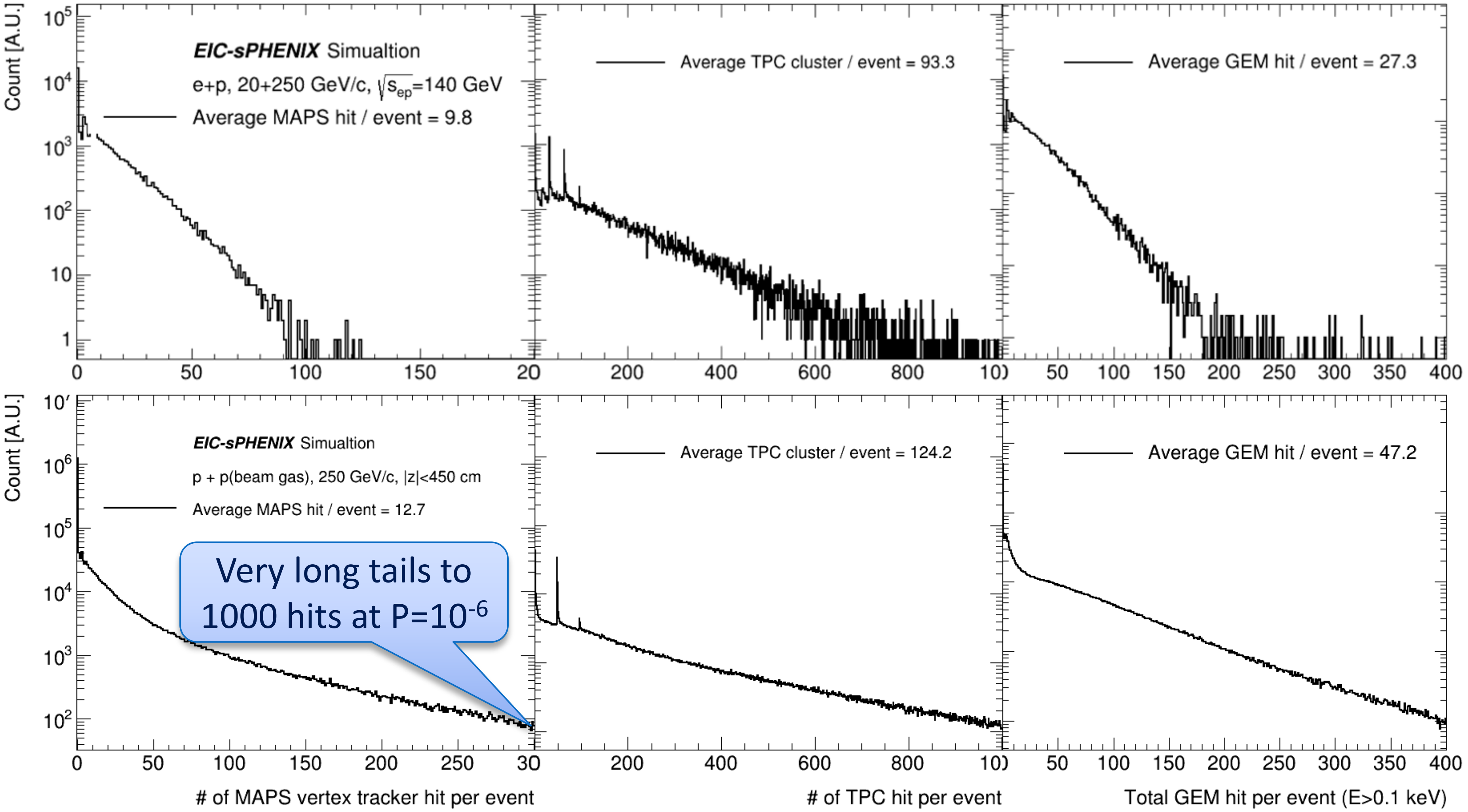
Raw data: 3x5 10 bit / TPC hit + headers (60 bits)

Forward/backward GEM

Raw data: 3x5 10 bit / GEM hit + headers (60 bits)

e+p, Pythia6 Q2>0

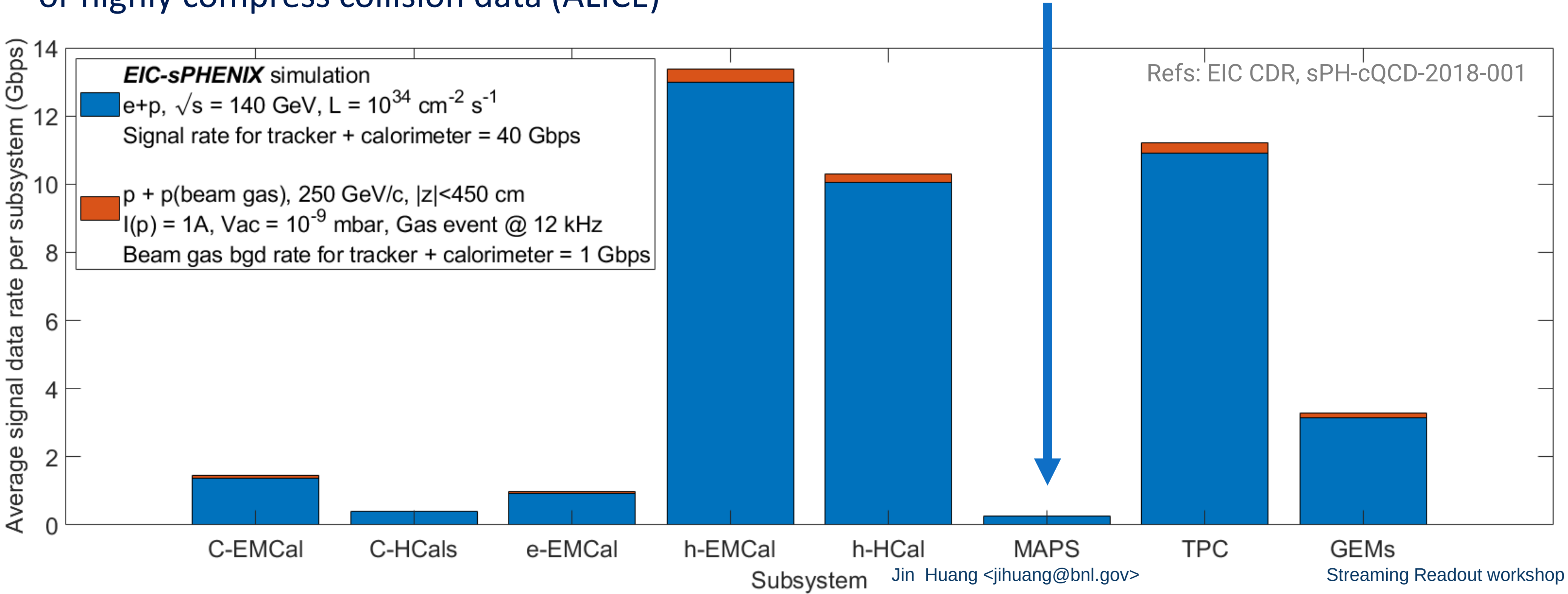
p+p(gas) Pythia8



Refs: ECI CDR, sPH-cQCD-2018-001: https://indico.bnl.gov/event/5283/

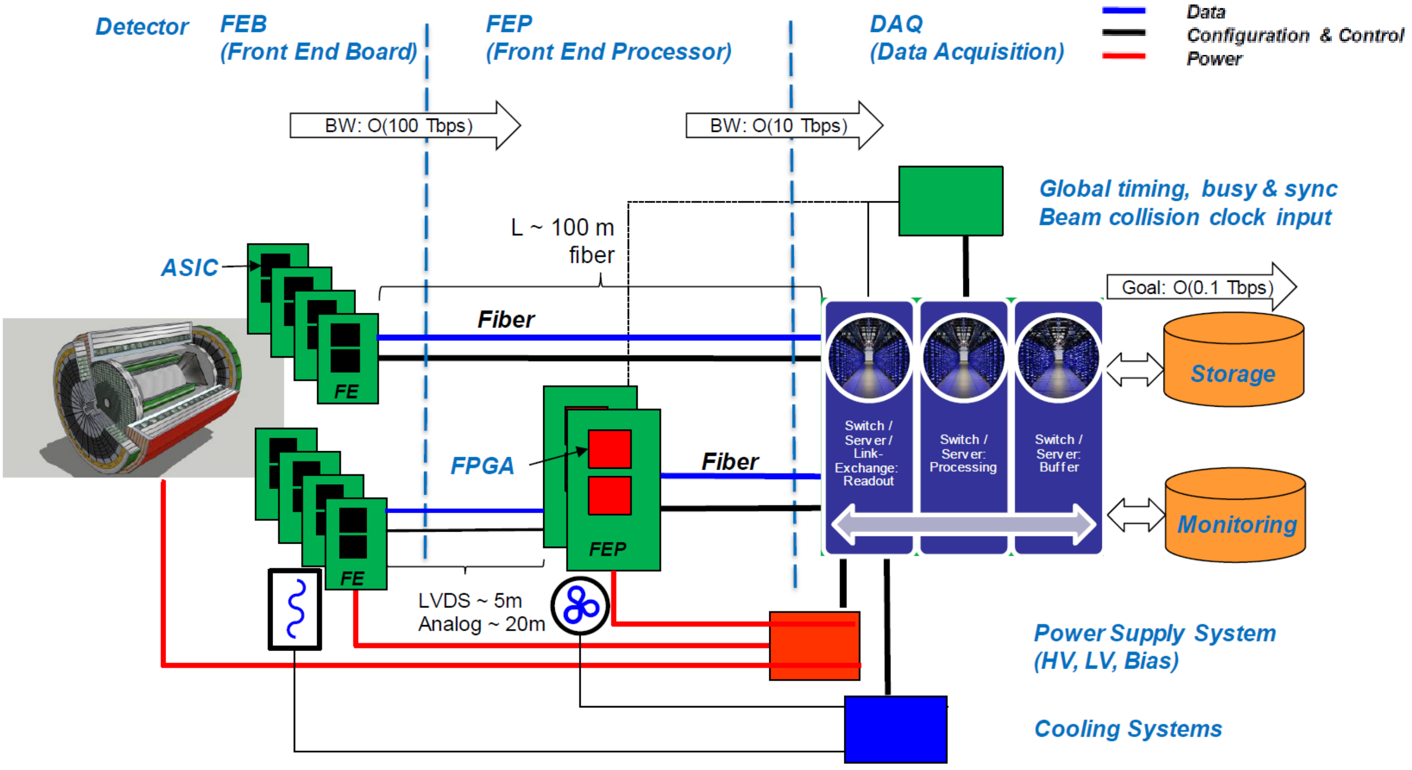
Signal data rate -> DAQ strategy

- What we want to record: total collision signal ~ 100 Gbps @ 10^{34} cm^{-2} s^{-1}
  - Assumption: sPHENIX data format, 100% noise, Less than sPHENIX peak disk rate. 10^{-4} comparing to LHC collision
- Therefore, we could choose to stream out all EIC collisions data
  - In addition, DAQ may need to filter out excessive beam background and electronics noise, if they become dominant.
  - Very different from LHC, where it is necessary to filter out uninteresting p+p collisions (CMS/ATLAS/LHCb) or highly compress collision data (ALICE)



Strategy for an EIC real-time system

- **EIC streaming DAQ**
  - → Triggerless readout front-end (buffer length : μs)
  - → DAQ interface to commodity computing (e.g. FELIX/CRU). Background filter if excessive background rate
  - → Disk/tape storage of streaming time-framed zero-suppressed raw data (buffer length : s)
  - → Online monitoring and calibration (latency : minutes)
  - → Final Collision event tagging in offline production (latency : days+)

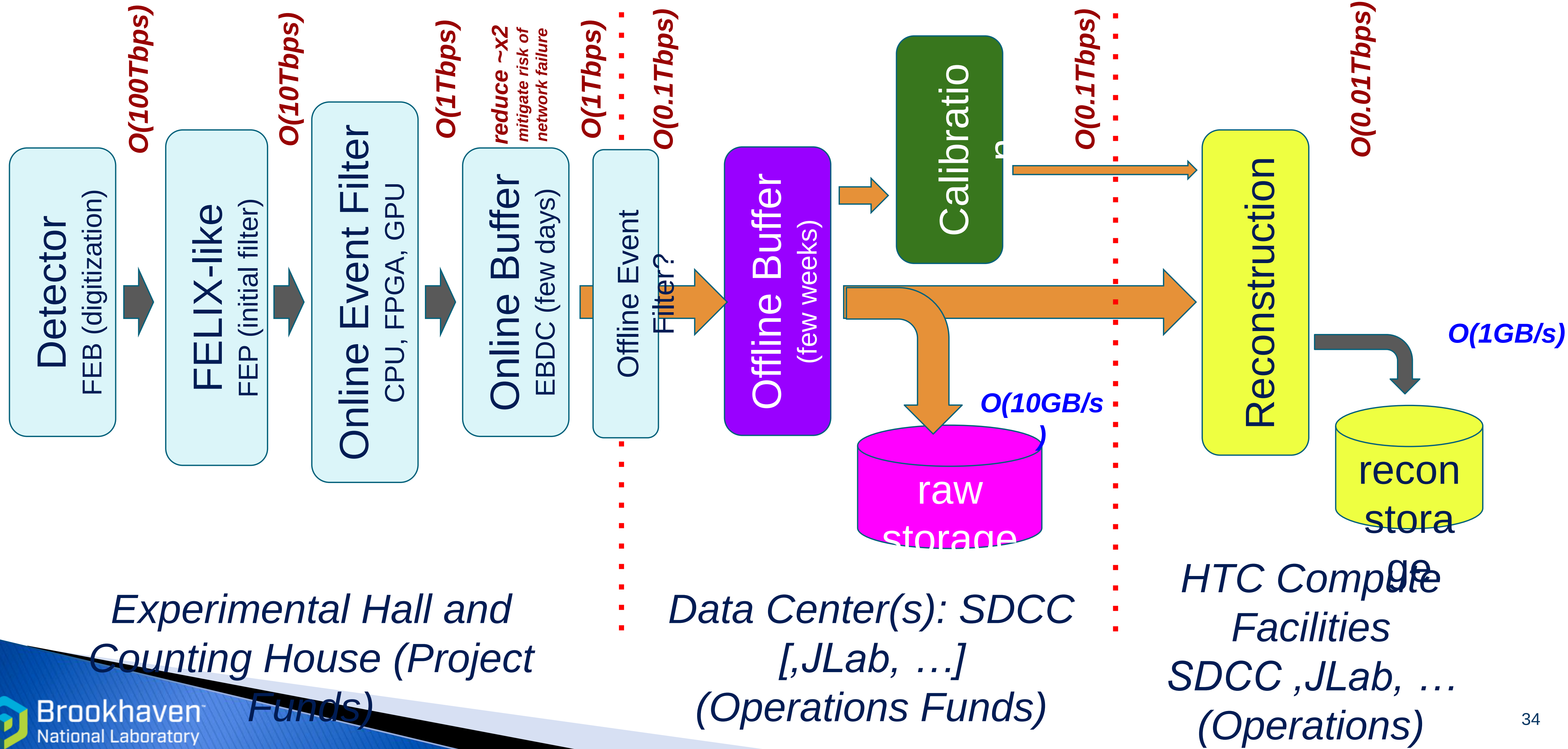


Ref: EIC-CDR

Blured boundary with offline computing

See also: last talk M. Battaglieri

Countesy: David Lawrence
ECCE computing model [link]

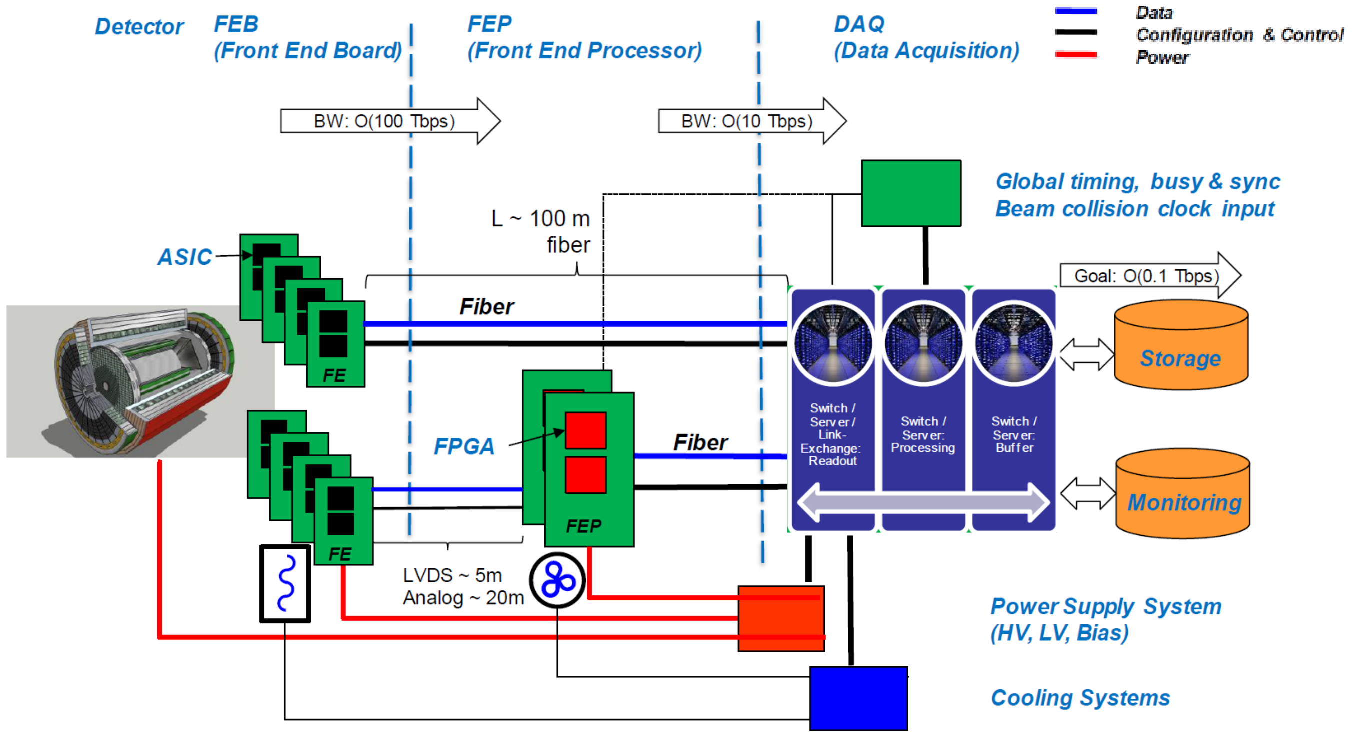


Real-time computing for streaming data pipeline

- Despite low signal rate, the raw data rate can be filled with noises and background
  - Need low background & low noise detector & electronics design
- An essential job of EIC real-time computing: reliable streaming data reduction to fit permanent storage (next topics)
- And more traditional roles for online/offline server farm:
  - Online monitoring/fault det.
  - Calibration
  - Production → Initial analysis pass

ASIC, FPGA FPGA, TPU, GPU, CPU

Digitizer BW: 10^2 Tbps → Readout BW: 10^2 Tbps → Storage: 10^{-1} Tbps



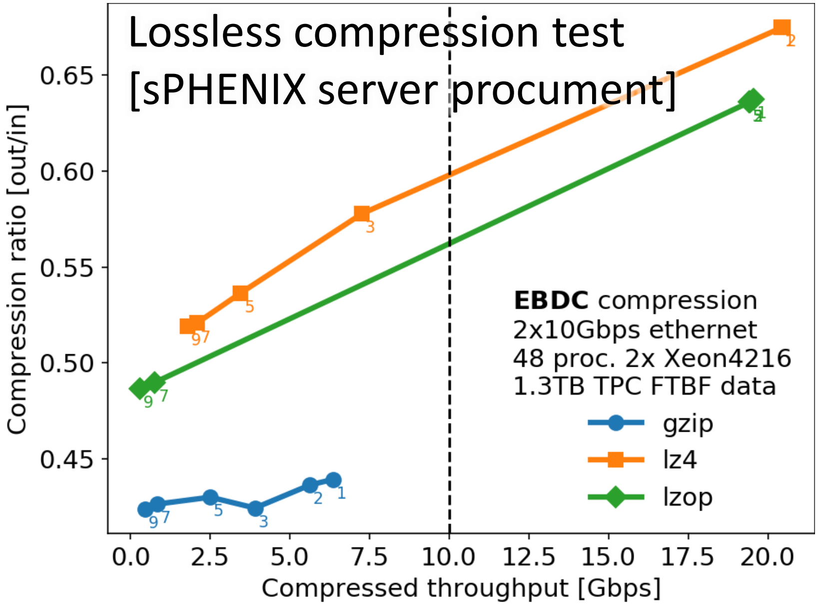
[EIC CDR]

Online computing for streaming data – trigger throttling

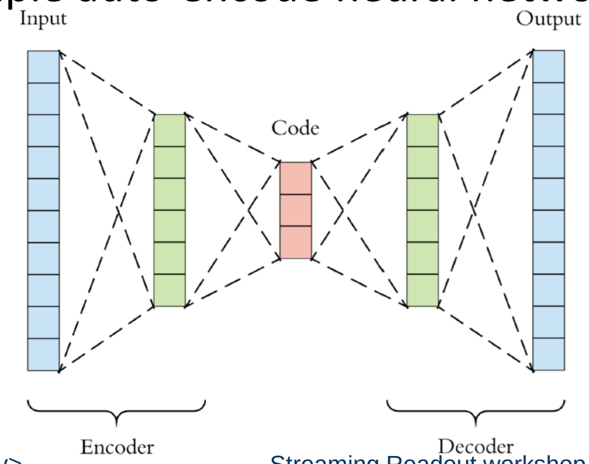
- At the beginning of the EIC operation, background & noise rate could be unpredictable and high
- A contingency method: throttling streaming data with triggering
  - Immediately reduce streaming data by orders of magnitudes
  - Widely used hardware producing trigger, fix latency or HLT (Aaji's talk)
  - Has physics loss, added systematic uncertainty for hardware trigger efficiency
- Can utilize ML to produce more complex triggering on FPGA
  - PID trigger, e.g. ref: S. Furletov @ streaming workshop VIII [link]
  - Tracking-event topology trigger: D. Yu @ AI4EIC workshop [link]

Online computing for streaming data - compression

- Lossless compression
  - Compress by ~1/2
  - Well established fast compression algorithm
- Lossy compression
  - Opportunity for unsupervised machine learning based on data, e.g.
  - Auto-encoder on ASIC for HGCal @ CMS [link]
  - Bicephalous Convolutional Neural Encoder for zero-suppressed data (next)

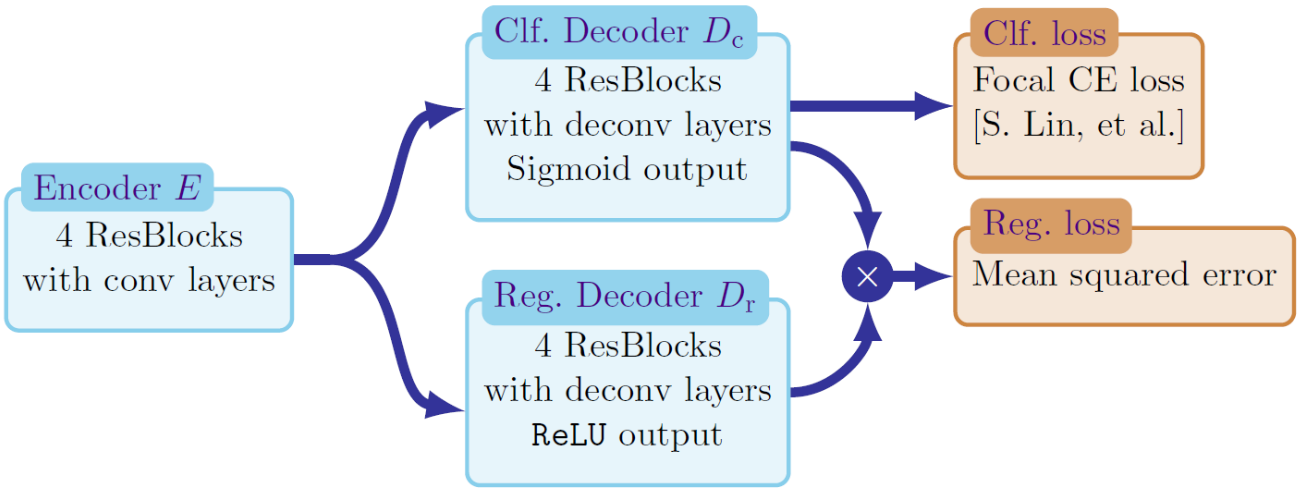


Simple auto-encode neural network

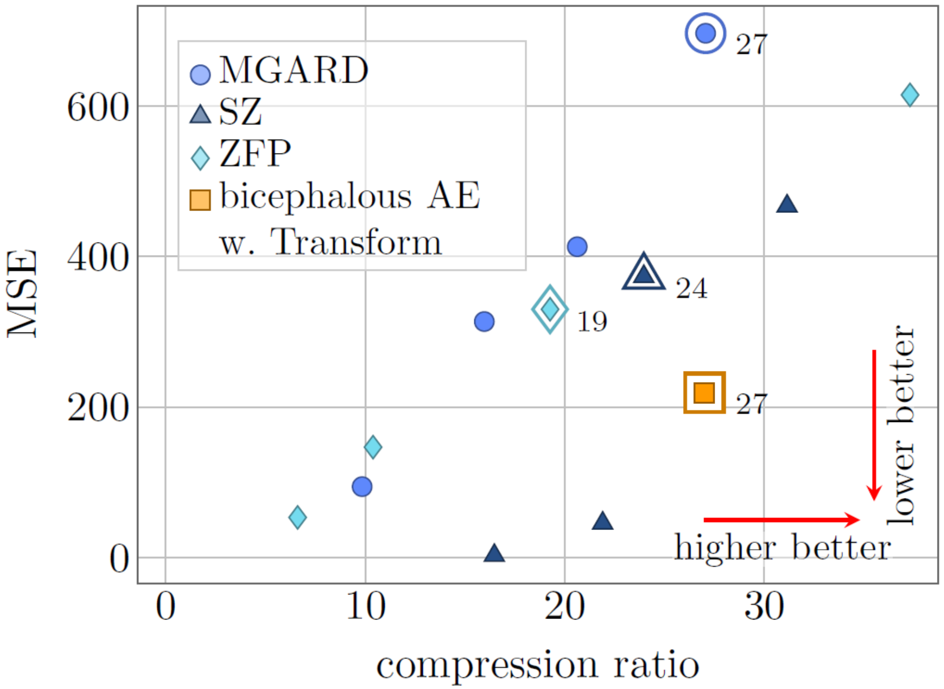


Bicephalous Convolutional Auto-Encoder for zero-suppressed data

- Some detector ADC data is challenging for Auto-Encoder, e.g. features such as zero-suppression cut off
- A dual-output auto encoder is designed to output both a region of interest and decompressed ADC. Possibility for further noise filtering
- Ref: Y. Huang @ AI4EIC workshop [link]



Compression comparison with published compressor tested on busiest sPHENIX TPC timeframes



Online computing for streaming data - feature building

- Another effective way of suppressing background is feature building, e.g.
- Clustering on calorimeter
  - Effective in suppressing single tower noise
  - e.g. CLAS12 test as in M. Battaglieri’s talk
- Tracklet building on tracker:
  - Effective in suppressing isolated noise, such as the synchrotron background
  - e.g. ALICE TPC streaming data [arXiv:1910.12214]. D. Yu @ AI4EIC workshop [link]
- ADC timeseries -> amplitude extraction
  - e.g. Specialized filters: C. Crawford @ Streaming readout VIII [link];
  - Neural network on ASIC: S. Miryala @ Streaming readout VIII [link]

EIC x-sec : further quantification [Courtesy E. Aschenauer]

- Inelastic e+p scattering x-sec:
  - For a luminosity of 10^{34} $cm^{-2}s^{-1}$ 50ub corresponds to **500 kHz**
- Elastic e+p cross-section:
  - For EIC central barrel, elastic cross section is **small** comparing to the inclusive QCD processes
- Beam gas interaction:
  - Beam proton – beam gas fix target inelastic interactions. The pp elastic cross section is smaller (~7 mb)
  - For a vacuum of 10^{-9} mbar in the detector volume (10m) this gives a rate of **14 kHz**

Beam [GeV]	HERA	5 x 50	10 x 100	18 x 275
$Q^2>10^{-9}$ GeV	65.6	**29.9**	**41.4**	**54.3 ub**
$Q^2>1$ GeV	1.29	0.45	0.65	0.94 ub

Beam [GeV]	HERA	5 x 50	10 x 100	18 x 275
σ $[y_{Exp} > -4]$	5 pb	**5 ub**	**0.7 ub**	**0.06 ub**
σ $[y_{Exp} > -6]$	11 ub	420 ub	100 ub	29 ub

E_p:	50 GeV	100 GeV	275 GeV	920 GeV
	38.4 mb	**38.4 mb**	**39.4 mb**	41.8 mb

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