ASIC and Microelectronics: Requirements and Design Process Considerations

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Instrumentation Division

Advancing and delivering technology: from basic research to scientific applications and partnership with industry

Strategic Thrust: to develop technologies to advance programs in science, energy, security, and industry

Key Capabilities: design, fabrication, assembly, and testing of detector components and systems

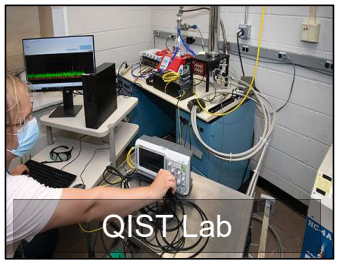
- sensors, microelectronics, photocathodes

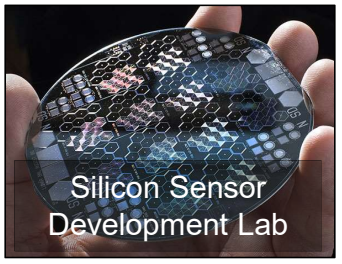
Focus on Emerging technologies:

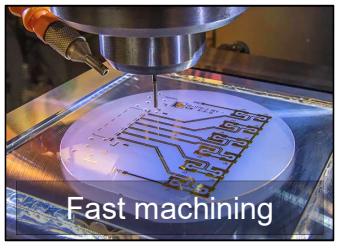
- quantum communication and sensors
- embedded AI / edge computing
- 5G and precision timing / synchronization

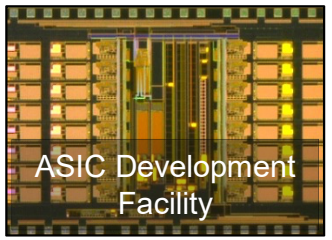
Partnerships:

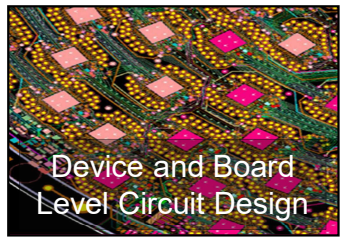
- Other laboratories, industry and academia











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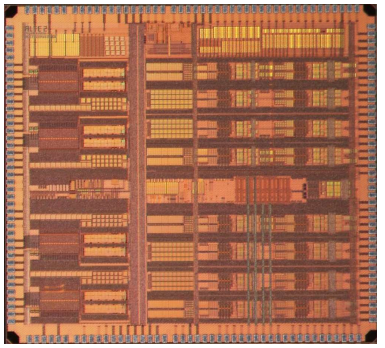
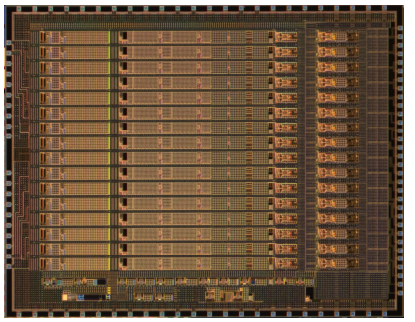
https://www.bnl.gov/instrumentation/

ASIC People and CAD/EDA Tools

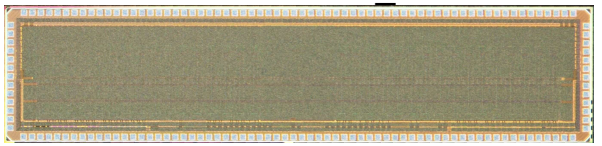
Expertise in low-noise, low power, large mixed-signal designs

- 7 full time ASIC designers
  (5 PhDs + 2 in PhD program, including industrial background)
- ongoing targeted hiring for satisfying needs across multiple programs
- open for hosting guest/visitors and grad/post-grad students
- hand-in-hand with in-house TDAQ, PCB, sensors and other groups





LArASIC_P4 180 nm
ALFE2 130 nm
AVG_DEV 65 nm



Design tools and methodologies

- industry-standard tools from Cadence, Siemens (Mentor), etc.
  (analog on top or digital on top flows)
  analog: full custom flow (VSE, VLE, ADE/Spectre, AMS, PVS, XACT3D-PEX)
  digital RTL2GDS: functional simulation, logic synthesis, automated P&R, parasitics extraction, static timing analysis (XCELIUM/GENUS/INNOVUS/QUANTUS QRC/TEMPUS)
  library characterization: custom standard cell libraries for designs for extreme environments: cryogenics and radiation
  verification: IR drop (VOLTUS/ VOLTUS-fi), functional (SV), physical (PVS, Calibre DRC/ERC/LVS)
  device modeling: TCAD, FEM solvers, transistor model parameter extraction (Silvaco ATHENA-ATLAS-VICTORY, Maxwell, UTMOTS4)
- foundry PDK's: *TSMC CMOS 350nm, 250nm, 180nm, 130nm, 65nm, GF CMOS and BiCMOS SiGe 130nm, 90nm, + specialized processes: monolithic CIS on HR, sensors co-design, High-Voltage etc.*
- access to foundries via: MOSIS, CERN-IMEC Foundry Services, IMEC and directly
- packaging: in house custom and through commercial sources

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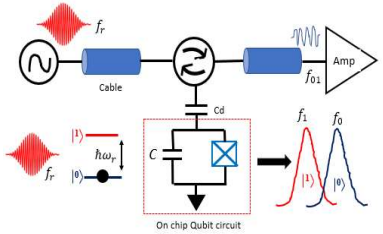
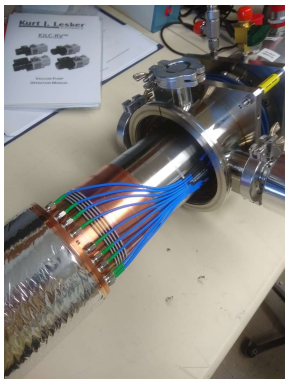
ASIC Collaborations, Areas of Activities and Research Interests



RF readout of qubits or quantum sensors / cryostat operating 4K for testing



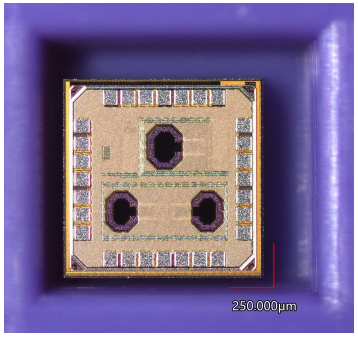
Collaborations:

- Universities: SMU, UMich, UPenn, MIT, Georgia Tech, Columbia, USF, UIUC
- National Laboratories: FNAL, LBNL, ORNL, NRL
- Industry: several industrial partners + more collaborators
- International: CERN, OMEGA, KIT Karlsruhe, AGH Krakow, UBonn

Support for the fast-developing scales and functionalities of modern microelectronics:

- meet customer's needs using established processes (130nm, 65nm)
- reaching for emerging technologies for R&D (28nm, specialized processes)

Quantum RF Chip Prototype 1 (QRFCP1)
With 5.12 GHz center frequency VCO and QVCO for PLL with CML divider and interfaces



Areas of Activities and Research Interests:

Low-noise and low-power

- custom analog front-end matched to a specific sensor
- front-end circuits optimized for amplitude & time-resolution
- data, event driven or zero-suppressed readout methodologies

Cryogenic operation

- readouts for liquid Noble gasses TPCs – R&D on readout electronics for DUNE's VD TPC, nEXO (lAr, lXe)
- long lifetime reliability
- development & maintenance of spice-type model parameters and characterization (.lib) of standard cell libraries
- RF electronics for quantum sensors (4K, ≤1K)

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V.Manthena et al, "A 1.2-V 6-GHz Dual-Path Charge-Pump PLL Frequency Synthesizer for Quantum Control and Readout in CMOS 65-nm Process", 2020 11th IEEE Annual Ubiquitous Computing, Electronics & Mobile Communication Conference (UEMCON), 2020, pp. 0570-0576

ASIC Collaborations, Areas of Activities and Research Interests

Radiation-Hardness

- immunity to TID, NIEL and SEE effects:
  - process (inherent to process)
  - design (achieved through proper design techniques)
- development of methodologies for radiation hardness
- development of methodologies for SEE immunity
- exploration of next-gen for HEP CMOS and BiCMOS processes

Hybrid-pixel detectors

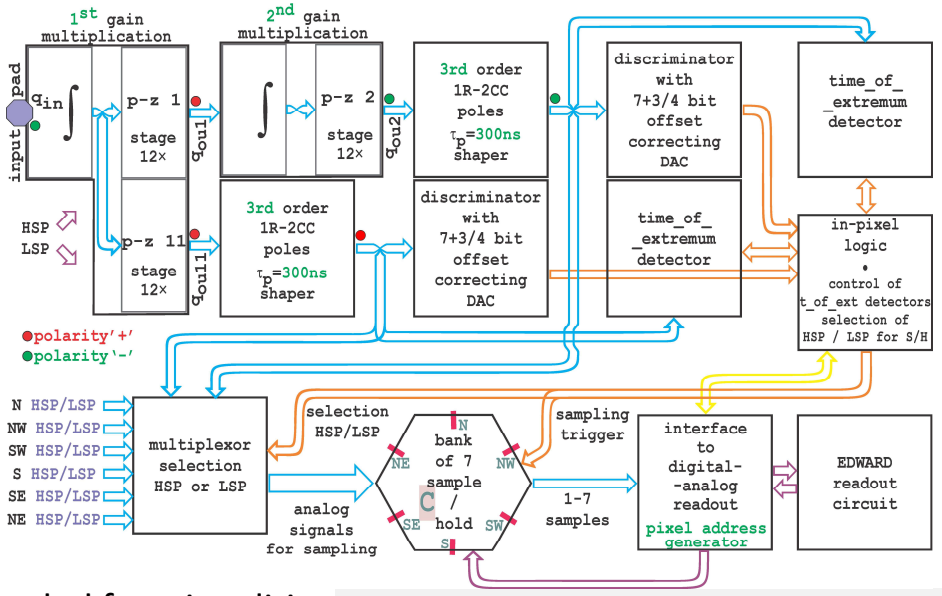
- spectroscopic detectors for X-ray detection (BES, BER, NASA)

Lightweight detectors, 3D-IC and HDI

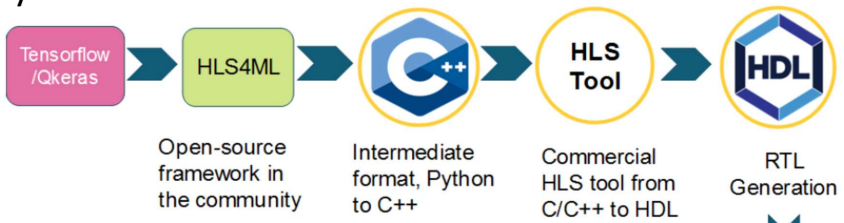
- edgeless and gapless, highly granular pixel detectors with extended functionalities
- development of large area sensors for the EIC vertex and tracking layers
- event-driven and neuromorphic suitable arrayed readouts

Embedded AI and neuromorphic processing

- data-science-driven co-design methodologies for FE ASICs
- matrix processing with new electron devices: memristors
- libraries from AI tools to Verilog and Spice, 3rd gen. NN (SNN)



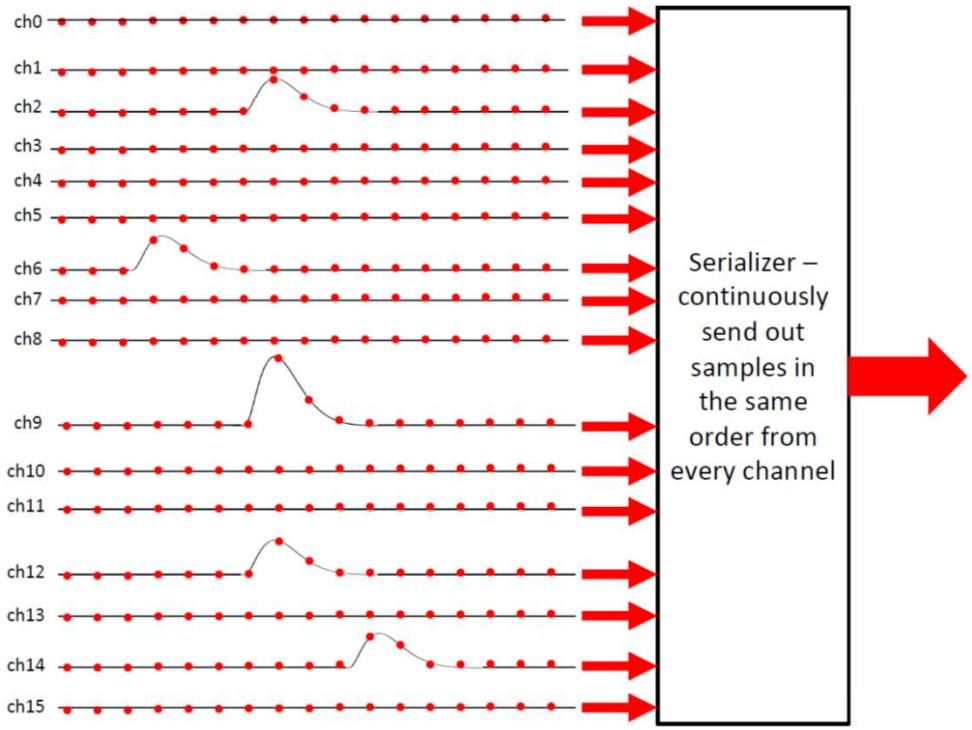
block diagram of the analog in-pixel front-end circuit.



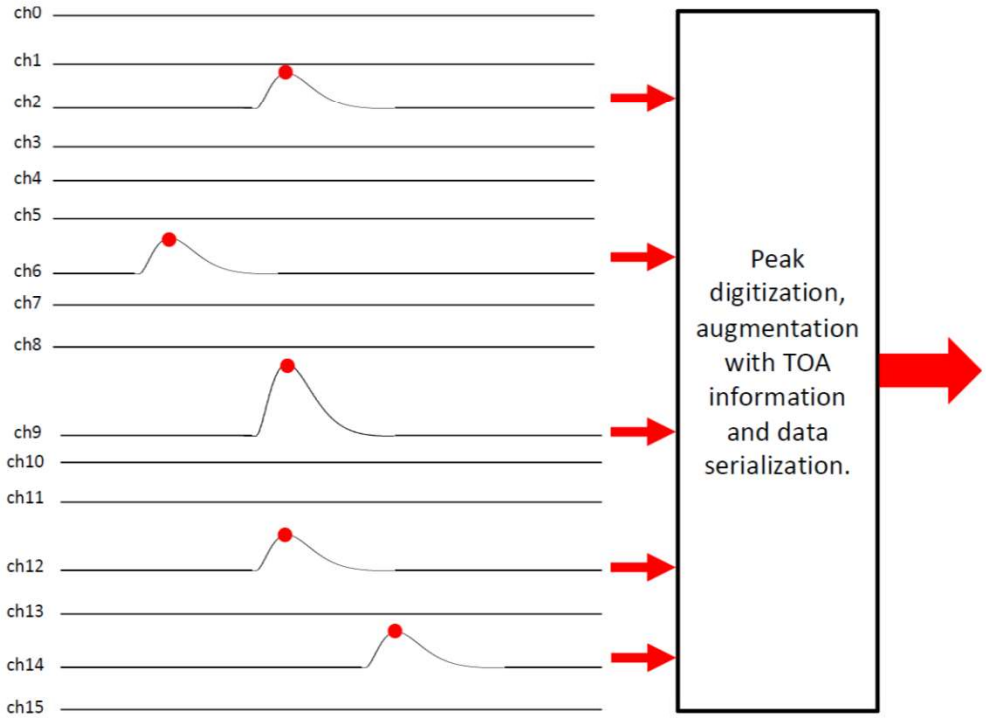
design flow for the synthesis methodology for FE embedded ANNs

S. Miryala et al., "Waveform processing using neural network algorithms on the front-end electronics", 2022 JINST 17 C01039

Streaming v.s. Data Push



Streaming all digitized waveform samples off



Sending extracted waveform features (amplitude, ToA, PID, direction etc.) off

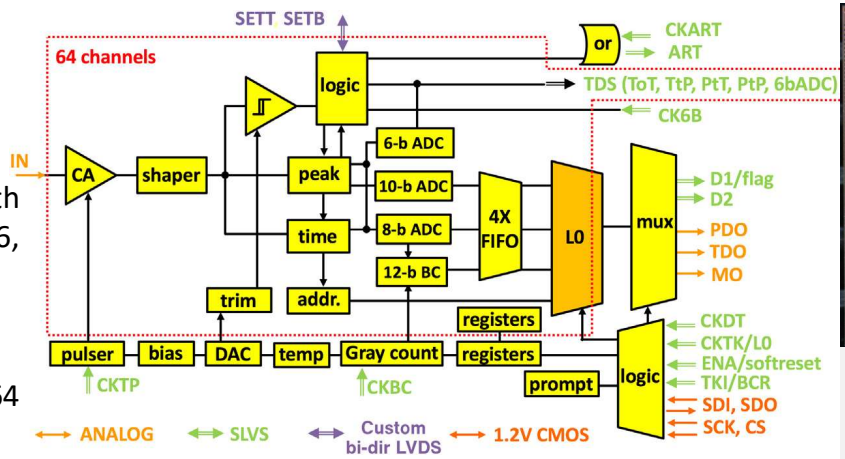
Digital Front-End ASIC can be designed allowing both strategies adapting to data rates, power that can be dissipated in the fiducial volume, confidence to processes data, etc.

Data Streaming or Sparsified Readout

- Detector readout concepts in multiple experiments are based on a very similar principle of:
  - pulse shaping signals with Front-End shaping filters,
  - digitization of waveforms (or digitization of detected signal extrema),
  - performing signal processing in the digital domain (extraction of additional features: amplitude, ToA, occurrence of pileups, etc.),
  - zero suppression or compression of data and conditioning for transmission,
  - transmission off the detector on high-speed, serial links.
- ➲ Streaming readout

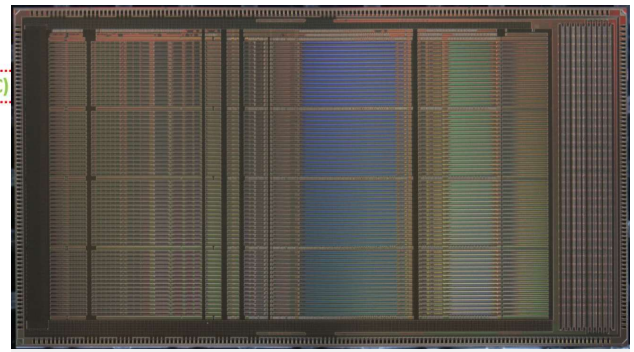
VMM3 features:

- 64 input channels / ASIC
- digital output for amplitude and ToA
- low power <10mW/ch
- τ_p=25, 50, 100, 200 ns (both polarities), and gain 0.5, 1, 3, 4.5, 6, 9, 12 , 16 mv/fC
- TAC slope 60, 100, 350, 650 ns
- neighbor logic, SPI for configuration
- buffering latency FIFO (up to 64 events)
- 8b/10b encoding



Architecture of the VMM. Most of the block diagram describes one of the identical 64 channels of the chip
(The VMM readout system, BNL-213684-2020-JAAM)

VMM
legacy successful BNL design
In GF 130 nm (former IBM 8RF-DM) process



VMM3/3a developed 2015-2017 10M FETs
VMM3a – production version

- Suitable for variety of application
- Nevertheless, its developmental version with upgraded functionalities is currently discussed

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Scalable next-gen. detector front-end

- Optimized two-chip solution:

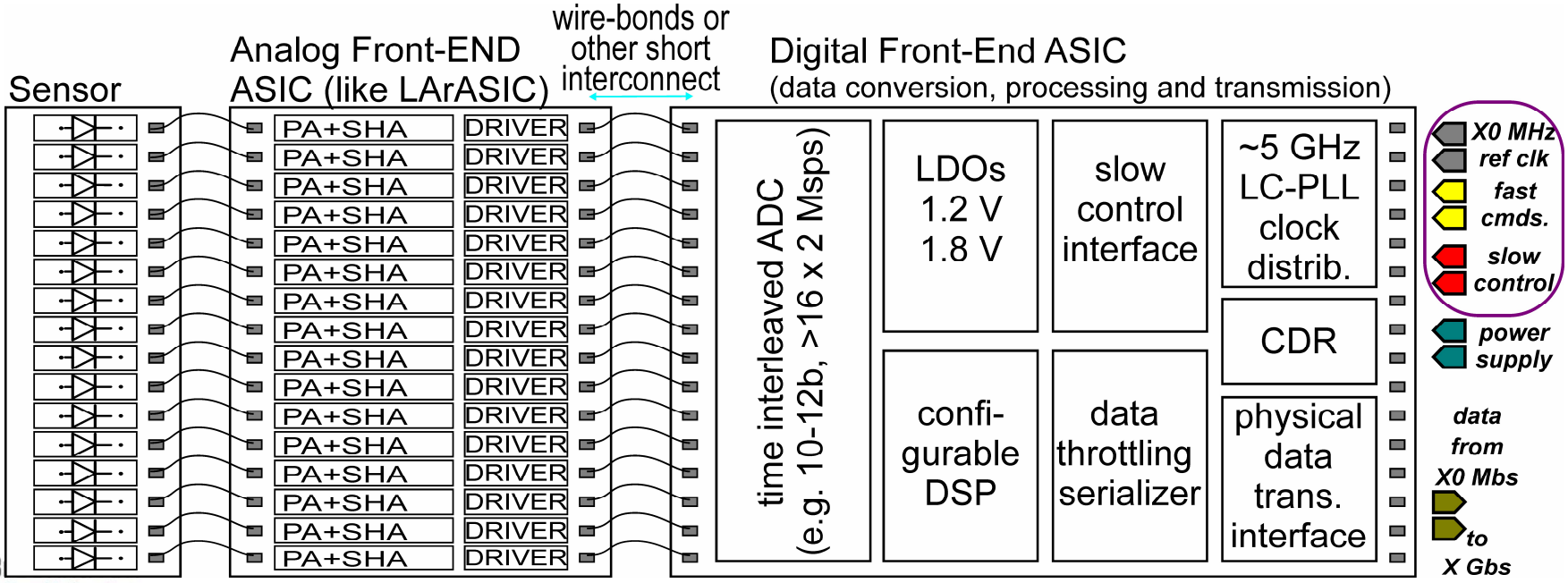
  Separates high-sensitivity analog from mixed-signal and digital circuits.

  Allows optimal allocation of functionality with fewer risks.

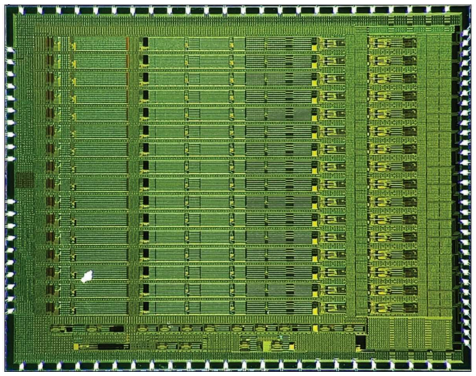
  Speeds up timeline by allowing for independent, parallel development paths.

  Does not significantly increase packaging complexity compared to a “single ASIC” approach.

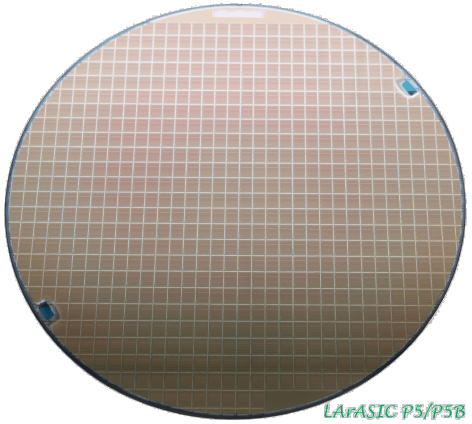
  Under active development for upcoming experiments such as nEXO.



Front-end ASIC design



CMOS 180 nm process, 1.8 V,
6 metal layers

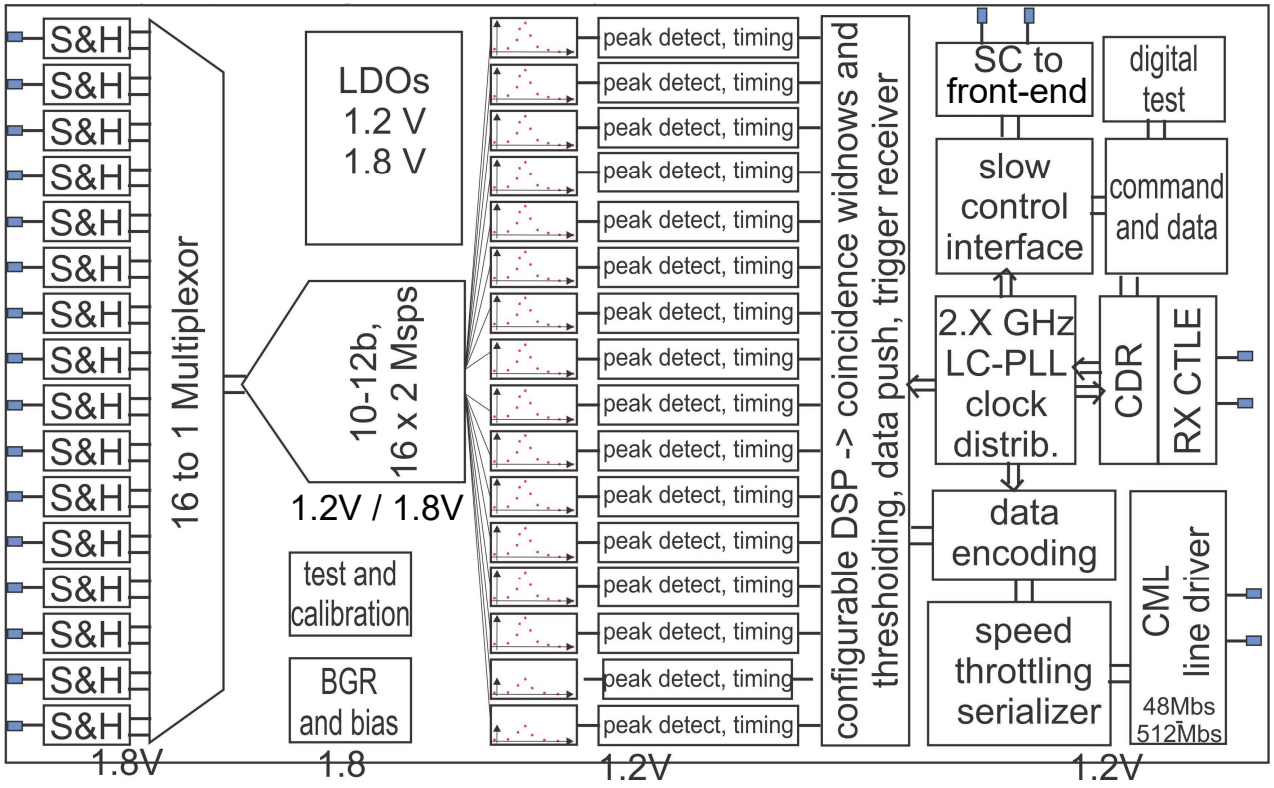


8” wafer with 610 LArASICs P5 and
P5A(B) w. increased ESD protection

- Based on existing LArASIC cryogenic front-end ASIC designed by BNL for the DUNE experiment.
- Can be ported to a more advanced process (e.g., 65 nm) to improve performance.
- LArASIC features:
  - 16 channels, two-stage charge amplifier, high-order filter (5^{th}).
  - Adjustable gain: 25, 14, 7.8, 4.7 mV/fC (max. charge 55, 100, 180, 300 fC).
  - Adjustable filter time constant (peaking time 0.5, 1, 2, 3 μs).
  - Selectable DC/AC coupling (100 μs HPF time-constant).
  - Integrated 6-bit pulse generator.
  - 144 configuration registers, SPI control interface.
  - Low power: 6 mW/channel without buffer (input MOSFET consumes 3.9 mW) + 4 mW for common circuitry.

Back-end ASIC design

Back-end ASIC (data processing and transmission)



SC = Slow Control
CTLE = Continuous-Time Linear Equalizer
CDR = Clock and data recovery, BGR = Band-gap reference

- Digital backend ASIC with DSP capability for Snippet waveform sampling (reduced data rates and volume)
- Pushes most embedded processing into the digital domain for improved reliability and configurability.
- Includes on-chip low-jitter clock distribution via LC-PLL.
- Supports hardware implementation of AI-based processing algorithms.
- Minimizes power consumption using low-power digital and mixed-signal design methods.
- Can support either separate clock, data, and SC links, or a combined high-speed link.

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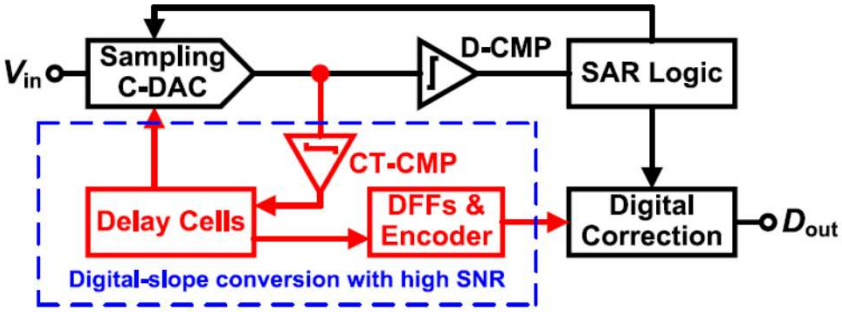
Building block #1: Fast, low-power ADC

Energy-efficient hybrid ADC for streaming data readout

Low-power 12-bit hybrid ADC design in 65 nm CMOS:

- Overall: 8-bit SAR (MSB) + 5-bit digital slope (LSB).
- SAR/digital slope boundary uses 1 redundant bit for robustness, thus resulting in 12-bit resolution.

- **Asynchronous successive approximation (SAR) converter:**
  - Fully-differential charge redistribution architecture.
  - Split capacitor DAC (C_{unit} = 20 fF) using an energy-efficient merge-and-split (MS) switching scheme.
  - Uses one redundant conversion cycle (9 cycles for 8 bits) to obtain robustness to comparator noise and V_{REF} settling error.
- **Asynchronous digital slope (DS) converter:**
  - Asynchronous (self-timed) delay line-based architecture to ensure low power and robustness to PVT variations.
  - DS capacitors ($C_0 = C_{unit}/8$ = 2.5 fF) are laid out within the SAR DAC to minimize SAR-DS gain mismatch and simplify calibration.
- **Additional features:**
  - On-chip reference buffer w/ cancellation of switching transients.
  - On-chip digital calibration of comparator offset; supports off-chip calibration of DAC capacitor mismatch.



Preliminary performance specifications

Parameter	Value
Sampling rate	Up to 50 MS/s
Output resolution	12-bit
Full-scale voltage	1.7 V_{pp}
Effective no. of bits (ENOB)	11.0
Core power (at 50 MS/sec)	820 µW
Reference buffer power	1.15 mW
Walden FOM (including buffer)	19.5 fJ/bit

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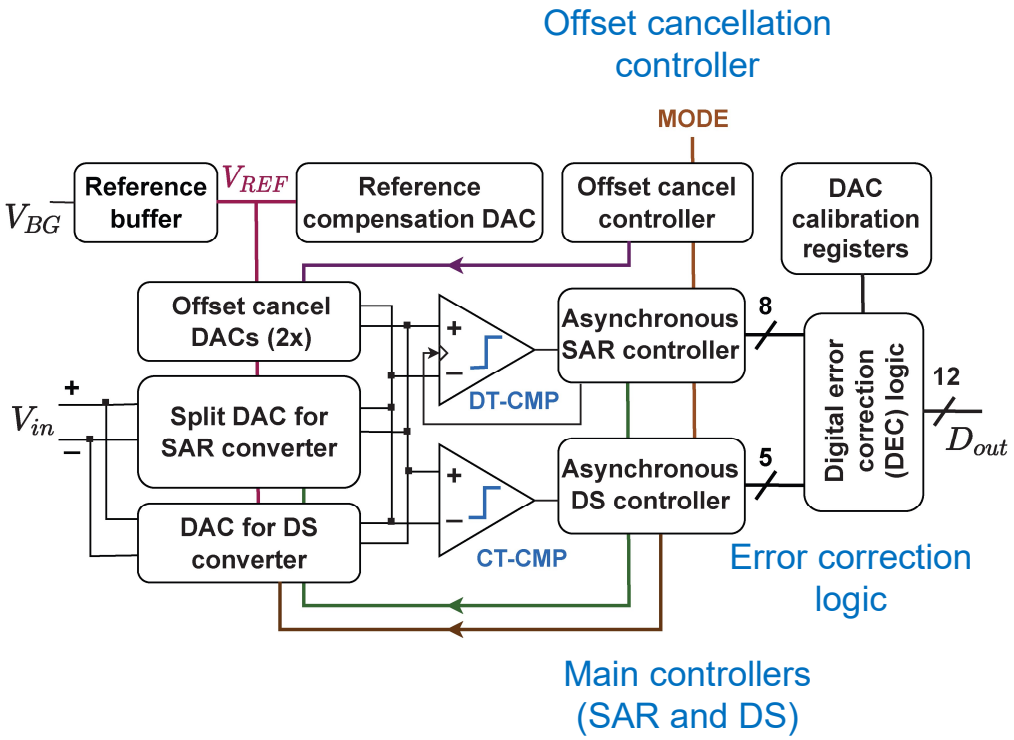
Block diagram of the hybrid ADC

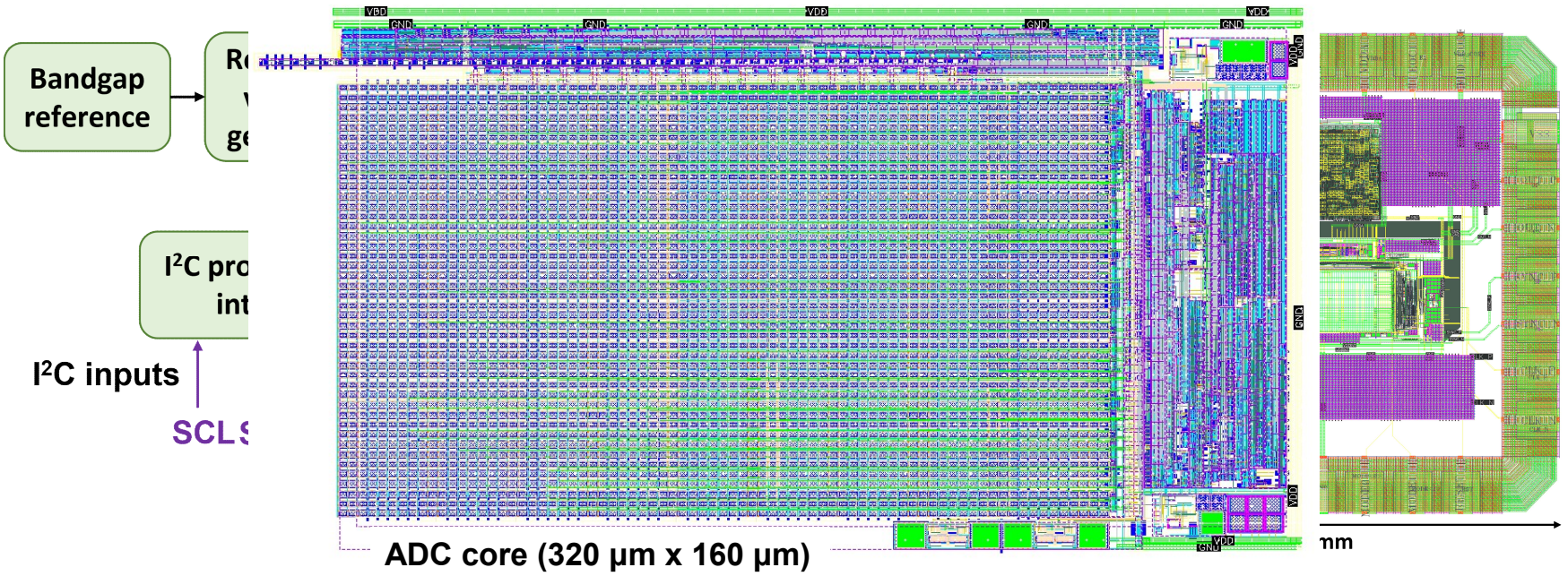


- Implemented in the TSMC 65 nm CMOS process.
- Includes four major operating modes:
  - Normal operation
  - Discrete-time comparator (DT-CMP) calibration
  - Continuous-time comparator (CT-CMP) calibration
  - DAC capacitor mismatch calibration
- All digital logic is realized inside deep N-wells to provide isolation from on-chip analog circuits.
- Uses separate analog and digital power supplies (VDD = 1.2 V, VDDA = 1.8 V).
  - The analog supply is used by the band-gap reference (V_{BG}) and reference buffer.
- Delay tuning bits within the controllers can be externally set (2-bit resolution).

Summary of the key design innovations

Description of the innovation	Main effects
Hybrid architecture: SAR + digital slope (DS)	Utilizes the complementary advantages of the two architectures to improve overall ADC FOM.
Asynchronous (self-timed) conversion	Reduces conversion time; eliminates high-speed clock
Merge-and-split (MS) capacitor switching	Reduces switching power consumption
Redundant SAR conversion with on-chip digital error correction (DEC) logic	Provides robustness to comparator errors and reference buffer settling transients; allows reduced buffer power
Reference buffer transient compensation	Allows buffer power to be further reduced
Neutralization of comparator input capacitance	Improves ENOB by reducing harmonic distortion
Comparator offset cancellation	Provides robustness to comparator offset
Foreground calibration of the capacitor DAC	Provides robustness to systematic capacitor mismatch
Tunable time delays within the asynchronous SAR, DS, and calibration controllers	Robustness to process-voltage-temperature (PVT) variations

Design of the ADC test chip



- Layout area of the ADC core (not including reference buffer) = 320 µm x 160 µm.
- The 1 mm^2 test chip integrates the ADC with accessory circuits (band-gap voltage reference, clock receiver, sampling clock generator, output serializer, serial programming interface, and power-on reset).
- Chip layout and verification is complete; queued for fabrication in mid-June.

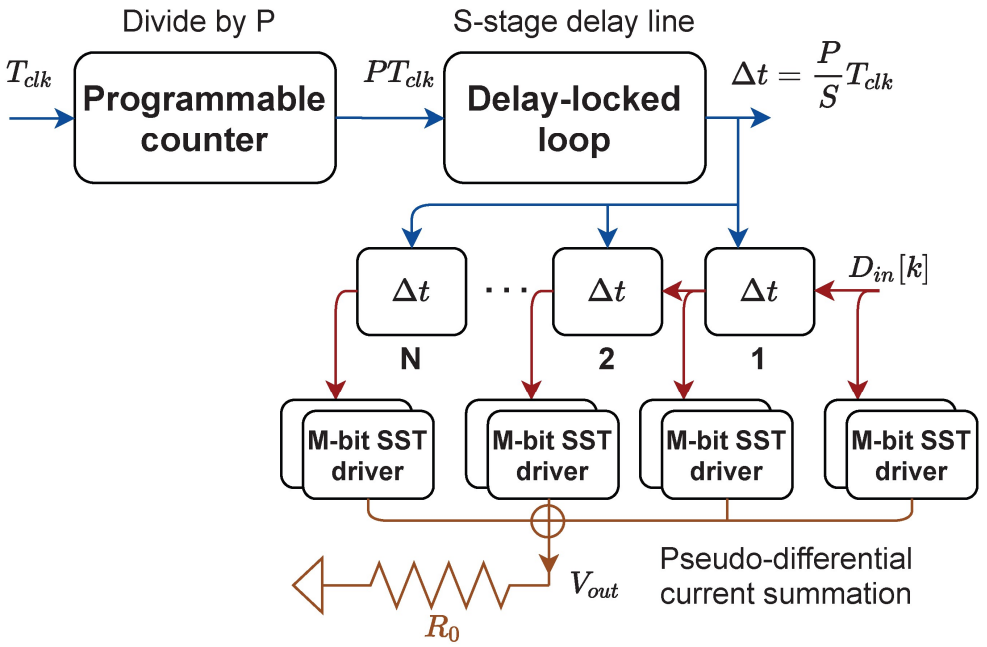
Building block #2: Low-power data driver

- Enables high-speed digital data transmission over lossy cables by implementing a multi-tap feed-forward equalizer (FFE).
  - Uses a programmable *N*-tap FFE (e.g., *N* = 3) to allow operation for multiple cable configurations.
  - Uses pseudo-differential source-series terminated (SST) drivers to reduce power consumption.
  - The FFE time delays are stabilized using an on-chip delay-locked loop (DLL).
  - Capable of reliable operation in high-radiation and/or cryogenic environments.

Preliminary performance specifications

Parameter	Value
Waveform programmability	UI / 16
Data rate	Up to 1 Gb/s
DLL power (at 1 Gb/s)	7.2 mW
Driver power	4.8 mW

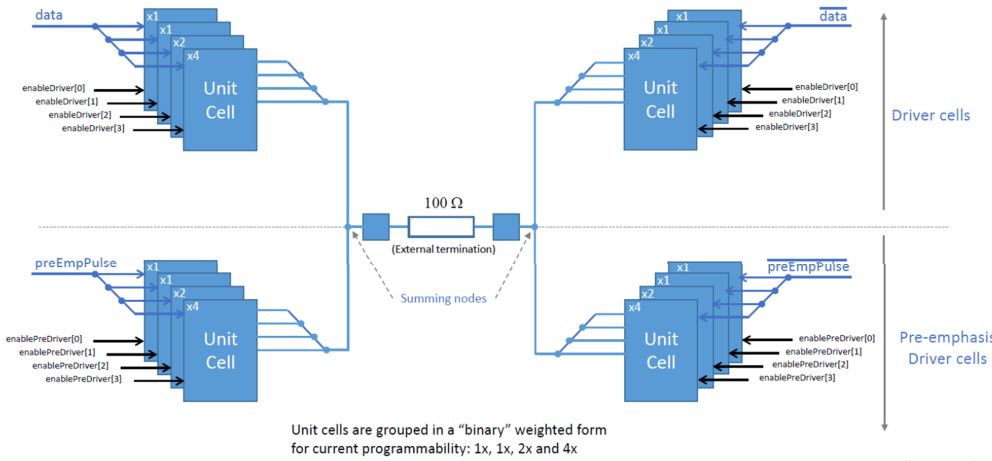
UI = Unit Interval (i.e., duration of 1 bit)



Low-Power Gigabit Line Driver with User-Configurable Pre-Emphasis for Lossy Transmission Lines

- Line drivers are very important blocks for many ASIC designs.
  - Effective line drivers must be designed specifically for the application at hand to effectively drive the desired cable in a power-efficient manner.
  - Rather than designing a custom line driver for each ASIC, a single block with configurable parameters is proposed to work optimally for a variety of cables.

Example of Current Line Driver Design: lpGBT



Paulo Moreira, CERN (2017)

- Upcoming experiments, such as nEXO, require line drivers capable of transmitting across very high loss radio-pure cables.

Pre-emphasis is needed to adequately drive such cables.

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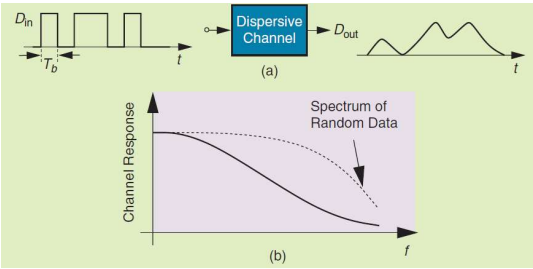
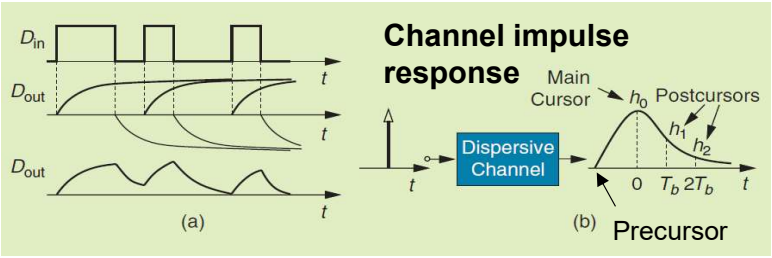
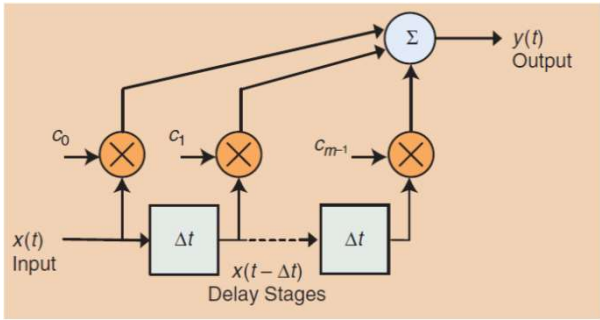
Effects of frequency-dependent channels on digital data



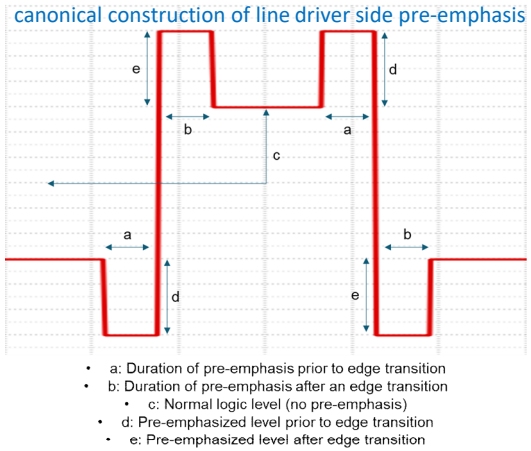


Behzad Razavi, *IEEE Solid-State Circuits Magazine*, 2017

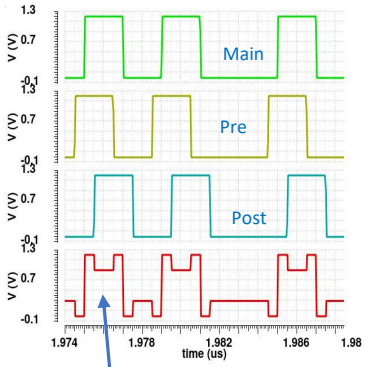
- Limited channel bandwidth results in attenuation, data-dependent jitter, and inter-symbol interference (ISI).
- Pre-Emphasis, also known as Feed-Forward Equalization (FFE) is a method in which the waveform of transmitted data is manipulated to cancel out the filtering effects of cable channels.
- Pre-Emphasis is generally implemented via a Finite Impulse Response (FIR) filter as shown right

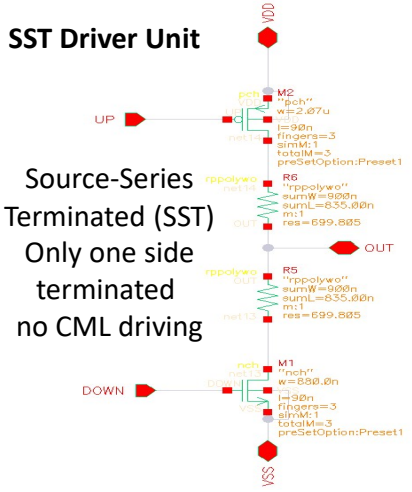


John F. Bulzacchelli, "Equalization for electrical links: current design techniques and future directions." *IEEE SSC Magazine* 7.4 (2015): 23-31.



- a: Duration of pre-emphasis prior to edge transition
- b: Duration of pre-emphasis after an edge transition
- c: Normal logic level (no pre-emphasis)
- d: Pre-emphasized level prior to edge transition
- e: Pre-emphasized level after edge transition



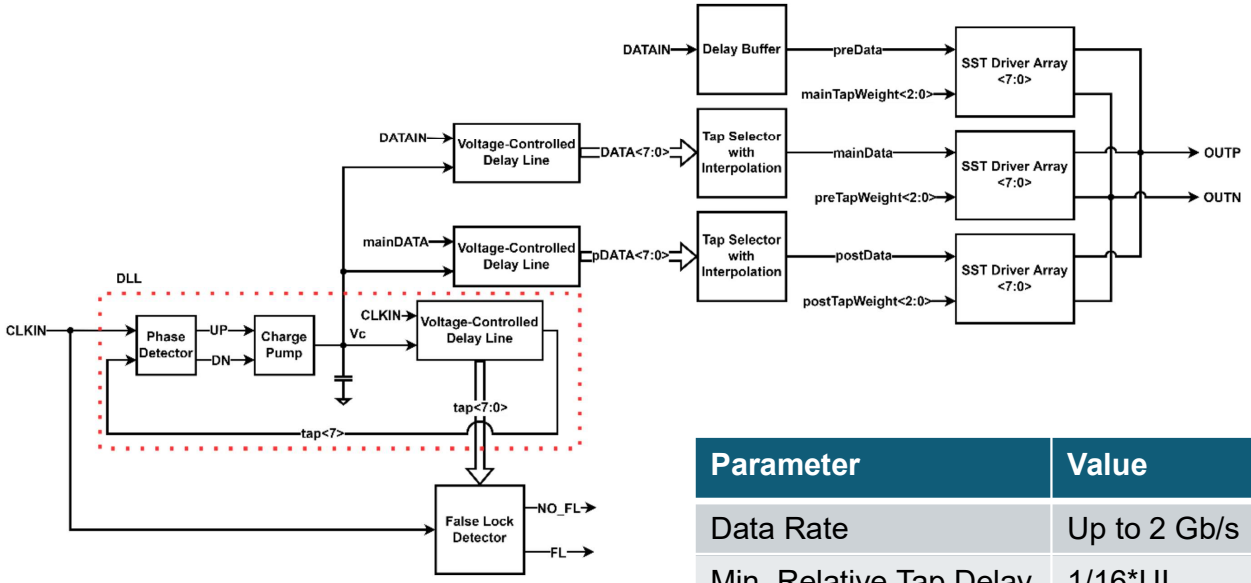


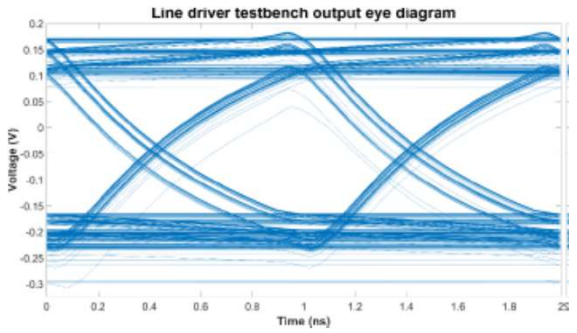
- Here we propose to implement generalized pre-emphasis functions in which both c_i and the time delays Δt are individually programmable.
- User-configurability (~10%)

Proposed Line Driver Block Diagram

The line driver will contain:

- An 8-Stage Delay-Locked Loop (DLL) with a single-test False Lock Detector.
- Replica Voltage-Controlled Delay Lines (VCDLs) that utilize the DLL to create delayed versions of the input data.
- Digital Interpolator blocks that allow the user to select a delayed data copy or interpolate two adjacent copies, giving the user a total of 16 delay options.
- Three programmable arrays of Source-Series Terminated (SST) drivers for power-efficient transmission and adjustable weights for each tap with acceptable impedance matching.





100 Ω terminated 3 m of high loss Taiflex cable with attenuation of -19 dB at 1 GHz

Parameter	Value
Data Rate	Up to 2 Gb/s
Min. Relative Tap Delay	1/16*UI
Min. Tap Amplitude	75 mV
Non-Driver Power (at 1Gb/s)	2.4 mW
Total System Power (at 1Gb/s)	7.2 mW

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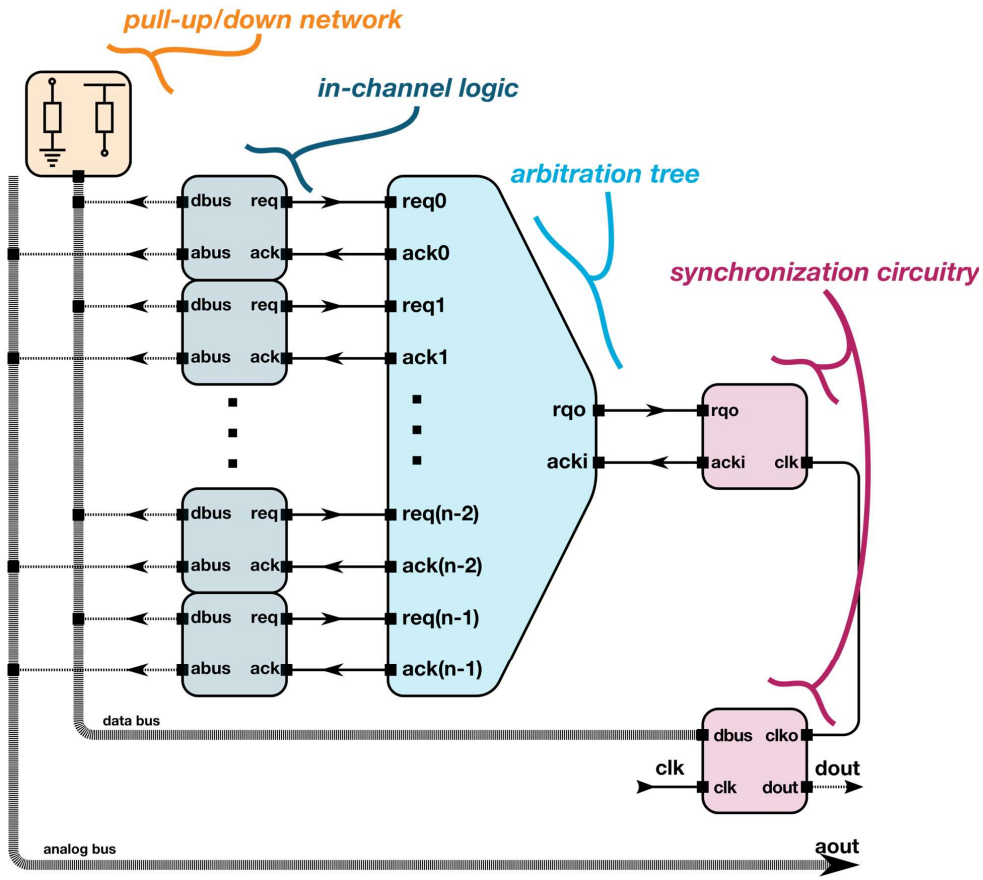
Building block #3: Efficient data readout architectures

EDWARD – **E**vent **D**riven **W**ith **A**ccess and **R**eset **D**ecoder

- Reset decoder provides guaranteed readout time for each transaction, and no dead time between them
  - No need to provide a clock to each pixel - requests can be sent asynchronously
    - Uninterrupted access to data within a pixel
      - No priority encoder



Event Driven Readout (EDWARD)

D.S. Gorni, et al., " Event driven readout architecture with non-priority arbitration for radiation detectors", 2022 JINST 17 C04027

TWEPP 2021

Introduction

The poster introduces an efficient system for collecting sparse data originating in multiple sources that operate asynchronously, ultimately sending data to the central data acquisition system in such a way that there is no direct relationship between spatial position of the channel and the order of the channels to be transmitted. The protocol and hardware architecture were developed for ASICs destined for reading out 1D or 2D multichannel radiation sensors that can be micro-strip or pixelated radiation sensors. The presented system can be used to read out both digital and analog data from the channels. It is done via shared digital data buses and analog wires.

Default bus state

The 'rqo' output from the arbitration tree is effectively the logical sum of requests from all channels. This signal, however, is not synchronized in any way with the acknowledgement tokens - the request may come after token expiration or come too late, and the token will not be able to start the transaction due to too short duration of the active state in the channel. For this reason, a mechanism should be provided to distinguish between data derived from readout of a channel and an empty state. This has been implemented as a **network of up and down pulls that delineate empty data**. The pattern thus determined can then be discarded on-chip by a peripheral circuit or off-chip in the acquisition system.

Arbitration tree

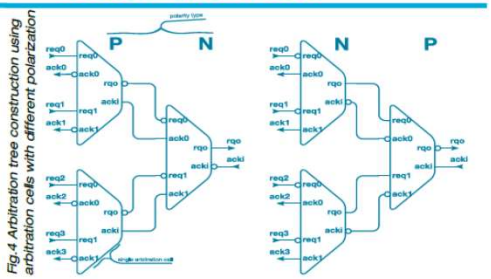


Fig.4 Arbitration tree construction using arbitration cells with different polarization

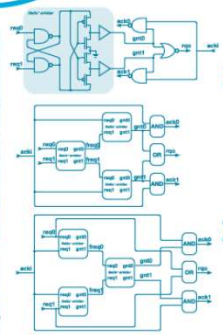


Fig.5 Diffrent embodiments of arbitration cell

- An arbitration cell upon receiving read request signals 'reqX', selects one of the read request signals and routes an acknowledge token 'acki' that reaches this cell as routed from another arbitration cell located above in the arbitration tree to the direction from which the read request signal has been accepted. Routing is done in a form of gating of the acknowledge signal with the use of grant signals (gnt0, gnt1) generated by the arbiter. The arbiter decides which of the two read request signals is selected and there is **no priority between signals.** When two read request signals arrive simultaneously, one of them is selected, whereas the selection is random.
- Basically, almost all the arbitration cells need to be able not only to decide which of the two read request signals can be services but also whether new read request signals arrive during the active level of the acknowledge signal. The latter goal is rising a need of arbitrating between the read request signals and the acknowledge signals, leading to the general concept of the readout control system with **arbitration that is operated without distributing any system clock.**

In-channel logic

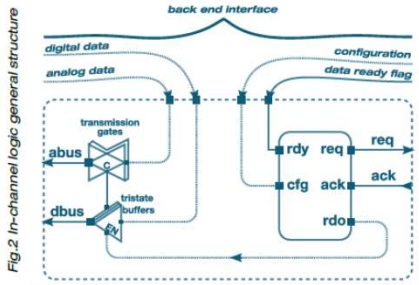


Fig.2 In-channel logic general structure

- This is a logic presented in each channel and its function is to manage readout transactions between the channel and global peripheries.
- When the data ready flag 'rdy' is set by the back end electronic (e.g. peak found, ADC conversion done) the controller block issues the read request 'req' **immediately.**
- When 'req' is active, the readout phaser block is sensitive to the transition to the active logic state on the channel acknowledge input 'ack'.
- This transition can be describes as receiving an **acknowledge token** with assigned expiration time, after which 'ack' switches back to the inactive state.

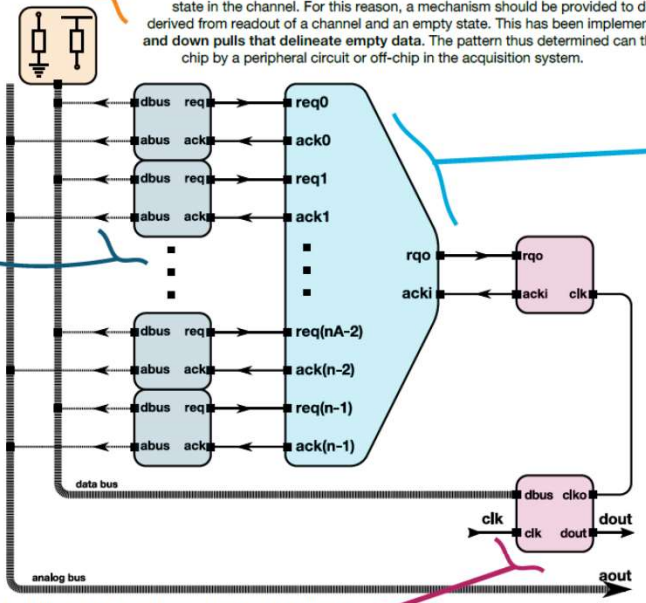


Fig.1 Block diagram of event driven readout system

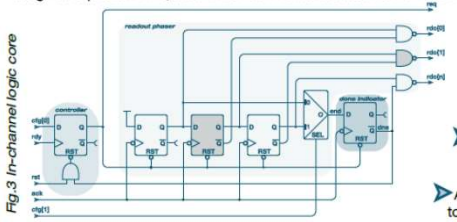


Fig.3 In-channel logic core

- The first token initiates readout transaction.
- A single transaction may consist of **multiple readout phases** in which different data (including data from adjacent channels) may be transmitted sequentially and uninterrupted by requests from other channels.
- The maximum number of phases is determined by the number of flip-flops in the phaser chain. However, the actual number of phases can be dynamically reduced by various 'cfg' configurations.
- Only one bit of the redaout control 'rdo' is active during each transaction This active bit is used to enable the corresponding bank of tristate buffers and transmission gates.
- After the last phase is processed done flag 'dne' is set and in result next token initiates reset procedure for in-channel logic during which 'req' is cleared.

Synchronization

The data are latched inside the output periphery by the clock 'clk'. Latching of the data synchronizes the readout with the data acquisition system. Data are latched before generation of each new token, yielding a new set of latched data for each token. Data can be sent serially off the chip. The **serialization clock is used therefore for generating readout tokens** through its appropriate division, whereas the duty cycle and frequency of the divided clock 'clko' can be decided with a significant level of a latitude.

Design and results

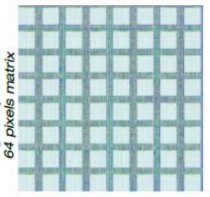


Fig.6 Layout of the 64 pixels matrix

In Fig.6 layout of the pixel matrix consisting of 64 channels is presented. Physical design was implemented with the use of the tools for automatic P&R and TSMC 65nm Standard Cell Library with added designs for Seitz' arbiters. The squares shown in the figure are placeholders for the analog frontend.

Transistor level simulation results are shown in Fig. 7. During transaction each channel sends its address (6bits) and group sends its address (8bits). Merged value is observed on digital bus. Config '00' result in one readout phase and '01' in two phases. It is worth to note how token is passed from one channel to other after transaction is done. Token is reused and **no dead time is observed.**

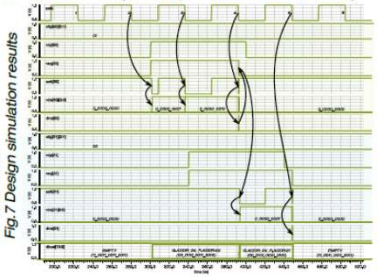


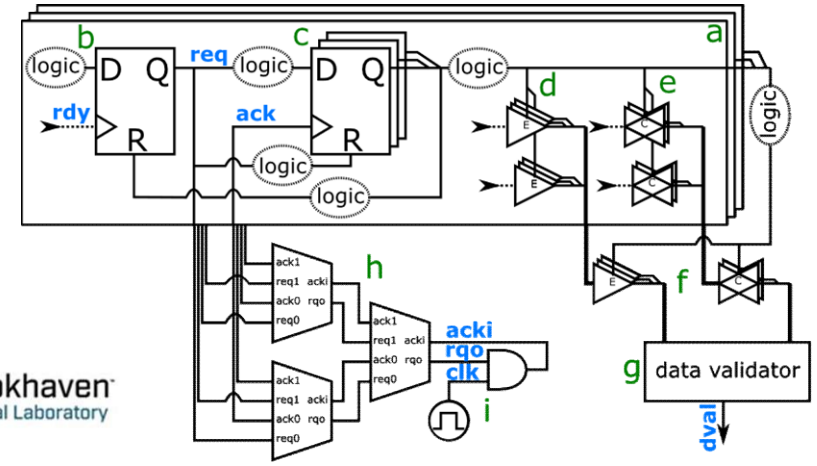
Fig.7 Design simulation results

All-Digital Platform for Pixel Detectors

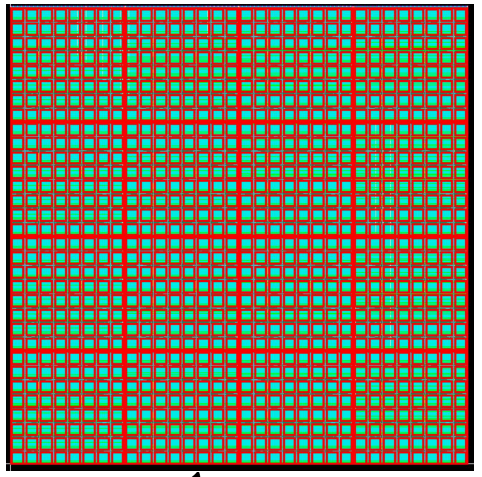
EDWARD –

Event **D**riven **W**ith **A**ccess and **R**eset **D**ecoder

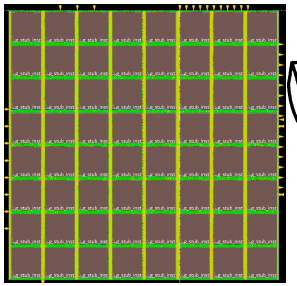
1. receives notification about channel ready to be read out (rdy signal),
2. sends request (req signal) to access shared bus,
3. transmits request signal to synchronization unit (rqo signal) with simultaneous arbitration if there are multiple requests,
4. transmits acknowledge token (acki signals) to channel (ack signal) that wins arbitration = granting permission for exclusive access to bus,
5. lets channel drive its data to bus,
6. defines access time frame to channel and, if necessary, lets several data packets from same channel uninterruptedly in multiple phases,
7. switches immediately, without dead time, between channels if there is still at least one readout request after completing current readout,
8. establishes default bus state if no channel is currently being read out.



Universal All-Digital Platform for Implementation of Configuration-Testability-Readout Functionalities within Pixel Detectors



32 × 32 pixels matrix obtained by tiling 4 × 4 basic groups that is suitable for tiling into still larger matrix sizes. All pins are placed on one side for easy connections to peripheral circuitry logic



8 × 8 pixels base group layout for a 100 × 100 μm^2 pixel detector. Each brown square is space left for AFE (size = 90 × 90 μm^2).

platform is based on developed RTL code that includes Configuration-Testability-Readout features that is parametrized and scalable to allow “virtual painting” of digital back-bones of pixel detectors with high efficiency of area usage for Analog Front-End circuitry that is added on top

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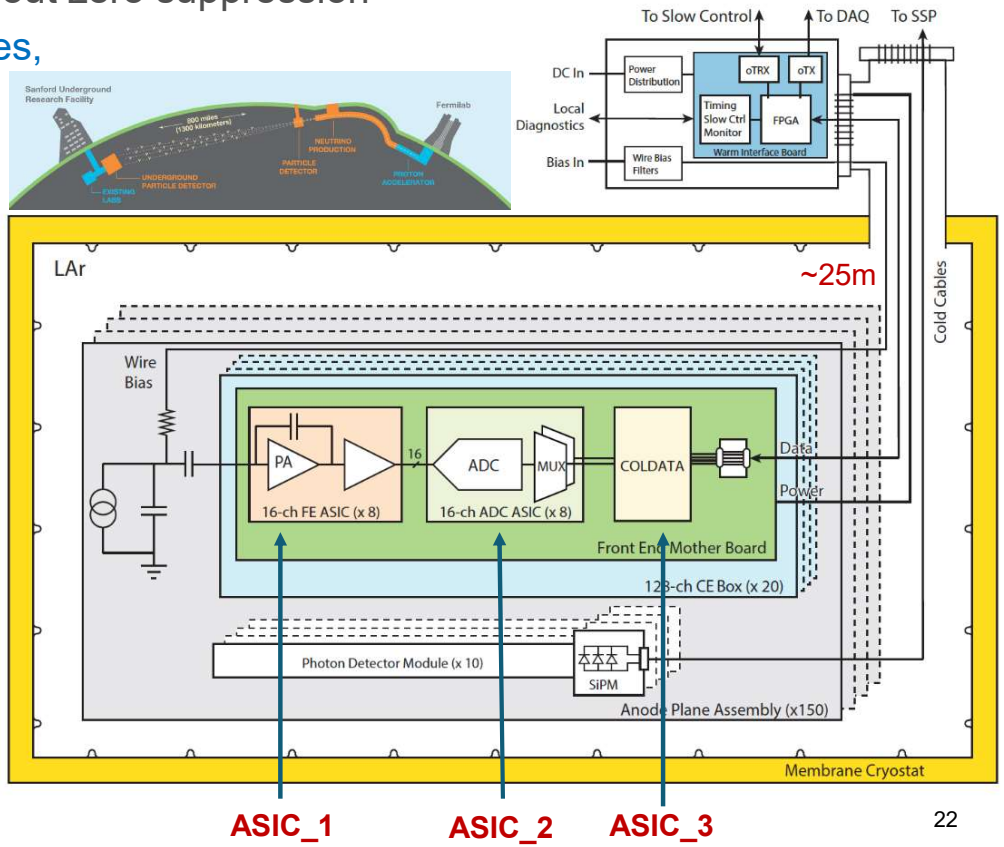
DUNE 3-ASIC IAr TPC Readout

- Integrated electronics in cryostat (giant TPC with ~5 m drift distance) in liquid Ar (80 K, not accessible for lifetime of DUNE experiment ➲ HCE reliability)
- Waveforms are digitized at 2 MHz and read out without zero suppression
- Electronics circuits are mounted near the sense wires,
  - Amplifier and Shaper 16 channels
  - ADC 16 channels
  - Data Merger and Serializer 2 × 1.25 Gbps
- 3-ASIC readout for DUNE far detector:
  - Front-End: LArASIC (180 nm) by BNL,
  - Time interleaved ADC: ColdADC (65 nm) by LBNL, FNAL, BNL)
  - Data concentrator/transceiver: ColdDATA by FNAL, BNL digital implementation and P&R
- One 10 kTon FD-1HD detector has:
  - 3000 x 128-channel Front End Mother Boards with 24000 x FE ASICs, 24000 x ADC ASICs, 6000 COLDATA ASICs

  Total 12000 1.28 Gbps links (9.2 Tbps of waveform data)



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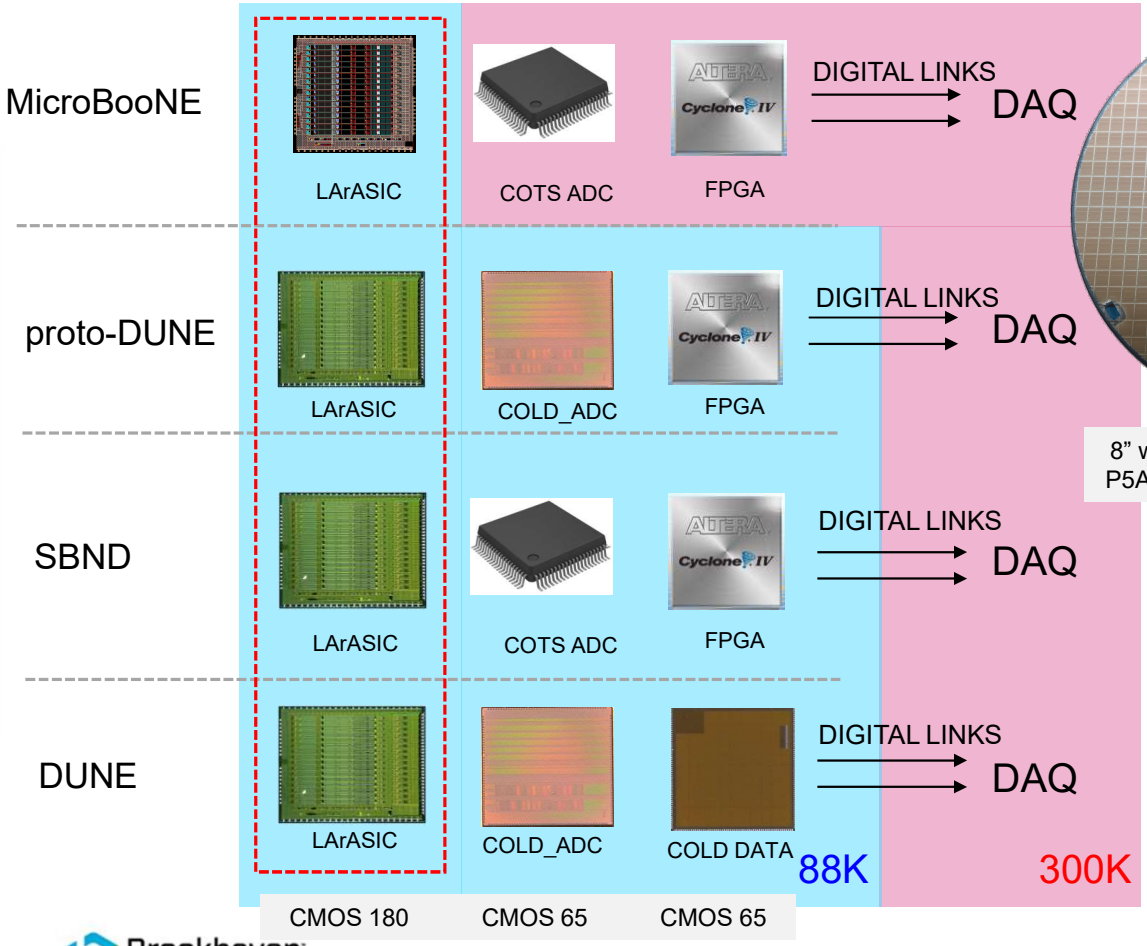
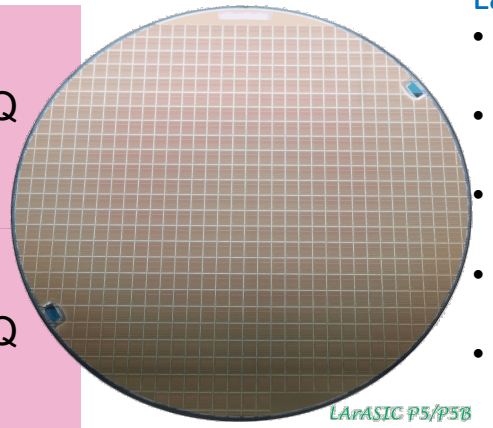
DUNE 3-ASIC IAr TPC Readout

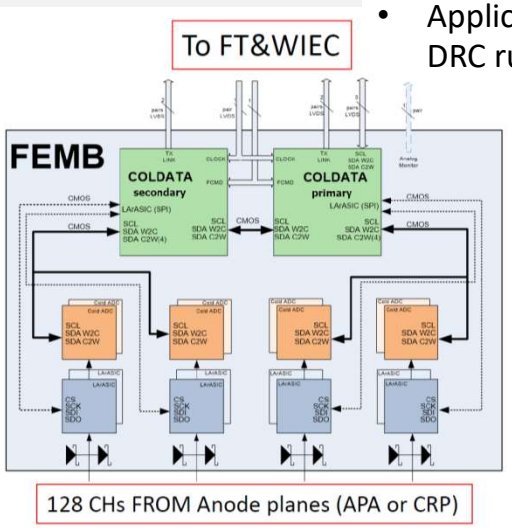




8" wafer with 610 LArASICs P5 and P5A(B) w. increased ESD protection

Last modification:

- Removed "ledge" effect (saturation) causing dead time
- Improved BGR reference to avoid ~10% "no-startup" chips
- improved linearity and range of calibration DAC
- addition of strength to input pad ESD protections
- solving reset-quiescent current mismatch problem at LNT
- Improving stability of output single-to-differential converter
- Application of recommended DRC rules where possible



250 wafers LArASIC production run for DUNE ~75k P5 and 75k P5B chips is under way

About a decade of development

Brookhaven National Laboratory

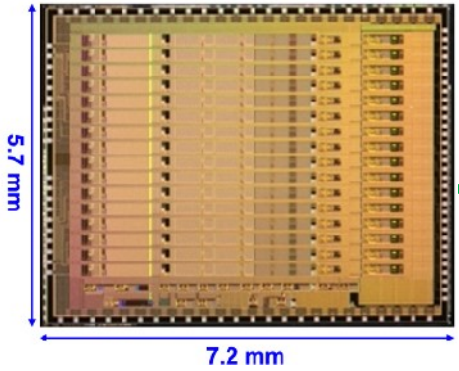
LArASIC P5/P5B Yield QA/QC testing

LArASIC MPW met all the DUNE requirements ⟶ fabricated ~1800 P5 and 1800 P5B chips (eng. run) for ProtoDUNE II

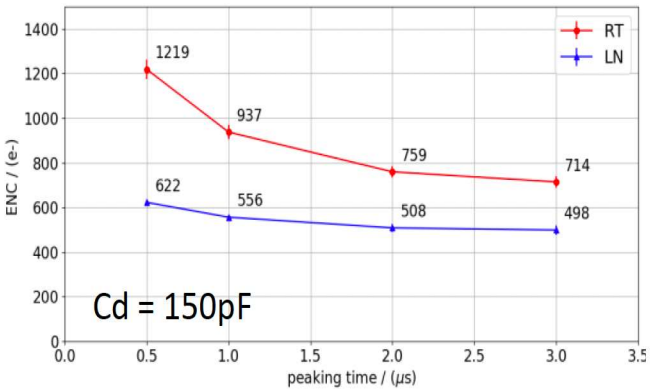
LArASIC Chips	Temp.	Tested Chips#	Good # (All channels are normal)	Yield
P5	RT	49	49	100 %
P5B	**RT**	**1642**	**1635***	**~99.57 %**
P5B	**LNT**	**317**	**317**	**100 %**

P5B has improved input ESD protection compared to P5

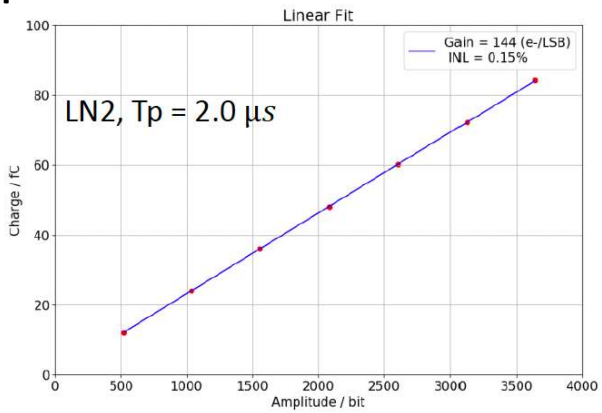
*Only 1 out of 16 channels in each of the two chips are non-functional



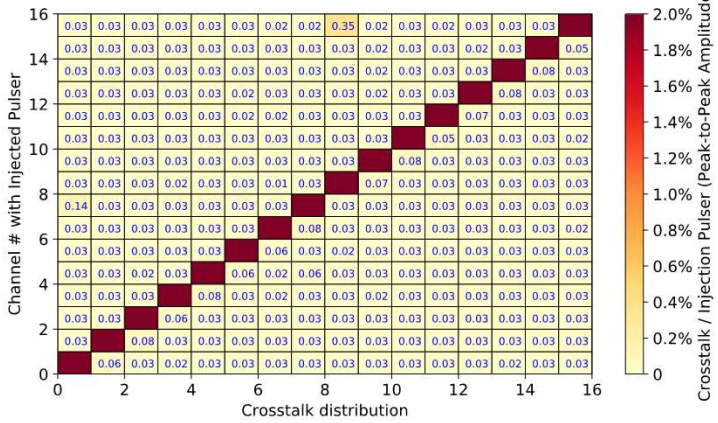
LArASIC performance with differential interface



Low Noise



High Linearity



Low Crosstalk

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already 24 FEMBs arrived at CERN for ProtoDUNE-II installation

Summary

- ASIC and microelectronics continue to evolve to address the challenges of new experiments
- Design methodologies and process technologies are critical drivers
- Competing tendencies: system on a chip vs chiplet approach
- Streaming comes with challenges and opportunities
  - New AI/ML methodologies implemented at the edge to improve data quality/rates
- Concepts and approaches presented in this talk have broad application

Work of the current BNL's ASIC team:
Soumyajit Mandala, Sandeep Miryala, Venkata Narasimha Manyam, Giovanni Pinaroli, Nick St. John, Dominik Gorni, Grzegorz Deptuch, and many others

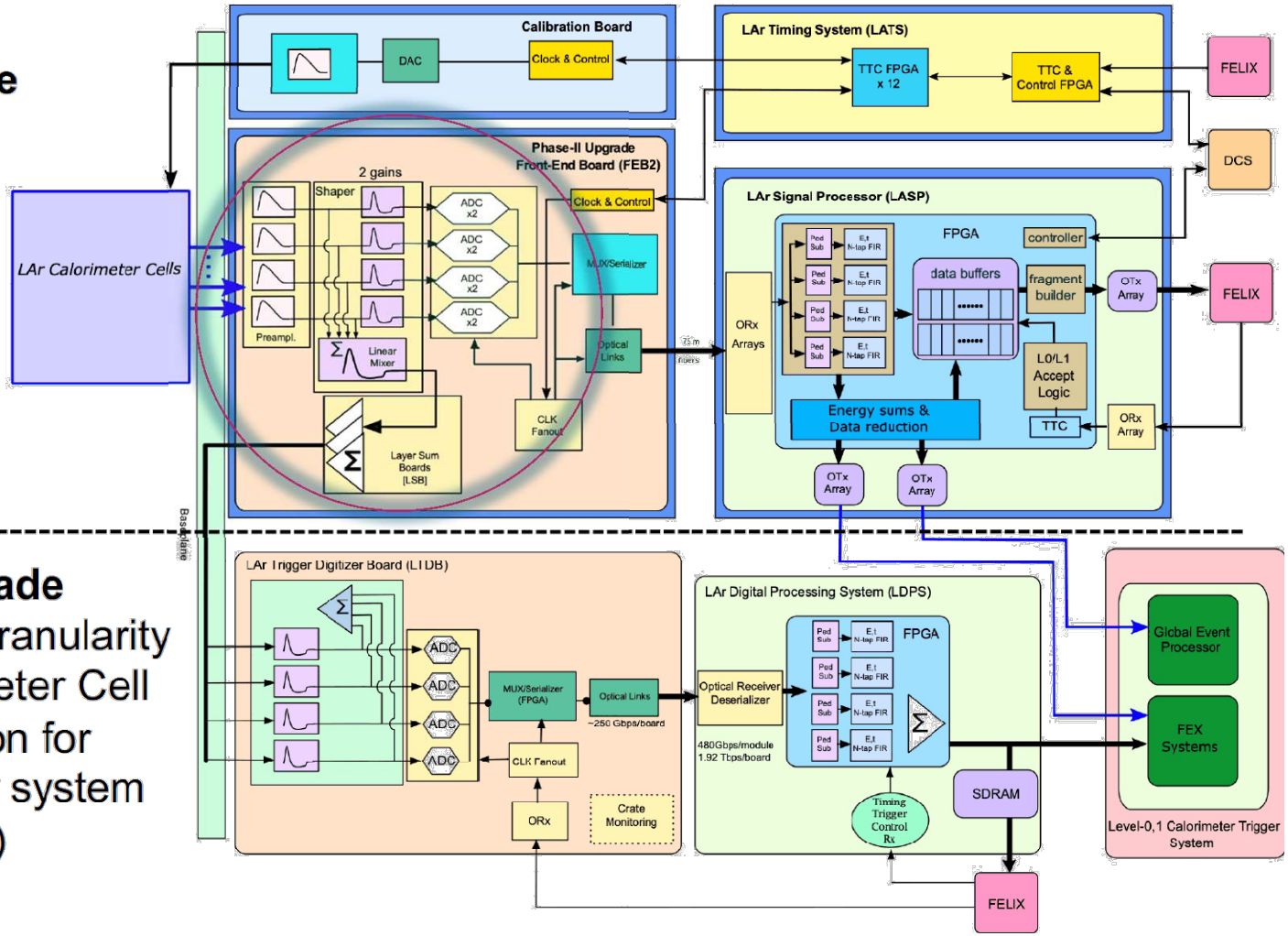
FE for LAr Calorimeter in ATLAS

Phase-II Upgrade

Digitize and readout the full calorimeter, at 40 MHz and provide the information to Level-0 trigger systems

Phase-I Upgrade

Increase the granularity of the Calorimeter Cell sum information for Level-1 trigger system (In-installation)

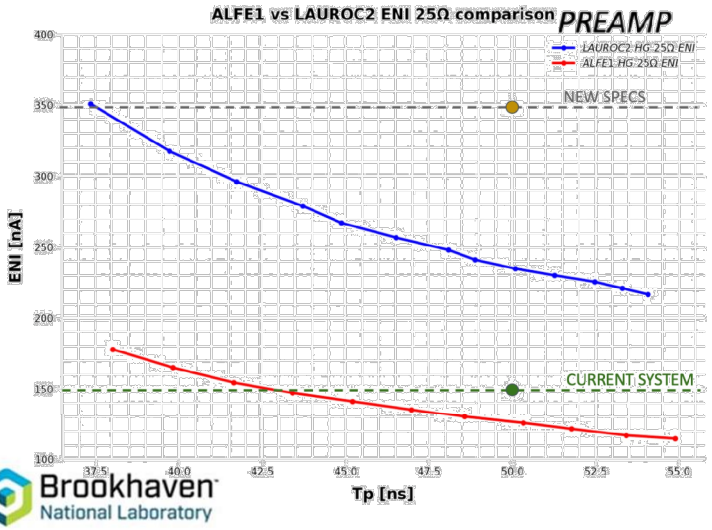


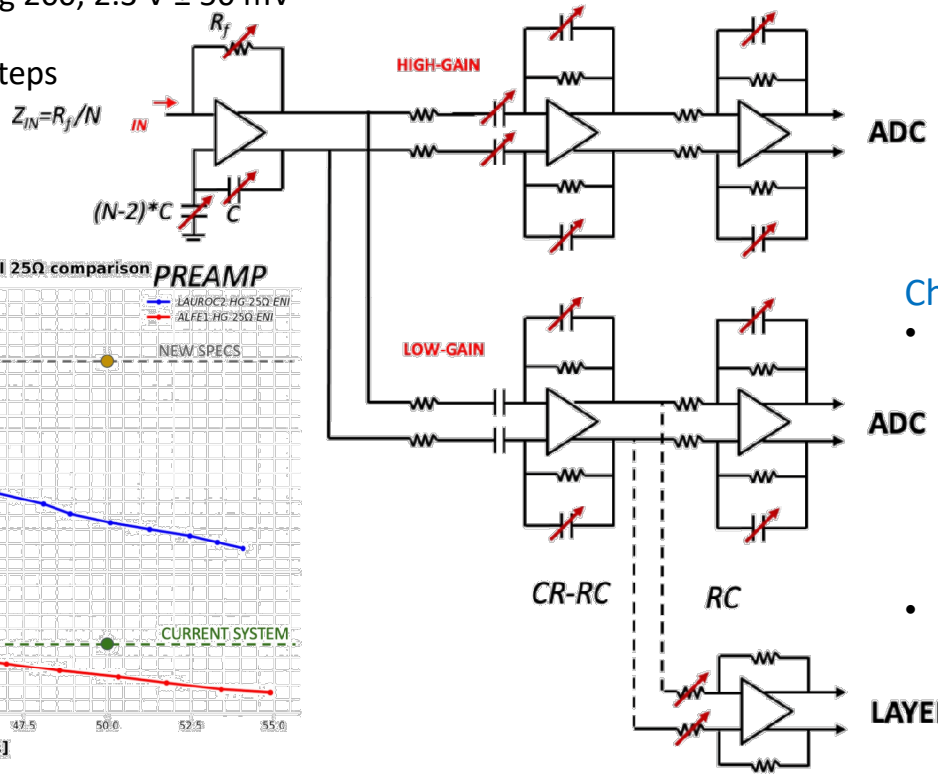
LAr Calorimeter in ATLAS

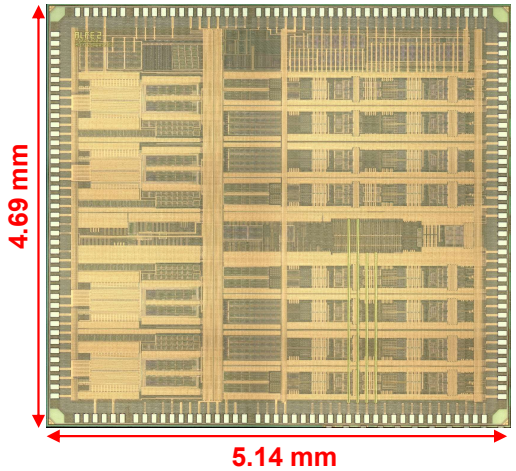
Requirements for FEB2 Preamplifier – Shaper (PA):

- 4 Channel input, 9 Channel output (4 x LG/HG + Trigger sum of 4 channels)
- Input impedance and Dynamic range programmability (25 Ohm 10 mA, 50 Ohm 2mA)
- Input impedance tuning < 2.5 % steps
- Peaking time tuning (15 ± 5 ns, 1 ns steps)
- Preamplifier DC level tuning 200, 2.3 V ± 50 mV
- DC output tuning,
  600 mV ± 360 mV, 30 mV steps

Two Front-End designs were carried out and compared







ALFE2 CMOS 130 nm

Choice of ALFE PA:

- ALFE PA was selected for the FEB2 due to its excellent noise performance and power supply noise rejection, Non-Linearity < 0.2 % (HG) over full DR, no change in performance under irradiation up to 1 Mrad (beyond specifications)
- 48,832 ASICs will be required to populate LAr Calorimeter's FEB2

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